Preliminary

Some of contents are subject to change without notice.

MH4V64/644AXJJ-5,-6,-5S,-6S

FAST PAGE MODE 268435456-BIT (4194304-WORD BY 64-BIT)DYNAMIC RAM

DESCRIPTION

This is family of 4194304 - word by 64 - bit dynamic RAM module. This consists of four industry standard 4Mx16 dynamic RAMs in TSOP and one industry EEPROM in TSSOP.

The mounting of TSOP on a card edge dual in line package provides any application where high densities and large of quantities memory are required.

This is a socket-type memory module,suitable for easy interchange of addition of modules.

FEATURES

	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)
MH4V64AXJJ-5,5S	50	13	25	13	90
MH4V64AXJJ-6,6S	60	15	30	15	110
MH4V644AXJJ-5,5S	50	13	25	13	90
MH4V644AXJJ-6,6S	60	15	30	15	110

- single 3.3V± 0.3V supply
- Low stand-by power dissipation
  7.2mW- - - - - - - - - LVCMOS input level
- operating power dissipation
  MH4V64AXJJ-5,5S - - - - - 1584 mW(max.)
  MH4V64AXJJ-6,6S - - - - - 1440mW(max.)
  MH4V644AXJJ-5,5S - - - - 2016 mW(max.)
  MH4V644AXJJ-6,6S - - - - 1872 mW(max.)
- Self refresh capability*
  Self refresh current - - - - 1600 uA(max.)
- All input, output LVTTL compatible and low capacitance
- Utilizes industry standard 4Mx16 RAMs in TSOP and industry standard EEPROM in TSSOP.
- Includes decoupling capacitor(0.22uFx4)
- Fast page mode , Read-modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh,Hidden refresh capabilities.
- Early-write mode,$\overline{OE}$ to control output buffer impedance.

ADDRESS

Part No.	Row Add.	Col Add.	Refresh	Refresh Cycle
MH4V64AXJJ	A0~A12	A0~A8	/RAS only Ref,Normal R/W	8192/64ms
			CBR Ref,Hidden Ref	4096/64ms
MH4V644AXJJ	A0~A11	A0~A9	/RAS only Ref,Normal R/W CBR Ref,Hidden Ref	4096/64ms

APPLICATION

Main memory unit for computer,Microcomputer memory,Refresh memory for CRT.

*:Applicable to self refresh version(MH4V64/644AXJJ-5S,-6S) only

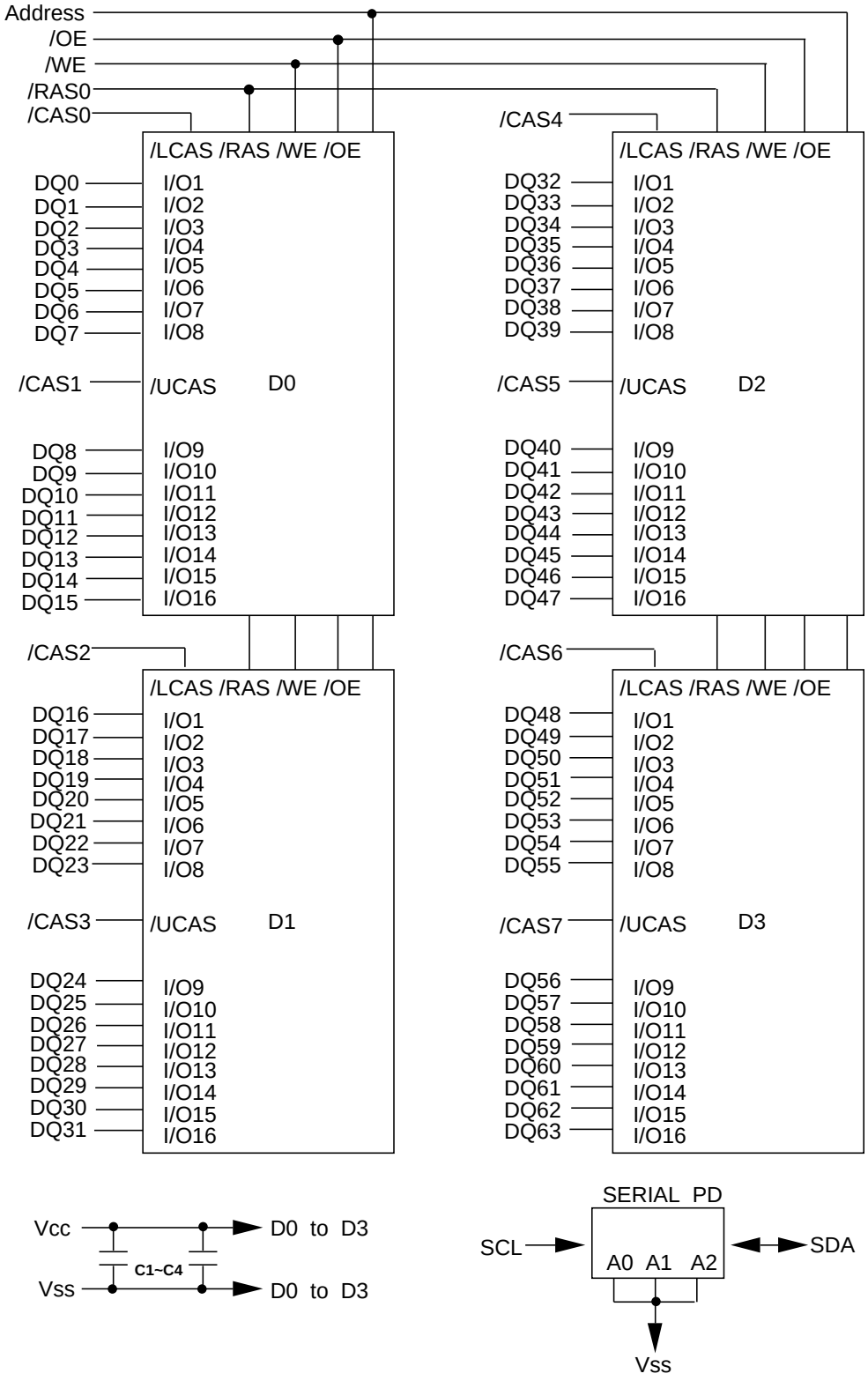
PIN CONFIGURATION

PIN Number	Front side Pin Name	PIN Number	Back side Pin Name	PIN Number	Front side Pin Name	PIN Number	Back side Pin Name
1	Vss	2	Vss	73	/OE	74	RFU
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	Reserved	78	Reserved
7	DQ2	8	DQ34	79	Reserved	80	Reserved
9	DQ3	10	DQ35	81	Vcc	82	Vcc
11	Vcc	12	Vcc	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	/CAS0	24	/CAS4	95	DQ21	96	DQ53
25	/CAS1	26	/CAS5	97	DQ22	98	DQ54
27	Vcc	28	Vcc	99	DQ23	100	DQ55
29	A0	30	A3	101	Vcc	102	Vcc
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	A11
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	A12/NC(note)
39	DQ9	40	DQ41	111	A10	112	NC
41	DQ10	42	DQ42	113	Vcc	114	Vcc
43	DQ11	44	DQ43	115	/CAS2	116	/CAS6
45	Vcc	46	Vcc	117	/CAS3	118	/CAS7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	Reserved	58	Reserved	129	Vcc	130	Vcc
59	Reserved	60	Reserved	131	DQ28	132	DQ60
61	RFU	62	FRU	133	DQ29	134	DQ61
63	Vcc	64	Vcc	135	DQ30	136	DQ62
65	RFU	66	RFU	137	DQ31	138	DQ63
67	/WE	68	RFU	139	Vss	140	Vss
69	/RAS0	70	RFU	141	SDA	142	SCL
71	NC	72	RFU	143	Vcc	144	Vcc

RFU:Reserved Future Use
NC,RFU,Reserved: NO CONNECTION

Note:A12 ... MH4V64AXJJ , NC ... MH4V644AXJJ

Block Diagram



Serial Presence Detece TABLE (MH4V64AXJJ-5,-6)

Bytes	Function described		SPD entry data	SPD DATA entry(Hex)
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		FPM DRAM	01
3	# Row Addresses on this assembly		A0-A12	0D
4	# Column Addresses on this assembly		A0-A8	09
5	# Module Banks on this assembly		1bank	01
6	Data Width of this assembly...		x64	40
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		3.3V LVTTL	02
9	RAS# access time of this assembly	-5	50ns	32
		-6	60ns	3C
10	CAS# access time of this assembly	-5	13ns	0D
		-6	15ns	0F
11	DIMM Configuration type (Non-parity,Parity,ECC)		non parity	00
12	Refresh Rate/Type		N/R(15.625uS)	00
13	DRAM width,Primary DRAM		x16	10
14	Error Checking DRAM data width		N/A	00
15-31	Reserved for future offerings		open	00
32-61	Superset Memory type(may be used in future)		open	00
62	SPD Data Revision Code		Rev 1	01
63	Checksum for bytes 0-62		Check sum for -5	32
			Check sum for -6	3E
64-71	Manufacturers JEDEC ID code per JEP-106		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Miyoshi,Japan	01
			Tajima,Japan	02
			NC,USA	03
			Germany	04
73-90	Manufacturer's Part Number		MH4V64AXJJ-5	4D483456363441584A4A2D352D35202020202020
			MH4V64AXJJ-6	4D483456363441584A4A2D362D36202020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yy/ww
95-98	Assembly Serial Number		serial number	ssssssss
99-125	Manufacturer Specific Data		open	00
126-127	Reserved		open	00
128-255	Open User Free-Form area not defined		open	00

Serial Presence Detece TABLE (MH4V64AXJJ-5S,-6S)

Bytes	Function described		SPD entry data	SPD DATA entry(Hex)
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		FPM DRAM	01
3	# Row Addresses on this assembly		A0-A12	0D
4	# Column Addresses on this assembly		A0-A8	09
5	# Module Banks on this assembly		1bank	01
6	Data Width of this assembly...		x64	40
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		3.3V LVTTL	02
9	RAS# access time of this assembly	-5S	50ns	32
		-6S	60ns	3C
10	CAS# access time of this assembly	-5S	13ns	0D
		-6S	15ns	0F
11	DIMM Configuration type (Non-parity,Parity,ECC)		non parity	00
12	Refresh Rate/Type		S/R(15.625uS)	80
13	DRAM width,Primary DRAM		x16	10
14	Error Checking DRAM data width		N/A	00
15-31	Reserved for future offerings		open	00
32-61	Superset Memory type(may be used in future)		open	00
62	SPD Data Revision Code		Rev 1	01
63	Checksum for bytes 0-62		Check sum for -5	B2
			Check sum for -6	BE
64-71	Manufacturers JEDEC ID code per JEP-106		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Miyoshi,Japan	01
			Tajima,Japan	02
			NC,USA	03
			Germany	04
73-90	Manufacturer's Part Number		MH4V64AXJJ-5S	4D483456363441584A4A2D355335532020202020
			MH4V64AXJJ-6S	4D483456363441584A4A2D365336532020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yy/ww
95-98	Assembly Serial Number		serial number	ssssssss
99-125	Manufacturer Specific Data		open	00
126-127	Reserved		open	00
128-255	Open User Free-Form area not defined		open	00

Serial Presence Detece TABLE (MH4V644AXJJ-5,-6)

Bytes	Function described		SPD entry data	SPD DATA entry(Hex)
0	Defines # bytes written into serial memory at module mfgr		128	80
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		FPM DRAM	01
3	# Row Addresses on this assembly		A0-A11	0C
4	# Column Addresses on this assembly		A0-A9	0A
5	# Module Banks on this assembly		1bank	01
6	Data Width of this assembly...		x64	40
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		3.3V LVTTL	02
9	RAS# access time of this assembly	-5	50ns	32
		-6	60ns	3C
10	CAS# access time of this assembly	-5	13ns	0D
		-6	15ns	0F
11	DIMM Configuration type (Non-parity,Parity,ECC)		non parity	00
12	Refresh Rate/Type		N/R(15.625uS)	00
13	DRAM width,Primary DRAM		x16	10
14	Error Checking DRAM data width		N/A	00
15-31	Reserved for future offerings		open	00
32-61	Superset Memory type(may be used in future)		open	00
62	SPD Data Revision Code		Rev 1	01
63	Checksum for bytes 0-62		Check sum for -5	32
			Check sum for -6	3E
64-71	Manufacturers JEDEC ID code per JEP-106		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Miyoshi,Japan	01
			Tajima,Japan	02
			NC,USA	03
			Germany	04
73-90	Manufacturer's Part Number		MH4V644AXJJ-5	4D48345636343441584A4A2D352D352020202020
			MH4V644AXJJ-6	4D48345636343441584A4A2D362D362020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yy/ww
95-98	Assembly Serial Number		serial number	ssssssss
99-125	Manufacturer Specific Data		open	00
126-127	Reserved		open	00
128-255	Open User Free-Form area not defined		open	00

Serial Presence Detece TABLE (MH4V644AXJJ-5S,-6S)

Bytes	Function described		SPD entry data	SPD DATA entry(Hex)
0	Defines # bytes written into serial memory at module mfgr		128	80
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		FPM DRAM	01
3	# Row Addresses on this assembly		A0-A11	0C
4	# Column Addresses on this assembly		A0-A9	0A
5	# Module Banks on this assembly		1bank	01
6	Data Width of this assembly...		x64	40
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		3.3V LVTTL	02
9	RAS# access time of this assembly	-5S	50ns	32
		-6S	60ns	3C
10	CAS# access time of this assembly	-5S	13ns	0D
		-6S	15ns	0F
11	DIMM Configuration type (Non-parity,Parity,ECC)		non parity	00
12	Refresh Rate/Type		S/R(15.625uS)	80
13	DRAM width,Primary DRAM		x16	10
14	Error Checking DRAM data width		N/A	00
15-31	Reserved for future offerings		open	00
32-61	Superset Memory type(may be used in future)		open	00
62	SPD Data Revision Code		Rev 1	01
63	Checksum for bytes 0-62		Check sum for -5S	B2
			Check sum for -6S	BE
64-71	Manufacturers JEDEC ID code per JEP-106		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Miyoshi,Japan	01
			Tajima,Japan	02
			NC,USA	03
			Germany	04
73-90	Manufacturer's Part Number		MH4V644AXJJ-5S	4D48345636343441584A4A2D3553355320202020
			MH4V644AXJJ-6S	4D48345636343441584A4A2D3653365320202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yy/ww
95-98	Assembly Serial Number		serial number	ssssssss
99-125	Manufacturer Specific Data		open	00
126-127	Reserved		open	00
128-255	Open User Free-Form area not defined		open	00

FUNCTION

The MH4V64/644AXJJ provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., Fast page mode, /RAS-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	/RAS	/CAS	/W	/OE	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
/RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
/CAS before /RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	
Self refresh *	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open
*MH4V64/644AXJJ-5S,-6S only

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5~4.6	V
VI	Input voltage		-0.5~4.6	V
VO	Output voltage		-0.5~4.6	V
IO	Output current		50	mA
Pd	Power dissipation	Ta=25°C	4	W
Topr	Operating temperature		0~ 70	°C
Tstg	Storage temperature (SOJ)		-40~ 100	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.0		Vcc+0.3	V
VIL	Low-level input voltage, all inputs	**-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)
[MH4V64AXJJ]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH=-2.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL=2.0mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V≤VOUT≤3.6V	-10		10	uA
I I	Input current		0V≤VIN≤3.6V, Other input pins=0V	-40		40	uA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	-5,-5S	/RAS, /CAS cycling tRC=tWC=min. output open			440	mA
		-6,-6S				400	
ICC2	Supply current from Vcc , stand-by		/RAS=/CAS =VIH, output open			4	mA
			/RAS=/CAS≥Vcc -0.2, output open			2	
ICC4(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	-5,-5S	/RAS=VIL,/CAS cycling tPC=min. output open			400	mA
		-6,-6S				360	
ICC6(AV)	Average supply current from Vcc /CAS before /RAS refresh mode (Note 3,5)	-5,-5S	/CAS before /RAS refresh cycling tRC=min.,/W≥Vcc-0.2 output open			560	mA
		-6,-6S				520	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column address can be changed once or less while /RAS=VIL and /CAS=VOH

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)
[MH4V644AXJJ]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH=-2.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL=2.0mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V≤VOUT≤3.6V	-10		10	uA
I I	Input current		0V≤VIN≤3.6V, Other input pins=0V	-40		40	uA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	-5,-5S	/RAS, /CAS cycling tRC=tWC=min. output open			560	mA
		-6,-6S				520	
ICC2	Supply current from Vcc , stand-by		/RAS=/CAS =VIH, output open			4	mA
			/RAS=/CAS≥Vcc -0.2, output open			2	
ICC4(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	-5,-5S	/RAS=VIL,/CAS cycling tPC=min.,/W≥Vcc-0.2 output open			420	mA
		-6,-6S				380	
ICC6(AV)	Average supply current from Vcc /CAS before /RAS refresh mode (Note 3,5)	-5,-5S	/CAS before /RAS refresh cycling tRC=min. output open			560	mA
		-6,-6S				520	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column address can be changed once or less while /RAS=VIL and /CAS=VOH

CAPACITANCE (Ta = 0~70°C, Vcc = 3.3V±0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (A)	Input capacitance, address inputs	VI=Vss f=1MHZ Vi=25mVrms			40	pF
CI	**Input capacitance, clock inputs except CAS**				45	pF
C(CAS)	Input capacitance, CAS				25	pF
C(DQ)	Input/Output capacitance,DATA				25	pF
C(SDA)	Input/Output capacitance,SDA				12	pF
C(SCL)	Input capacitance, SCL				12	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted , see notes 6,13,14)

Symbol	Parameter		Limits				Unit
			-5,-5S		-6,-6S		
			Min	Max	Min	Max	
tCAC	Access time from /CAS	(Note 7,8)		13		15	ns
tRAC	Access time from /RAS	(Note 7,9)		50		60	ns
tAA	Column address access time	(Note 7,10)		25		30	ns
tCPA	Access time from /CAS precharge	(Note 7,11)		30		35	ns
tOEA	Access time from /OE	(Note 7)		13		15	ns
tCLZ	Output low impedance time from /CAS low	(Note 7)	5		5		ns
tOFF	Output disable time after /CAS high	(Note 12)	0	13	0	15	ns
tOEZ	Output disable time after /OE high	(Note 12)	0	13	0	15	ns

Note 6: An initial pause of 500us is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a /RAS clock such as /RAS-Only refresh).
Note the /RAS may be cycled during the initial pause . And any 8 /RAS or /RAS /CAS cycles are required after prolonged periods (greater than 64 ms) of /RAS inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-2mA)/VOL=0.4V(IOL=2mA) loads and 100pF. The reference levels for measuring of output signals are 2.0(VOH)and 0.8(VOL).
8: Assumes that tRCD≥tRCD(max), tASC≥tASC(max) and tCP≥tCP(max).
9: Assumes that tRCD≤tRCD(max) and tRAD≤tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table,tRAC will increase by amount that tRCD exceeds the value shown.
10: Assumes that tRAD≥tRAD(max) and tASC≤tASC(max).
11: Assumes that tCP≤tCP(max) and tASC≥tASC(max).
12: tOFF(max) and tOEZ(max) defines the time at which the output achieves the high impedance state (IOUT≤ I ±10uAI) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)
(Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted ,see notes 13,14)

Symbol	Parameter		Limits				Unit
			-5,-5S		-6,-6S		
			Min	Max	Min	Max	
tREF	Refresh cycle time			64		64	ms
tRP	/RAS high pulse width		30		40		ns
tRCD	Delay time, /RAS low to /CAS low	(Note15)	18	37	20	45	ns
tCRP	Delay time, /CAS high to /RAS low		5		10		ns
tRPC	Delay time, /RAS high to /CAS low		0		0		ns
tCPN	/CAS high pulse width		10		10		ns
tRAD	Column address delay time from /RAS low	(Note16)	13	25	15	30	ns
tASR	Row address setup time before /RAS low		0		0		ns
tASC	Column address setup time before /CAS low	(Note17)	0	5	0	10	ns
tRAH	Row address hold time after /RAS low		8		10		ns
tCAH	Column address hold time after /CAS low		13		15		ns
tDZC	Delay time, data to /CAS low	(Note18)	0		0		ns
tDZO	Delay time, data to /OE low	(Note18)	0		0		ns
tCDD	Delay time, /CAS high to data	(Note19)	13		15		ns
tODD	Delay time, /OE high to data	(Note19)	13		15		ns
tT	Transition time	(Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.VIH(min) and VIL(max) of the switching characteristics are 2.0V and 0.8V respectively.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.tRCD(min) is specified as tRCD(min)=tRAH(min)+2tT+tASC(min) .
16: tRAD(max) is specified as a reference point only. If tRAD≥tRAD(max) and tASC≤tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD≥tRCD(max) and tASC≥tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		-5,-5S		-6,-6S		
		Min	Max	Min	Max	
tRC	Read cycle time	90		110		ns
tRAS	/RAS low pulse width	50	10000	60	10000	ns
tCAS	/CAS low pulse width	13	10000	15	10000	ns
tCSH	/CAS hold time after /RAS low	50		60		ns
tRSH	/RAS hold time after /CAS low	13		15		ns
tRCS	Read Setup time after /CAS high	0		0		ns
tRCH	Read hold time after /CAS low (Note 21)	0		0		ns
tRRH	Read hold time after /RAS low (Note 21)	10		10		ns
tRAL	Column address to /RAS hold time	25		30		ns
tOCH	/CAS hold time after /OE low	13		15		ns
tORH	/RAS hold time after /OE low	13		15		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		-5,-5S		-6,-6S		
		Min	Max	Min	Max	
tWC	Write cycle time	90		110		ns
tRAS	/RAS low pulse width	50	10000	60	10000	ns
tCAS	/CAS low pulse width	13	10000	15	10000	ns
tCSH	/CAS hold time after /RAS low	50		60		ns
tRSH	/RAS hold time after /CAS low	13		15		ns
tWCS	Write setup time before /CAS low (Note 23)	0		0		ns
tWCH	Write hold time after /CAS low	10		10		ns
tCWL	/CAS hold time after /W low	13		15		ns
tRWL	/RAS hold time after /W low	13		15		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before /CAS low or /W low	0		0		ns
tDH	Data hold time after /CAS low or /W low	10		10		ns
tOEH	/OE hold time after /W low	13		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		-5,-5S		-6,-6S		
		Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note22)	130		150		ns
tRAS	/RAS low pulse width	85	10000	95	10000	ns
tCAS	/CAS low pulse width	50	10000	50	10000	ns
tCSH	/CAS hold time after /RAS low	85		95		ns
tRSH	/RAS hold time after /CAS low	50		50		ns
tRCS	Read setup time before /CAS low	0		0		ns
tCWD	Delay time, /CAS low to /W low (Note23)	30		30		ns
tRWD	Delay time, /RAS low to /W low (Note23)	65		75		ns
tAWD	Delay time, address to /W low (Note23)	40		45		ns
tCWL	/CAS hold time after /W low	15		15		ns
tRWL	/RAS hold time after /W low	15		15		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before /W low	0		0		ns
tDH	Date hold time after /W low	10		10		ns
tOEH	/OE hold time after /W low	10		15		ns

Note 22: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.
23:tWCS, tCWD,tRWD ,tAWD and,tCPWD are specified as reference points only. If tWCS≥tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≥tCWD(min), tRWD≥tRWD (min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min) (for Fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied,the DQ (at access time and until /CAS or /OE goes back to VIH) is indeterminate.

Fast Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits				Unit
		-5,-5S		-6,-6S		
		Min	Max	Min	Max	
tPC	Hyper page mode read/write cycle time	35		40		ns
tPRWC	**Hyper page mode read write/read modify write cycle time**	70		75		ns
tRAS	/RAS low pulse width for read write cycle (Note25)	85	**125000**	100	**100000**	ns
tCP	/CAS high pulse width (Note26)	5	10	10	15	ns
tCPRH	/RAS hold time after /CAS precharge	30		35		ns
tCPWD	Delay time, /CAS precharge to /W low (Note23)	30		35		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective Fast page mode cycle.
25: tRAS(min) is specified as two cycles of /CAS input are performed.
26: tCP(max) is specified as a reference point only.If tCP≥tCP(max),access time is controlled exclusively by tCAC.

/CAS before /RAS Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		-5,-5S		-6,-6S		
		Min	Max	Min	Max	
tCSR	/CAS setup time before /RAS low	5		5		ns
tCHR	/CAS hold time after /RAS low	10		10		ns
tRSR	Read setup time before /RAS low	10		10		ns
tRHR	Read hold time after /RAS low	10		10		ns

Note 27: Eight or more /CAS before /RAS cycles instead of eight /RAS cycles are necessary for proper operation of /CAS before /RAS refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item,line -5S / -6S. The other characteristics and requirements then below are same as normal device.

ELECTRIC CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
ICC9(AV)*	**Average supply current from Vcc Self-Refresh mode (Note 6)**	-5S,-6S	**/RAS=/CAS<0.2V /OE=/W=A0~A12(A11)=Vcc-0.2V or 0.2V output=Vcc-0.2V,0.2V or open**			1600	µA

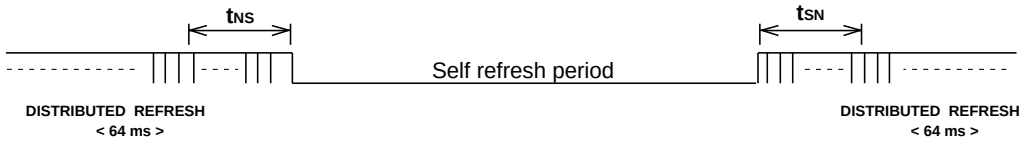
TIMING REQUIREMENTS (Ta=0~70°C, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted ,see notes 13,14)

Symbol	Parameter	Limits				Unit
		-5S		-6S		
		Min	Max	Min	Max	
t_{RASS}	CBR Self Refresh $\overline{RAS}$ low pulse width	100		100		us
t_{RPS}	CBR Self Refresh $\overline{RAS}$ high precharge time	90		110		ns
t_{CHS}	CBR Self Refresh $\overline{RAS}$ hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

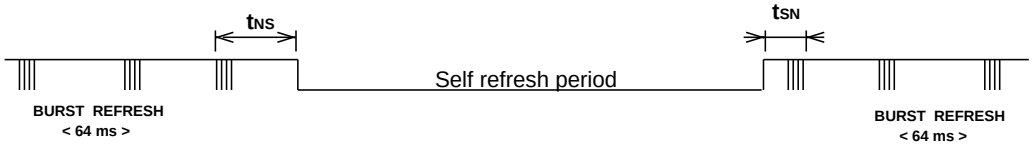
(1) In case of CBR distributed refresh

The last / first full refresh cycles must be made within tNS / tSN before / after self refresh , on the condition of tNS≤ 64 ms and tSN ≤ 64 ms.



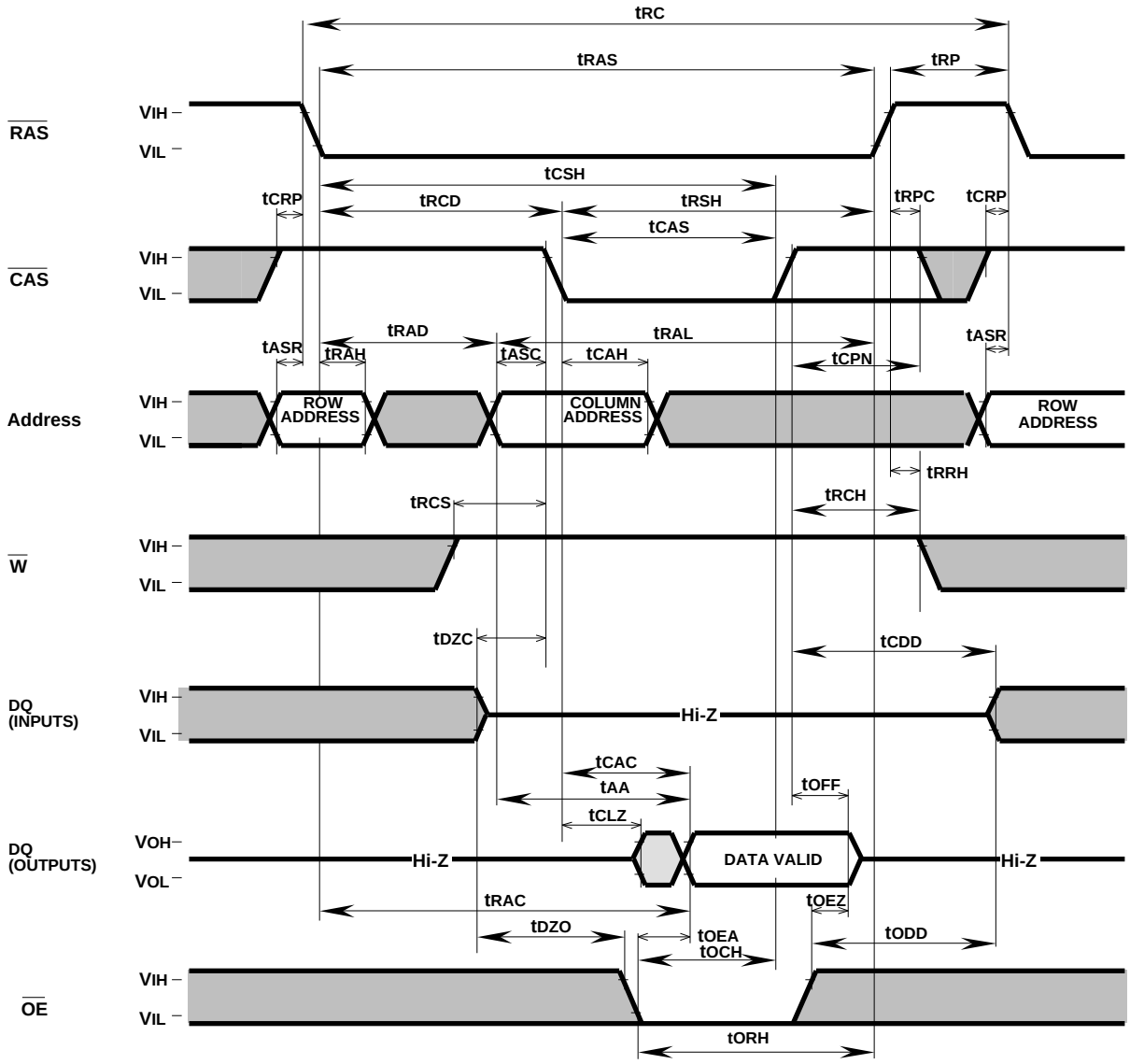
(2) In case of burst refresh

The last / first full refresh cycles must be made within tNS / tSN before / after self refresh , on the condition of tNS ≤ 16ms and tSN ≤ 16 ms.



Timing Diagrams (Note 28)

Read Cycle

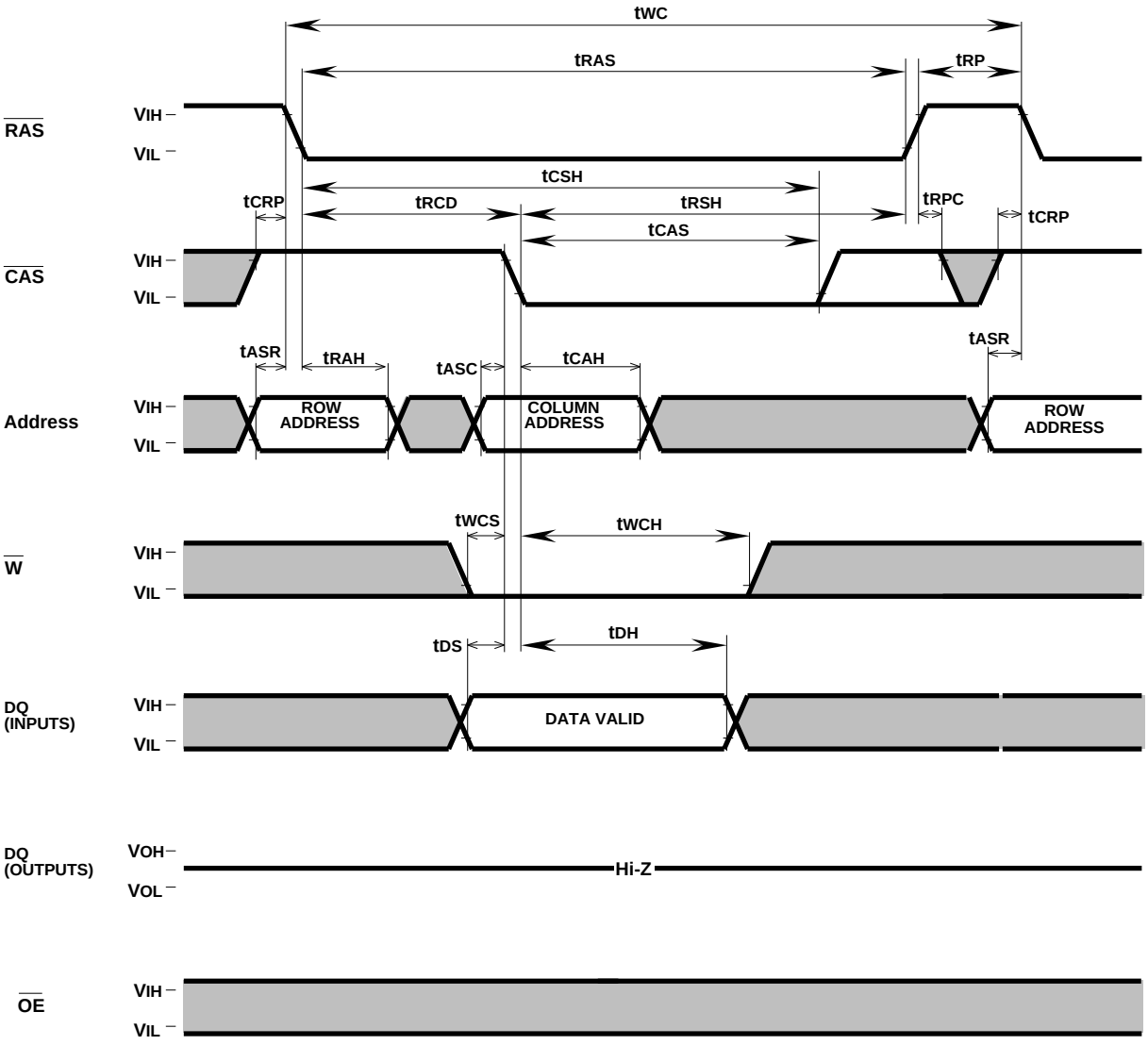


Note 28

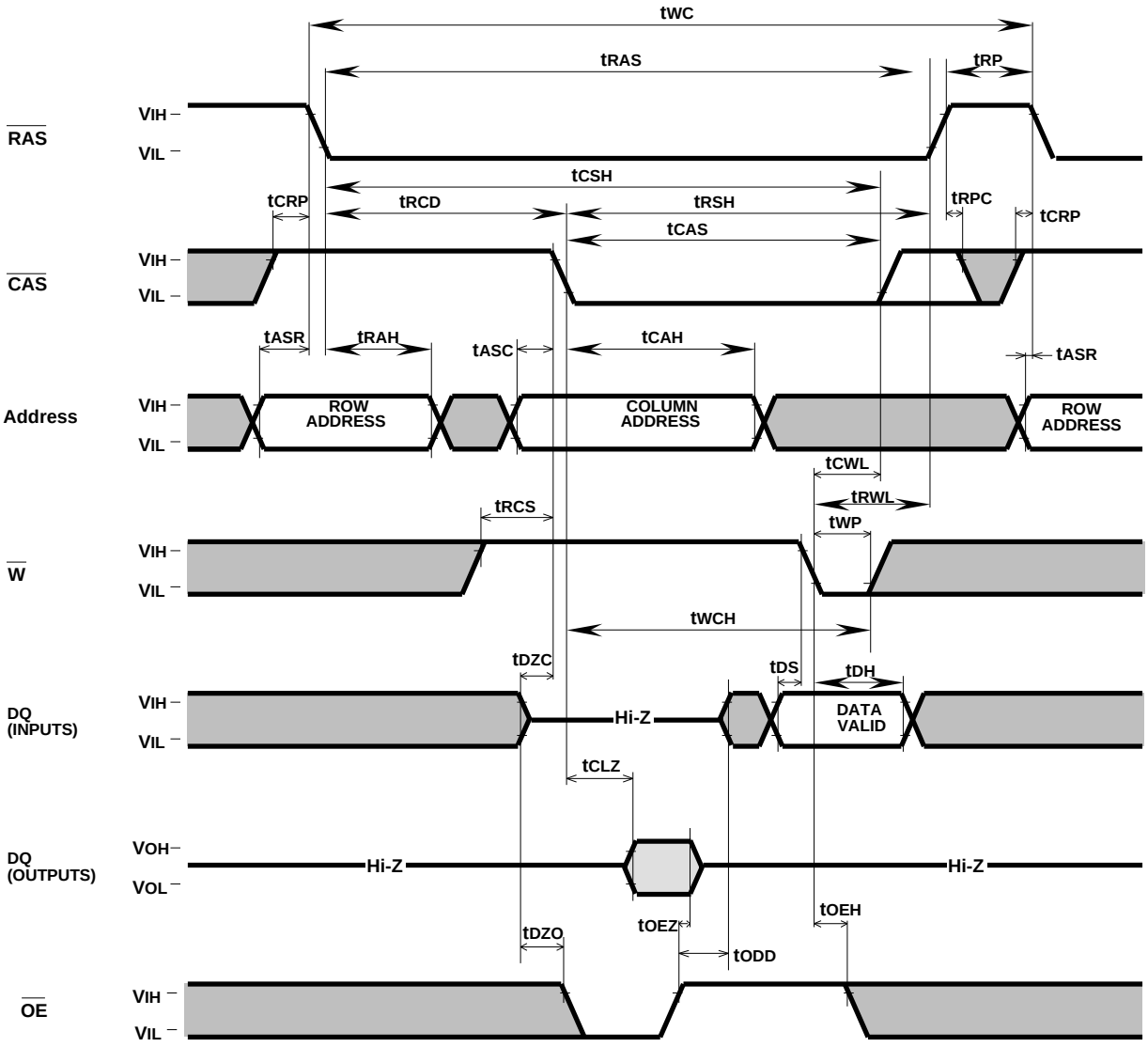
Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

Indicates the invalid output.

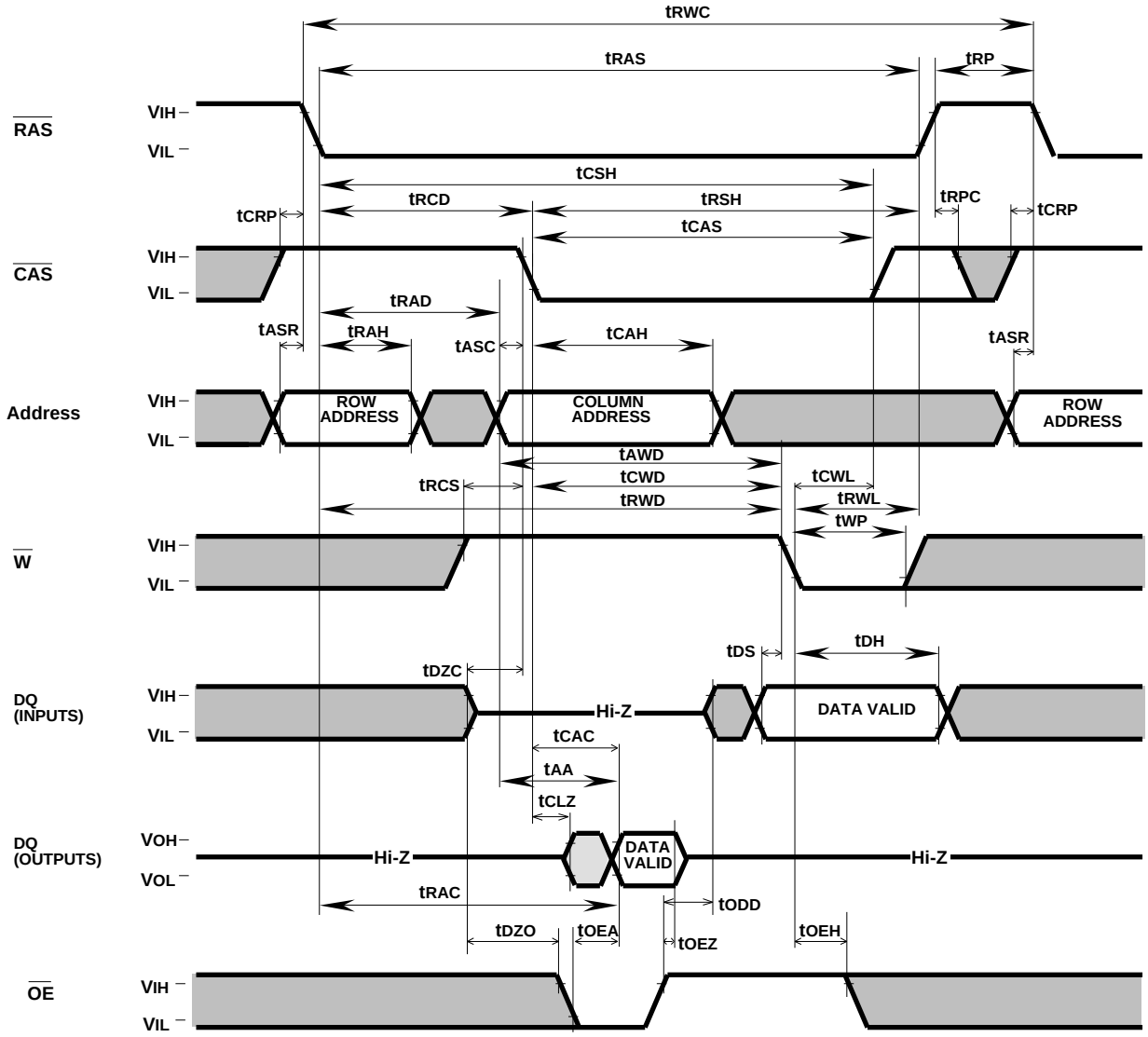
Write Cycle (Early write)



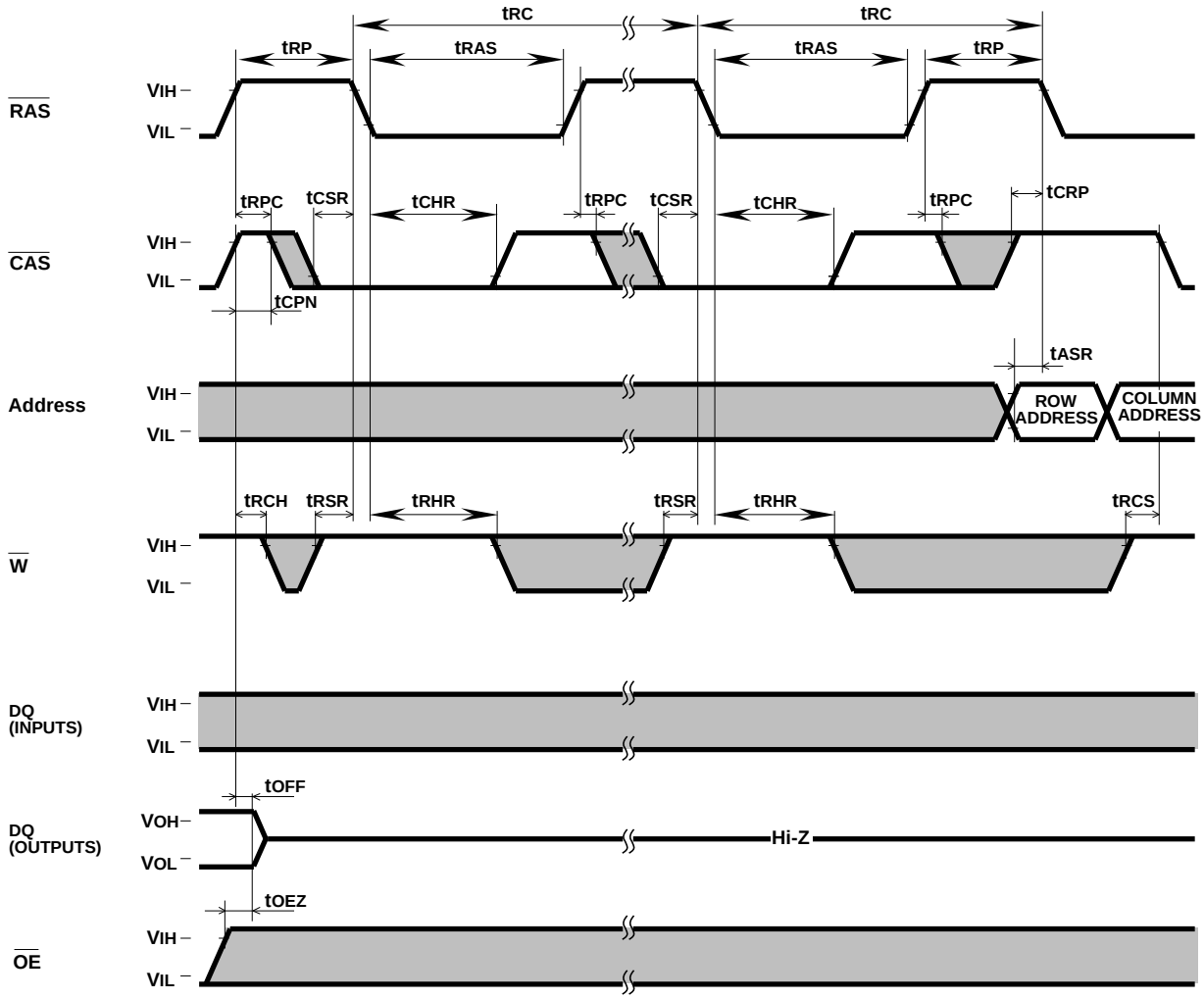
Write Cycle (Delayed write)



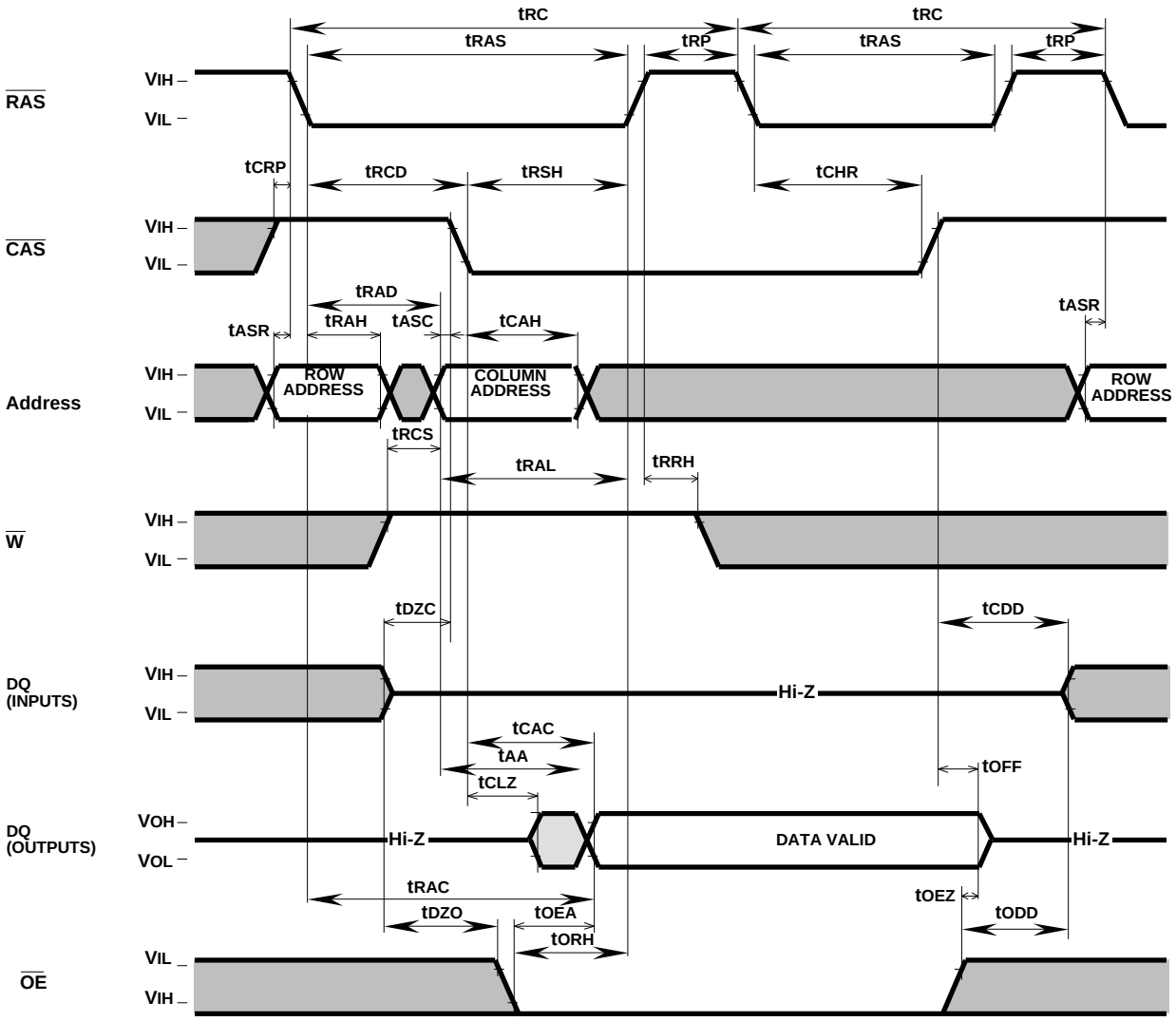
Read-Write, Read-Modify-Write Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

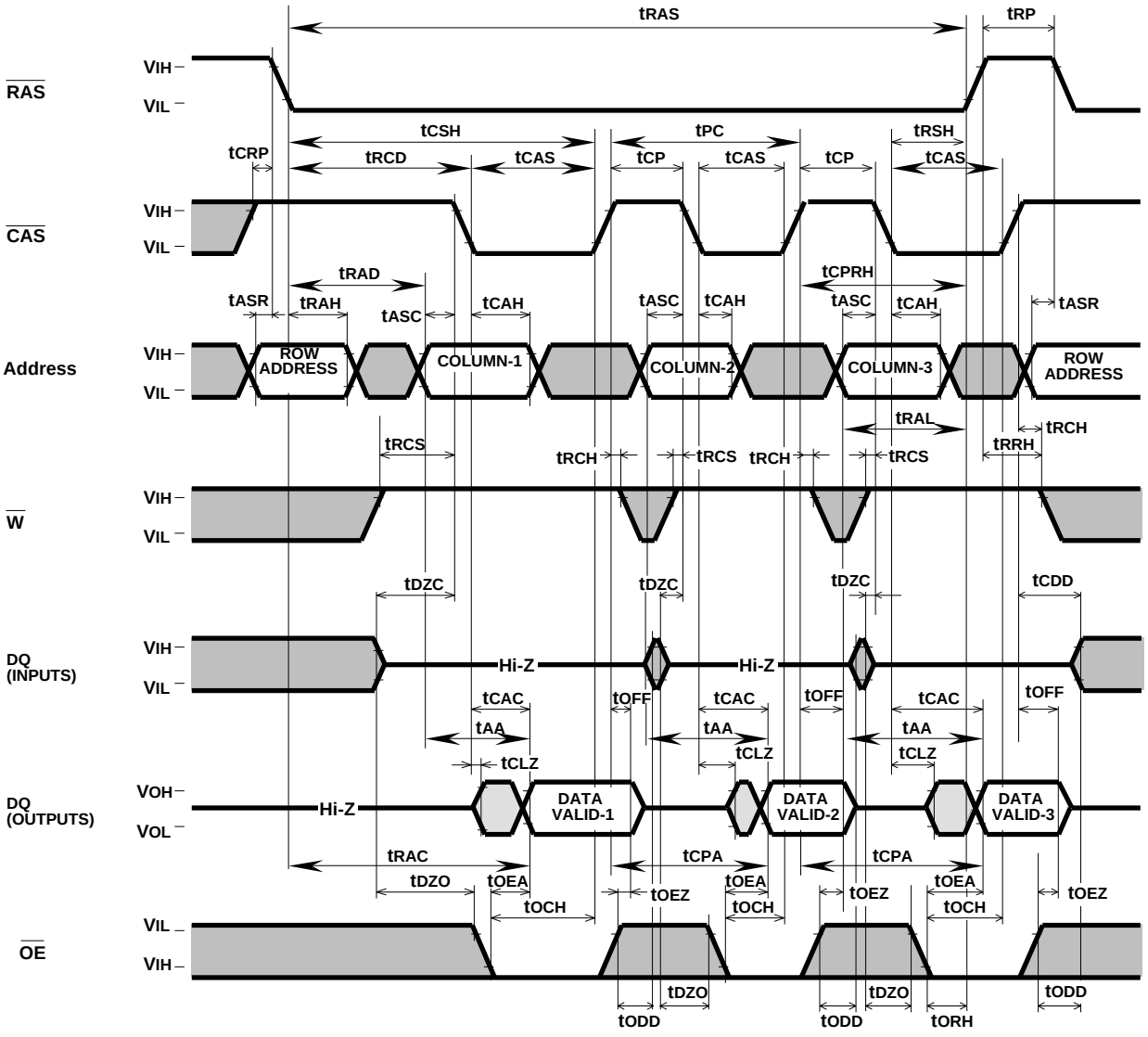


Hidden Refresh Cycle (Read) (Note 29)

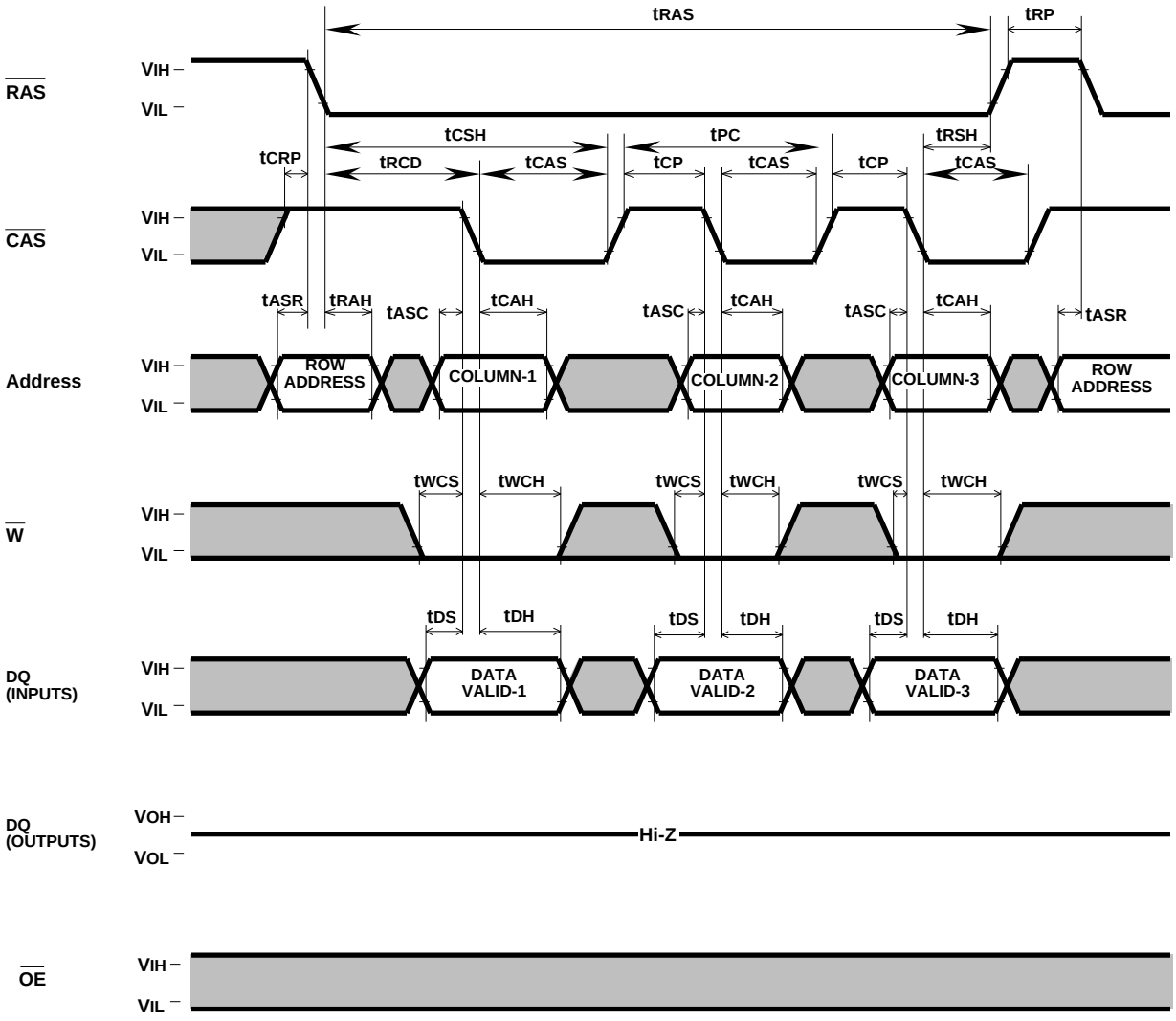


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

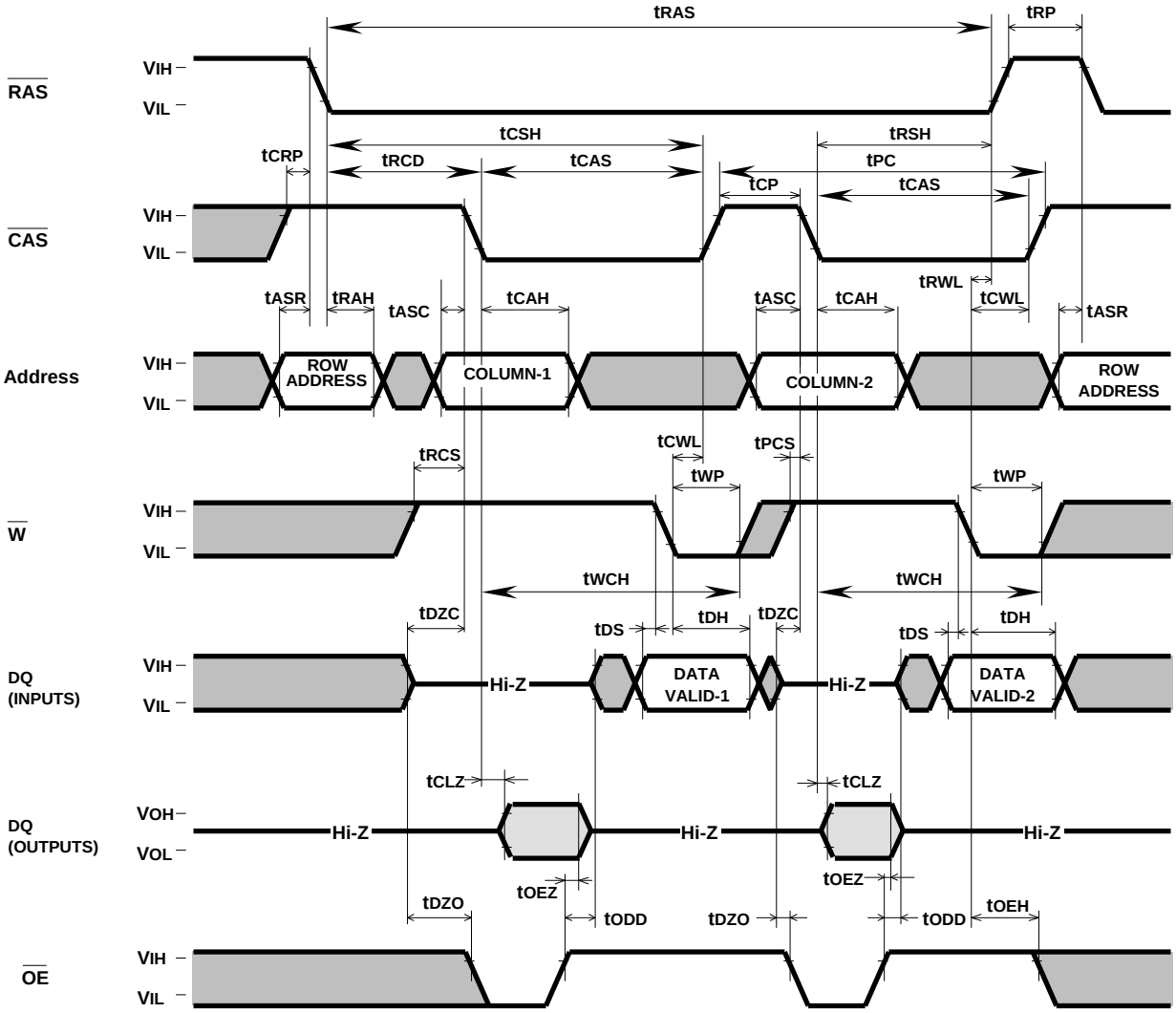
Fast Page Mode Read Cycle



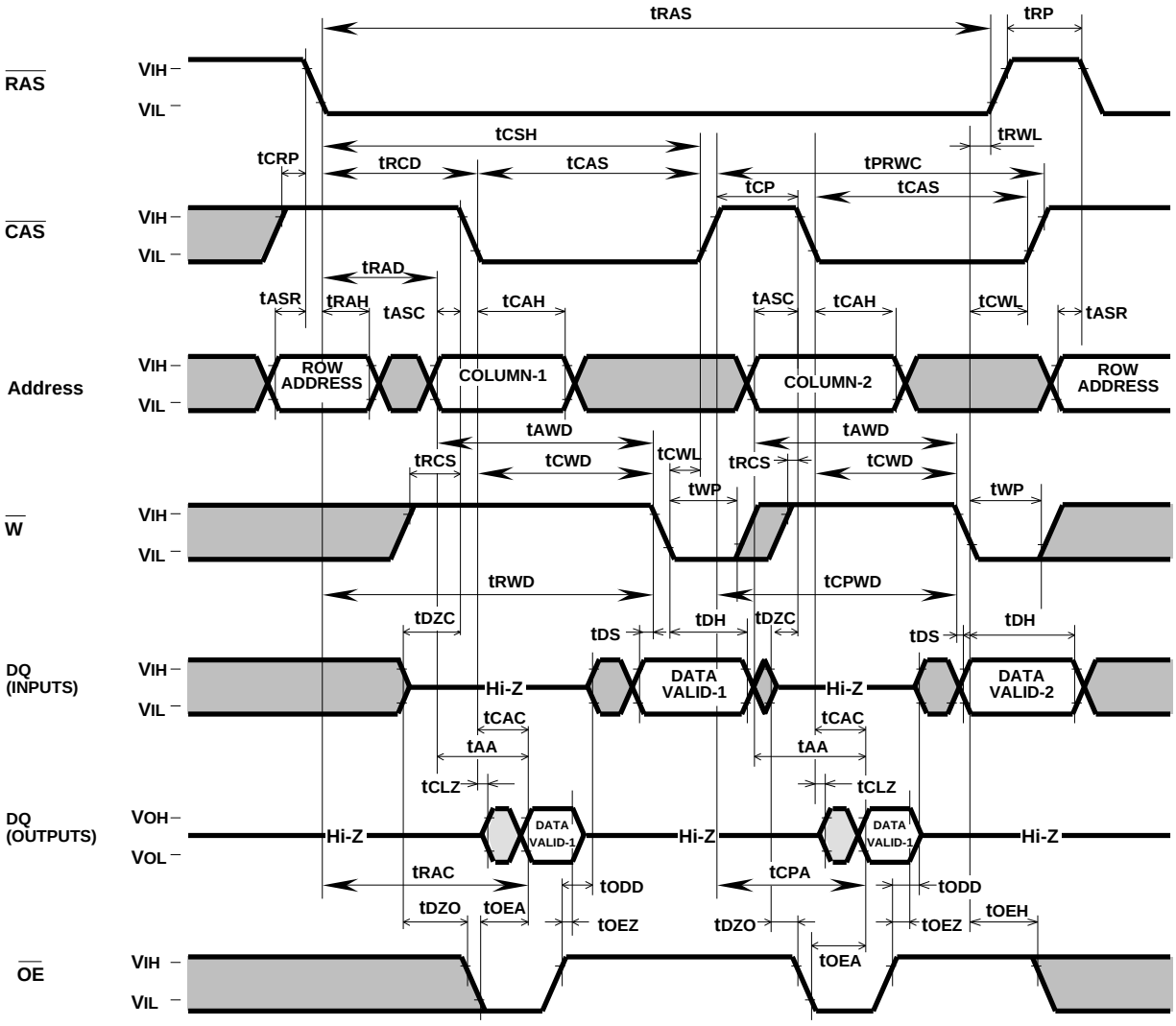
Fast Page Mode Write Cycle (Early Write)



Fast-Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write,Read-Modify-Write Cycle



Outline