MH4V36AM-6,-7

FAST PAGE MODE 150994944-BIT (4194304-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH4V36AM is an 4M word by 36-bit dynamic RAM module and consists of 2 industry standard 4M X 16 dynamic RAMs in TSOP and 1 industry standard 4M X 4(4CAS) dynamic RAMs in TSOP.

The ICs are mounted on both sides of one small ceracom PC board with flash gold plating and form a convenient 68-pin package.

FEATURES

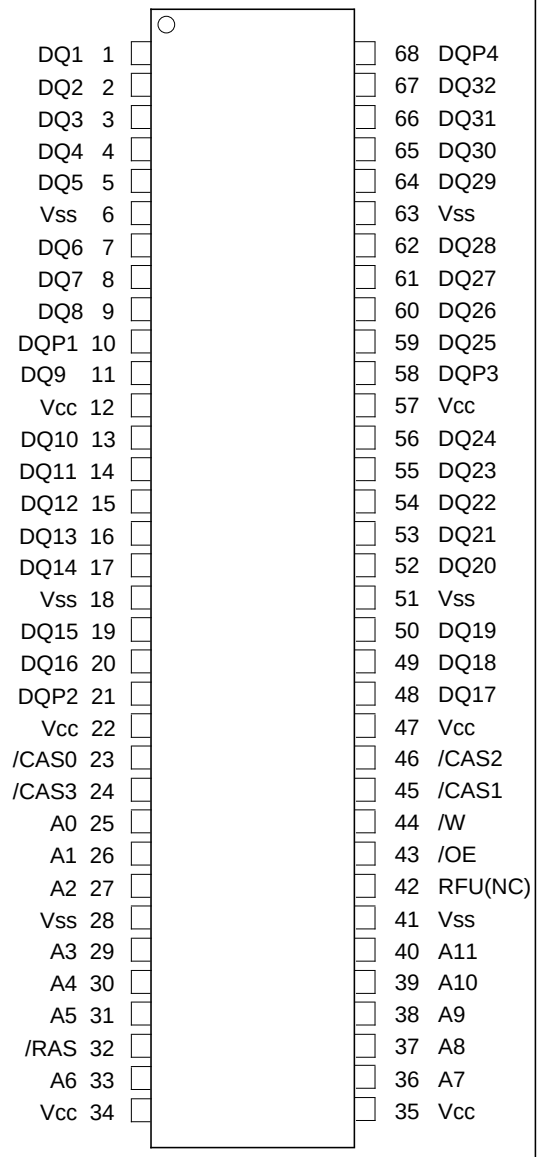
Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)
MH4V36AM-6	60	15	30	15	110
MH4V36AM-7	70	20	35	20	130

- **Utilizes industry standard 4M X 16 DRAMs in TSOP package and industry standard 4M X 4(4CAS) DRAM in TSOP package**
- **Single 3.3V +/- 0.3V supply**
- **Low stand-by power dissipation**
  5.4mW (Max) . . . . . CMOS Input level
- **Low operating power dissipation**
  MH4V36AM - 6 . . . . . 1.155W (Max)
  MH4V36AM - 7 . . . . . 1.100W (Max)
- **All inputs, output TTL compatible and low capacitance**
- **4096 refresh cycles every 64ms (A_0 ~ A_{11})**
- **Includes 2pcs 0.22uF decoupling capacitors**

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



FUNCTION

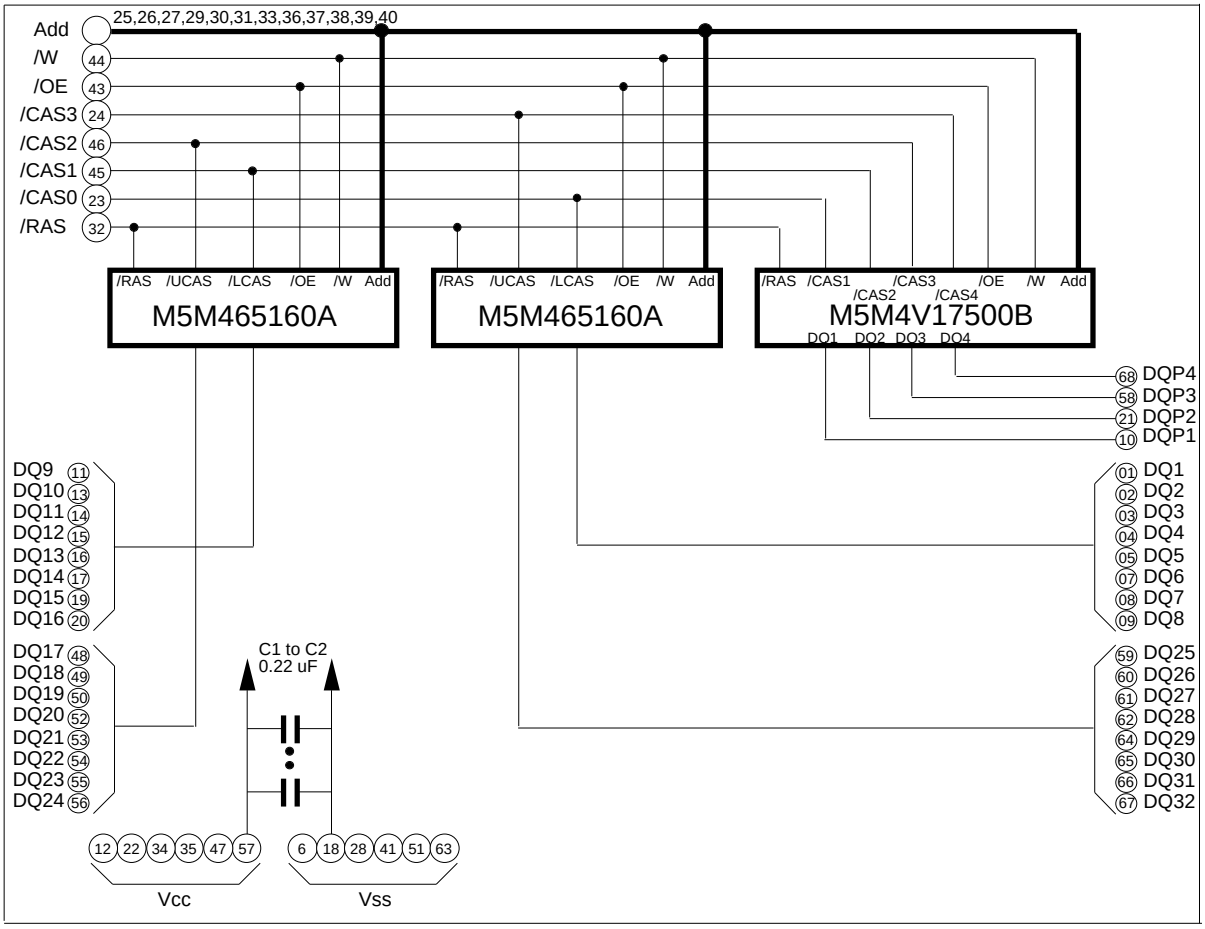
The MH4V36AM provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{CAS}$ before $\overline{RAS}$ refresh, and delayed-write. The input conditionsfor each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs				Input/Output	
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Input	Output
Read	ACT	ACT	NAC	ACT	OPN	VLD
Write	ACT	ACT	ACT	NAC	VLD	OPN
Read-modify-write	ACT	ACT	ACT	ACT	VLD	VLD
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	DNC	OPN
Hidden refresh	ACT	ACT	DNC	ACT	OPN	VLD
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5 ~ 4.6	V
VI	Input voltage		-0.5 ~ 4.6	V
V0	Output voltage		-0.5 ~ 4.6	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	3	W
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-40 ~ 100	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~70 °C , unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	3.0		3.6	V
VIL	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~70 °C, Vcc=3.3V+/- 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH=-2.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL=2.0mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V ≤ VOUT ≤ 3.6V	-10		10	µA
I I	Input current		**0V ≤ VIN ≤ 3.6V, Other inputs pins = 0V**	-30		30	µA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	-6	$\overline{RAS}$, $\overline{CAS}$ cycling tRC=tWC=min. output open			380	mA
		-7				305	
ICC2	Supply current from Vcc , stand-by		$\overline{RAS}$= $\overline{CAS}$ =VIH, output open			4	mA
			$\overline{RAS}$= $\overline{CAS}$≥Vcc -0.2V, output open			1.4	
ICC4(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	-6	$\overline{RAS}$=VIL, $\overline{CAS}$ cycling tPC=min. output open			260	mA
		-7				240	
ICC6(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	-6	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC=min. , $\overline{W}$ ≥ Vcc - 0.2 output open			380	mA
		-7				365	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be channged once or less while RAS=VIL and CAS=VIH

CAPACITANCE (Ta=0~70°C , Vcc=3.3V+/-0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (A)	Input capacitance, address inputs	VI=Vss f=1MHZ Vi=25mVrms			30	pF
CI ($\overline{OE}$)	Input capacitance, $\overline{OE}$ input				36	pF
CI ($\overline{W}$)	Input capacitance, write control input				36	pF
CI ($\overline{RAS}$)	Input capacitance, $\overline{RAS}$ input				36	pF
CI ($\overline{CAS}$)	Input capacitance, $\overline{CAS}$ input				30	pF
CI / O	Input/Output capacitance, data ports				25	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C , Vcc=3.3V +/-0.3V, Vss=0V, unless otherwise noted , see notes 6,13,14)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ (Note 7,8)		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 7,9)		60		70	ns
t_{AA}	Columu address access time (Note 7,10)		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (Note 7,11)		35		40	ns
t_{OEA}	Access time from $\overline{OE}$ (Note 7)		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low (Note 7)	5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note 12)	0	15	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (Note 12)	0	15	0	15	ns

Note 6: An initial pause of 500 µs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-Only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-2mA)/VOL=0.4V(IOL=2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OFF(max)}$ and $t_{OEZ\ (max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq$ I +/- 10 µAI) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70 °C, Vcc=3.3V +/- 0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t_{REF}	Refresh cycle time		64		64	ms
t_{RP}	$\overline{RAS}$ high pulse width	40		50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note15)	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note16)	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note17)	0	10	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note18)	0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note18)	0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note19)	15		15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data (Note19)	15		15		ns
t_T	Transition time (Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed t_T =5ns.

14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

15: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}$.

16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

18: Either t_{DZC} or t_{DZO} must be satisfied.

19: Either t_{CDD} or t_{ODD} must be satisfied.

20: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t_{RC}	Read cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{RCS}	Read Setup time after $\overline{CAS}$ high	0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ low (Note 21)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ low (Note 21)	10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t_{WC}	Write cycle time	110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	10		10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{WP}	Write pulse width	10		10		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note22)	155		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	105	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	60	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	105		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	60		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note23)	40		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note23)	85		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note23)	55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		ns
t_{WP}	Write pulse width	10		10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	10		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.
23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		45		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	85		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note25)	100	125000	115	125000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note26)	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note23)	60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26: $t_{CP(max)}$ is specified as a reference point only.

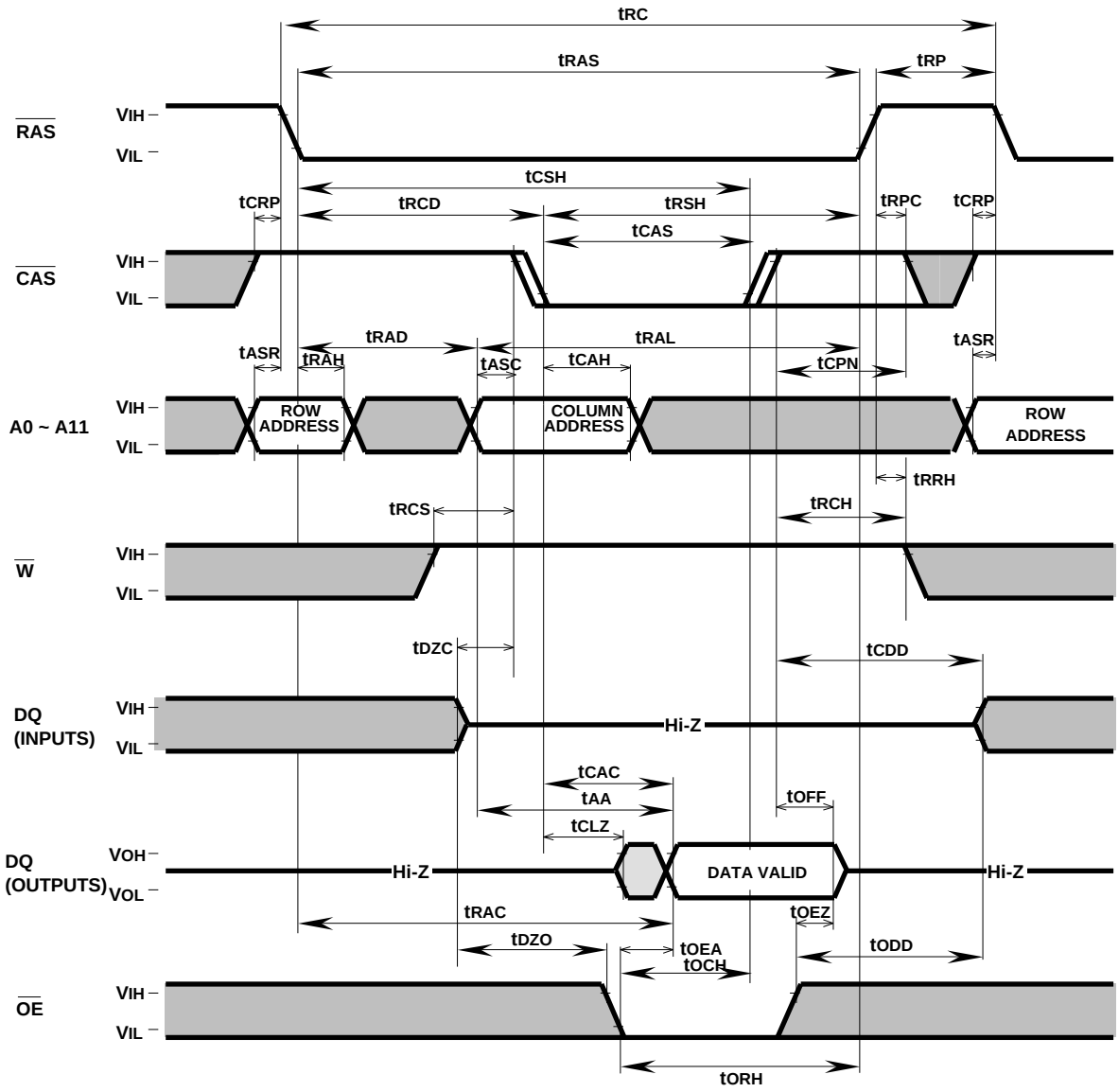
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 28)

Read Cycle



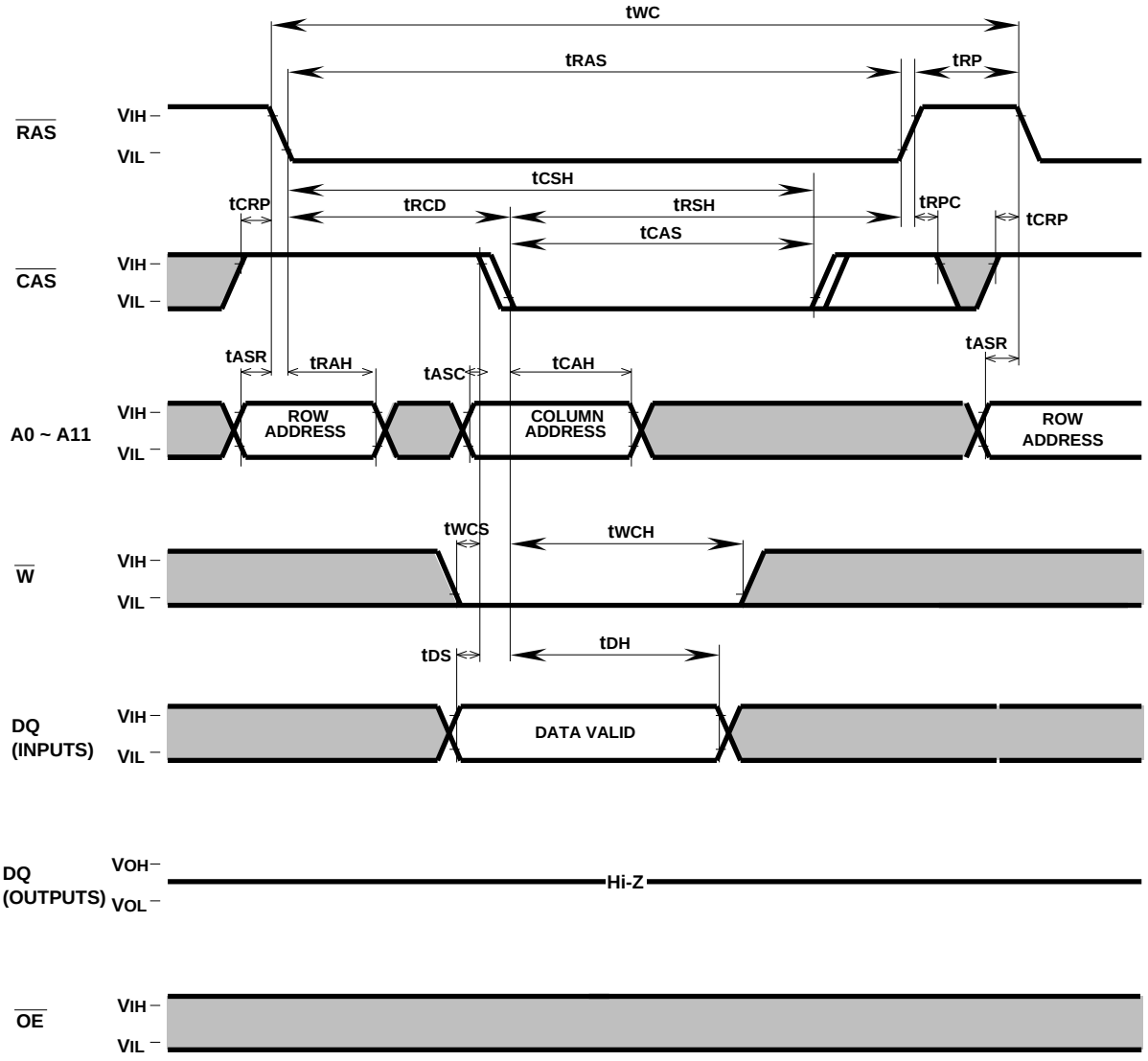
Note 28

Indicates the don't care input.
VIH(min)≤VIN≤VIH(max) or VIL(min)≤VIN≤VIL(max)

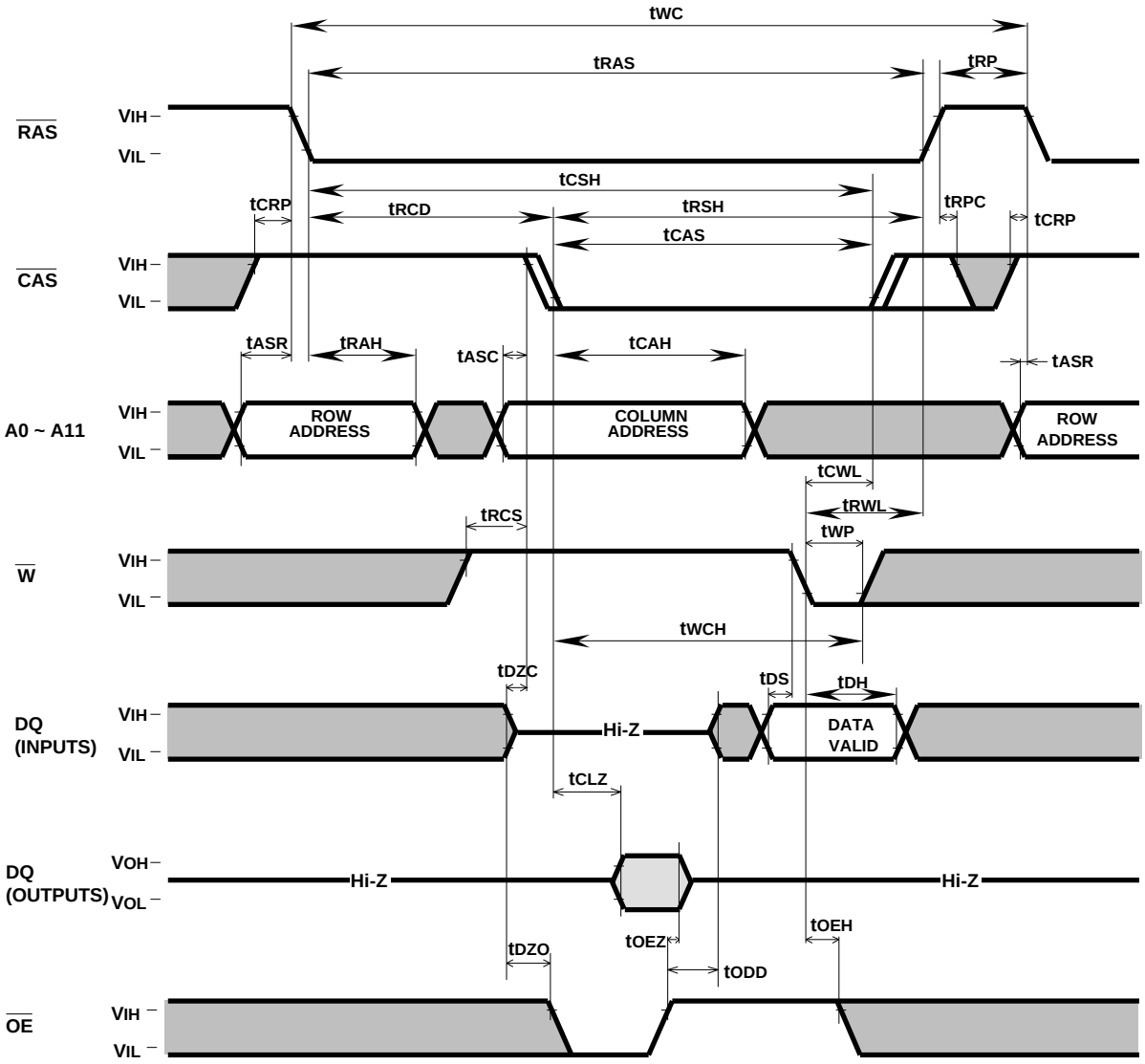
Indicates the invalid output.

Indicates the skew of the four inputs.

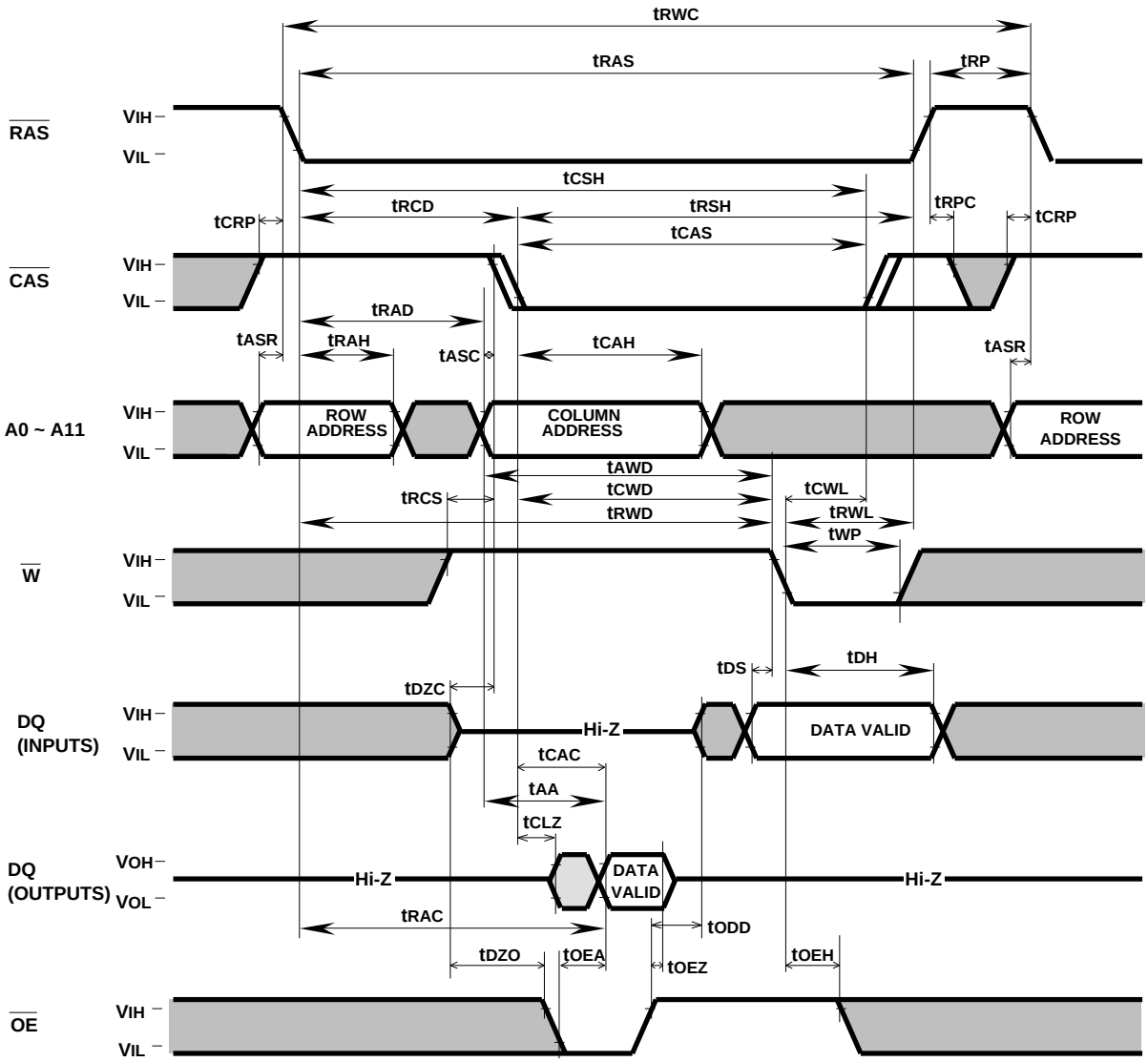
Write Cycle (Early write)



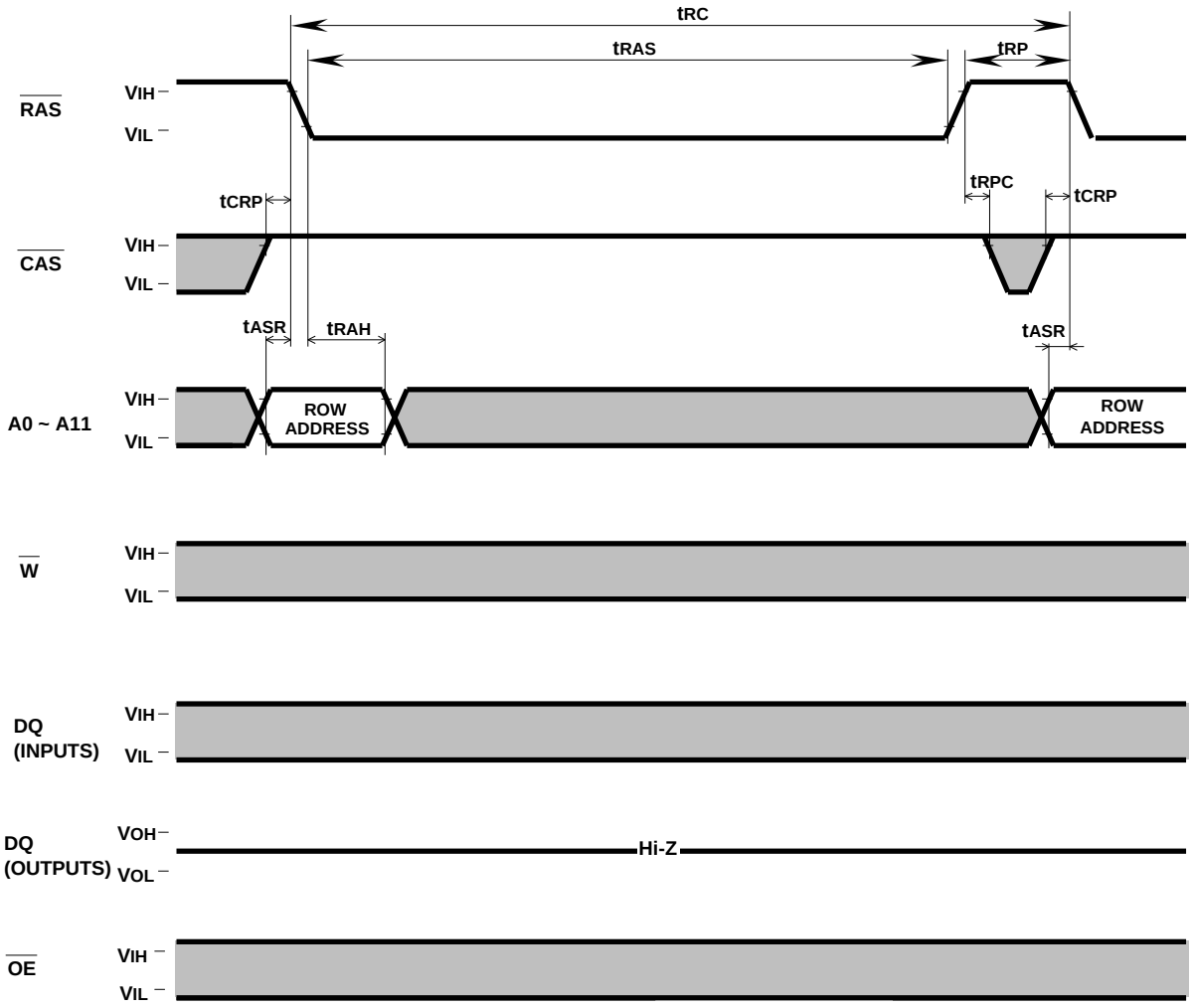
Write Cycle (Delayed write)



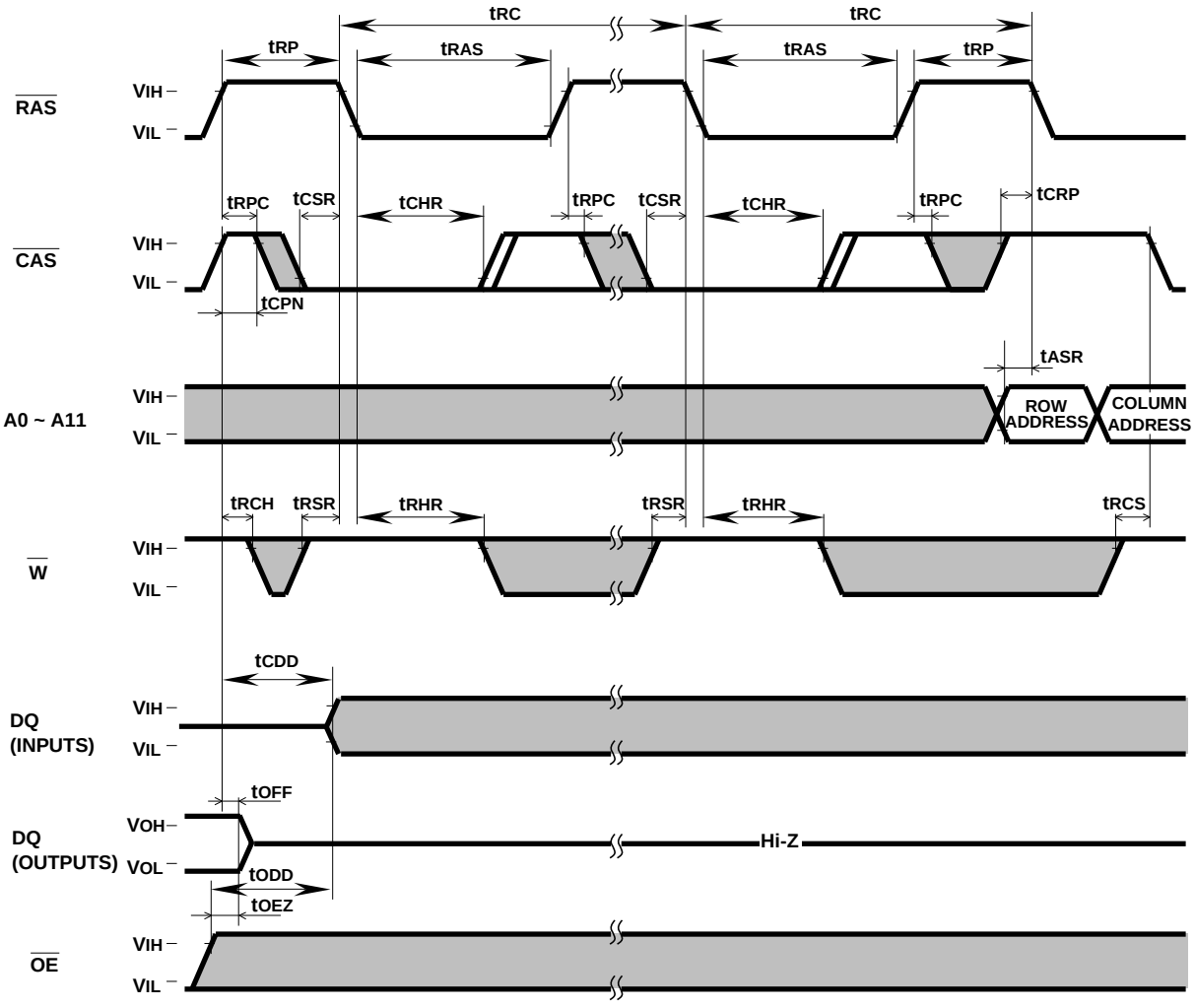
Read-Write, Read-Modify-Write Cycle



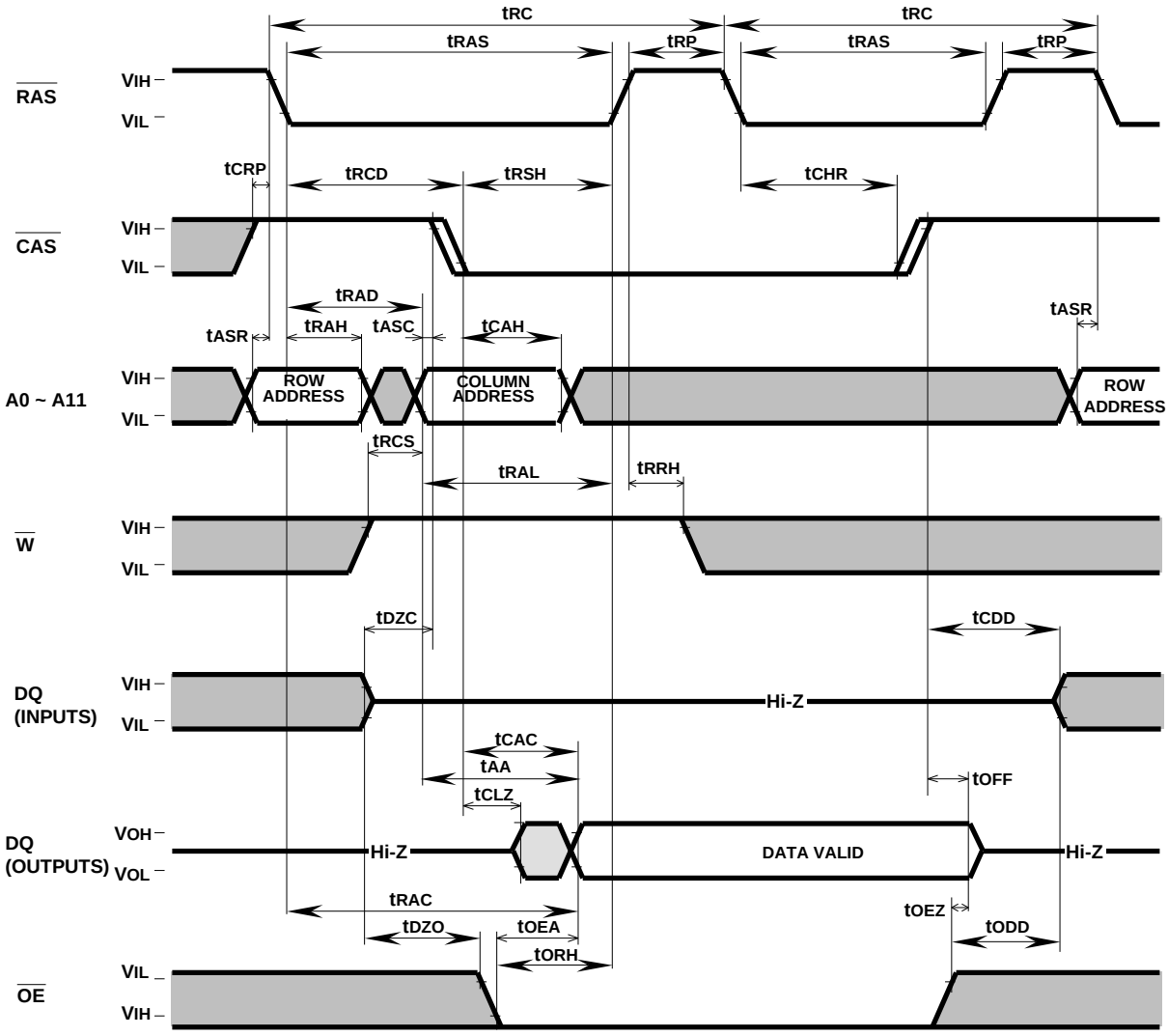
$\overline{\text{RAS}}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

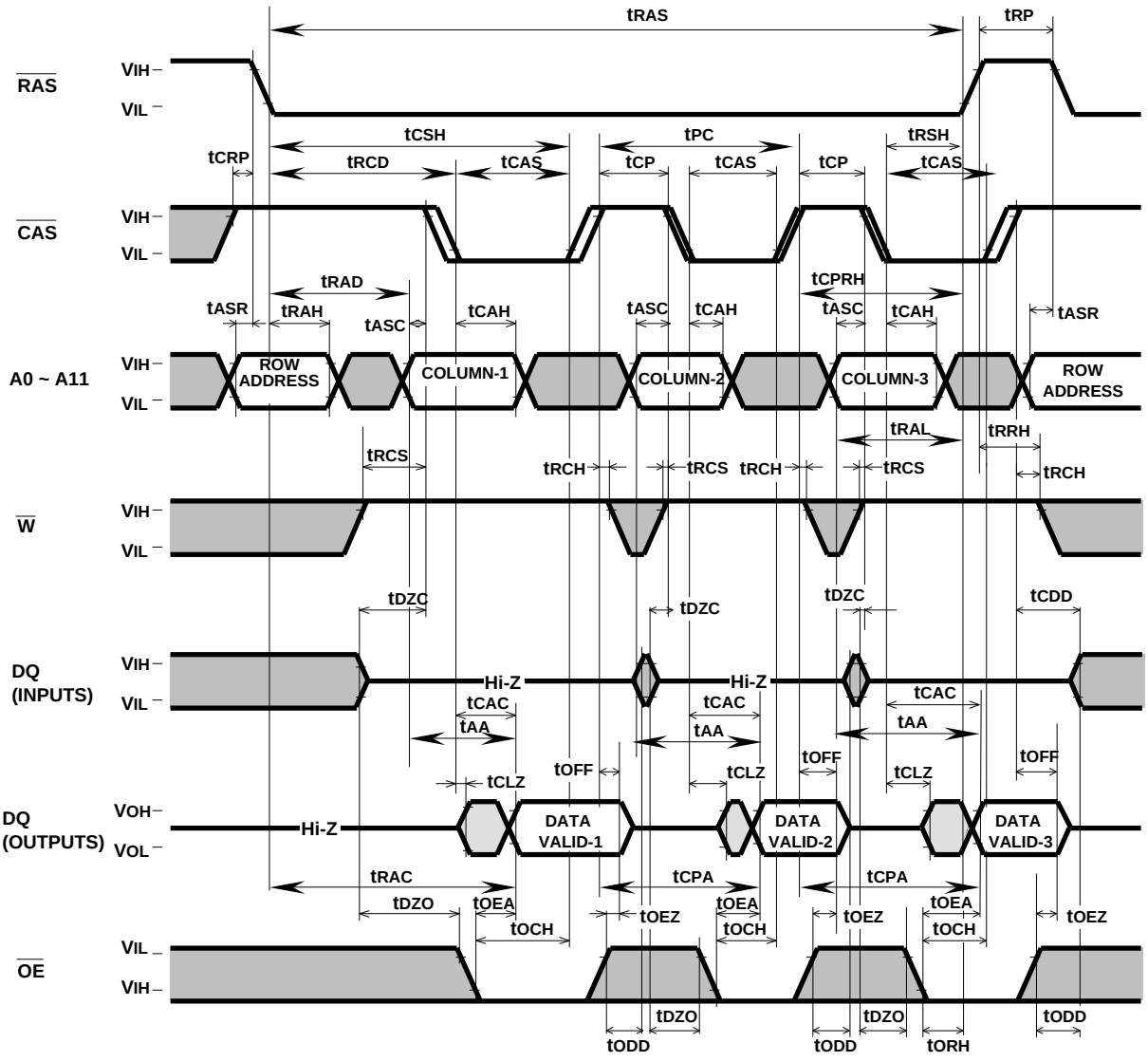


Hidden Refresh Cycle (Read) (Note 29)

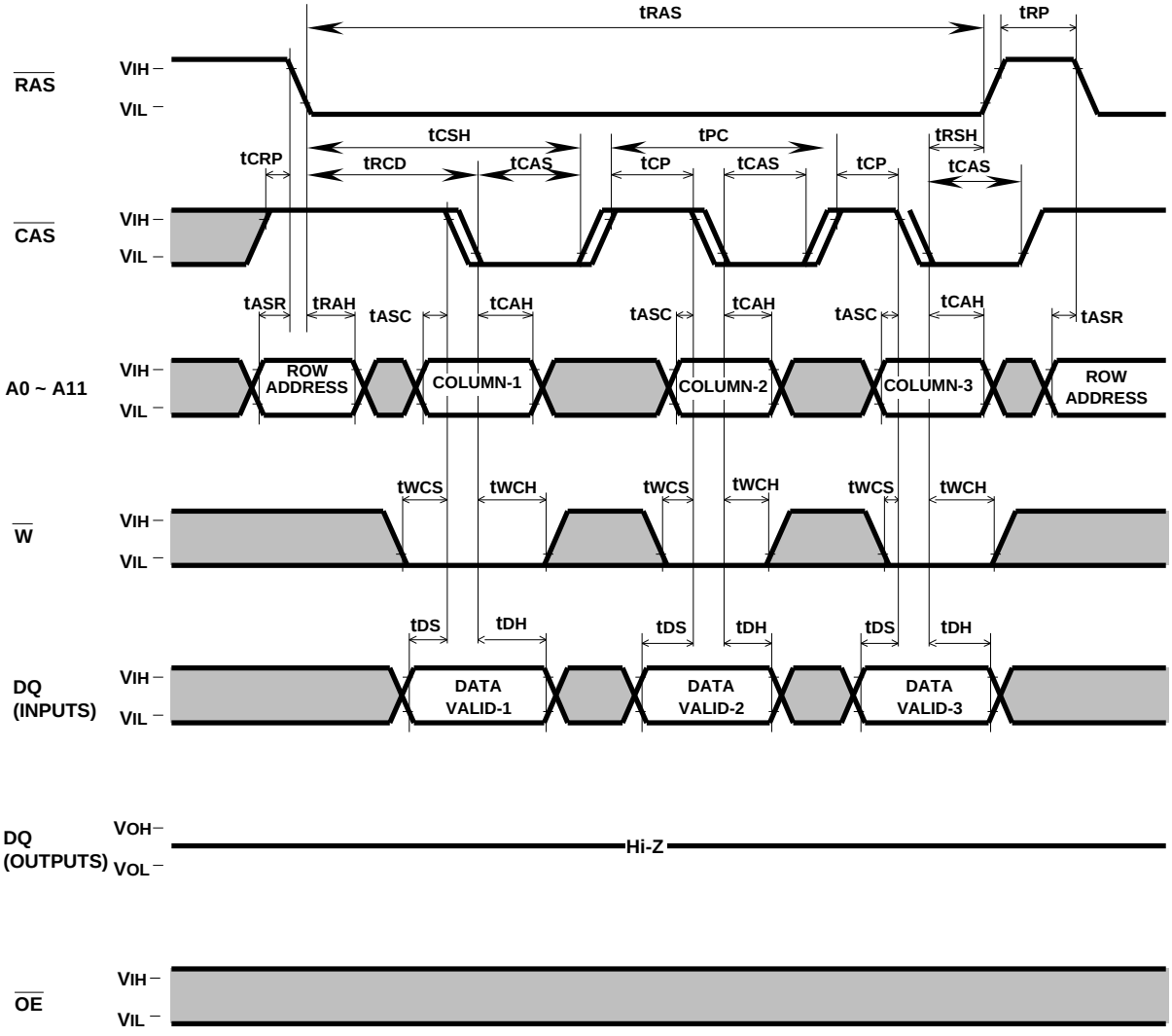


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

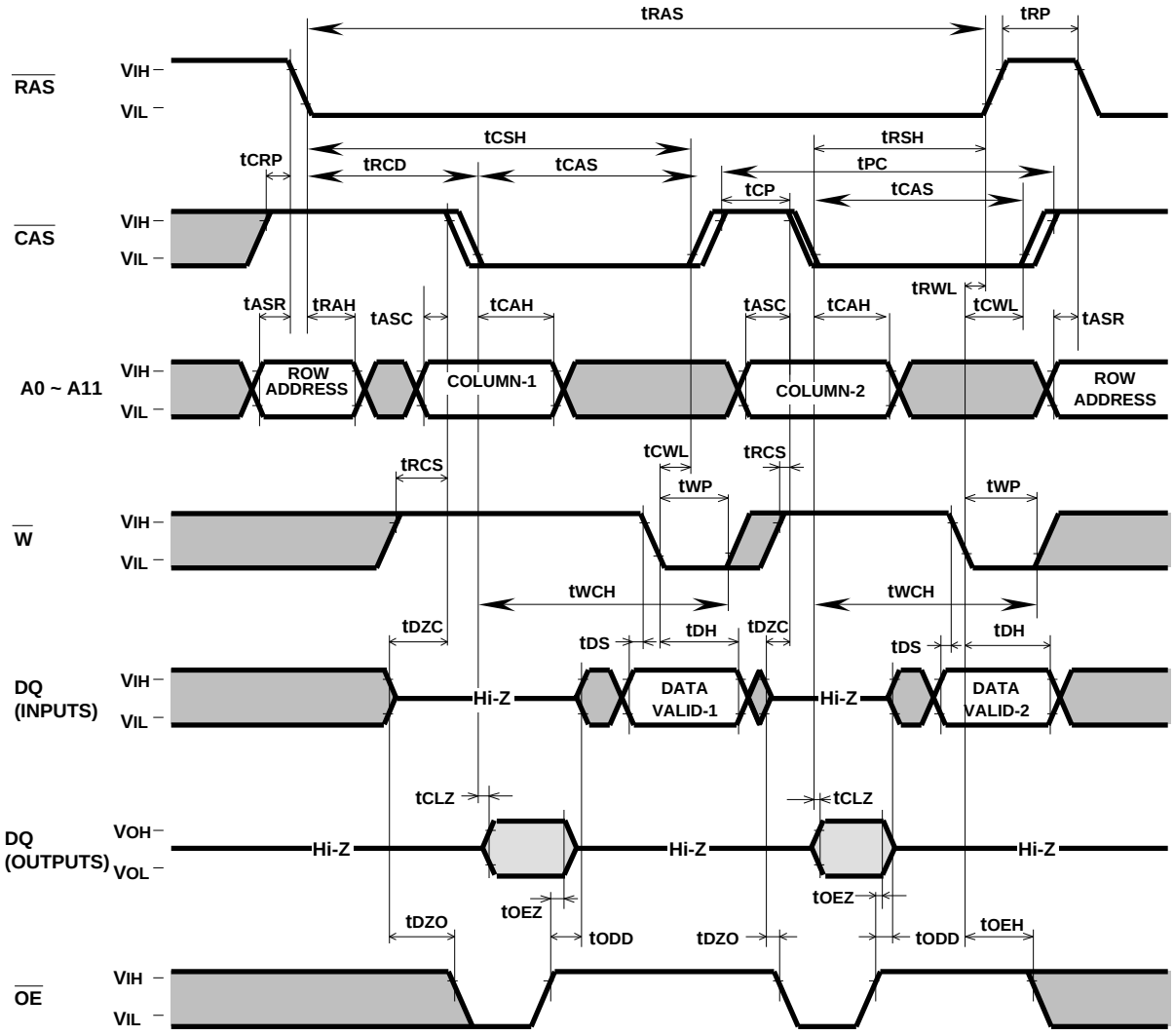
Fast Page Mode Read Cycle



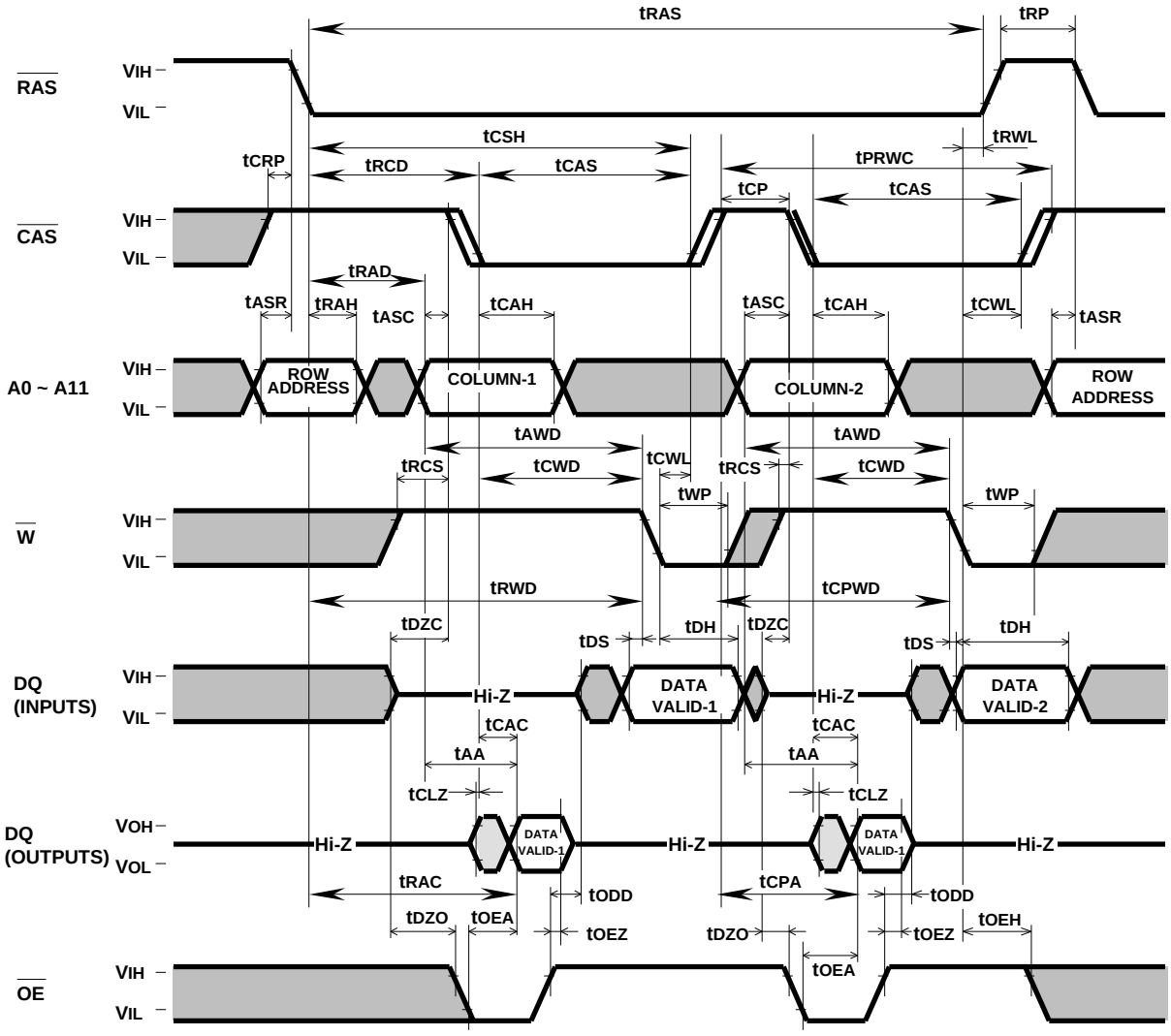
Fast Page Mode Write Cycle (Early Write)



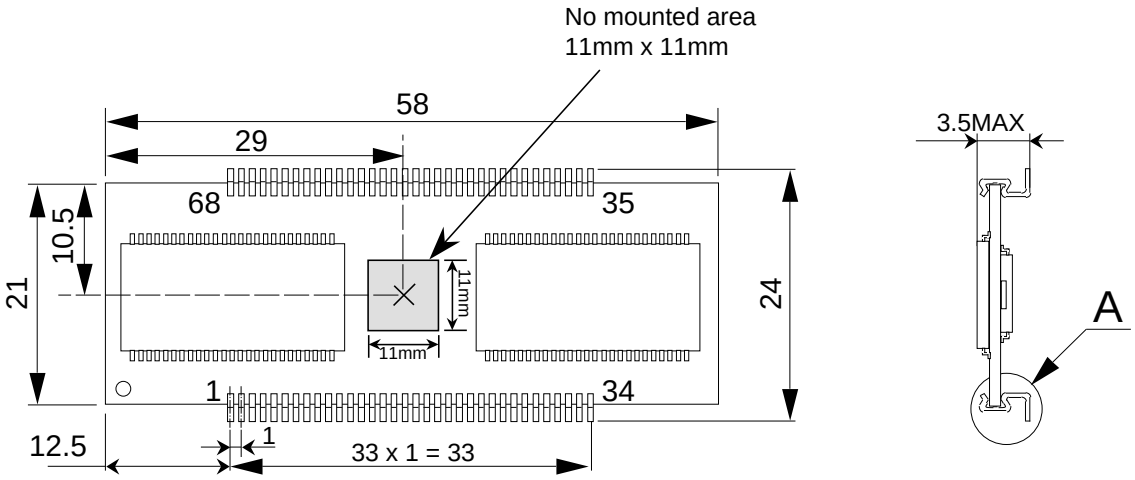
Fast-Page Mode Write Cycle (Delayed Write)

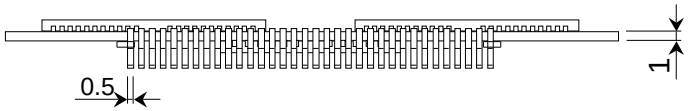


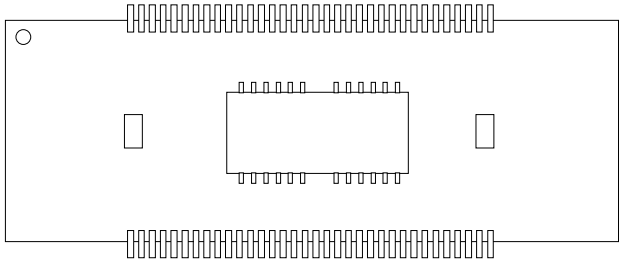
Fast Page Mode Read-Write,Read-Modify-Write Cycle

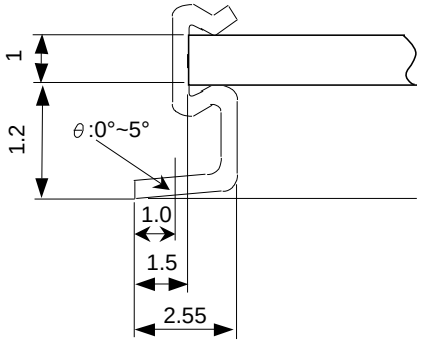


MH4V36AM OUTLINE









Detail A