

ASIC 5SE Standard Cell/Gate Array

Value ASIC for high function and price-performance applications

Highlights

- Extensive portfolio of cores for your data processing, communications, and consumer applications
- Designs up to 2.8 million gates
- Low-power libraries; low-power, high-density, compilable register arrays
- Automatic gate array fill of free space for quick turn engineering change options
- Space-saving plastic packages for cost-sensitive applications: Quad Flat Pack, Low-Profile Quad Flat Pack, Ball Grid Array
- Ceramic packages for high I/O requirements: Ball Grid Array, Column Grid Array
- Data path optimization with bit stacking for performance and density

Product Description

The IBM Blue Logic™ core program has reached the highest levels of design and production with this ASIC 5SE product. System-level-silicon is a reality for our communications, data processing, and consumer customers today. With over 50 cores introduced in 5SE, you get value and experience.

5SE is a standard cell and gate array ASIC with up to 2.8 million gates, low-power features, and a broad array of price-performance packages. It is targeted for wide application in communications, consumer, and data processing products.

The low-power, high-performance features of 5SE are available to you today.

Product Specifications

- $L_{eff} = 0.27 \mu m$, $L_{drawn} = 0.35 \mu m$
- 2.8 million wireable gates
- Power Supply (internal logic and I/O): 3.3V
- Power Dissipation of 0.18 μW /MHz/gate @ 3.3V
- Gate Delays of 145 ps @ 3.3V
- 6 levels of metal: 5 for global routing, 1 for local interconnect
- Ambient Operating Temperature Range: -40°C to 100°C
- High Reliability: Average Failure Rate 10 FITs

Packaging

5SE packaging options offer both density and price performance.

- Ceramic Ball Grid Array (CBGA): C4; 624 maximum total leads
- Ceramic Column Grid Array (CCGA): C4; 1657 maximum total leads
- Plastic Ball Grid Array (PBGA): Wire bond 529 maximum total leads (in development — 352 in production)
- Plastic Quad Flat Pack (PQFP): Wire bond 240 total leads
- Low Profile Plastic Quad Flat Pack (LQFP): Wire bond 144 total leads (in development)

IBM Blue Logic Core Program

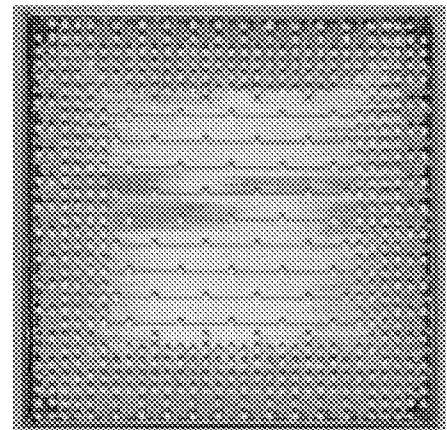
IBM's Blue Logic core program adds the value of our unique ASIC intellectual property to your ASIC design, quickly and easily. Our Blue Logic cores are designed for the communications, data processing, and consumer industries. By using cores optimized for your industry, you can quickly build and deliver to market cus-

tomers-specific products. Our experience in linking complex functions means that we can help you get to market faster and less expensively. 5SE offers a rich portfolio of cores, from processors to voice/data networking to data compression to multimedia functions.

IBM Blue Logic Design Methodology and Tools

IBM delivers first-time-right design to help reduce product development time and improve your market responsiveness. IBM Blue Logic design methodology is flexible enough to produce half-million gate ASICs and extensible enough to handle multimillion-gate designs, with seamless inclusion of your choice of cores for system-level-silicon. For your convenience, we support many industry-standard CAD tools, and to make your life even easier, we offer Blue Logic design tools with special features such as:

- *Static timing analysis*, which replaces gate-level simulation, resulting in shorter run times and maximum path checking



Embedded Memory and Macros

Function	Capability
High Performance Compilable 1-Port SRAM	Maximum size: 256K bits, Maximum words: 8192 Maximum width: 128 bits, Multiple Array Built-in Self Test 1.7 ns Access, 1.8 ns Cycle (typical, 4096 words x 32 bits)
High Performance Compilable 2-Port SRAM	Maximum size: 128K bits, Maximum words: 4096 Maximum width: 128 bits, Multiple Array Built-in Self Test 1.7 ns Access, 1.9 ns Cycle (typical, 1024 words x 32 bits)
Compilable ROM	Maximum size: 256K bits, Maximum words: 8192 Maximum width: 64 bits, Built-in Self Test 2.0 ns Access, 2.6 ns Cycle (typical, 4096 words x 32 bits)
Compilable Register Arrays 2-Port through 4-Port	Up to 10.2K bits 1.3 ns read (typical conditions, 32 words x 32 bits, 2-port)
Compilable Register Arrays 5-Port, 6-Port	Up to 5.1K bits 1.4 ns read (typical conditions, 32 words x 32 bits, 5-port)
Phase-Locked Loop (PLL)	30 MHz-500 MHz lock-in range. Fully integrated mixed-mode design. No external components. Programmable multiplication factor (1-16)

- *Automatic Test Pattern Generation (ATPG)*, which does away with the tedious, time-consuming generation of test vectors
- *A new clock distribution methodology*, which improves skew, latency, and power management
- *ASIC sign-off toolkit*, which integrates an extensive and important process into a single EDA package
- *Floorplanning*, which avoids congested areas.

IBM Blue Logic Design Services

The IBM ASIC Design Center is staffed by a team of highly experienced engineers, programmers, and technicians to provide you with expert design, development, consultation, and logical and physical processing services for every phase of CMOS chip design. Our Blue Logic services are customized to meet your specific needs through one-on-one design consultation, extensive documentation, and focused education in tools and methodology tailored to your team and your project requirements.

Input/Output Library Elements

- LVCMOS/LVTTL, GTL, PCI, SCSI, PECL, AGP, USB, LVDS
- Three-state, push-pull, open drain drivers with transceiver option
- Slew rate control

- Output buffer impedance options: 20, 35, 50, 65 ohms
- ESD protection $\geq 3.0\text{kV}$

Internal Library Elements (Multiple drive strengths available)

5SE typical power dissipation is $0.18\mu\text{W}/\text{MHz/gate}$ at 3.3V operation. All library elements are available in three to five drive strengths, and a set of the most commonly used elements is available in three additional lower drive strengths for further power reduction.

- AND/NAND-OR/NOR (2 to 4 inputs)
- Decoders
- Multiplexer
- AND-OR/AND-OR-INVERT
- Full Adder
- OR-AND/OR-AND-INVERT
- Clock Timing Terminators
- XOR/XNOR (2 or 3 inputs)
- Clock Drivers, Splitters, and Choppers with balanced rise/fall times
- Comparators
- Delay Line
- Data Path Elements

Full-Scan Latch Library Elements (Multiple drive strengths available)

- D Latches (1 and 2 Ports)
- Set-Reset Latches
- Scannable D Flip-Flops



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