

# DATA SHEET

## **TEA1210TS**

High efficiency, high current DC/DC  
converter

Preliminary specification  
File under Integrated Circuits, IC03

1999 Mar 08

## High efficiency, high current DC/DC converter

## TEA1210TS

### FEATURES

- Fully integrated DC/DC converter circuit, featuring internal very low  $R_{DSon}$  power MOSFETs
- Up-or-down conversion
- Start-up from 1.85 V input voltage
- Adjustable output voltage
- High efficiency over large load range
- 600 kHz switching frequency
- Low quiescent power consumption
- Synchronizing with external clock
- Two selectable current limits for efficient battery use in case of dynamic loads
- Up to 100% duty cycle in down mode
- Undervoltage lockout
- Shut-down function
- 16-pin small body SSOP16 package.

### APPLICATIONS

- Cellular phones, Personal Digital Assistants (PDAs) and others
- Supply voltage source for low-voltage chip sets
- Portable computers
- Battery backup supplies.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1210TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

### GENERAL DESCRIPTION

The TEA1210TS is a fully integrated DC/DC converter. Efficient, compact and dynamic power conversion is achieved using a novel digitally controlled concept like Pulse Width Modulation (PWM) or Pulse Frequency Modulation (PFM), integrated low R CMOS power switches with low parasitic capacitances, and fully synchronous rectification.

The device operates at 600 kHz switching frequency which enables the use of external components with minimum size. The switching frequency can be locked to an external high-frequency clock.

Optionally, the device can be kept in the Pulse Width Modulation (PWM) mode regardless of the load applied.

Deadlock is prevented by an on-chip undervoltage lockout circuit.

Two selectable current limits in upconversion mode enable efficient battery use even at highly dynamic loads such as cellular phone electronics.

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**QUICK REFERENCE DATA**

$T_{amb} = -40$  to  $+80$  °C; all voltages measured with respect to ground; positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Voltage levels</b>						
UPCONVERSION; pin $\bar{U}/D = \text{LOW}$						
$V_I$	input voltage		$V_{I(\text{start})}$	–	5.50	V
$V_O$	output voltage		2.90	–	5.50	V
$V_{I(\text{start})}$	start-up input voltage	$I_L < 200$ mA	1.20	1.60	1.85	V
$V_{I(\text{uvlo})}$	undervoltage lockout input voltage		1.50	2.10	2.70	V
DOWNCONVERSION; pin $\bar{U}/D = \text{HIGH}$						
$V_I$	input voltage		2.90	–	5.50	V
$V_O$	output voltage		1.30	–	5.50	V
<b>GENERAL</b>						
$V_{fb}$	feedback input voltage		1.20	1.25	1.30	V
$\Delta V_{\text{window}}$	output voltage window	PWM mode	1.5	2.0	3.0	%
<b>Current levels</b>						
$I_q$	quiescent current on pins LX	$V_I = 2.40$ V; $V_O = 3.60$ V	100	125	150	$\mu\text{A}$
$I_{\text{shdwn}}$	current in shut-down mode		–	2	10	$\mu\text{A}$
$\Delta I_{\text{lim}(\text{up})}$	current limit deviation in up mode	$I_{\text{lim}(\text{up})}$ set to 2.0 A	–12	–	+12	%
$I_{\text{lim}(\text{down})}$	current limit in down mode			4.8		A
$I_{LX}$	maximum continuous current on pins LX	$T_{amb} = 60$ °C	–	–	1.8	A
<b>Power MOSFETs</b>						
$R_{DSon(N)}$	drain-to-source on-state resistance NFET	$T_j = 27$ °C	–	56	63	m $\Omega$
$R_{DSon(P)}$	drain-to-source on-state resistance PFET	$T_j = 27$ °C	–	68	77	m $\Omega$
<b>Efficiency</b>						
$\eta$	efficiency upconversion	$V_I = 2.4$ V; $V_O = 3.6$ V; $T_{amb} = 20$ °C $I_L = 1$ mA $I_L = 100$ mA $I_L = 500$ mA $I_L = 1.5$ A; not continual	83 90 92 84	86 93 94 86	– – – –	% % % %
<b>Timing</b>						
$f_{sw}$	switching frequency	PWM mode	480	600	720	kHz
$f_{sync}$	synchronization clock input frequency		9	13	20	MHz
$t_{res}$	response time	from standby to $P_{o(\text{max})}$	–	25	–	$\mu\text{s}$



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## PINNING

SYMBOL	PIN	DESCRIPTION
UPOUT	1, 16	output voltage in up mode; input voltage in down mode
SYNC	2	synchronization clock input
SHDWN	3	shut-down input
LX	4, 5, 12, 13	inductor connection
$\bar{U}/D$	6	up-or-down mode selection input; active LOW for up mode
ILIMH	7	current limiting resistor 1 connection
GND	8, 9	ground
ILIML	10	current limiting resistor 2 connection
ILIMSEL	11	current limiting selection input
PWM	14	PWM-only mode selection input
FB	15	feedback input

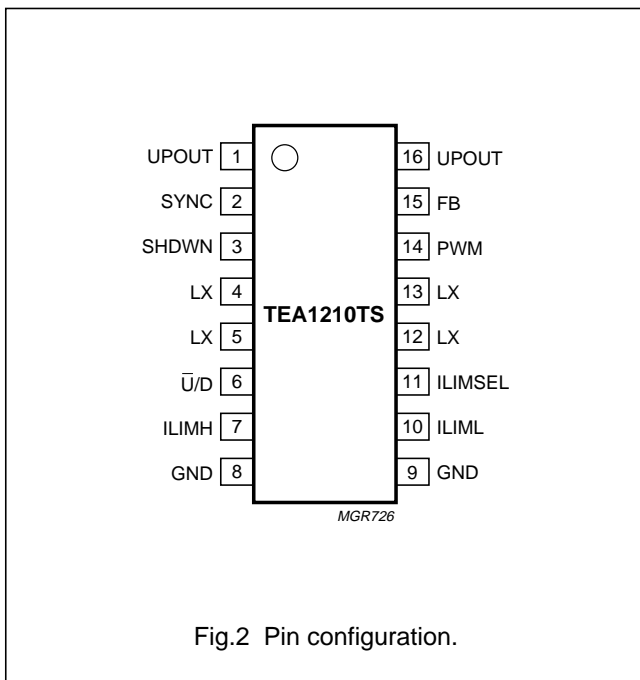


Fig.2 Pin configuration.

For all possible applications, the following groups of pins must be connected together:

- Pins 4, 5, 12 and 13 (pins LX)
- Pins 1 and 16 (pins UPOUT)
- Pins 8 and 9 (pins GND).

## FUNCTIONAL DESCRIPTION

### Control mechanism

The TEA1210TS DC/DC converter is able to operate in PFM (discontinuous conduction) or PWM (continuous conduction) operating mode. All switching actions are completely determined by a digital control circuit which uses the output voltage level as its control input. This novel digital approach enables the use of a new pulse width and frequency modulation scheme, which ensures optimum power efficiency over the complete operating range of the converter.

When high output power is requested, the device will operate in PWM (continuous conduction) operating mode. This results in minimum AC currents in the circuit components and hence optimum efficiency, cost and EMC. In this operating mode, the output voltage is allowed to vary between two predefined voltage levels. As long as the output voltage stays within this so-called window, switching continues in a fixed pattern. When the output voltage reaches one of the window borders, the digital controller immediately reacts by adjusting the pulse width and inserting a current step in such a way that the output voltage stays within the window with higher or lower current capability. This approach enables very fast reaction to load variations. Figure 3 shows the converter's response to a sudden load increase. The upper trace shows the output voltage. The ripple on top of the DC level is a result of the current in the output capacitor, which changes in sign twice per cycle, times the capacitor's internal Equivalent Series Resistance (ESR). After each ramp-down of the inductor current, i.e. when the ESR effect increases the output voltage, the converter determines what to do in the next cycle. As soon as more load current is taken from the output the output voltage starts to decay.

When the output voltage becomes lower than the low limit of the window, a corrective action is taken by a ramp-up of the inductor current during a much longer time. As a result, the DC current level is increased and normal PWM control can continue. The output voltage (including ESR effect) is again within the predefined window.

Figure 4 depicts the spread of the output voltage window. The absolute value is most dependent on spread, while the actual window size is not affected. For one specific device, the output voltage will not vary more than 2% typically.

In low output power situations, the TEA1210TS will switch over to PFM (discontinuous conduction) operating mode in case the PWM-only mode is not active.

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In the PFM mode, regulation information from earlier PWM operating modes is used. This results in optimum inductor peak current levels in the PFM mode, which are slightly larger than the inductor ripple current in the PWM mode. As a result, the transition between PFM and PWM mode is optimum under all circumstances. In the PFM mode, TEA1210TS regulates the output voltage to the high window limit shown in Fig.3.

### Synchronous rectification

For optimum efficiency over the whole load range, synchronous rectifiers inside the TEA1210TS ensure that during the whole second switching phase, all inductor current will flow through the low-ohmic power MOSFETs. Special circuitry is included which detects that the inductor current reaches zero. Following this detection, the digital controller switches off the power MOSFET and proceeds regulation.

### PWM-only mode

When pin PWM is pulled to HIGH-level in the upconversion mode, the TEA1210TS will use PWM regulation independent of the load applied. As a result, the switching frequency does not vary over the whole load range. Furthermore, the P-type power MOSFET is always on when the input voltage exceeds the target output voltage. The internal synchronous rectifier still takes care

that the inductor current does not fall below zero. In this way, the achieved efficiency is higher than in standard PWM-controlled converters.

### Start-up

Start-up from low input voltage in boost mode is realized by an independent start-up oscillator, which starts switching the N-type power MOSFET as soon as the voltage on pins UPOUT is measured to be sufficiently high. The switch actions of the start-up oscillator will increase the output voltage. As soon as the output voltage is high enough for normal regulation, the digital control system takes over the control of the power MOSFETs.

### Undervoltage lockout

As a result of too high load or disconnection of the input power source, the output voltage can drop so low that normal regulation cannot be guaranteed. In that case, the device switches back to start-up mode. If the output voltage drops down even further, switching is stopped completely.

### Shut-down

When the shut-down input is made HIGH, the converter disables both switches and power consumption is reduced to a few microamperes.

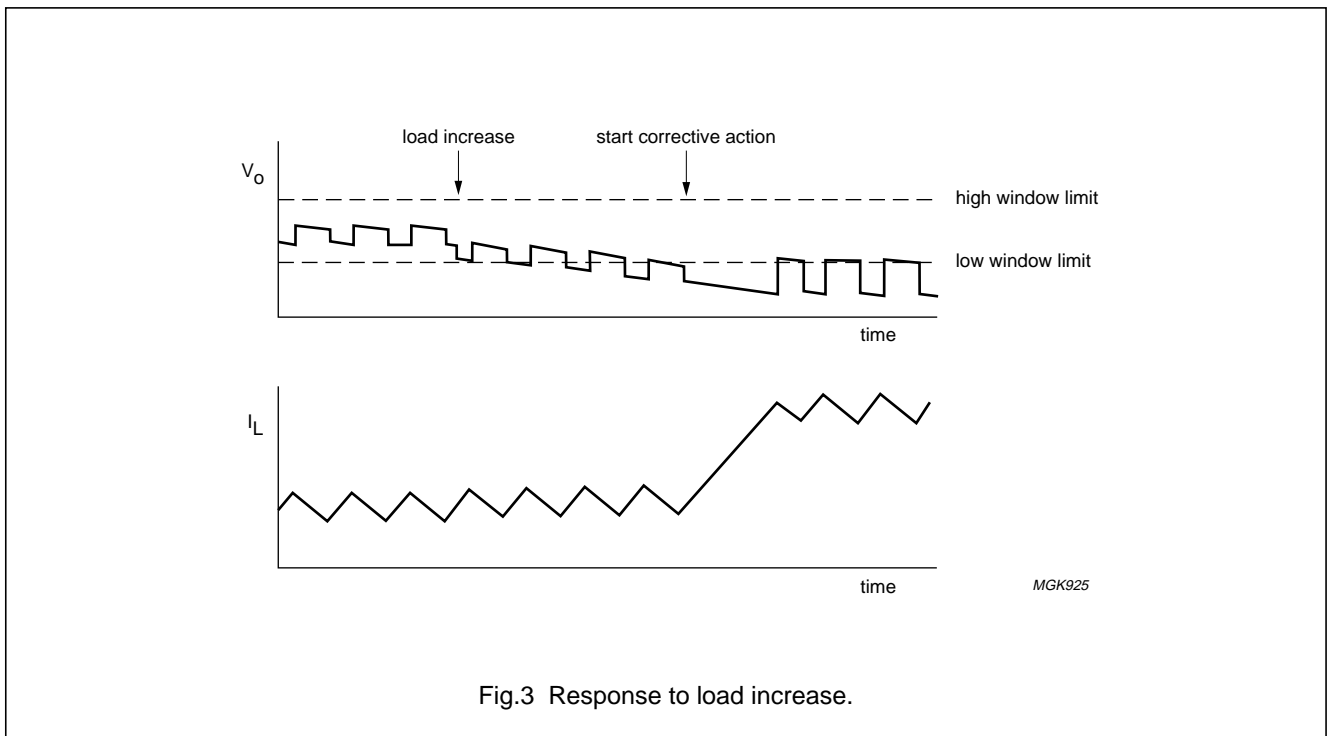


Fig.3 Response to load increase.

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### Power switches

The power switches in the IC are one N-type and one P-type power MOSFET, having a typical drain-to-source resistance of 56 and 68 mΩ respectively. The maximum average current in the power switches is 1.8 A at  $T_{amb} = 60\text{ }^{\circ}\text{C}$ .

### Temperature protection

When the device operates in the PWM mode, and the die temperature gets too high (typically 175 °C), the converter stops operating. It resumes operation when the die temperature falls below 175 °C again. As a result, low-frequent cycling between on and off state will occur. It should be noted that in the event of device temperatures around the cut-off limit, the application differs strongly from maximum specifications.

### Current limiters

If the current in one of the power switches exceeds its limit in the PWM mode, the current ramp is stopped immediately, and the next switching phase is entered. Current limiting is required to keep power conversion efficient during temporary high loads. Furthermore, current limiting protects the IC against overload conditions, inductor saturation, etc.

In the upconversion mode, the first current limit is set by an external resistor connected between the pins ILIMH and UPOUT and the second current limit is set by an external resistor connected between the pins ILIML and UPOUT. The digital signal on the current limiting selection input determines which resistor sets the limit level (pin ILIMSEL = HIGH results in the use of pin ILIMH). The current limiting selection input can accept a digital signal having a HIGH-level of just 55% of the voltage on pins UPOUT. The noise margin on this input is increased by a low-pass filter, having a cutoff frequency of about 50 MHz. However, for stability reasons the level on the current limiting selection input shall not change within a period shorter than 20 ms.

In case just one current limit is sufficient, the unused pin (pin ILIML or ILIMH) must be connected either to the other pin (pin ILIMH or ILIML), or to pin UPOUT.

In the downconversion mode, the current limiting level is set internally at a fixed value which is higher than the current level that most applications require. It should be regarded as a protection function only. In the downconversion mode, pins ILIMH and ILIML must be connected to pin UPOUT.

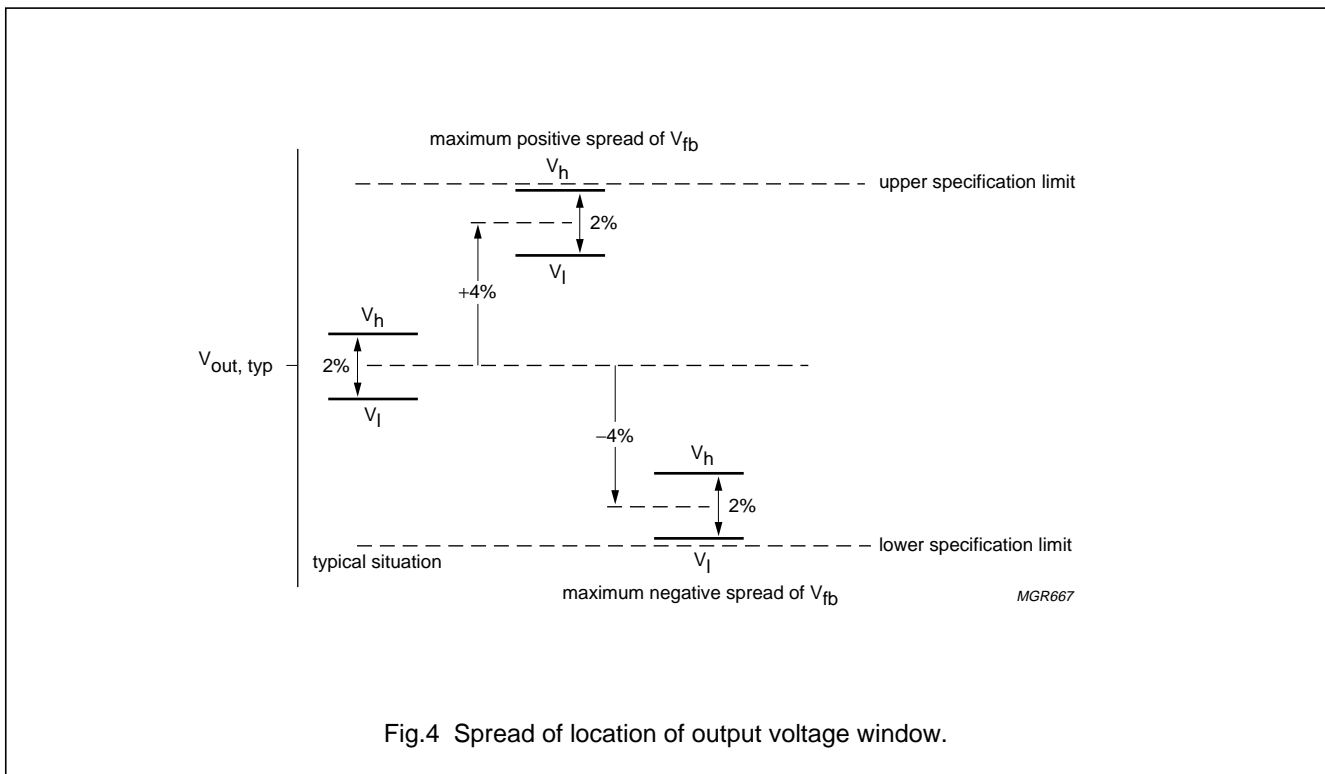


Fig.4 Spread of location of output voltage window.

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**External synchronization**

If an external high-frequency clock is applied to the synchronization clock input, the switching frequency in PWM mode will be exactly that frequency divided by 22. In PFM mode, the switching frequency is always lower. The quiescent current of the device increases when an external clock is applied. In case no external synchronization is necessary, the synchronization clock input must be connected to ground level.

**Behaviour at input voltage exceeding the specified range**

In general, an input voltage exceeding the specified range is not recommended since instability may occur. There are two exceptions:

- Upconversion: at an input voltage higher than the target output voltage, but up to 6 V, the converter will stop switching. As long as the device is in the PWM mode, the internal P-type power MOSFET will be conducting and the output voltage will equal  $V_I$  minus some resistive

voltage drop. In case the converter is in the PFM mode at high input voltage, the output voltage will equal  $V_I$  minus the voltage drop over the external diode. The current limiting function is not active.

- Downconversion: when the input voltage is lower than the target output voltage, but higher than 2.9 V, the P-type power MOSFET will stay conducting resulting in an output voltage being equal to the input voltage minus some resistive voltage drop. The current limiting function remains active.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_n$	voltage on any pin	shut-down mode	-0.2	+6.5	V
		operating mode	-0.2	+5.9	V
$T_j$	junction temperature		-40	+150	°C
$T_{amb}$	operating ambient temperature		-40	+80	°C
$T_{stg}$	storage temperature		-40	+125	°C
$V_{es}$	electrostatic handling	human body model; note 1	-1500	+1500	V
		machine model; note 2	-300	+300	V

**Notes**

1. Equivalent to discharging a 100 pF capacitor through a 1.5 k $\Omega$  resistor.
2. Equivalent to discharging a 200 pF capacitor via a 0.75  $\mu$ H inductor.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	140	K/W

**QUALITY SPECIFICATION**

Product lifetime is fully guaranteed over 2000 hours of operation at an ambient temperature of 60 °C with a continuously repeating current profile on pins LX of 4 A during 577  $\mu$ s followed by 1 A during 4.0 ms. All remaining quality specifications are in accordance with "SNW-FQ-611 part E".



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**CHARACTERISTICS**

$T_{amb} = -40$  to  $+80$  °C; all voltages are measured with respect to ground; positive currents flow into the IC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Voltage levels</b>						
UPCONVERSION; pin $\bar{U}/D = \text{LOW}$						
$V_I$	input voltage		$V_{I(\text{start})}$	–	5.50	V
$V_O$	output voltage		2.90	–	5.50	V
$V_{I(\text{start})}$	start-up input voltage	$I_L < 200$ mA	1.20	1.60	1.85	V
$V_{I(\text{uvlo})}$	undervoltage lockout input voltage	note 1	1.50	2.10	2.70	V
DOWNCONVERSION; PIN $\bar{U}/D = \text{HIGH}$						
$V_I$	input voltage	note 2	2.90	–	5.50	V
$V_O$	output voltage		1.30	–	5.50	V
GENERAL						
$V_{fb}$	feedback input voltage		1.20	1.25	1.30	V
$\Delta V_{\text{window}}$	output voltage window	PWM mode	1.5	2.0	3.0	%
<b>Current levels</b>						
$I_q$	quiescent current on pins LX	up mode; note 3	100	125	150	$\mu\text{A}$
$I_{\text{shdwn}}$	current in shut-down mode		–	2	10	$\mu\text{A}$
$\Delta I_{\text{lim}(\text{up})}$	current limit deviation in up mode	note 4 $I_{\text{lim}(\text{up})}$ set to 0.4 A $I_{\text{lim}(\text{up})}$ set to 2.0 A	–20 –12	– –	+20 +12	% %
$I_{\text{lim}(\text{down})}$	current limit in down mode		–	4.8	–	A
$I_{LX}$	maximum continuous current on pins LX	$T_{amb} = 80$ °C	–	–	1.5	A
		$T_{amb} = 60$ °C	–	–	1.8	A
$I_{\text{UPOUT}}$	maximum continuous current on pins UPOUT	up mode; $V_I = 1.8$ V; $V_O = 3.6$ V; $T_{amb} = 80$ °C	–	–	0.65	A
<b>Power MOSFETs</b>						
$R_{\text{DSon}(\text{N})}$	drain-to-source on-state resistance NFET	$T_j = 27$ °C	–	56	63	m $\Omega$
		$T_j = 100$ °C	–	75	84	m $\Omega$
$R_{\text{DSon}(\text{P})}$	drain-to-source on-state resistance PFET	$T_j = 27$ °C	–	68	77	m $\Omega$
		$T_j = 100$ °C	–	92	104	m $\Omega$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Efficiency</b>							
$\eta_1$	efficiency upconversion	$T_{amb} = 20\text{ }^\circ\text{C};$ $V_I = 1.8\text{ V}; V_O = 3.6\text{ V};$ note 5					
			$I_L = 1\text{ mA}$	80	82	–	%
			$I_L = 4\text{ mA}$	84	86	–	%
			$I_L = 100\text{ mA}$	89	91	–	%
			$I_L = 500\text{ mA}$	89	91	–	%
	$I_L = 1.5\text{ A};$ note 6	73	75	–	%		
$\eta_2$	efficiency upconversion	$T_{amb} = 80\text{ }^\circ\text{C};$ $V_I = 1.8\text{ V}; V_O = 3.6\text{ V};$ note 5					
			$I_L = 1\text{ mA}$	78	80	–	%
			$I_L = 4\text{ mA}$	82	84	–	%
			$I_L = 100\text{ mA}$	87	89	–	%
			$I_L = 500\text{ mA}$	88	90	–	%
	$I_L = 1.5\text{ A};$ note 6	67	72	–	%		
$\eta_3$	efficiency upconversion	$T_{amb} = 20\text{ }^\circ\text{C};$ $V_I = 2.4\text{ V}; V_O = 3.6\text{ V};$ note 5					
			$I_L = 1\text{ mA}$	83	86	–	%
			$I_L = 4\text{ mA}$	87	90	–	%
			$I_L = 100\text{ mA}$	90	93	–	%
			$I_L = 500\text{ mA}$	92	94	–	%
	$I_L = 1.5\text{ A};$ note 6	84	86	–	%		
$\eta_4$	efficiency upconversion	$T_{amb} = 80\text{ }^\circ\text{C};$ $V_I = 2.4\text{ V}; V_O = 3.6\text{ V};$ note 5					
			$I_L = 1\text{ mA}$	81	83	–	%
			$I_L = 4\text{ mA}$	85	87	–	%
			$I_L = 100\text{ mA}$	88	90	–	%
			$I_L = 500\text{ mA}$	91	93	–	%
	$I_L = 1.5\text{ A};$ note 6	82	85	–	%		
<b>Timing</b>							
$f_{sw}$	switching frequency	PWM mode	480	600	720	kHz	
$f_{sync}$	synchronization clock input frequency		9	13	20	MHz	
$t_{start}$	start-up time	note 7	–	6	–	ms	
$t_{res}$	response time	from standby to $P_{o(max)}$	–	25	–	$\mu\text{s}$	
<b>Temperature</b>							
$T_{amb}$	operating ambient temperature		–40	+25	+80	$^\circ\text{C}$	
$T_{max}$	internal cut-off temperature		150	175	200	$^\circ\text{C}$	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Digital levels</b>						
$V_{IL}$	LOW-level input voltage on pins SHDWN, ILIMSEL, $\bar{U}/D$ and SYNC		0	–	0.4	V
$V_{IH}$	HIGH-level input voltage on pins $\bar{U}/D$ and PWM	note 8	$V_1 - 0.4$	–	$V_1 + 0.3$	V
	on pins SYNC and SHDWN	note 8	$0.55V_1$	–	$V_1 + 0.3$	V
	on pin ILIMSEL	notes 8 and 9	$0.55V_1$	–	$V_1 + 0.3$	V

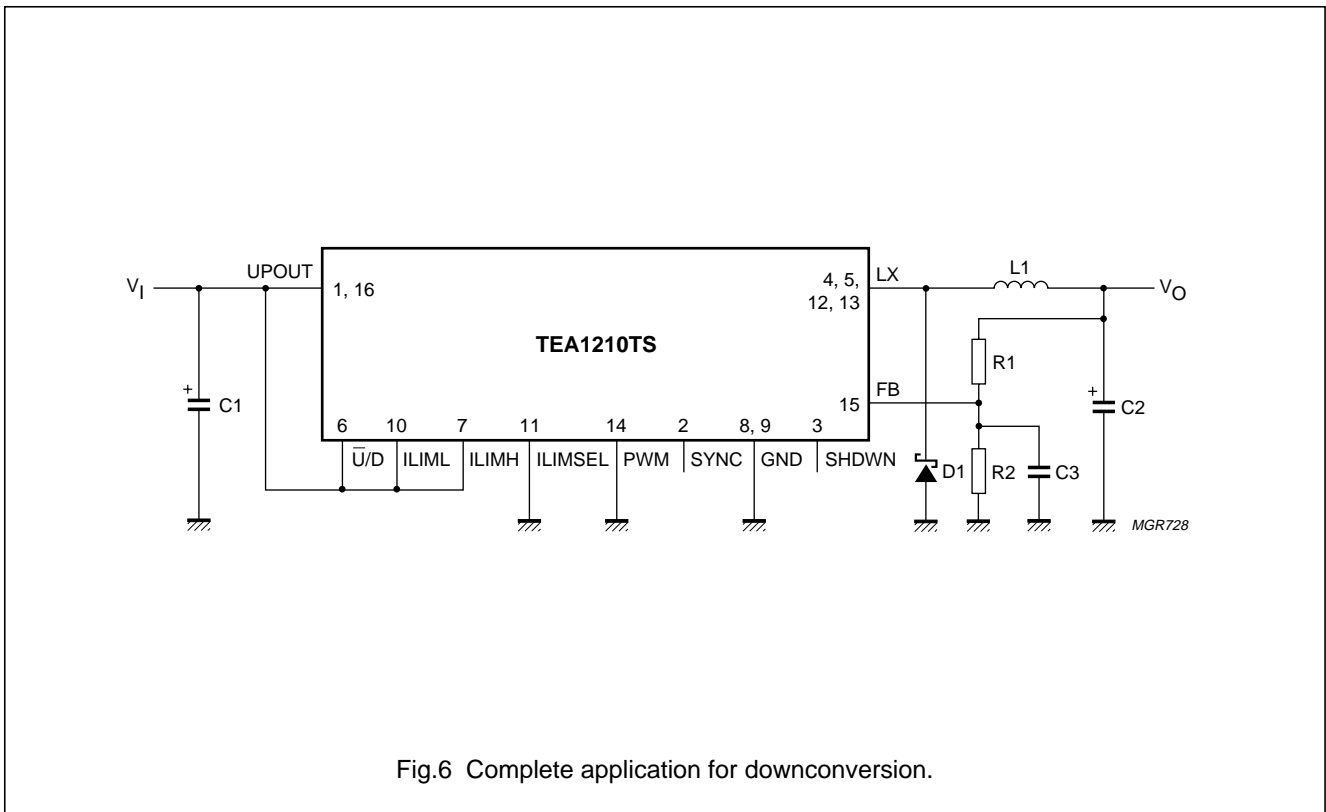
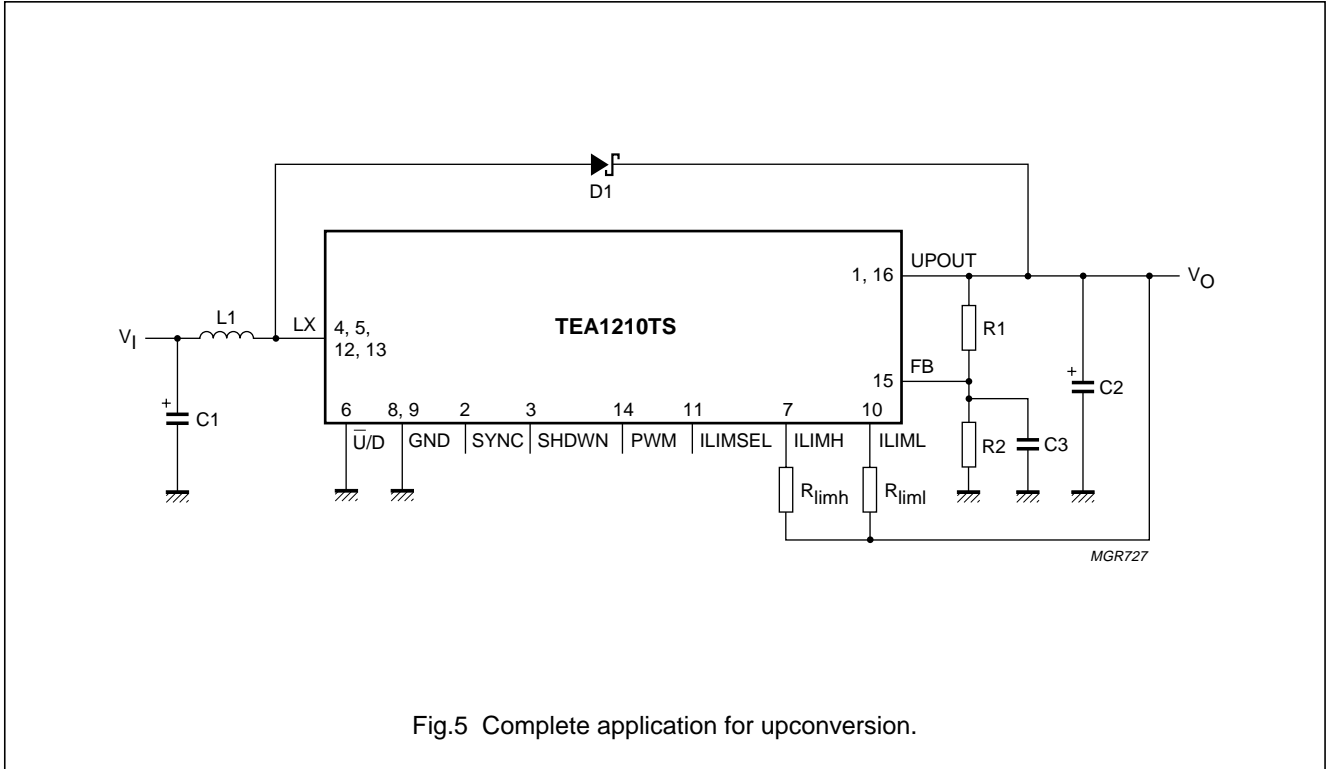
**Notes**

- The undervoltage lockout voltage shows wide specification limits since it decreases at increasing temperature. When the temperature increases, the minimum supply voltage of the digital control part of the IC decreases and therefore the correct operation of this function is guaranteed over the whole temperature range.
- When  $V_1$  is lower than the target output voltage but higher than 2.9 V, the P-type power MOSFET will remain conducting (100% duty cycle), resulting in  $V_O$  following  $V_1$ .
- The quiescent current is specified as the input current in the upconversion configuration at  $V_1 = 2.40$  V and  $V_O = 3.60$  V, using  $L1 = 6.8$   $\mu$ H,  $R1 = 178$  k $\Omega$  and  $R2 = 93.1$  k $\Omega$  (see Fig.5).
- The current limit is defined by the external current limiting resistors, see Section "Current limiting resistors".  $R_{limx} = 996$   $\Omega$  results in a typical current limit of 400 mA and  $R_{limx} = 178$   $\Omega$  results in a typical current limit of 2.0 A. The spread of the current limit decreases with increasing the  $I_{lim}$  setpoint.
- The specified efficiency is valid when using an output capacitor having an ESR of 0.04  $\Omega$  and an inductor having an inductance of 6.8  $\mu$ H, an ESR of 0.04  $\Omega$ , and a sufficient saturation current level. The current limit is assumed to be set at 4.0 A. In the PWM-only mode, the efficiency at  $I_L = 1$  mA and  $I_L = 4$  mA is lower than the values specified.
- The specified efficiency at  $I_L = 1.5$  A is only valid if the average input current does not exceed the maximum value of  $I_{LX}$ . In most practical applications, this means that the load current is not continuous.
- The specified start-up time is the time between the connection of a 2.40 V input voltage source and the moment the output reaches 3.60 V. The output capacitance equals 2000  $\mu$ F, the inductance equals 6.8  $\mu$ H, no load is present.
- $V_1$  is the voltage on the pins UPOUT. If the applied HIGH-level voltage is less than  $V_1 - 1$  V, the quiescent current of the device will increase.
- Maximum additional supply current on the pins UPOUT is 50  $\mu$ A in case the voltage  $V_1 = 5.0$  V and the input voltage on pin ILIMSEL is 2.2 V.

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APPLICATION INFORMATION



## High efficiency, high current DC/DC converter

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**External component selection****INDUCTOR L1**

The performance of the TEA1210TS is not very sensitive to inductance value. Best efficiency performance over a wide load current range is achieved by using an inductance of 6.8  $\mu$ H and a saturation current level of 3.0 A at least. In case the maximum output current is lower, other inductors are also suitable such as the TDK SLF7032 range.

**DIODE D1**

The Schottky diode is only used a short time during takeover from N-type power MOSFET and P-type power MOSFET and vice versa. Therefore, a medium-power diode such as Philips PRL5819 is sufficient in most applications.

**INPUT CAPACITOR C1**

The value of capacitor C1 strongly depends on the type of input source. In general, a 100  $\mu$ F tantalum capacitor will do, or a 10  $\mu$ F ceramic capacitor featuring very low series resistance (ESR value).

**OUTPUT CAPACITOR C2**

The value and type of capacitor C2 depend on the maximum output current and the ripple voltage which is allowed in the application. Low-ESR tantalum capacitors show best results. The most important specification of capacitor C2 is its ESR value, which mainly determines the output voltage ripple.

**FEEDBACK CAPACITOR C3**

Capacitor C3 prevents the feedback voltage from polluting by switching noise. A ceramic type of capacitor having a maximum value of 33 pF is recommended.

**FEEDBACK RESISTORS R1 AND R2**

The output voltage is determined by the resistors R1 and R2. The following conditions apply:

- Use 1% accurate SMD type resistors
- Resistors R1 and R2 should have a maximum value of 50 k $\Omega$  when connected in parallel. A higher value will result in inaccurate operation.

Under these conditions, the output voltage can be

calculated by the formula:  $V_O = 1.25 \times \left(1 + \frac{R1}{R2}\right)$

**CURRENT LIMITING RESISTORS**

The maximum instantaneous current in upconversion mode is set by one of the external resistors  $R_{limh}$  and  $R_{liml}$ . The preferred type is SMD, 1% accurate.

The digital level on pin ILIMSEL defines which one of the resistors is used to determine the current limiting level. The functionality of both settings is identical.

In case one current limit is enough, the unused pin (pin ILIML or ILIMH) must be connected either to the other pin (pin ILIMH or ILIML), or to pin UPOUT.

The values of the current limiting resistors can be derived from the simplified formula:

$$R_{limh} = \frac{346}{I_{lim(up)} - 0.05}, \text{ active when ILIMSEL = HIGH}$$

$$R_{liml} = \frac{346}{I_{lim(up)} - 0.05}, \text{ active when ILIMSEL = LOW}$$

The average inductor current during limited current operation also depends on the inductance value and the resistive losses in all components in the power path. Ensure that both current limiting levels do not exceed the saturation current of the inductor.

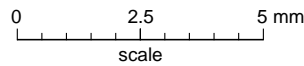
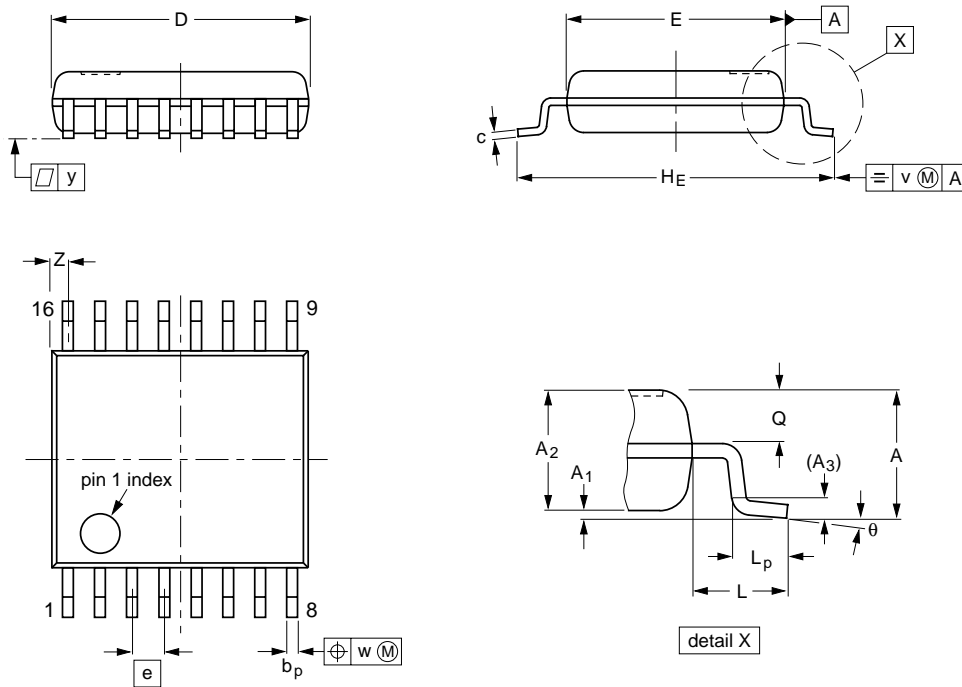
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PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm

SOT369-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.30 5.10	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT369-1						94-04-20 95-02-04

## High efficiency, high current DC/DC converter

## TEA1210TS

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 489 4339/4239, Fax. +30 1 481 4240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 319762,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 62 5344, Fax. +381 11 63 5777

**For all other countries apply to:** Philips Semiconductors,  
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,  
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

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