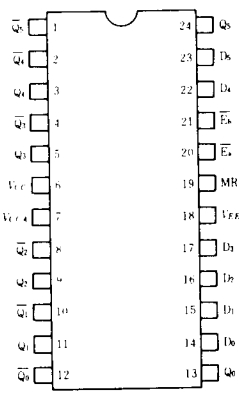
Hex D-type Latches

The HD100150 contains six D type latches with the True and Complement Outputs, a pair of Common Enables ($\overline{Ea}$ and $\overline{Eb}$), and a common Master Reset(MR). A Q output follows its D input when both $\overline{Ea}$ and $\overline{Eb}$ are low. When either $\overline{Ea}$ or $\overline{Eb}$ (or both) are high, a latch stores the last valid data present on its D input before $\overline{Ea}$ or $\overline{Eb}$ went high. The MR input overrides all other inputs and makes the Q outputs low.

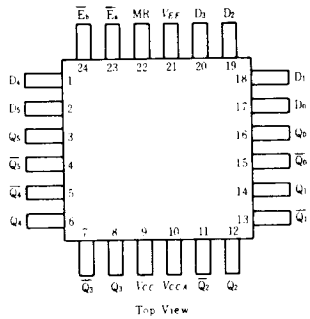
■ PIN ARRANGEMENT

● HD100150



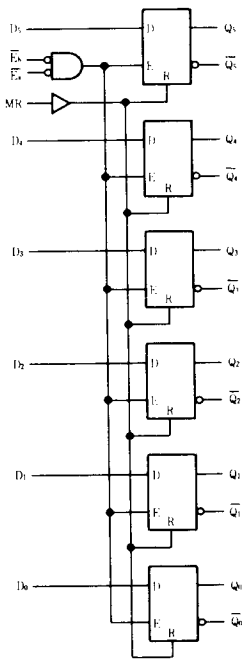
(Top View)

● HD100150F



Top View

■ LOGIC DIAGRAM



■ TRUTH TABLE (each latch)

Dn	$\overline{Ea}$	$\overline{Eb}$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
×	H	×	L	*
×	×	H	L	*
×	×	×	H	L

H = High Level
L = Low Level
× = Immaterial
* = Retains data present before $\overline{E}$ positive transition

■ DC CHARACTERISTICS ($V_{EE}=-4.5$V, $V_{CC}=$GND, $Ta=0$ to $+85$℃)

Item	Symbol	Test Condition		min	typ	max	Unit
Supply Current	I_{EE}	All input open		79	113	159	mA
Input Current	I_{IH}	$V_{IN}=V_{IL\,max}$	MR input	—	—	450	μA
			Data input	—	—	340	μA
			Enable input	—	—	520	μA

Note) As for other items, refer to the "Common DC Characteristics".

■AC CHARACTERISTICS ($V_{EE} = -2.2$ to -2.8V, $V_{CC} = V_{CCA} = 2.0$V)

● HD100150

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{E_a}$, $\overline{E_b}$ input	0.75	1.70	0.75	1.15	1.70	0.85	1.70	ns
			MR input	1.00	2.25	1.00	1.55	2.35	1.00	2.35	
			D_n input	0.50	1.35	0.55	0.60	1.40	0.55	1.40	
Transition Time	t_{TLH}, t_{THL}			0.35	1.50	0.35	0.70	1.50	0.35	1.50	ns
Setup Time	t_{SI}		D_n input	0.60		0.60	—		0.60	—	ns
			MR input (Release Time)	1.90		2.10			2.10	—	
Hold Time	t_h		D_n input	0.50		0.50			0.40	—	ns
Pulse Width	t_w		$\overline{E_a}$, $\overline{E_b}$ (L)	0.95		0.95			0.95	—	ns
			MR (H)	1.50		1.50	—		1.50	—	

● HD100150F

Item	Symbol	Test Condition		0℃ min	0℃ max	25℃ min	25℃ typ	25℃ max	85℃ min	85℃ max	Unit
Propagation Delay Time	t_{PLH}, t_{PHL}	See test circuit and waveform	$\overline{E_a}$, $\overline{E_b}$ input	0.70	1.45	0.75	1.05	1.50	0.75	1.50	ns
			MR input	1.00	2.10	1.00	1.50	2.20	1.00	2.20	
			D_n input	0.50	1.10	0.55	0.85	1.15	0.55	1.15	
Transition Time	t_{TLH}, t_{THL}			0.45	1.50	0.45	0.70	1.50	0.45	1.50	ns
Setup Time	t_{SI}		D_n input	0.60		0.60	—		0.60	—	ns
			MR input (Release Time)	1.80		2.00	—		2.00	—	
Hold Time	t_h		D_n input	0.30		0.30			0.20		ns
Pulse Width	t_w		$\overline{E_a}$, $\overline{E_b}$ (L)	0.75		0.75	—		0.75	—	ns
			MR (H)	1.30		1.30			1.30		

Note) The circuits in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5m/s (500 linear fpm) is maintained.

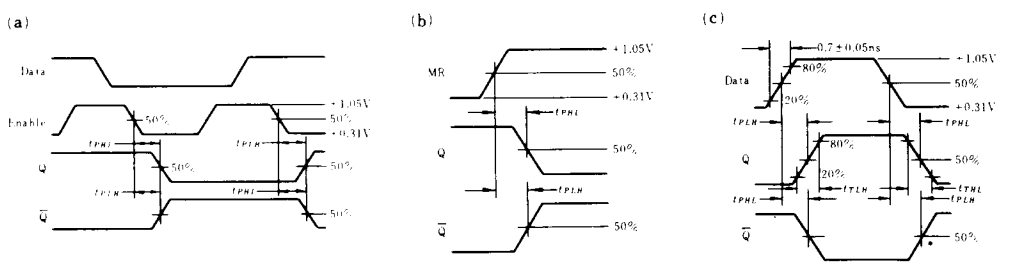


Fig. 1 Propagation Delay Time

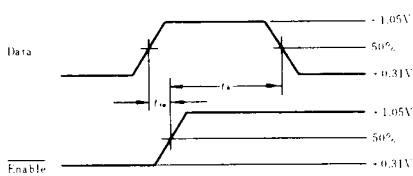


Fig. 2 Set-up and Hold Time