
HB56D473EJ Series

4,194,304-word $\times$ 72-bit High Density Dynamic RAM Module

HITACHI

ADE-203-439 (Z)

Rev. 0.0

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Description

The HB56D473EJ belongs to 8 byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56D473EJ is a 4 M $\times$ 72 dynamic RAM module, mounted 16 pieces of 16-Mbit DRAM (HM5117400BS) sealed in SOJ package and 8 pieces of 4-Mbit DRAM (HM514100CS) sealed in SOJ package, 1 piece of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package and 1 piece of 20-bit BiCMOS line driver (74ABT16827) sealed in TSSOP package. An outline of the HB56D473EJ is 168-pin socket type package (dual lead out). Therefore, the HB56D473EJ makes high density mounting possible without surface mount technology. The HB56D473EJ provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the its module board.

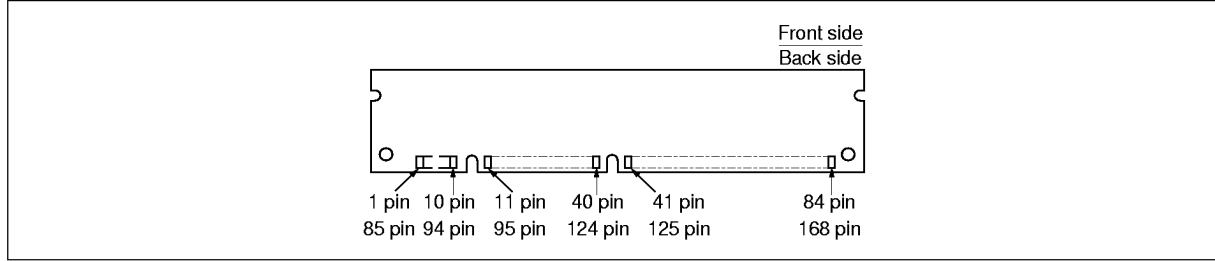
Features

- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: $t_{\text{RAC}} = 60/70/80$ ns (max)
 - Access time: $t_{\text{CAC}} = 20/25/25$ ns (max)
- Low power dissipation
 - Active mode: 14.2/13.0/11.7 W (max)
 - Standby mode (TTL): 588 mW (max)
 - Standby mode (CMOS): 462 mW (max).
- Buffered input except $\overline{\text{RAS}}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- Fast page mode capability
- 2,048 refresh cycle: 32 ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL compatible

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Ordering Information

Type No.	Access time	Package	Contact pad
HB56D473EJ-6B	60 ns	168-pin dual lead out socket type	gold
HB56D473EJ-7B	70 ns		
HB56D473EJ-8B	80 ns		

Pin Arrangement


Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	26	V _{CC}	51	NC	76	DQ34
2	DQ0	27	WE ₀	52	DQ18	77	DQ35
3	DQ1	28	CE ₀	53	DQ19	78	V _{SS}
4	DQ2	29	CE ₂	54	V _{SS}	79	PD1
5	DQ3	30	RE ₀	55	DQ20	80	PD3
6	V _{CC}	31	OE ₀	56	DQ21	81	PD5
7	DQ4	32	V _{SS}	57	DQ22	82	PD7
8	DQ5	33	A0	58	DQ23	83	ID0 (NC)
9	DQ6	34	A2	59	V _{CC}	84	V _{CC}
10	DQ7	35	A4	60	DQ24	85	V _{SS}
11	DQ8	36	A6	61	NC	86	DQ36
12	V _{SS}	37	A8	62	NC	87	DQ37
13	DQ9	38	A10	63	NC	88	DQ38
14	DQ10	39	NC	64	NC	89	DQ39
15	DQ11	40	V _{CC}	65	DQ25	90	V _{CC}
16	DQ12	41	NC	66	DQ26	91	DQ40
17	DQ13	42	NC	67	DQ27	92	DQ41
18	V _{CC}	43	V _{SS}	68	V _{SS}	93	DQ42
19	DQ14	44	OE ₂	69	DQ28	94	DQ43
20	DQ15	45	RE ₂	70	DQ29	95	DQ44
21	DQ16	46	CE ₄	71	DQ30	96	V _{SS}
22	DQ17	47	CE ₆	72	DQ31	97	DQ45
23	V _{SS}	48	WE ₂	73	V _{CC}	98	DQ46
24	NC	49	V _{CC}	74	DQ32	99	DQ47
25	NC	50	NC	75	DQ33	100	DQ48

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Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
101	DQ49	118	A3	135	NC	152	V _{SS}
102	V _{CC}	119	A5	136	DQ54	153	DQ64
103	DQ50	120	A7	137	DQ55	154	DQ65
104	DQ51	121	A9	138	V _{SS}	155	DQ66
105	DQ52	122	A11 (NC)	139	DQ56	156	DQ67
106	DQ53	123	NC	140	DQ57	157	V _{CC}
107	V _{SS}	124	V _{CC}	141	DQ58	158	DQ68
108	NC	125	NC	142	DQ59	159	DQ69
109	NC	126	B0	143	V _{CC}	160	DQ70
110	V _{CC}	127	V _{SS}	144	DQ60	161	DQ71
111	NC	128	NC	145	NC	162	V _{SS}
112	$\overline{\text{CE1}}$	129	NC	146	NC	163	PD2
113	$\overline{\text{CE3}}$	130	$\overline{\text{CE5}}$	147	NC	164	PD4
114	NC	131	$\overline{\text{CE7}}$	148	NC	165	PD6
115	NC	132	$\overline{\text{PDE}}$	149	DQ61	166	PD8
116	V _{SS}	133	V _{CC}	150	DQ62	167	ID1 (V _{SS})
117	A1	134	NC	151	DQ63	168	V _{CC}

Pin Description

Pin name	Function
A0 to A10, B0	Address input : A0 to A10, B0 Row address : A0 to A10, B0 Column address : A0 to A10, B0 Refresh address (D0 to D15) : A0 to A10, B0 Refresh address (M0 to M7) : A0 to A9, B0
DQ0 to DQ71	Data-in/data-out
$\overline{RE0}$, $\overline{RE2}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE7}$	Column address strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD8	Presence detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence detect enable
NC	No connection

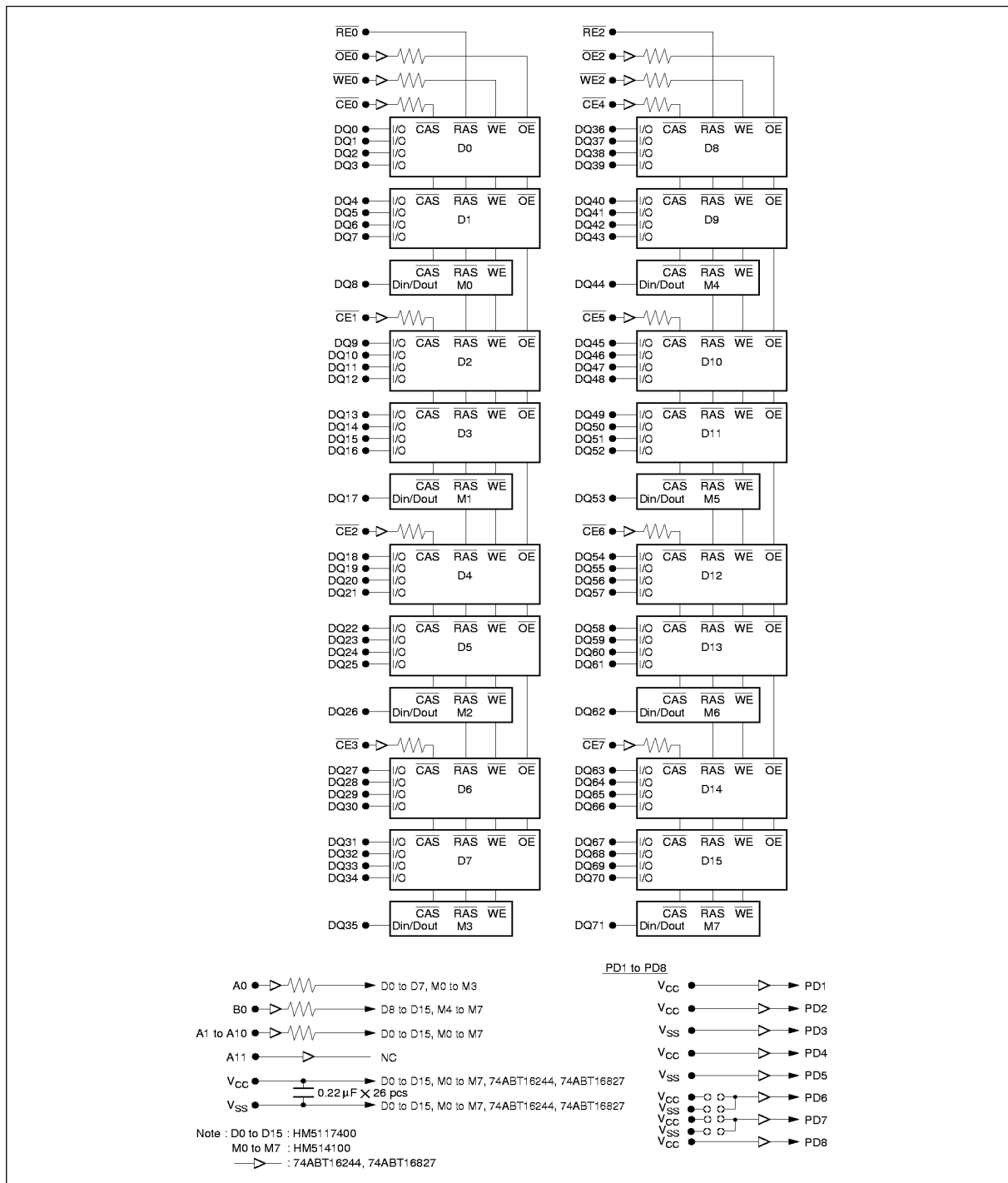
Presence Detect Pin Assignment

Pin name	Pin No.	$\overline{PDE}$ = Low			$\overline{PDE}$ = High
		60 ns	70 ns	80 ns	All
PD1	79	1	1	1	High-Z
PD2	163	1	1	1	High-Z
PD3	80	0	0	0	High-Z
PD4	164	1	1	1	High-Z
PD5	81	0	0	0	High-Z
PD6	165	1	0	1	High-Z
PD7	82	1	1	0	High-Z
PD8	166	1	1	1	High-Z

Note: 1: High level (Driver output)
0: Low level (Driver output)

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Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	25	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

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Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	2704	—	2464	—	2224	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	112	—	112	—	112	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
		—	88	—	88	—	88	mA	CMOS interface RAS, CAS ≥ V _{CC} – 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	2704	—	2464	—	2224	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	184	—	184	—	184	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	2704	—	2464	—	2224	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	2224	—	1984	—	1824	mA	t _{PC} = min	1, 3
Input leakage current	I _{LI}	–10	10	–10	10	–10	10	μA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I _{LO}	–10	10	–10	10	–10	10	μA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = –5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while R_{AS} = V_{IL}.

3. Address can be changed once or less while C_{AS} = V_{IH}.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{\text{RAS}}$)	C_{I3}	—	99	pF	1
I/O capacitance (DQ0 to 7, 9 to 16, 18 to 25, 27 to 34, 36 to 43, 45 to 52, 54 to 61, 63 to 70)	$C_{I/O1}$	—	20	pF	1, 2
I/O capacitance (DQ8, 17, 26, 35, 44, 53, 62, 71)	$C_{I/O2}$	—	25	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

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AC Characteristics ($T_a = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 5\%$, $V_{SS} = 0 \text{ V}$)^{*1, *2}

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HB56D473EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40	—	50	—	60	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	15	10000	20	10000	20	10000	ns	
Row address setup time	t _{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	40	20	45	20	55	ns	3
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	15	35	ns	4
$\overline{\text{RAS}}$ hold time	t _{RSH}	20	—	25	—	25	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	15	—	15	—	15	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{OED}	20	—	25	—	25	—	ns	5, 19
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	0	—	ns	6, 19
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	7
Refresh period	t _{REF}	—	32	—	32	—	32	ms	18

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Read Cycle

		HB56D473EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	25	—	25	ns	9, 10, 17
Access time from address	t_{AA}	—	35	—	40	—	45	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	20	—	25	—	25	ns	9, 19
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	30	—	35	—	40	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	2	—	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	19
Output buffer turn-off time	t_{OFF}	—	20	—	25	—	25	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	20	—	25	—	25	ns	13, 19
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	20	—	25	—	25	—	ns	5

Write Cycle

		HB56D473EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t _{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t _{WP}	10	—	10	—	10	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t _{DH}	20	—	20	—	20	—	ns	15

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Refresh Cycle

		HB56D473EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
CAS setup time (CBR refresh cycle)	t_{CSR}	15	—	15	—	15	—	ns	
CAS hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
WE setup time (CBR refresh cycle)	t_{WRP}	5	—	5	—	5	—	ns	
WE hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	10	—	ns	
RAS precharge to CAS hold time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

		HB56D473EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode RAS pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from CAS precharge	t_{CPA}	—	40	—	45	—	50	ns	9, 17
RAS hold time from CAS precharge	t_{CPRH}	40	—	45	—	50	—	ns	

- Notes: 1. AC measurements assume $t_T = 5$ ns.
2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh cycle or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

11. Assumes that $t_{RCD} \leq t_{RCD} \text{ (max)}$ and $t_{RAD} \geq t_{RAD} \text{ (max)}$.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. $t_{OFF} \text{ (max)}$ and $t_{OEZ} \text{ (max)}$ are defined the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS} is not restrictive operating parameters. It is included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS} \text{ (min)}$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycle.
16. t_{RASP} defines RAS pulse width in fast page mode cycles.
17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
18. t_{REF} is determined by 2,048 refresh cycle.
19. Parity bit of this item must not use. (DQ8, 17, 26, 35, 44, 53, 62, 71)

Timing Waveforms

Refer to the HM5117400B Series data sheet.

Physical Outline

Unit: mm/inch

