
HB56A464EJ Series

4,194,304-word $\times$ 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-438 (Z)

Rev. 0.0

Jul. 24, 1995

Description

The HB56A464EJ belongs to 8 byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications.

The HB56A464EJ is a 4 M $\times$ 64 dynamic RAM module, mounted 16 pieces of 16-Mbit DRAM (HM5116400BS) sealed in SOJ package, 1 piece of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package and 1 piece of 20-bit BiCMOS line driver (74BT16827) sealed in TSSOP package. An outline of the HB56A464EJ is 168-pin socket type package (dual lead out). Therefore, the HB56A464EJ makes high density mounting possible without surface mount technology. The HB56A464EJ provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the module board.

Features

- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: $t_{RAC} = 60/70/80$ ns (max)
 - Access time: $t_{CAC} = 20/23/25$ ns (max)
- Low power dissipation
 - Active mode: 7.06/6.22/5.80 W (max)
 - Standby mode (TTL): 504 mW (max)
 - Standby mode (CMOS): 420 mW (max)
- Buffered input except $\overline{RAS}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- Fast page mode capability
- 4,096 refresh cycle: 64 ms
- 2 variations of refresh
 - $\overline{RAS}$ -only refresh
 - $\overline{CAS}$ -before- $\overline{RAS}$ refresh
- TTL compatible

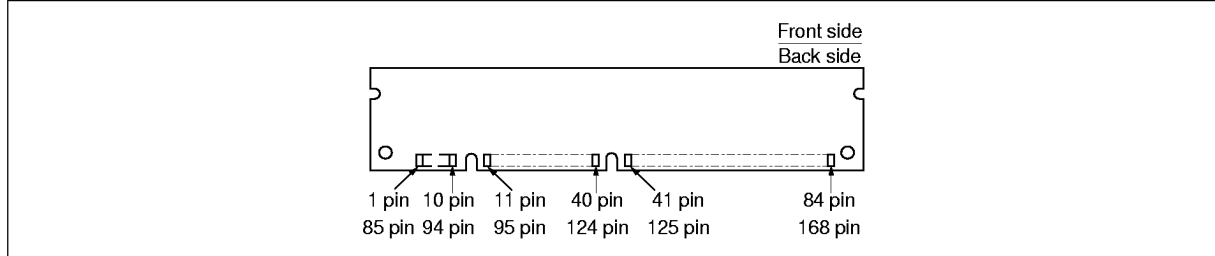
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Ordering Information

Type No.	Access time	Package	Contact pad
HB56A464EJ-6B	60 ns	168-pin dual lead out socket type	gold
HB56A464EJ-7B	70 ns		
HB56A464EJ-8B	80 ns		

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Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	26	V _{CC}	51	NC	76	DQ34
2	DQ0	27	$\overline{WE0}$	52	DQ18	77	NC
3	DQ1	28	$\overline{CE0}$	53	DQ19	78	V _{SS}
4	DQ2	29	$\overline{CE2}$	54	V _{SS}	79	PD1
5	DQ3	30	$\overline{RE0}$	55	DQ20	80	PD3
6	V _{CC}	31	$\overline{OE0}$	56	DQ21	81	PD5
7	DQ4	32	V _{SS}	57	DQ22	82	PD7
8	DQ5	33	A0	58	DQ23	83	ID0 (V _{SS})
9	DQ6	34	A2	59	V _{CC}	84	V _{CC}
10	DQ7	35	A4	60	DQ24	85	V _{SS}
11	NC	36	A6	61	NC	86	DQ36
12	V _{SS}	37	A8	62	NC	87	DQ37
13	DQ9	38	A10	63	NC	88	DQ38
14	DQ10	39	NC	64	NC	89	DQ39
15	DQ11	40	V _{CC}	65	DQ25	90	V _{CC}
16	DQ12	41	NC	66	NC	91	DQ40
17	DQ13	42	NC	67	DQ27	92	DQ41
18	V _{CC}	43	V _{SS}	68	V _{SS}	93	DQ42
19	DQ14	44	$\overline{OE2}$	69	DQ28	94	DQ43
20	DQ15	45	$\overline{RE2}$	70	DQ29	95	NC
21	DQ16	46	$\overline{CE4}$	71	DQ30	96	V _{SS}
22	NC	47	$\overline{CE6}$	72	DQ31	97	DQ45
23	V _{SS}	48	$\overline{WE2}$	73	V _{CC}	98	DQ46
24	NC	49	V _{CC}	74	DQ32	99	DQ47
25	NC	50	NC	75	DQ33	100	DQ48

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Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
101	DQ49	118	A3	135	NC	152	V _{SS}
102	V _{CC}	119	A5	136	DQ54	153	DQ64
103	DQ50	120	A7	137	DQ55	154	DQ65
104	DQ51	121	A9	138	V _{SS}	155	DQ66
105	DQ52	122	A11	139	DQ56	156	DQ67
106	NC	123	NC	140	DQ57	157	V _{CC}
107	V _{SS}	124	V _{CC}	141	DQ58	158	DQ68
108	NC	125	NC	142	DQ59	159	DQ69
109	NC	126	B0	143	V _{CC}	160	DQ70
110	V _{CC}	127	V _{SS}	144	DQ60	161	NC
111	NC	128	NC	145	NC	162	V _{SS}
112	$\overline{CE1}$	129	NC	146	NC	163	PD2
113	$\overline{CE3}$	130	$\overline{CE5}$	147	NC	164	PD4
114	NC	131	$\overline{CE7}$	148	NC	165	PD6
115	NC	132	$\overline{PDE}$	149	DQ61	166	PD8
116	V _{SS}	133	V _{CC}	150	NC	167	ID1 (V _{SS})
117	A1	134	NC	151	DQ63	168	V _{CC}

Pin Description

Pin name	Function
A0 to A11, B0	Address input : A0 to A11, B0 Row address : A0 to A11, B0 Column address : A0 to A9, B0 Refresh address : A0 to A11, B0
DQ0 to DQ7, DQ9 to DQ16, DQ18 to DQ25, DQ27 to DQ34, DQ36 to DQ43, DQ45 to DQ52, DQ54 to DQ61, DQ63 to DQ70	Data-in/data-out
$\overline{\text{RE0}}, \overline{\text{RE2}}$	Row address strobe ($\overline{\text{RAS}}$)
$\overline{\text{CE0}}$ to $\overline{\text{CE7}}$	Column address strobe ($\overline{\text{CAS}}$)
$\overline{\text{WE0}}, \overline{\text{WE2}}$	Read/write enable
$\overline{\text{OE0}}, \overline{\text{OE2}}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD8	Presence detect
ID0, ID1	ID bit
$\overline{\text{PDE}}$	Presence detect enable
NC	No connection

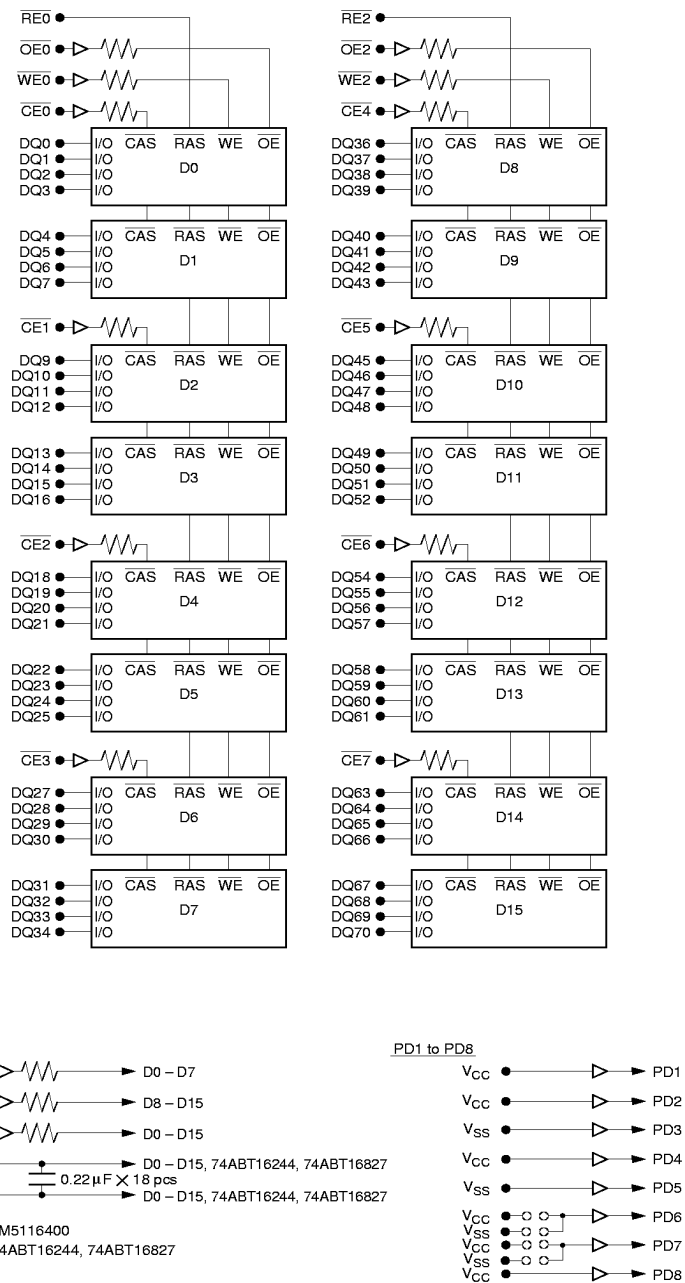
Presence Detect Pin Assignment

Pin name	Pin No.	$\overline{\text{PDE}} = \text{Low}$			$\overline{\text{PDE}} = \text{High}$
		60 ns	70 ns	80 ns	All
PD1	79	1	1	1	High-Z
PD2	163	1	1	1	High-Z
PD3	80	0	0	0	High-Z
PD4	164	1	1	1	High-Z
PD5	81	0	0	0	High-Z
PD6	165	1	0	1	High-Z
PD7	82	1	1	0	High-Z
PD8	166	1	1	1	High-Z

Note: 1: High level (Driver output)
0: Low level (Driver output)

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Block Diagram



D0 to D15 : HM5116400
: 74ABT16244, 74ABT16827

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	17	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–0.5	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$)

		HB56A464EJ								
		60 ns		70 ns		80 ns				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	1344	—	1184	—	1104	mA	$t_{RC} = \min$	1, 2
Standby current	I_{CC2}	—	96	—	96	—	96	mA	TTL interface $\overline{RAS}, \overline{CAS} = V_{IH}$ Dout = High-Z	
		—	80	—	80	—	80	mA	CMOS interface $\overline{RAS}, \overline{CAS}$ $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
$\overline{RAS}$ -only refresh current	I_{CC3}	—	1344	—	1184	—	1104	mA	$t_{RC} = \min$	2
Standby current	I_{CC5}	—	144	—	144	—	144	mA	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ Dout = enable	1
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	—	1344	—	1184	—	1104	mA	$t_{RC} = \min$	
Fast page mode current	I_{CC7}	—	1184	—	1024	—	864	mA	$t_{PC} = \min$	1, 3
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 5.5\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 5.5\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	71	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable Dout.

