CYPRESS SEMICONDUCTOR

CY7B155
CY7B156

16K x 16 Synchronous Static RAM

Features

- **16K x 16 common I/O**
- **BiCMOS for optimum speed/power**
- **12 ns maximum access delay (clock to output)**
- **Input address latch**
- **Input data latch with separate latch control signal (DLE)**
- **8-bit address counter with 2- and 8-bit wraparound operations (7B156 only)**
- **Supports Intel 486 burst address sequence (7B155 only)**
- **Supports suspended burst**
- **Simple counter control**
- **Self-timed write with synchronous user-adjustable write trigger**
- **Byte write supported**
- **52-pin PLCC, LCC, and QFP packages**

Functional Description

The CY7B155 and CY7B156 are 16K by 16 synchronous static RAMs targeted for high-performance burst-oriented applications. Address-increment logic is provided in both versions. Counter control is simple and involves only three signals: clock, load enable, and count enable.

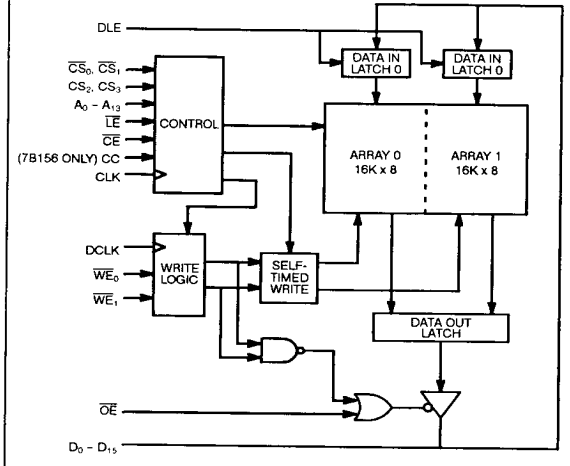
In the CY7B156, an integrated 8-bit wraparound counter automatically increments addresses for a maximum of 256 consecutive references. The counter can be switched from an 8-bit wraparound mode to a 2-bit wraparound mode via a control input. In the CY7B155, A_0 through A_7 are sequenced based on the 2-bit Intel 80486 burst order (see *Table 1*).

Write operations are synchronously triggered and self-timed to simplify processor interface. A delayed write mechanism supporting a user-adjustable write trigger provides maximum checking time for external protection circuits; if the write access is determined to be faulty, memory will not be modified.

The write enable inputs are sampled on the falling edge of the delayed clock (DCLK) input. Write is initiated only when one or both sampled values are LOW. Because the DCLK is a variable input signal, the user can hand-tune the write sampling point by adjusting the amount of the delay on DCLK.

Each byte can be written individually with its own write enable input. A 16-bit data latch is provided on-chip to capture write data from the processor. This latch can be bypassed by connecting the data latch enable (DLE) input to a high level. Memory expansion is also simplified by the incorporation of four self-decoding chip select inputs. Up to four memory banks can be supported without any external decoding logic. Maximum access delay from clock rise to output is 12 ns.

Logic Block Diagram



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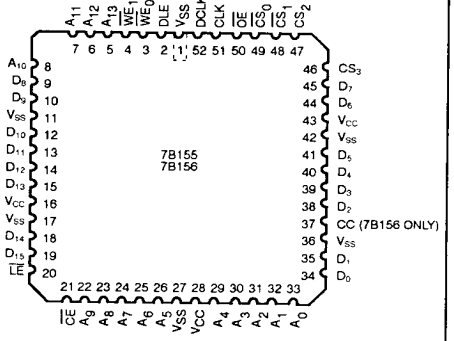
Pin Configuration

LCC/PLCC
Top View



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Selector Guide

	7B155–12 7B156–12	7B155–15 7B156–15	7B155–20 7B156–20
Maximum Access Time (ns)	12	15	20
Maximum Operating Current (mA)	250	250	250

Pin Definitions

Signal Name	I/O	Description
$A_0 - A_{13}$	I	Address Inputs
CLK	I	Clock
DCLK	I	Delayed Clock
$\overline{WE}_0$	I	Low Byte Write Enable
$\overline{WE}_1$	I	High Byte Write Enable
$\overline{OE}$	I	Output Enable
$\overline{CS}_0$, $\overline{CS}_1$	I	Chip Selects 0, 1
CS_2, CS_3	I	Chip Selects 2, 3
$\overline{LE}$	I	Load Enable
$\overline{CE}$	I	Counter Enable
CC	I	Count Control (CY7B156 only)
DLE	I	Data Latch Enable
$D_0 - D_{15}$	I/O	Data I/O
V_{CC}	-	+5V Power Supply
V_{SS}	-	Ground

Table 1. Burst Read/Write Sequence

First Address		First Address		First Address		First Address	
A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
0	0	0	1	1	0	1	1
0	1	0	0	1	1	1	0
1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	0

Application Example

Figure 1 shows a 64-Kbyte cache using two CY7B156 cache RAMs with burst capability and a CY7B181 high-speed cache tag. The complexity of the cache controller is reduced because the CY7B181 generates the write enable signal to the RAM automatically during write hits.

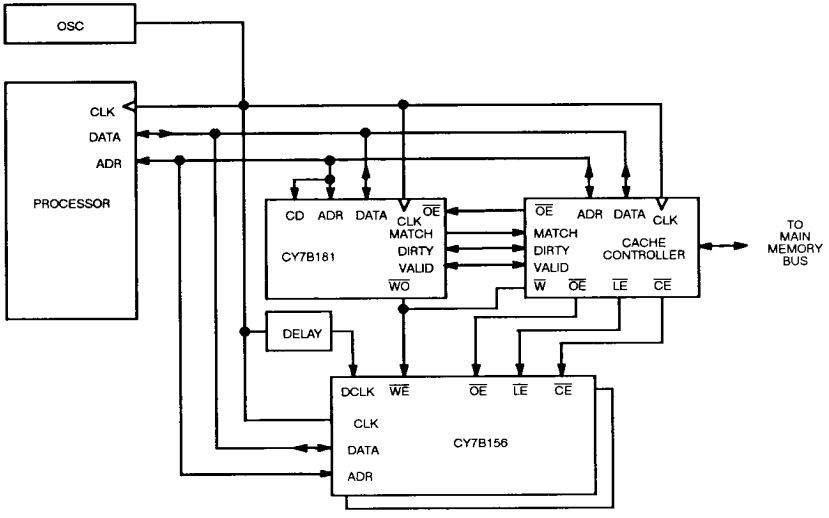

Figure 1. Cache Using CY7B156s

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage on V_{CC} Relative to GND .. – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... – 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

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Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7B155–12 7B156–12		7B155–15, 20 7B156–15, 20		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	6.0	2.2	6.0	V
V_{IL}	Input LOW Voltage[1]		–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	–10	+ 10	–10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled	–10	+ 10	–10	+ 10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. , I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$		250		250	mA

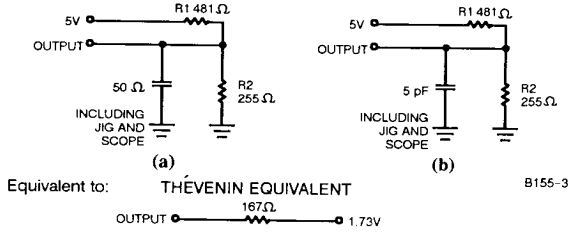
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. $V_{IL\,(min.)}$ = – 1.5V for pulse durations of less than 20 ns.
2. T_A is the "instant on" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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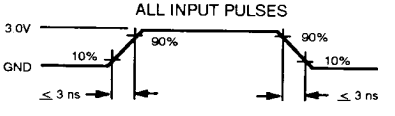

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Switching Characteristics Over the Operating Range[5]

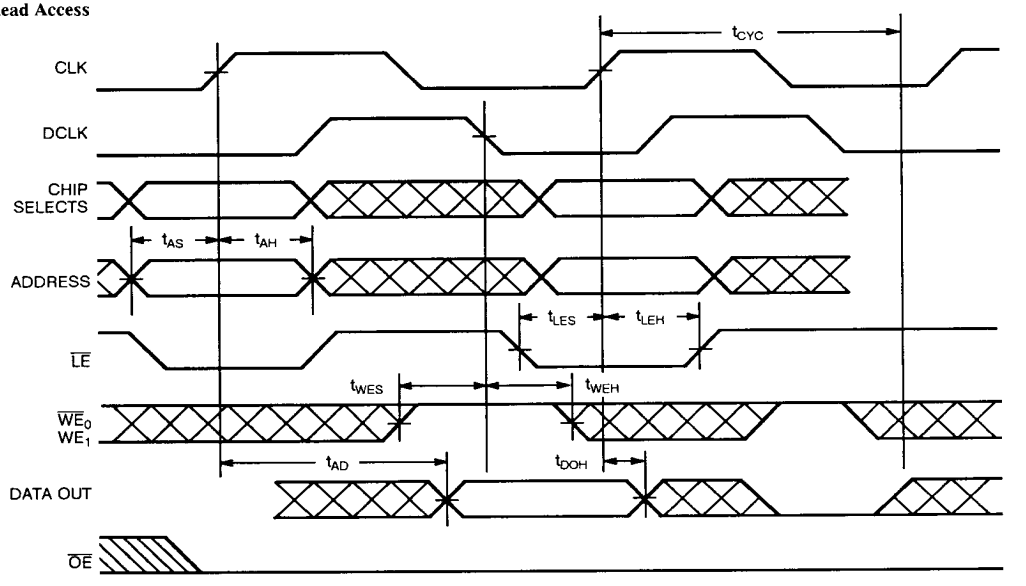
Parameters	Description	7B155–12 7B156–12		7B155–15 7B156–15		7B155–20 7B155–20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	20		25		30		ns
t_{AD}	Access Delay for Clock Rise	12		15		20		ns
t_{DOH}	Data Output Hold After Clock Rise	3		3		3		ns
t_{AS}	Address Set-Up Before CLK Rise	3		4		5		ns
t_{AH}	Address Hold After CLK Rise	3		4		4		ns
t_{LES}	Load Enable Set-Up Before CLK Rise	3		4		5		ns
t_{LEH}	Load Enable Hold After CLK Rise	3		4		4		ns
t_{WES}	Write Enable Set-Up Before DCLK Fall	2		3		4		ns
t_{WEH}	Write Enable Hold After DCLK Fall	4		5		6		ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[6]		7		8		9	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		7		8		9	ns

Notes:

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 50-pF load capacitance.
6. t_{EOZ} is specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.

Switching Waveforms

Read Access



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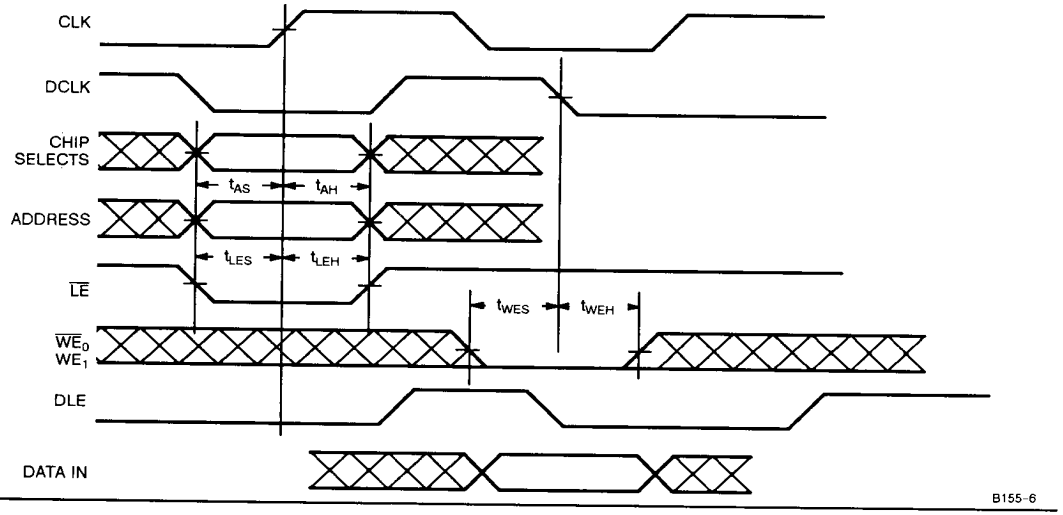
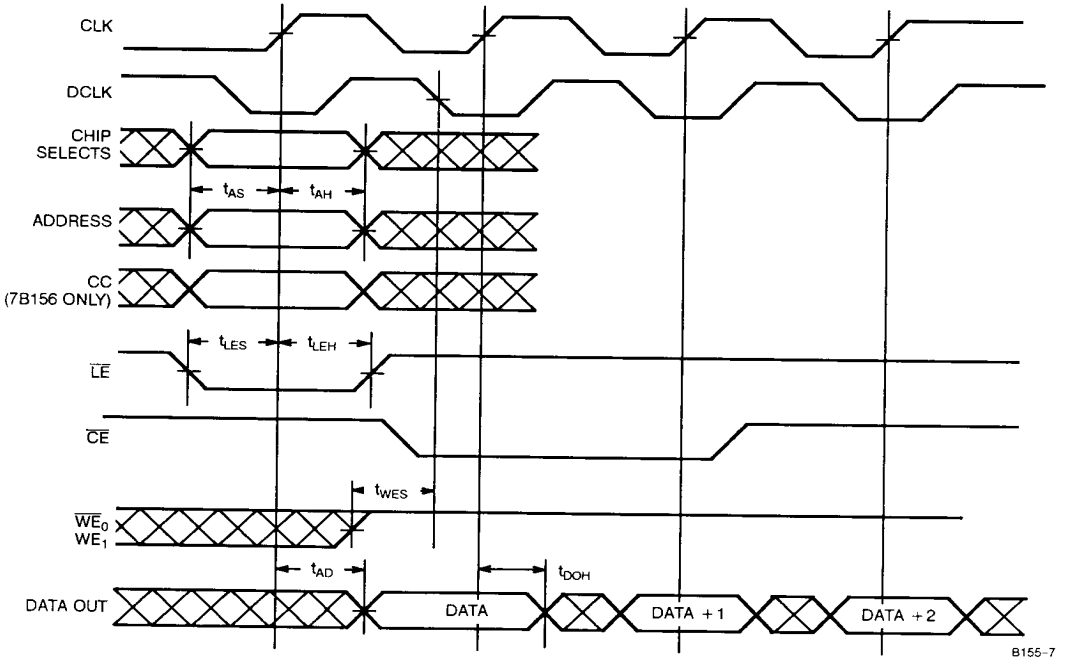
Switching Waveforms (continued)

Latched Write



Burst Read Sequence with Three Accesses



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B155-12JC	J69	Commercial
	CY7B155-12LC	L69	
15	CY7B155-15JC	J69	Commercial
	CY7B155-15LC	L69	
20	CY7B155-20JC	J69	Commercial
	CY7B155-20LC	L69	

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B156-12JC	J69	Commercial
	CY7B156-12LC	L69	
15	CY7B156-15JC	J69	Commercial
	CY7B156-15LC	L69	
20	CY7B156-20JC	J69	Commercial
	CY7B156-20LC	L69	

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