

Description

The GM76U8128CL/CLL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits. Using a 0.6 μ m advanced CMOS technology and it provides high speed operation with minimum cycle time of 85/100ns. The device is placed in a low power standby mode with /CS1 high or CS2 low and the output enable (/OE) allows fast memory access. Thus it is suitable for high speed and low power applications, especially where battery back-up is required.

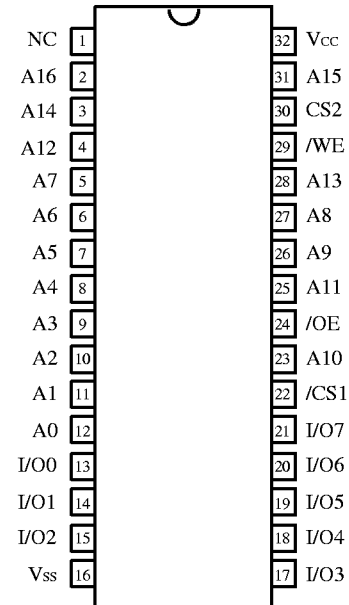
Features

- * Fast Speed : 85/100ns
- * Low Power Standby and Low Power Operation
 - Standby : 66 μ W Max. at TA = - 40 ~ 85C(LLE/LLI)
 - 99 μ W Max. at TA = - 40 ~ 85C(LE/LI)
 - 49.5 μ W Max. at TA = 0 ~ 70C(LL)
 - 165 μ W Max. at TA = 0 ~ 70C(L)
- Operation : 132mW (Max)
- * Completely Static RAM : No Clock or Timing Strobe Required
- * Equal Access and Cycle Time
- * TTL compatible inputs and outputs
- * Capability of Battery Back-up Operation
- * Single + 3.0V \pm 0.3V Operation
- * Standard 32DIP, SOP and TSOP-I,STSOP-I
- * Temperature Range
 - Commercial(0; > 70C) : GM76U8128C
 - Extended (-25 ~ 85C) : GM76U8128C-E
 - Industrial (-40 ~ 85C) : GM76U8128C-I

Pin Description

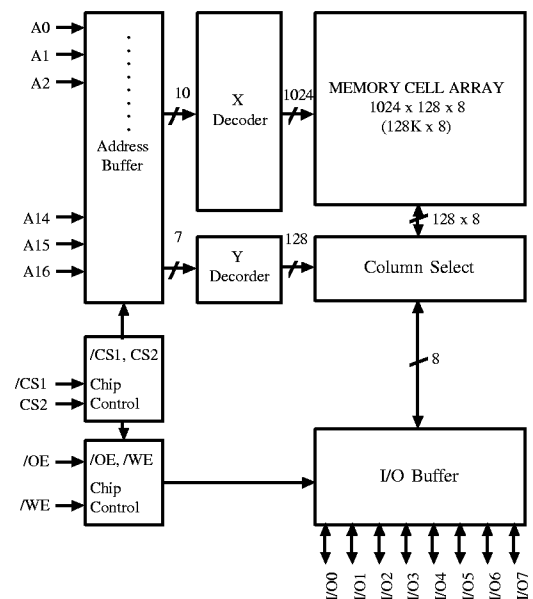
Pin	Function
A0-A16	Address Inputs
/WE	Write Enable Input
/CS1, CS2	Chip Select Input
/OE	Output Enable Input
I/O0-I/O7	Data Inputs/Outputs
Vcc	Power Supply (2.7V ~3.3V)
Vss	Ground
NC	No Connection

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit	
T _A	Ambient Temperature under Bias	GM76U8128C	0 ~ 70	C
		GM76U8128C-E	-25 ~ 85	C
		GM76U8128C-I	-40 ~ 85	C
T _{STG}	Storage Temperature	-55 ~ 150	C	
T _{SOL}	Soldering Temperature and Time	260, 10 (at lead)	C, S	
V _{CC}	Supply Voltage	-0.5 ~ 4.6	V	
V _{IN}	Input Voltage	-0.5 ~ V _{CC} + 0.5	V	
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{CC} + 0.5	V	
P _D	Power Dissipation	0.7	W	

*: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = -40 ~ 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.7	3.0	3.3	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-0.3*	-	0.4	V

*Note : V_{IL}(min) = -3.0V for ≤ 50ns pulse

Truth Table

/CS1	CS2	/OE	/WE	A0 to A16	DATA I/O	MODE
L	H	L	H	Stable	Output Data	Read
L	H	X	L	Stable	Input Data	Write
L	H	H	H	Stable	Hi-Z	Output Disable
H	X	X	X	-	Hi-Z	Standby
X	L	X	X	-	Hi-Z	

*Note: X means don't care

DC Operating Characteristics ($V_{CC} = 3.0V \pm 0.3V$, $T_A = -40 \sim 85C$)

Symbol	Parameter		Conditions	Min	*Typ	Max	Unit	
$I_{i(L)}$	Input Leakage Current		$V_{IN} = 0$ to V_{CC}	-1	-	1	μA	
$I_{o(L)}$	Output Leakage Current		$/CS1 = V_{IH}$ or $CS2 = V_{IL}$ $/OE = V_{IH}$, $V_{SS} \leq V_{OUT} \leq V_{CC}$	-1	-	1	μA	
V_{OH}	High Level Output Voltage		$I_{OH} = -1.0mA$	2.2	-	-	V	
V_{OL}	Low Level Output Voltage		$I_{OL} = 2.1mA$	-	-	0.4	V	
I_{CC}	Operating Supply Current		$/CS1 = V_{IL}$ and $CS2 = V_{IH}$ $V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0mA$	-	-	5	mA	
I_{CC1}	Average Operating Current		$/CS1 = V_{IL}$ and $CS2 = V_{IH}$ $V_{IN} = V_{IH}/V_{IL}$ $I_{OUT} = 0mA$ tcycle = Min, cycle	-	-	40	mA	
I_{CC2}			$/CS1 = 0.2V$, $CS2 = V_{CC} - 0.2V$ $V_{IN} = V_{CC} - 0.2V/0.2V$ $I_{OUT} = 0mA$ tcycle = 1 μs	-	-	5	mA	
I_{CCS1}	Standby Current(TTL)		$/CS1 = V_{IH}$, $CS2 = V_{IL}$	-	-	0.5	mA	
I_{CCS2}	Standby Current(CMOS)	GM76U8128C	$/CS1 = V_{CC} - 0.2V$, $CS2 = 0.2V$	L - Version	-	-	50	μA
		LL - Version		-	-	15	μA	
		GM76U8128C-E GM76U8128C-I		L - Version	-	-	30	μA
				LL - Version	-	-	20	μA

*Typ. Values are measured at 25C

Capacitance ($f = 1MHz$, $T_A = 25C$)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	$V_i = 0V$	-	6	pF
C_{IO}	Output Capacitance	$V_o = 0V$	-	8	pF

*Note: This parameter is sampled and not 100% tested.

AC Operating Characteristics

Test Conditions ($V_{CC} = 3.0V \pm 0.3V$, $T_A = -40 \sim 85C$, unless otherwise noted.)

Parameter	Value
Input Pulse Level	0.4 to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 100$ pF + 1TTL Load

AC Operating Characteristics ($V_{CC} = 3.0V \pm 0.3V$, $T_A = -40 \sim 85C$)

Read Cycle

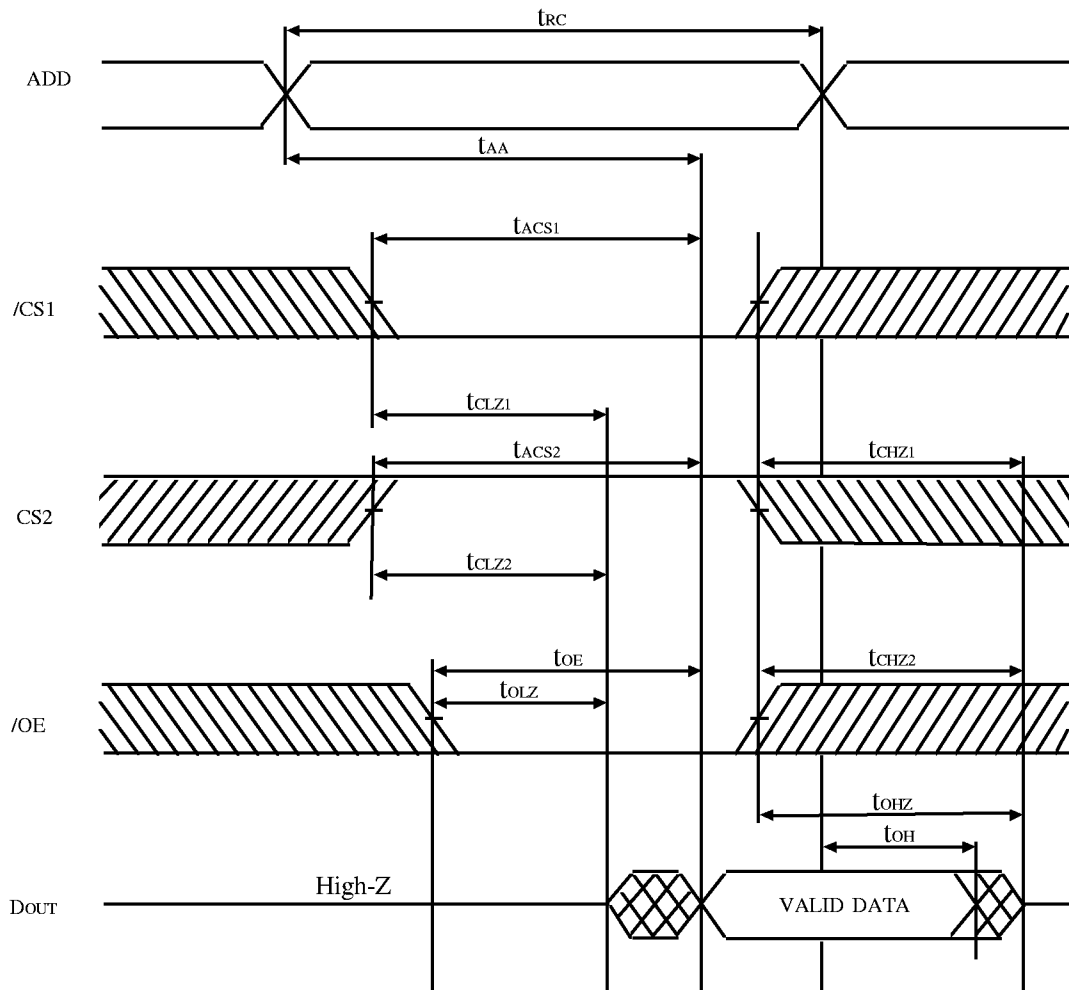
Symbol	Parameter	GM76U8128C-85		GM76U8128C-10		Unit
		Min	Max	Min	Max	
t _{RC}	Read Cycle Time	85	-	100	-	ns
t _{AA}	Address Access Time	-	85	-	100	ns
t _{ACS1}	Chip Select 1 Access Time	-	85	-	100	ns
t _{ACS2}	Chip Select 2 Access Time	-	85	-	100	ns
t _{OE}	Output Enable Access Time	-	45	-	50	ns
t _{CLZ1}	Chip Select 1 Output Setup Time	10	-	10	-	ns
t _{CHZ1}	Chip Select 1 Output Floating	-	30	-	35	ns
t _{CLZ2}	Chip Select 2 Output Setup Time	10	-	10	-	ns
t _{CHZ2}	Chip Select 2 Output Floating	-	30	-	35	ns
t _{OLZ}	Output Enable Output Setup Time	0	-	0	-	ns
t _{OHZ}	Output Enable Output Floating	-	30	-	35	ns
t _{OH}	Output Hold Time	10	-	10	-	ns

Write Cycle

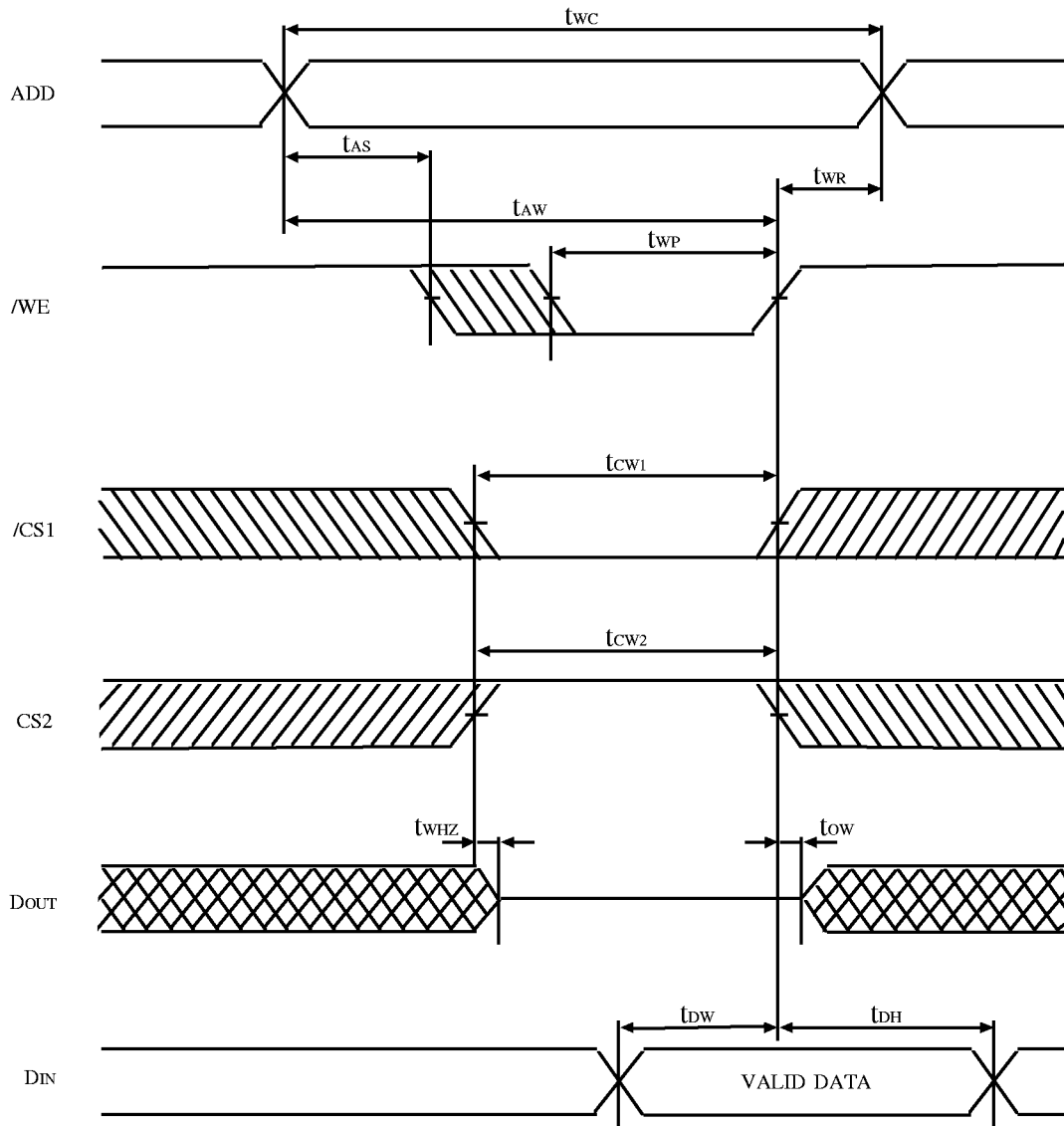
Symbol	Parameter	GM76U8128C-85		GM76U8128C-10		Unit
		Min	Max	Min	Max	
t _{wc}	Write Cycle Time	85	-	100	-	ns
t _{cw1}	Chip Select Time 1	75	-	85	-	ns
t _{cw2}	Chip Select Time 2	75	-	85	-	ns
t _{AW}	Address Enable Time	70	-	80	-	ns
t _{AS}	Address Setup Time	0	-	0	-	ns
t _{wP}	Write Pulse Width	60	-	70	-	ns
t _{wR}	Write Recovery Time	0	-	0	-	ns
t _{dW}	Input Data Setup Time	35	-	40	-	ns
t _{dH}	Input Data Hold Time	0	-	0	-	ns
t _{wHZ}	Write to Output in High-Z	-	30	-	35	ns
t _{ow}	Output Active from End of Write	0	-	0	-	ns

Timing Waveforms

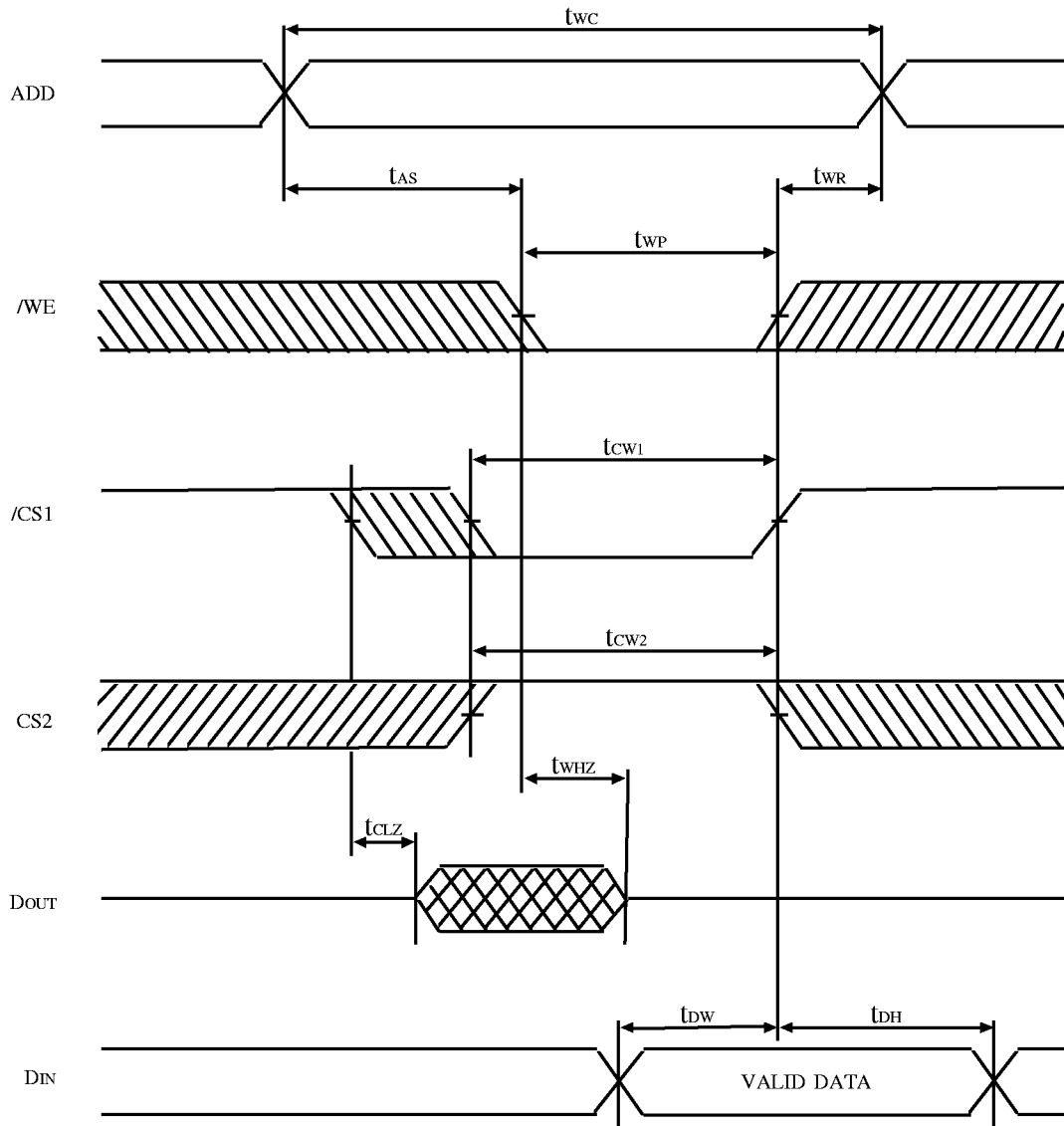
Read Cycle (Note 1)



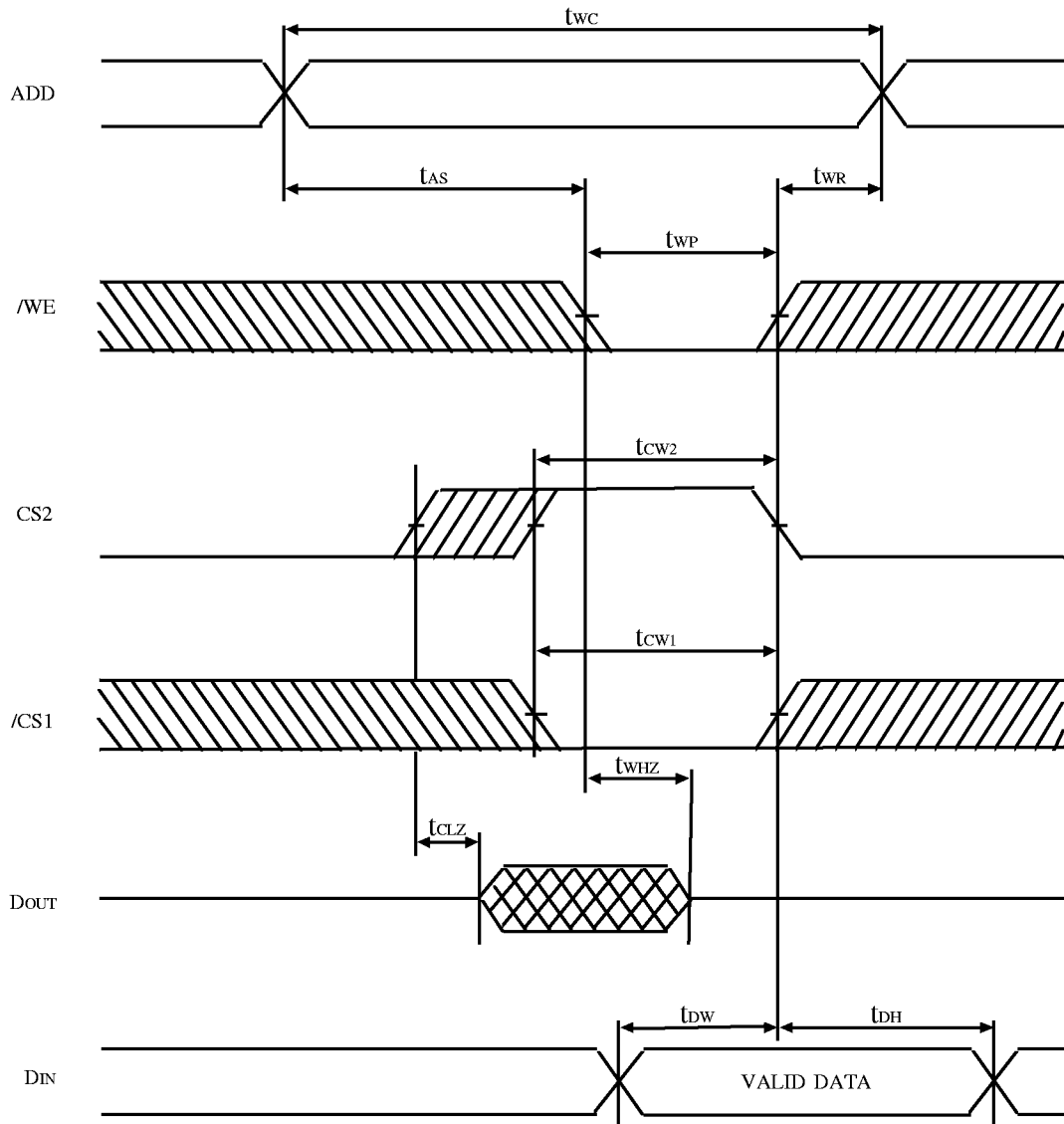
Write Cycle (1) (/WE Controlled) (Notes 2, 3, 4)



Write Cycle (2) (/CS1 Controlled) (Notes 4)



Write Cycle (3) (CS2 Controlled) (Notes 4)



Notes:

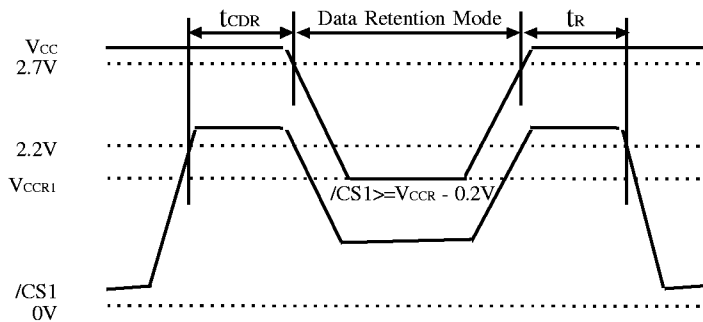
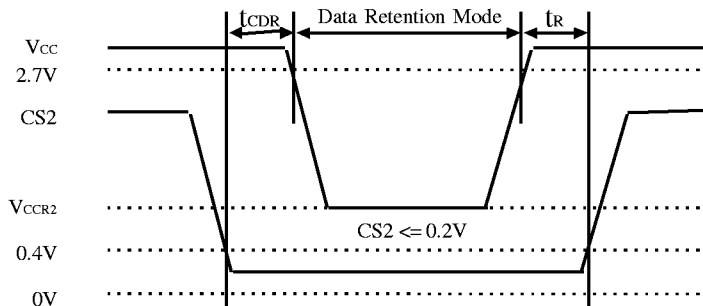
1. /WE is High for Read Cycle.
2. Assuming that /CS1 Low transition or CS2 High transition occurs coincident with or after /WE Low transition. Outputs remain in a high impedance state.
3. Assuming that /CS1 High transition or CS2 Low transition occurs coincident with or prior to /WE High transition. Outputs remain in a high impedance state.
4. Assuming that /OE is high for write cycle. Outputs are in a high impedance state during this period.

Data Retention Characteristics

Symbol	Parameter			Min	Typ	Max	Unit	
V_{CCR}	Data Retention Supply Voltage			2.0	-	3.3	V	
I_{CCR}	Data Retention Current	GM76U8128C	$V_{CC}=3.0V$	L - Version	-	1	50	μA
				LL - Version	-	0.5	15*	
		GM76U8128C-E GM76U8128C-I		L - Version	-	1	30	
				LL - Version	-	0.5	20*	
t_{CDR}	Chip Select to Data Retention Time			0	-	-	ns	
t_R	Operation Recovery Time			t_{RC}^{**}	-	-	ns	

* $3\mu A$ max at $T_A = 0 \sim 40C$

** t_{RC} = Read Cycle

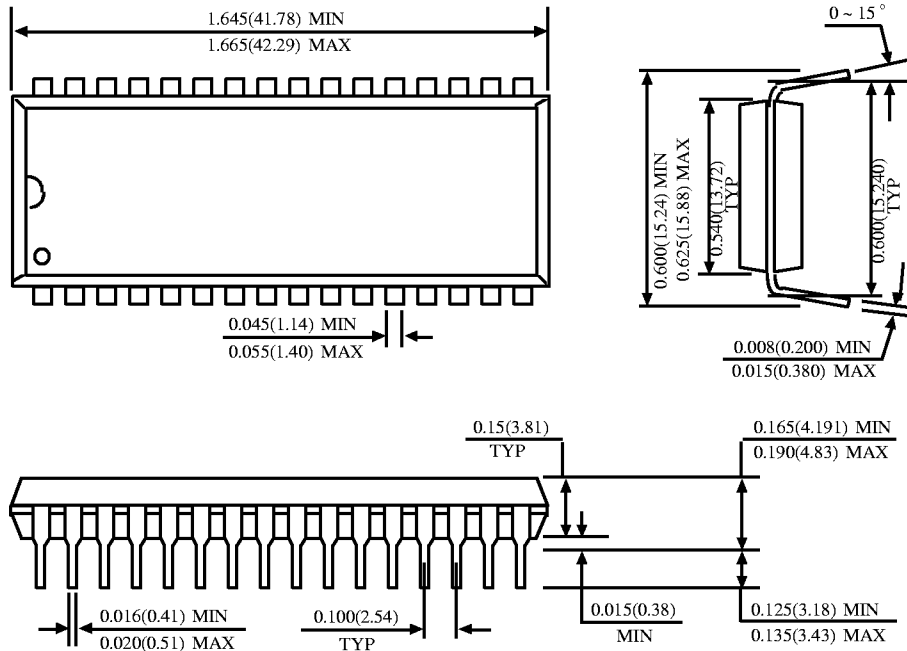
* Low V_{CC} Data Retention Mode: (1) /CS1 Controlled* Low V_{CC} Data Retention Mode: (2) CS2 Controlled

Notes: In Data Retention Mode, CS2 controls the Address, /WE, /CS1, /OE and D_{IN} buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If /CS1 controls the data retention mode, CS2 must satisfy either $CS2 > V_{CCR} - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (Address, /WE, /OE, I/O) can be in the high impedance state.

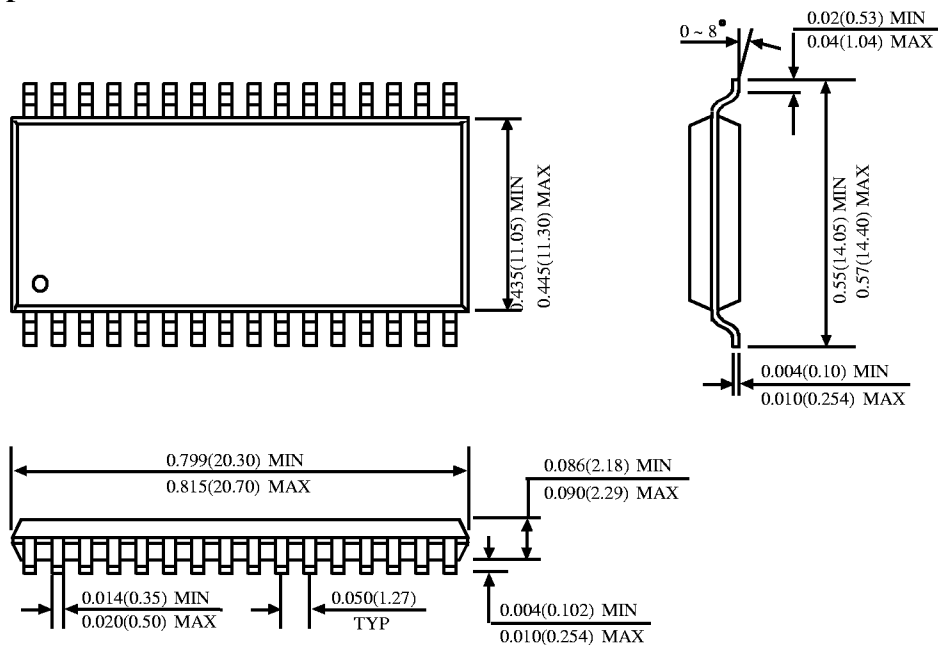
Package Dimensions

Unit: Inches (mm)

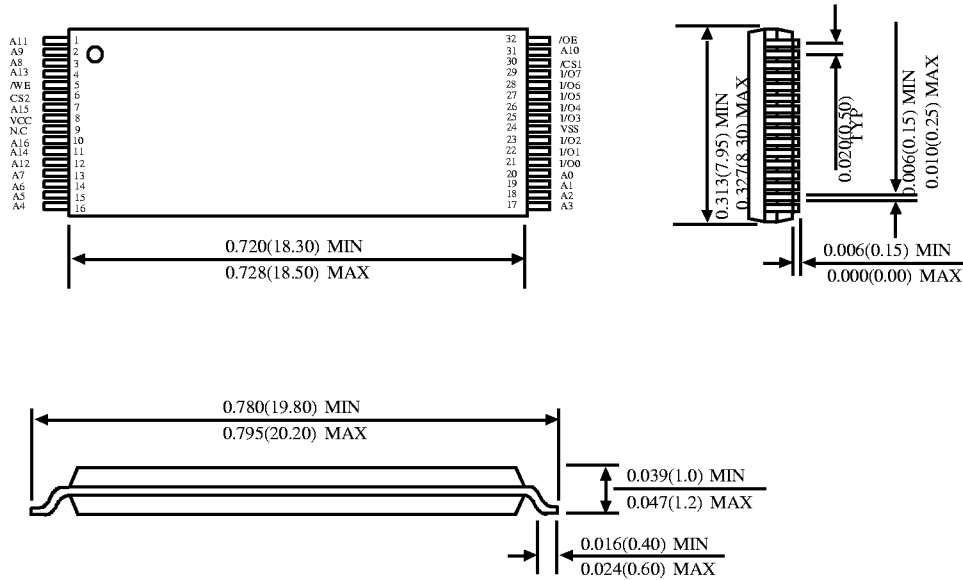
32 DIP



32 SOP



32 TSOP I (8x20mm)



32Small TSOP-I(8x13.4mm)

