T-51-10-10

10-bit tracking monolithic A-D converter

ZN433 Series

FEATURES

- ±½LSB linearity error
- 3 operating temperature ranges
- 1 μs conversion time (assuming continuous tracking)
- Input range as desired
- ±5V supplies, TTL/CMOS compatible
- Parallel and serial outputs
- Bipolar monolithic construction
- No missing codes over full operating temperature range

DESCRIPTION

The ZN433 range of tracking A-D converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), tracking logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast window comparator with good overload recovery.

The tracking principle ensures continuous up to date conversion data. This is suitable for single channel conversion, e.g. digital transducers, and often obviates the need for sample and hold.

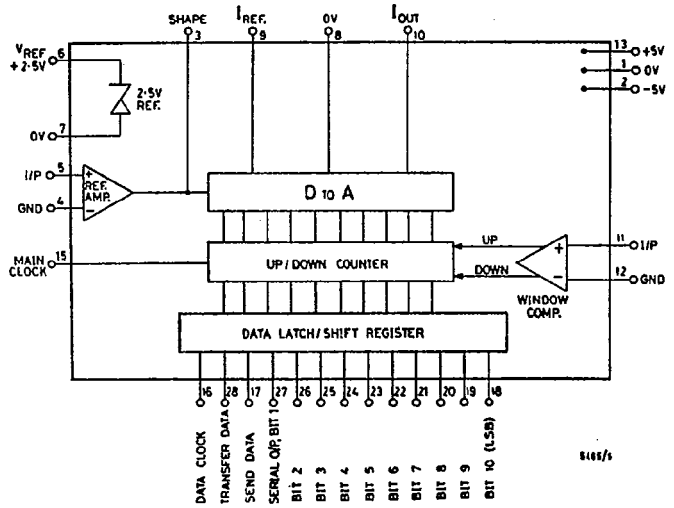

Fig. 1 System diagram

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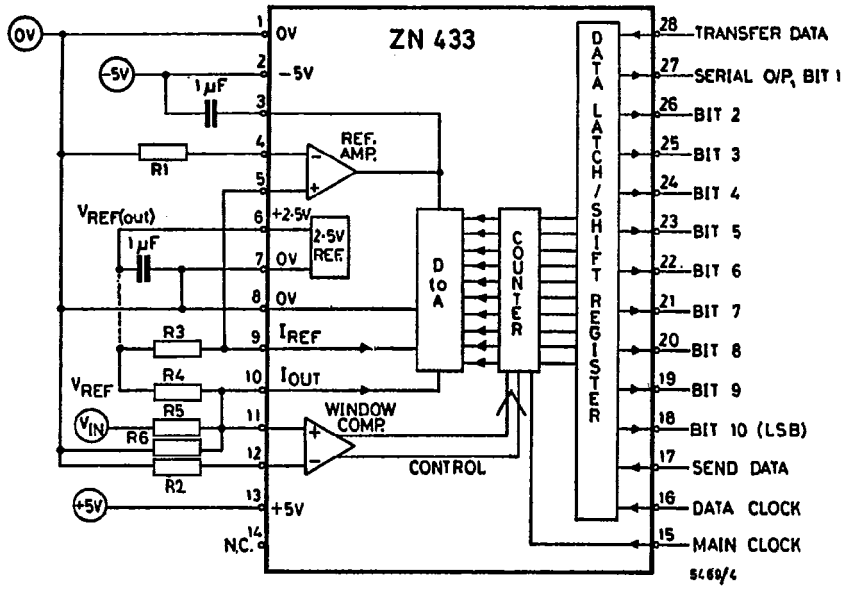

Fig. 2 Typical external components

See page 2-50 for calculation of resistor values. When the internal reference is used, $V_{REF(out)}$ (pin 6) is connected to R3 and R4 as shown. An external reference may also be used, which for ratiometric operation can vary by ±20% of nominal.

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN433J-10	−55 to +125°C	Ceramic
ZN433BJ-10	−40 to +85°C	Ceramic
ZN433CJ-10	0 to 70°C	Ceramic

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ABSOLUTE MAXIMUM RATINGS

Supply voltage	±7V
Logic input voltage	$+V_{CC}$ and 0V
Storage temperature range	−55 to +125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	t_{amb} = +25°C			Over Spec. Temp. range		Units	Conds.
	Min.	Typ.	Max.	Min.	Max.		
Converter Resolution	10			10		Bits	Note 1
Non-linearity			±0.5			LSB	
Differential non-linearity		±0.5				LSB	Note 1
D-A reference current, I_{REF} (pin 9)	0.8		1.2	0.8	1.2	mA	Note 2
Max. clock rate	1	1.2		1		MHz	Note 3
Nominal analogue input range	−2.5		+2.5			V	Note 4
Supply rejection		0.1				%/V	
Gain T.C. (note 5)		10				ppm/°C	
Zero T.C.		7				ppm/°C	
Supply voltage	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current		50				mA	
Power consumption		500				mW	
Internal voltage reference Output voltage		2.480				V	
Output voltage tolerance (note 6)			±1.5			%	
Slope impedance		0.75				Ω	
Maximum reference load current		±4				mA	

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CHARACTERISTICS (Cont.)

Parameter	t_{amb} = +25°C			Over Spec. Temp. range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
Logic							
High level input voltage	2.0			2.0		V	
Low level input voltage			0.8		0.8	V	
High level input current		7				μA	$V_S = \pm 5.5V$, $V_I = 2.4V$
		50				μA	$V_S = \pm 5.5V$, $V_I = 5.5V$
Low level input current		1				μA	$V_S = \pm 5.5V$, $V_I = 0.4V$
High level output voltage	2.4			2.4		V	$I_{load} = -40\mu A$
Low level output voltage			0.4		0.4	V	$I_{load} = 1.6mA$

Note 1 No missing codes over full temperature range.

Note 2 The full-scale D-A output current $I_{OUT} = 4$ times I_{REF}. For optimum performance $I_{REF} = 1.0mA$.

Note 3 For main clock waveform see Fig. 5, page 2-51. Input signals which do not change by more than 1LSB/μs may be tracked continuously without the need for a sample and hold. This corresponds to a full-scale bandwidth of 300Hz. Higher frequencies may be tracked if the amplitude is reduced, e.g. the half full-scale bandwidth is 600Hz.

Note 4 Single polarity and other input ranges may be provided by different input resistor values (see page 2-50).

Note 5 Excluding reference.

Note 6 For typical temperature performance see Fig. 6, page 2-52.

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TEST CIRCUIT

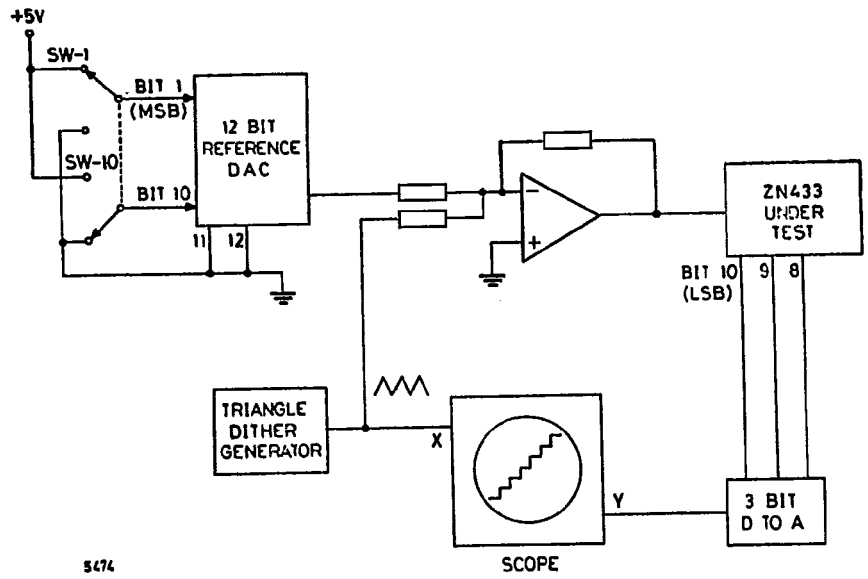

Fig. 3 Dynamic crossplot accuracy test

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the charactristic to be displayed. For example, code 10000 00000 would select half full-scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = ±4 × LSB) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference DAC in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN433 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit DAC of at least 6-bit accuracy and the analogue output used as the Y deflection of the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

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CALCULATION OF EXTERNAL RESISTORS (See Fig. 2, page 2-46).

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator which both operate in a virtual earth mode. Thus: $R_1 = R_3$

   And R_2 = parallel combination of R_4, R_5, and R_6.
3. I_{REF} should be 1.0mA, though it may be varied from 0.8 to 1.2mA.

   Therefore $$R_3 = \frac{V_{REF}}{1.0mA}$$

   $I_{out\ FS}$ is four times I_{REF}, i.e., 4mA (I_{out} for zero reading is 0mA).
4. Analysing the network yields the following:

$$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$

$$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{outFS}}$$

   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 625Ω as this determines the D-A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	2.5kΩ	625Ω	2.5kΩ	1.25kΩ	1.25kΩ	∞
+2.5	−2.5	5*	5kΩ	625Ω	5kΩ	2.5kΩ	1.25kΩ	2.5kΩ
+2.5	0	2.5	2.5kΩ	625Ω	2.5kΩ	∞	625Ω	∞
+5	0	2.5	2.5kΩ	625Ω	2.5kΩ	∞	1.25kΩ	1.25kΩ
+4	−2	2.5	2.5kΩ	625Ω	2.5kΩ	1.875kΩ	1.5kΩ	2.5kΩ
+4	−2	12*	12kΩ	625Ω	12kΩ	1.875kΩ	1.5kΩ	2.5kΩ
+10	−10	2.5	2.5kΩ	625Ω	2.5kΩ	1.25kΩ	5kΩ	1.67kΩ

Note 1 Nearest prefered value may be used for R_1, R_2 and R_6.

*Note 2 External reference.

7. For setting up R_4 will adjust the offset.
   R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

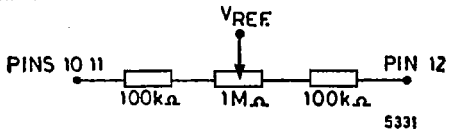

Fig. 4 Offset circuit with unipolar operation

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LOGIC DETAILS

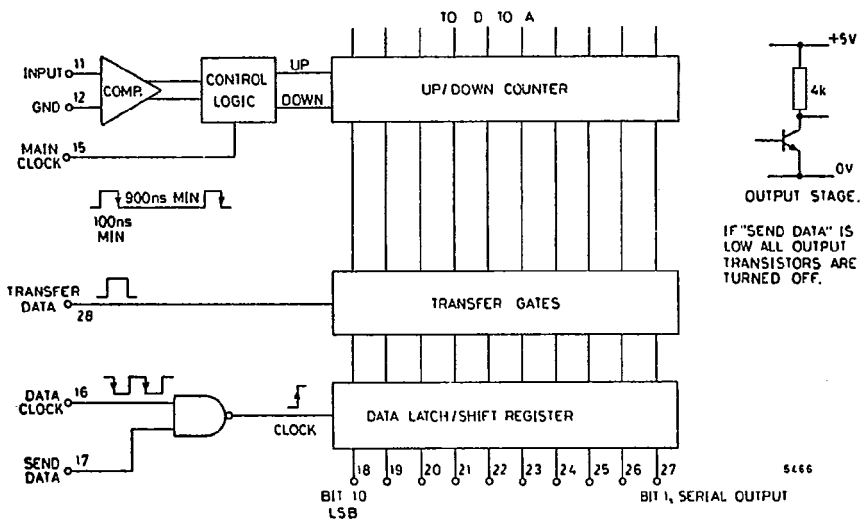

Fig. 5 Logic system

NOTES ON LOGIC DIAGRAM

1. The Window comparator and control logic determine whether the counter will clock up or down or keep the same value on an active (negative going) edge of the main clock.

2. Parallel data from the up/down counter will be loaded into the output data latch/shift register when the TRANSFER DATA input is HIGH. TRANSFER DATA should not be taken HIGH until 150ns after the MAIN CLOCK edge and should go LOW before the next MAIN CLOCK edge. The minimum TRANSFER DATA pulse width is 50ns.

If TRANSFER DATA is held permanently HIGH then the counter outputs will appear directly at the bit outputs.

3. Serial output data (MSB first) can be obtained from the MSB output (pin 27) by applying a DATA CLOCK (pin 16, 1MHz maximum, 100ns minimum pulse width).

4. A LOW on SEND DATA (pin 17) disables the DATA CLOCK and turns off all the output transistors so that all the bit outputs are HIGH (see diagram of output).

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LOGIC CODING

Table 1 Unipolar operation

Analogue input Notes 1, 2	Digital output code MSB LSB
FS – 1LSB	1111111111
FS – 2LSB	1111111110
¾FS	1100000000
½FS + 1LSB	1000000001
½FS	1000000000
½FS – 1LSB	0111111111
¼FS	0100000000
1LSB	0000000001
0	0000000000

Table 2 Bipolar operation

Analogue input Notes 1, 2	Digital output code MSB LSB
+ (FS – 1LSB)	1111111111
+ (FS – 2LSB)	1111111110
+ (½FS)	1100000000
+ (1LSB)	1000000001
0	1000000000
– (1LSB)	0111111111
– (½FS)	0100000000
– (FS – 1LSB)	0000000001
– FS	0000000000

Notes:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full-scale.

OFFSET AND GAIN SETTING

For unipolar operation, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

For bipolar operation, supply an input of – (full-scale – ½LSB) for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

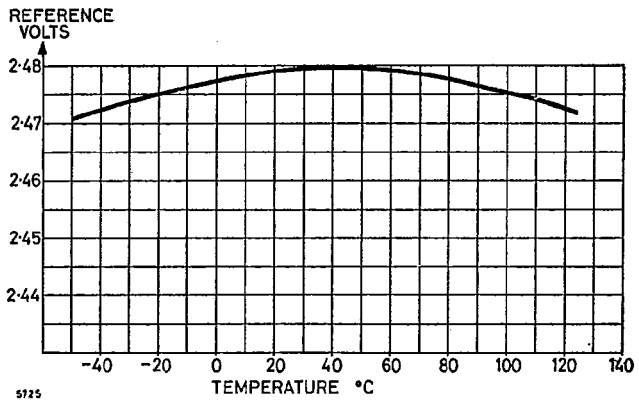

Fig. 6 Typical reference voltage v temperature (all types)

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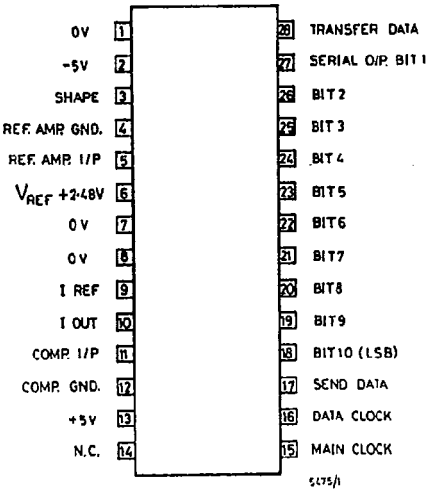
PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT