

FEATURES

- 13-bit resolution
- Pin compatible with AD7839
- Eight DACs in one package
- Buffered voltage outputs
- Wide output voltage swing $V_{DD}-2.5\text{ V}$ to $V_{SS}+2.5\text{ V}$
- 15 μs settling time to $\pm 0.5\text{ LSB}$
- Double-buffered digital inputs
- Microprocessor and TTL/CMOS compatible

APPLICATIONS

- Automatic test equipment
- Instrumentation
- Process control

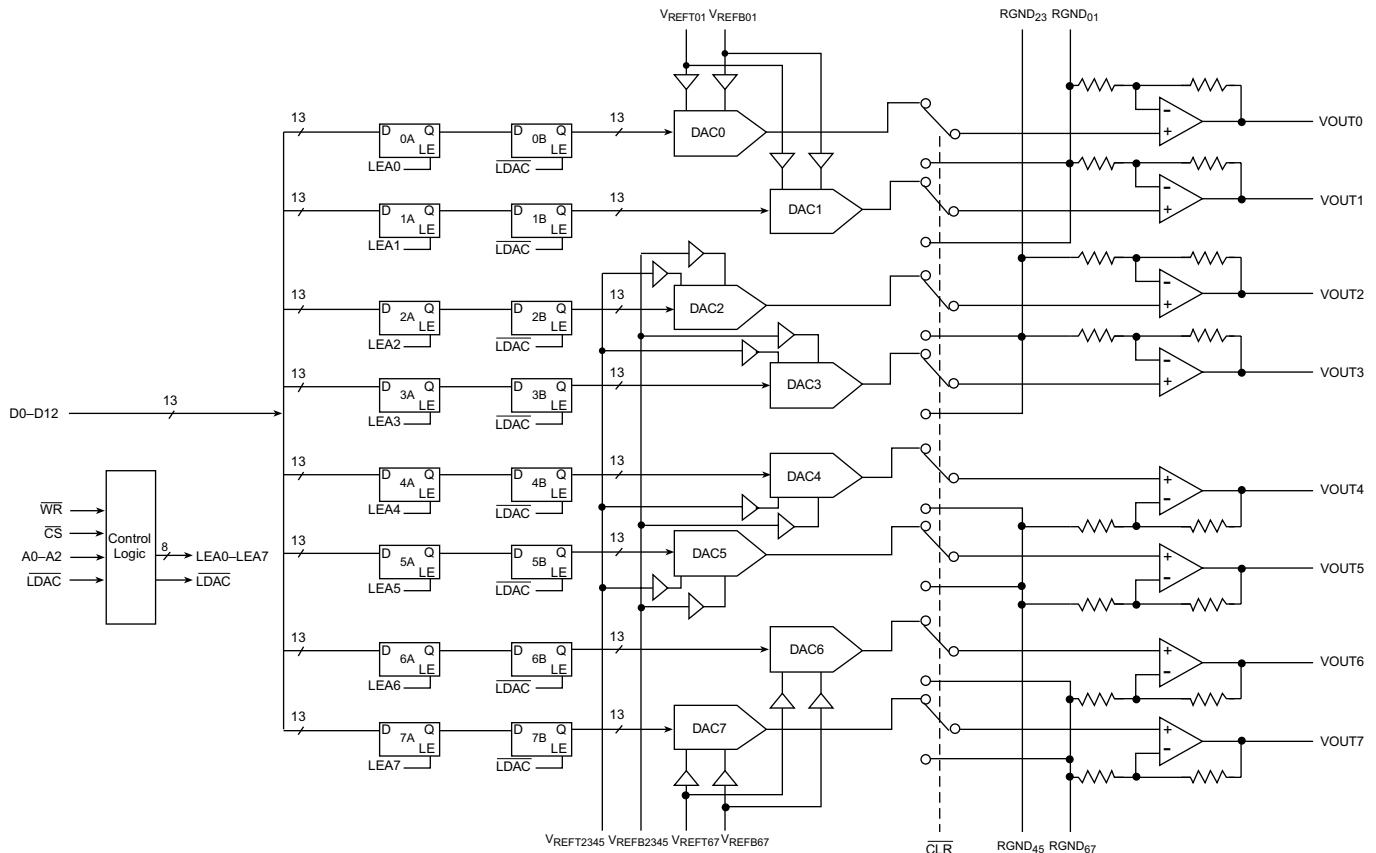
GENERAL DESCRIPTION

The SPT5420 contains eight 13-bit digital-to-analog CMOS converters designed primarily for automatic test equipment applications. It uses novel circuit topology to convert the 13-bit digital inputs into output voltages which are proportionate to the applied reference voltages. Each

DAC's full-scale output voltage and output voltage offset are adjustable with analog inputs (RGND, V_{REFB} , V_{REFT}).

The SPT5420 operates over an industrial temperature range of $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and is available in a 10 x 10 mm, 44-lead metric quad flat pack (MQFP) plastic package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25 °C

Supply Voltages

V _{CC}	+6 V
V _{DD}	+15 V
V _{SS}	-15 V

Temperature

Operating Temperature	-40 to +85 °C
Storage	-65 to +150 °C

Input Voltages

V _{REFT}	V _{SS} -0.3 V to V _{DD} +0.3 V
V _{REFB}	V _{DD} +0.3 V to V _{SS} -0.3 V
Digital inputs	-0.3 V to V _{CC} +0.3 V

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = T_{MIN} to T_{MAX}, V_{CC} = +5.0 V, V_{DD} = +11.5 V, V_{SS} = -8.0 V, V_{REFT} = 3.5 V, V_{REFB} = -1.5 V, R_L = +10 kΩ, C_L = 50 pF, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5420			UNITS
			MIN	TYP	MAX	
Accuracy						
Resolution		VI	13			Bits
Integral Linearity Error (ILE)		VI	-2.0	±0.5	+2.0	LSB
Differential Linearity Error (DLE)		VI	-1.0	±0.3	+1.0	LSB
Zero-Scale Error		VI	-25		+25	mV
Full Scale Error		VI	-25		+25	mV
Gain Error		VI	-25		+25	mV
Reference Inputs						
Input Current		IV			±100	nA
V _{REFT} ¹		VI	0	+3.5	+5.0	V
V _{REFB} ²		VI	-5.0	-1.5	0	V
RGND Inputs						
DC Input Impedance		V		60		kΩ
Input Range		IV	-2.0		2.0	V
Output Characteristics						
Output Swing ^{3,4}		VI		+7/-3		V
Short Circuit Current		IV			15	mA
Resistive Load		VI	5			kΩ
DC Output Impedance		IV			1.0	Ω
Digital Inputs						
Logic 1 Voltage		VI	2.4			V
Logic 0 Voltage		VI			0.8	V
Maximum Input Current		VI	-10		10	μA/pin
Input Capacitance		V		10		pF

Notes:

- V_{REFT} < 8 V + (V_{SS} × 0.5); e.g., if V_{SS} = -8 V, then V_{REFT} < 4 V
- V_{REFB} > (V_{DD} × 0.5) - 9.5 V; e.g., if V_{DD} = 11 V, then V_{REFB} > -4 V
- V_{SS} + 2.5 V ≤ V_{OUT} ≤ V_{SS} + 16.0 V for 18.5 V ≤ V_{DD} - V_{SS} ≤ 20.0 V
V_{SS} + 2.5 V ≤ V_{OUT} ≤ V_{DD} - 2.5 V for V_{DD} - V_{SS} ≤ 18.5 V
- V_{OUT} = 2 × (V_{REFB} + [V_{REFT} - V_{REFB}] × $\frac{\text{INPUT CODE}}{8192}$) - V_{RGND}

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = +5.0$ V, $V_{DD} = +11.5$ V, $V_{SS} = -8.0$ V, $V_{REFT} = 3.5$ V, $V_{REFB} = -1.5$ V, $R_L = +10$ k Ω , $C_L = 50$ pF, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5420			UNITS
			MIN	TYP	MAX	
Power Requirements						
V_{CC} Supply Voltage (Digital)		IV	4.75	5	5.25	V
V_{DD} Supply Voltage (Analog) ^{1,2}		VI	5	11.5	12.5	V
V_{SS} Supply Voltage (Analog) ^{1,2}		VI	-12.5	-8	-5	V
I_{CC} Supply Current		VI			0.5	mA
I_{DD} Supply Current	Outputs Unloaded	VI		5	10	mA
I_{SS} Supply Current	Outputs Unloaded	VI		5	10	mA
Power Supply Rejection Ratio	$\Delta V_{DD} / \Delta Full$ Scale	IV		80		dB
	$\Delta V_{SS} / \Delta Full$ Scale	IV		80		dB
Dynamic Performance						
Output Settling Time ³ (Full Scale Change to ± 0.5 LSB)	$C_L \leq 220$ pF	IV			15	μ s
Slew Rate		V		2.0		V/ μ s
Glitch Impulse		V		35		nV-s
Channel to Channel Isolation		V		100		dB
DAC to DAC Crosstalk		V		40		nV-s
Digital Crosstalk		V		1		nV-s
Digital Feedthrough		V		1		nV-s
Timing Characteristics (See page 4)						
		IV				

- Supplies should provide 2.5 V headroom above and below max output swing.
- $V_{DD} - V_{SS} \leq 20$ V
- Output can drive 10,000 pF without oscillation, but with settling time degradation.

DEFINITION OF SELECTED TERMINOLOGY

Channel-to-Channel Isolation

Channel-to-Channel isolation refers to the proportion of input signal from one DAC's reference input that appears at the output of the other DAC. It is expressed in dBs.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is defined as the glitch impulse that appears at one DAC's output due to both the digital change and subsequent analog output change at any other DAC. It is specified in nV-s.

Digital Crosstalk

The glitch impulse transferred to one DAC's output due to a change in digital input code of any other DAC. It is specified in nV-s.

Digital Feedthrough

Digital feedthrough is the noise at a DAC's output caused by changes to D0–D12 while \overline{WR} is high.

TEST LEVEL CODES

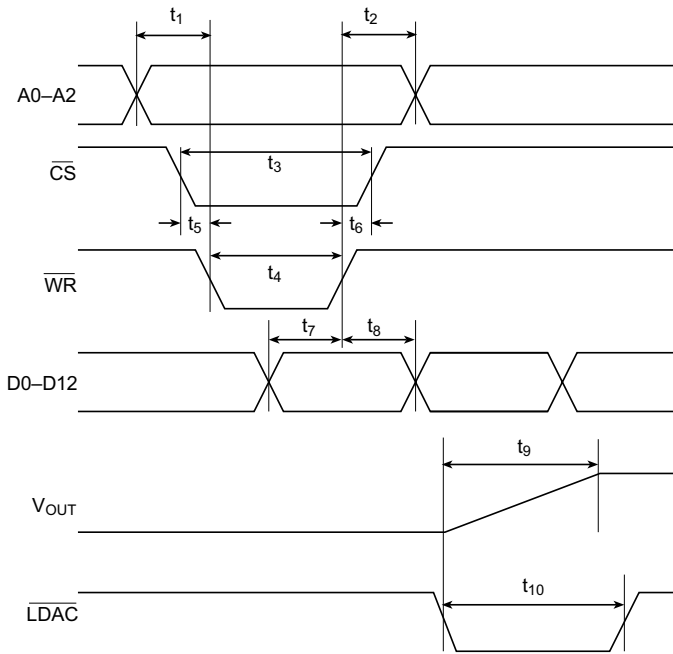
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

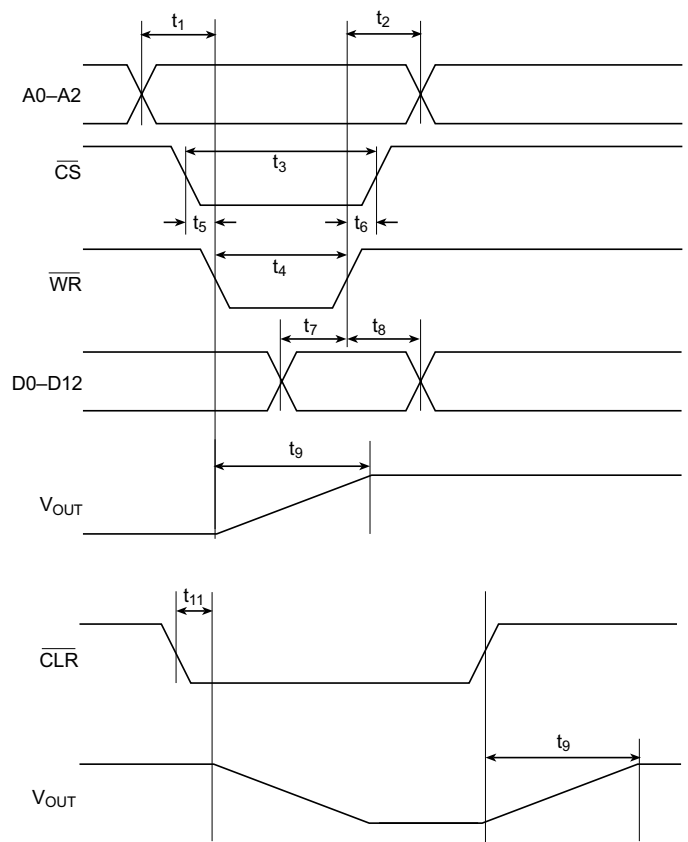
LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at $T_A = +25$ °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at $T_A = +25$ °C. Parameter is guaranteed over specified temperature range.

TIMING CHARACTERISTICS

**Figure 1a – Timing Diagram: Latched Mode
(LDAC Strobed)**



**Figure 1b – Timing Diagram: Transparent Mode
(LDAC Held Low)**



PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Address Valid to WR Setup	t_1	20			ns
Address Valid to WR Hold	t_2	0			ns
CS Pulse Width Low	t_3	50			ns
WR Pulse Width Low	t_4	50			ns
CS to WR Setup	t_5	0			ns
WR to CS Hold	t_6	0			ns
Data Setup	t_7	25			ns
Data Hold	t_8	0			ns
Settling Time ¹	t_9			15	us
LDAC Pulse Width Low	t_{10}	50			ns
CLR Pulse Activation	t_{11}			300	ns

NOTES:

All digital input rise and fall times are measured from 10% to 90% of +5 V.
 $t_r = t_f = 5$ ns.

1. $R_L = 10$ k Ω
 $C_L \leq 220$ pF

VOLTAGE REFERENCES AND ANALOG GROUND INPUTS

Three V_{REFTXX} and three V_{REFBXX} inputs set the output range of the three corresponding groups of DACs (0 and 1; 2 through 5; 6 and 7). Four $RGND_{XX}$ inputs set the output offset voltage of the four corresponding groups of DACs (0 and 1; 2 and 3; 4 and 5; 6 and 7). The formula for output swing and offset is presented in the “Analog Outputs” section below.

DAC ADDRESSING AND LATCHING

Each DAC has an input latch which receives data from the data bus, and a DAC latch which receives data from the input latch. The analog output of each DAC corresponds to the data in its DAC latch. One of the eight input latches is addressed by the address lines A(2:0) according to Table I. While \overline{CS} and \overline{WR} are low, the addressed input latch is transparent and the seven other input latches are latched. Bringing \overline{CS} or \overline{WR} high latches data into the addressed input latch. While \overline{LDAC} is low, all eight DAC latches are transparent. Bringing \overline{LDAC} high latches data into the DAC latches. While \overline{CS} , \overline{WR} and \overline{LDAC} are low, both latches are transparent and input data is transferred directly to the selected DAC. While \overline{CLR} is low, all DAC outputs are set to their corresponding $RGND_{XX}$. Bringing \overline{CLR} high returns each DAC’s output to the voltage corresponding to the data in each DAC latch.

Table II summarizes this information, and figures 1a and 1b should be referenced for timing limitations.

POWER SUPPLY SEQUENCING

The sequence in which V_{DD} , V_{SS} and V_{CC} come up is not critical. The reference inputs, V_{REFTXX} and V_{REFBXX} , must come on only after V_{DD} and V_{SS} have been established. However, they may be turned on prior to V_{CC} . The digital inputs must be driven only after V_{DD} , V_{SS} and V_{CC} have been established. Reverse the power-on sequence for power-down.

ANALOG OUTPUTS VS DIGITAL INPUT CODE

The output voltage range is equal to twice the difference between V_{REFTXX} and V_{REFBXX} . The output voltage is given by:

$$V_{OUT} = 2 \times (V_{REFB} + [V_{REFT} - V_{REFB}] \times \frac{INPUT\ CODE}{8192}) - V_{RGND}$$

CODE = 0 – 8191

Table I – DAC Addressing

A2	A1	A0	Addressed Input Latch DAC#
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table II – Control Logic Table

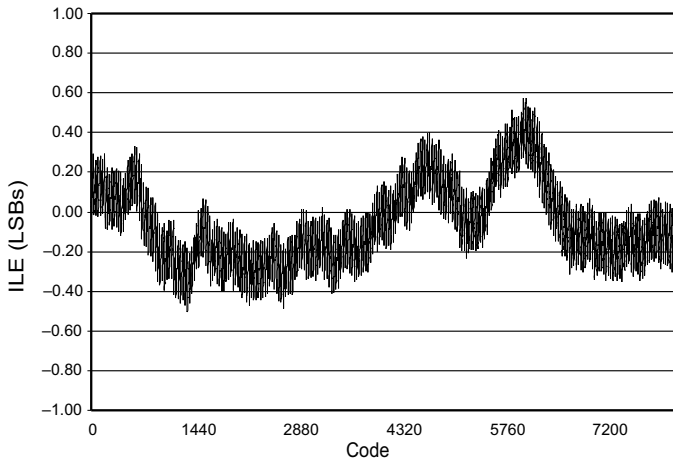
\overline{WR}	\overline{CS}	\overline{LDAC}	\overline{CLR}	Input Latch	DAC Latch
0	0	x	1	transparent ¹	x
1	x	x	1	latched	x
x	1	x	1	latched	x
x	x	0	1	x	transparent
x	x	1	1	x	latched
x	x	x	0	DAC outputs at $RGND_{XX}$	

Note:

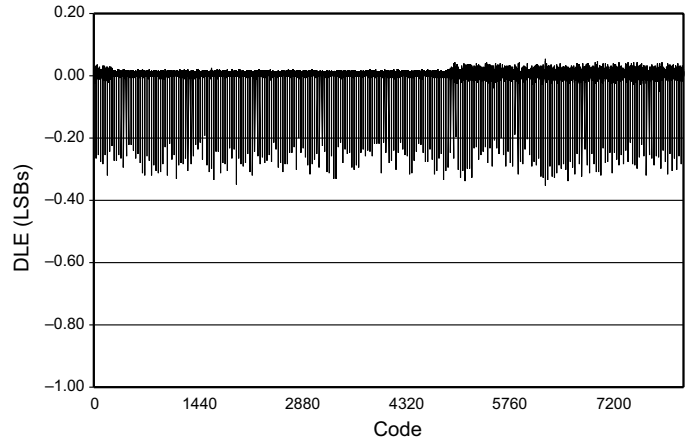
1. Only the input latch addressed by A(2:0) is transparent. The other input latches are latched.

TYPICAL PERFORMANCE CHARACTERISTICS

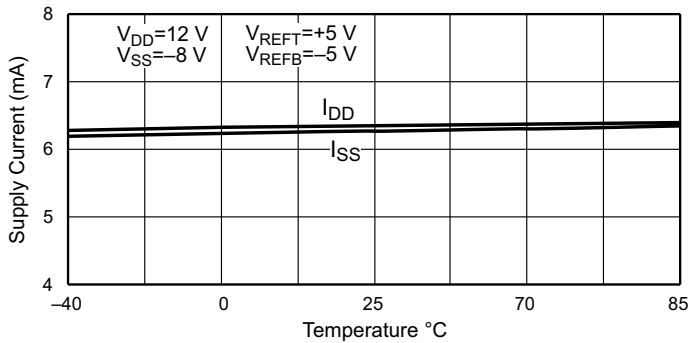
Integral Linearity Error vs Code



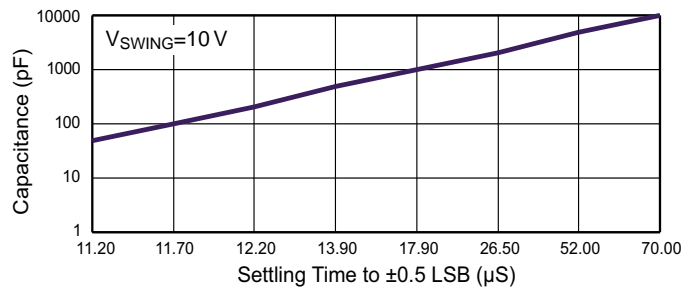
Differential Linearity Error vs Code



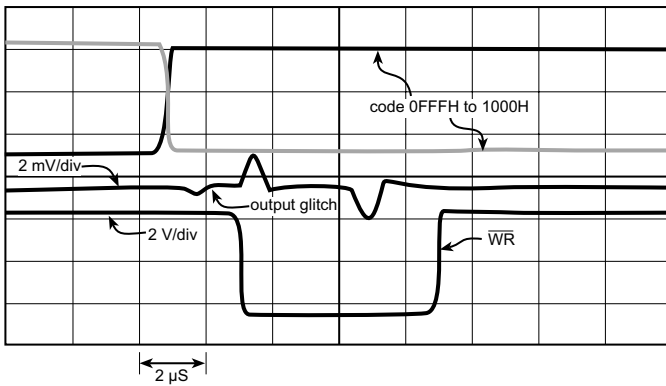
I_{DD}/I_{SS} vs Temperature



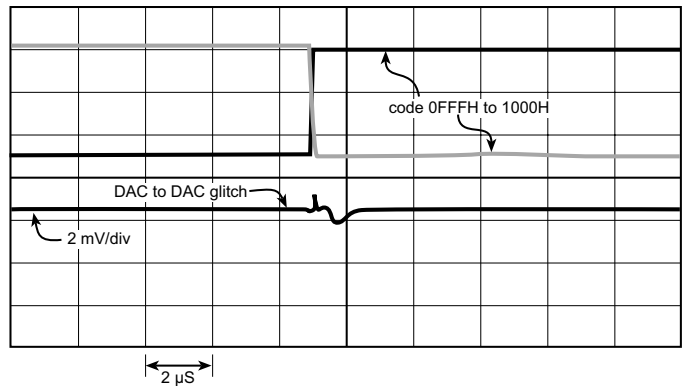
Load Capacitance vs Settling Time



Digital-to-Analog Glitch Impulse

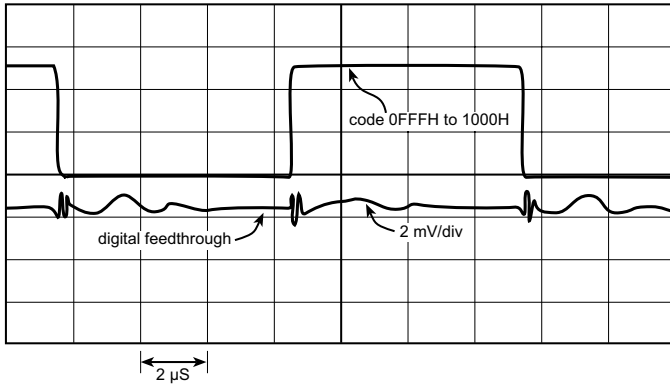


DAC to DAC Crosstalk

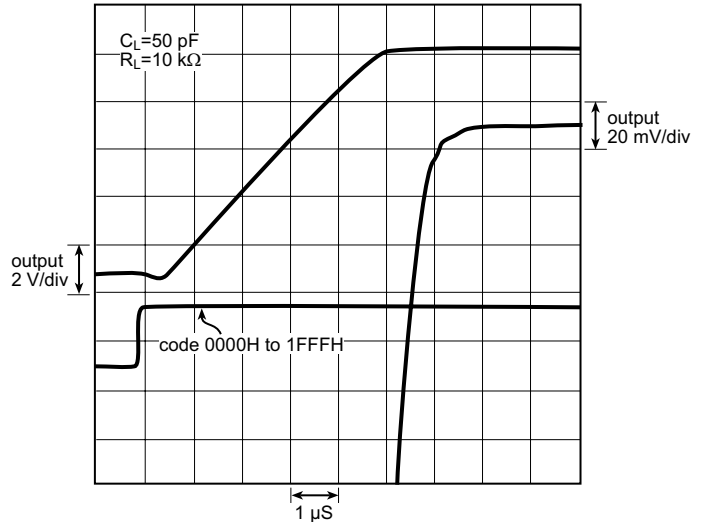


TYPICAL PERFORMANCE CHARACTERISTICS

Digital Feedthrough

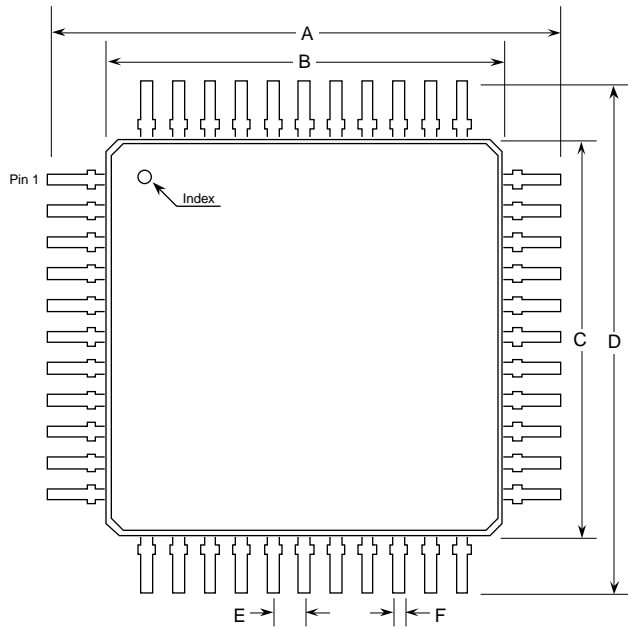


Slew and Settling Time

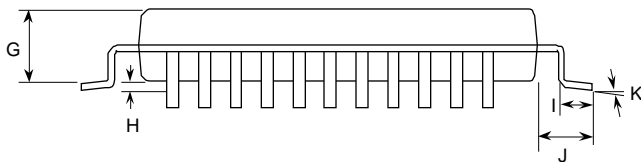


PACKAGE OUTLINE

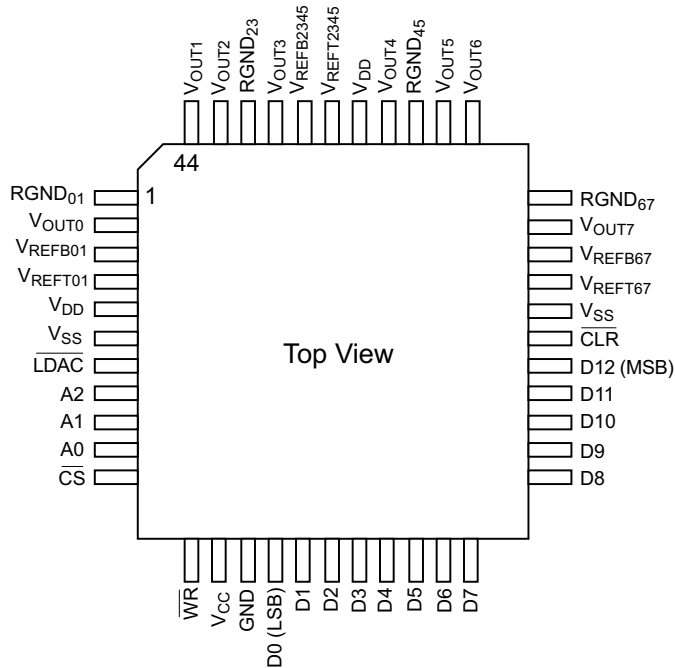
44-Lead MQFP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.5098	0.5295	12.95	13.45
B	0.3917	0.3957	9.95	10.05
C	0.3917	0.3957	9.95	10.05
D	0.5098	0.5295	12.95	13.45
E	0.0311	0.0319	0.79	0.81
F	0.0118	0.0177	0.30	0.45
G	0.0768	0.0827	1.95	2.10
H	0.0039	0.0098	0.10	0.25
I	0.0287	0.0406	0.73	1.03
J	0.0630 REF		1.60 REF	
K	0°	7°	0°	7°



PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
DIGITAL CONTROL PINS	
\overline{CS}	Chip Select (Active Low)
\overline{WR}	Level Triggered Write Input (Active Low). Used in conjunction with \overline{CS} to write data to the SPT5420 input data latches. Data is latched into selected input data latch on the rising edge of \overline{WR} .

\overline{CLR}	(Active Low) Analog Clear. Sets the output voltages to RGND. (Each RGND is common to a DAC pair.) \overline{CLR} does not reset the digital latches. When \overline{CLR} is brought back high, the DAC outputs revert back to their original outputs as determined by the data in their DAC latches.
LDAC	When this logic input is taken low, the contents of the input latches are transferred to their respective DAC latches. (Active Low) Data is latched on rising edge.
A0 – A2	Addresses DAC0 to DAC7 for loading the eight input latches.
D0 – D12	Digital Inputs (D0 = LSB)

ANALOG PINS

VREFT01	Top Reference Voltage for DACs 0 and 1
VREFT2345	Top Reference Voltage for DACs 2, 3, 4 and 5
VREFT67	Top Reference Voltage for DACs 6 and 7
VREFB01	Bottom Reference Voltage for DACs 0 and 1
VREFB2345	Bottom Reference Voltage for DACs 2, 3, 4 and 5
VREFB67	Bottom Reference Voltage for DACs 6 and 7
RGND ₀₁	Reference Ground for Output Amplifiers 0 and 1
RGND ₂₃	Reference Ground for Output Amplifiers 2 and 3
RGND ₄₅	Reference Ground for Output Amplifiers 4 and 5
RGND ₆₇	Reference Ground for Output Amplifiers 6 and 7
VOUT ₀₋₇	Output Voltage Pins for DAC0 – DAC7

POWER SUPPLY PINS

VCC	Digital +5 V Supply
VDD	Analog +11.5 V Supply (Nominal)
VSS	Analog –8 V Supply (Nominal)
GND	Ground

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT5420SIM	–40 to +85 °C	44L MQFP

For additional information regarding our products, please visit CADEKA at: cadeka.com

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