

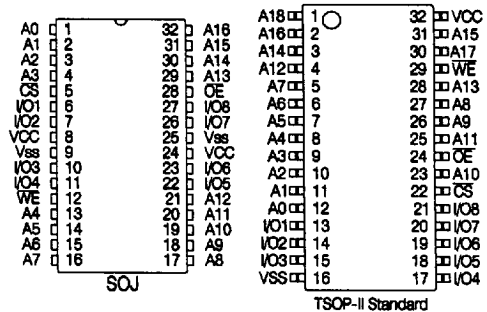
DESCRIPTION

The HY638100 is a 1,048,576-bit high-speed Static Random Access Memory organized as 131,072 words by 8 bits. The HY638100 uses eight common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using HYUNDAI's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

FEATURES

- High speed - 15/17/20/25ns
- Low power consumption
 - HY638100AS
 - Active : 150mA (max.)
 - Standby (TTL) : 50mA (max.)
 - (CMOS) : 2mA (max.)
 - HY638100AL
 - Active : 150mA (max.)
 - Standby (TTL) : 50mA (max.)
 - (CMOS) : 100µA (max.)
- Single 5V±10% power supply
- TTL compatible inputs and outputs
- 32 pin 400 mil SOJ(Revolutionary)
- 32 pin 400 mil TSOP-II

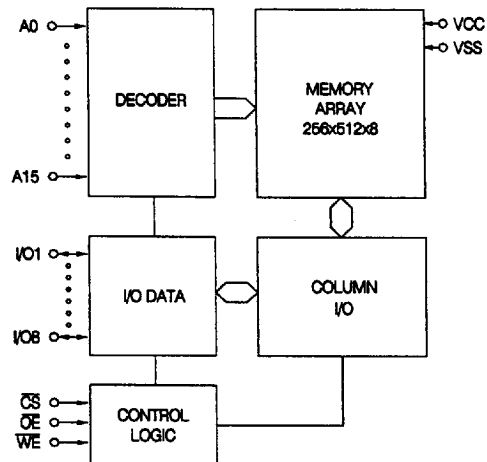
PIN CONNECTION



BLOCK DIAGRAM

PIN DESCRIPTION

Pin Name	Pin Function
CS	Chip Select
WE	Write Enable
OE	Output Enable
A0-A15	Address Inputs
I/O1-I/O8	Data Input/Output
Vcc	Power(+5V)
Vss	Ground



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNIT
VCC, VIN, VOUT	Power Supply, Input/Output Voltage	-0.5 to 7.0	V
TA	Operating Temperature	0 to 70	°C
TBIAS	Temperature Under Bias	-10 to 125	°C
TSTG	Storage Temperature	-65 to 150	°C
Pd	Power Dissipation	1.0	W
IOUT	Data Output Current	50	mA
TSOLDER	Lead Soldering Temperature & Time	260 • 10	°C • sec

Note:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.2	-	VCC + 0.5	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	-	0.8	V

Note:

1. VIL = -3.0V for pulse width less than 10ns

TRUTH TABLE

MODE	I/O OPERATION	CS	WE	OE
Standby	High-Z	H	X	X
Output Disabled	High-Z	L	H	H
Read	Data out	L	H	L
Write	Data in	L	L	X

Note:

1. X= Don't Care

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DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V± 10%, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	TYP.	MAX.	UNIT
II	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$		-2	-	2	μA
ILO	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$		-2	-	2	μA
ICC1	Average Operating Current	$\overline{CS} = V_{IL}$, $I_{IO} = 0mA$ Min. Duty Cycle = 100%	15ns	-	-	150	mA
			17ns	-	-	150	mA
			20ns	-	-	140	mA
			25ns	-	-	130	mA
ISB	TTL Standby Current (TTL Inputs)	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} , Min. Cycle		-	-	50	mA
ISB1	CMOS Standby Current (CMOS Inputs)	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		-	-	2	mA
			L	-	20	100	μA
VOL	Output Low Voltage	$I_{OL} = 8.0mA$		-	-	0.4	V
VOH	Output High Voltage	$I_{OH} = -4.0mA$		2.4	-	-	V

Note:

1. Typical values are at VCC=3.3V, T=25°C

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AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V ±10%, unless otherwise noted.)

#	SYMBOL	PARAMETER	15		17		20		25		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE											
1	t _{RC}	Read Cycle Time	15	-	17	-	20	-	25	-	ns
2	t _{AA}	Address Access Time	-	15	-	17	-	20	-	25	ns
	t _{ACS}	Chip Select Access Time	-	15	-	17	-	20	-	25	ns
4	t _{OE}	Output Enable to Output Valid	-	8	-	9	-	10	-	12	ns
5	t _{CLZ}	Chip Select to Low -Z Output	3	-	3	-	3	-	3	-	ns
6	t _{OLZ}	Output Enable to Low-Z Output	3	-	3	-	3	-	3	-	ns
7	t _{CHZ}	Chip Disable to High -Z Output	0	8	0	8	0	8	0	8	ns
8	t _{OHZ}	Output Disable to High -Z Output	0	8	0	8	0	10	0	10	ns
9	t _{OH}	Output Hold from Address Change	3	-	3	-	3	-	3	-	ns
WRITE CYCLE											
10	t _{WC}	Write Cycle Time	15	-	17	-	20	-	25	-	ns
11	t _{CW}	Chip Select to End of Write	11	-	12	-	13	-	15	-	ns
12	t _{AW}	Address Valid to End of Write	11	-	12	-	13	-	15	-	ns
13	t _{AS}	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	t _{WP}	Write Plus Width	11	-	11	-	13	-	15	-	ns
15	t _{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	t _{WHZ}	Write to High-Z Output	0	8	0	8	0	9	0	10	ns
17	t _{DW}	Data to Write Time Overlap	8	-	10	-	10	-	15	-	ns
18	t _{DH}	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
19	t _{OW}	Output Active from End of Write	3	-	3	-	3	-	3	-	ns

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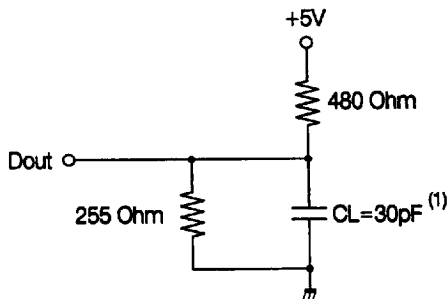
AC TEST CONDITIONS

(TA=0°C to 70°C, VCC=5V ±10%, unless otherwise specified.)

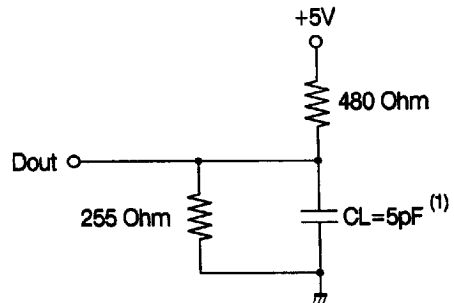
PARAMETER	VALUE
Input Pulse Level	0V to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

AC TEST LOADS

Output Load (A)



Output Load (B)
(for tCHZ, tCLZ, tOLZ, tOHZ, tWHZ & tOW)



Note:
1. Including jig and scope capacitance.

CAPACITANCE

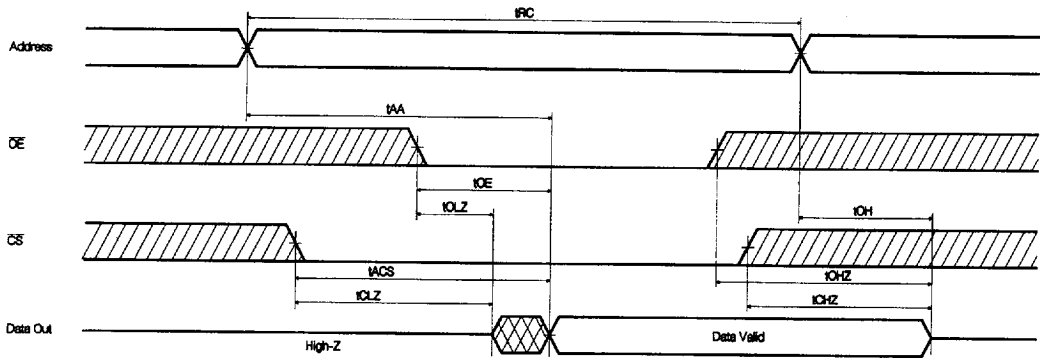
(TA=25°C, f= 1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CIO	Input/Output Capacitance	VIO=0V	10	pF

Note:
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAM

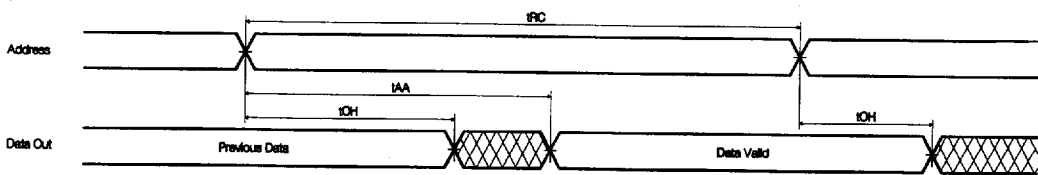
READ CYCLE1



Note (READ CYCLE):

1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. \overline{WE} is high for read cycle.

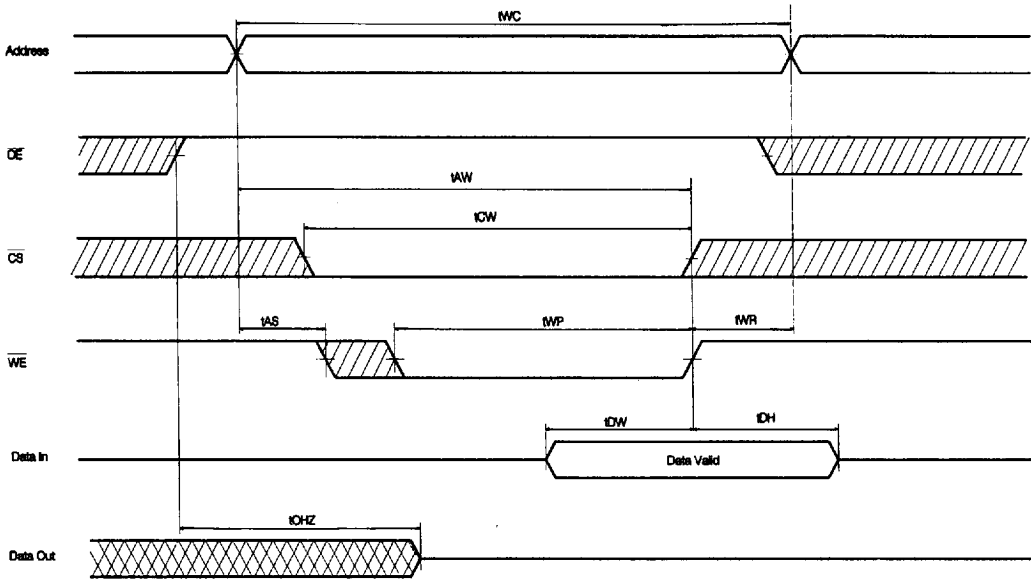
READ CYCLE2



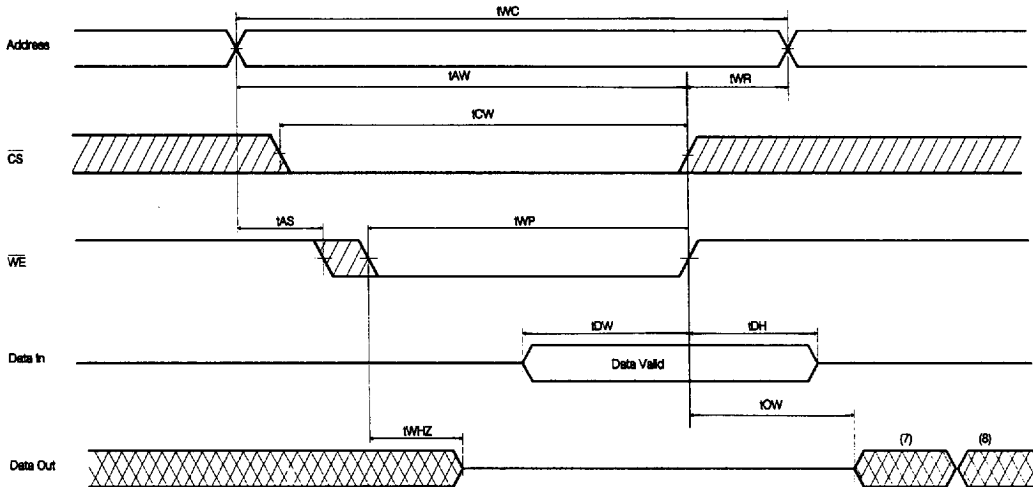
Note (READ CYCLE):

1. \overline{WE} is high for read cycle.
2. Device is continuously selected $\overline{CS}=V_{IL}$.
3. $\overline{OE}=V_{IL}$.

WRITE CYCLE 1 (\overline{OE} Clocked)



WRITE CYCLE 2 (\overline{OE} Low Fixed)



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Note (WRITE CYCLE):

1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going low, and \overline{WE} going low. A write ends at the earliest transition among \overline{CS} going high and \overline{WE} going high. t_{wp} is measured from the beginning of write to the end of write.
2. t_{cw} is measured from the later of \overline{CS} going low to end of write.
3. t_{as} is measured from the address valid to the beginning of write.
4. t_{wr} is measured from the end of write to the address change. t_{wr} applied in case a write ends as \overline{CS} or \overline{WE} going high.
5. If \overline{OE} and \overline{WE} are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If \overline{CS} goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high impedance state.
7. D_{out} is the same phase of latest written data in this write cycle.
8. D_{out} is the read data of the new address.

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DATA RETENTION CHARACTERISTICS (L Version)

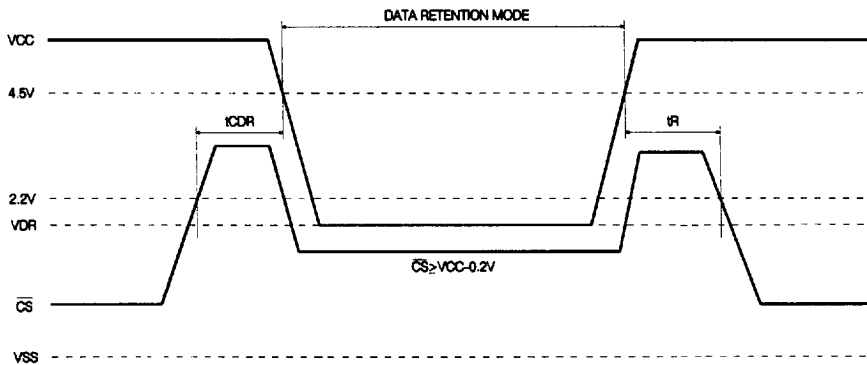
(TA=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	POWER	MIN.	TYP.	MAX.	UNIT
VDR	VCC for Data Retention	$\overline{CS} \geq V_{CC}-0.2V$ $V_{SS} \leq V_{IN} \leq V_{CC}$		2.0	-	-	V
ICCDR	Data Retention Current	$V_{CC}=3.0V$ $\overline{CS} \geq V_{CC}-0.2V$ $V_{SS} \leq V_{IN} \leq V_{CC}$	L	-	10	50	μA
tCDR	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time		tRC ⁽²⁾	-	-	-	ns

Notes:

1. Typical values are at the condition of TA=25°C.
2. tRC is read cycle time.

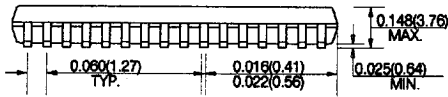
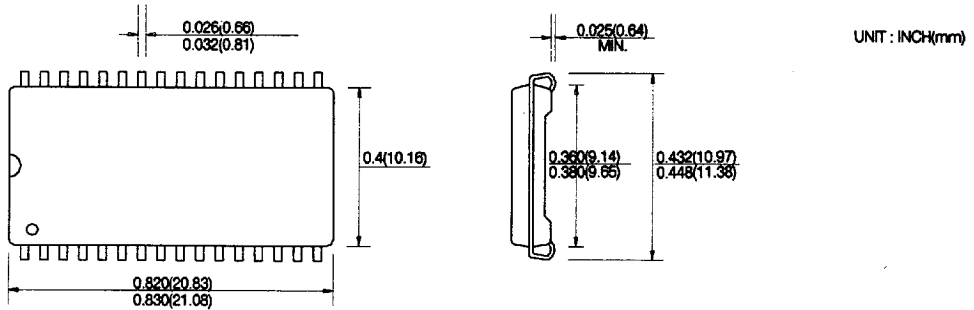
DATA RETENTION TIMING DIAGRAM



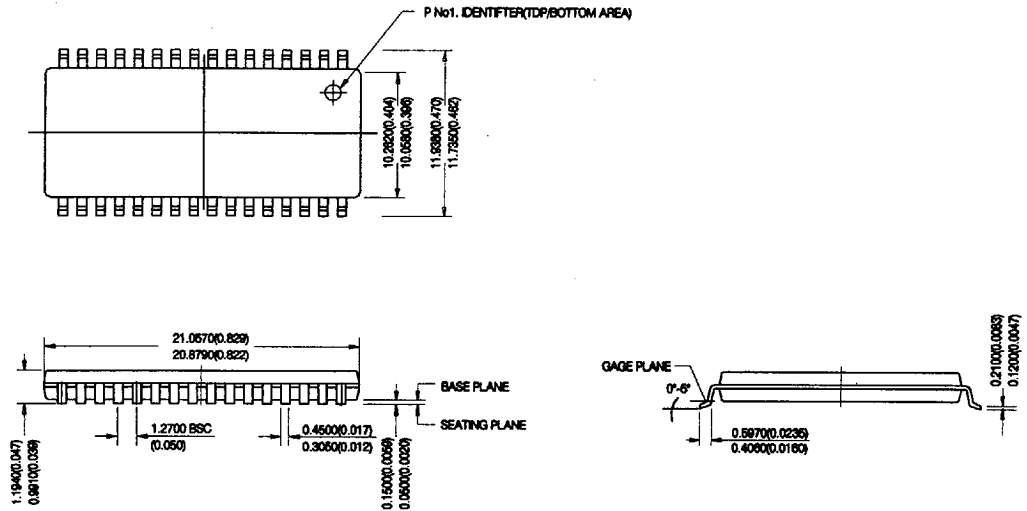
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PACKAGE INFORMATION

400mil 32 pin Small Outline J-Form Package (J)



400 mil 32 pin Plastic Thin Small Outline Package (T2)



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ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY638100AJ	15/17/20/25		SOJ
HY638100ALJ	15/17/20/25	L-part	SOJ
HY638100AT2	15/17/20/25		TSOP-II
HY638100ALT2	15/17/20/25	L-part	TSOP-II
HY638100AR2	15/17/20/25		TSOP-II(R)
HY638100ALR2	15/17/20/25	L-part	TSOP-II(R)

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