

VS-502 Voltage Controlled SAW Oscillator



Features

- Output frequencies from 300 MHz to 1350 MHz
- Ultra low jitter < 0.2 ps-rms (12 kHz to 20 MHz)
< 0.2 ps-rms (50 kHz to 80 MHz)
- Low phase noise, -160 dBc/Hz @ 1 MHz offset (1 GHz)
- Small low profile 9.0 * 14.0 * 4.5 mm SMT package
- 3.3 V, 5.0 V and 12V Supply Options
- LV-PECL, PECL, or Sinewave (0 to +10 dBm into 50 Ω)
- Output disable feature (For LVPECL - PECL option)



Product is free of lead and compliant to EC RoHS Directive

Applications

- Point to Point / Point to Multi Point Radios
- Instrumentation
- PLL Frequency Translation
- Test & Measurement
- Military & Avionics

Description

The VS-502 is a SAW based voltage controlled oscillator that operates at the fundamental frequency of the internal SAW resonator. This direct approach enables this series to achieve low phase noise and jitter performance at high output frequencies and over wide operating temperature range. The oscillator is housed in a hermetically sealed J-lead surface mount package offered on tape and reel. As an option, it has an output disable to facilitate on-board test

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Table 1. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Center Frequency	F_N	300		1350	MHz	1,2
Absolute Pull Range	APR	± 50			ppm	9,2,3
Linearity (+12V Supply)				± 20	%	4,2,9,3
Linearity (+5V Supply)				± 10	%	4,2,9,3
Linearity (+3.3V Supply)				± 10	%	4,2,9,3
Gain Transfer			+ 350		ppm/V	2,8
Temperature Stability (-40°C to +85°C)			± 200		ppm	6,9
Supply						
Voltage (B)	V_{CC}	11.4	12	12.6	V	2,3
Voltage (C)	V_{CC}	4.75	5	5.25	V	2,3
Voltage (D) - PECL Output Only	V_{CC}	3.135	3.3	3.450	V	2,3
Current (No Load)	I_{CC}		55	70	mA	2,3
Output- Sinewave Options						
Sinewave, into 50 Ω (G)	P_O	0			dBm	2,3
Sinewave, into 50 Ω (H)	P_O	+3			dBm	2,3
Sinewave, into 50 Ω (J)	P_O	+7			dBm	2,3
Sinewave, into 50 Ω (K)	P_O	+10			dBm	2,3
Harmonics				-20	dBc	2,3
Jitter @ 622.08 MHz (12 kHz to 20 MHz)			0.10		ps,rms	7,6
Jitter @ 622.08 MHz (50 kHz to 80 MHz)			0.10		ps,rms	7,6
Output- PECL Logic Option (F)						
Output Level Low	V_{OL}			$V_{CC}-1.63$	V	2,3,5
Output Level High	V_{OL}	$V_{CC}-0.98$			V	2,3,5
Rise & Fall Time	t_R, t_F		200	350	ps	2,3,5
Symmetry (Duty Cycle)	SYM	45	49/51	55	%	2,3,5
Control Voltage						
Input Impedance	Z_C	104	110	115	k Ω	6
Modulation BW (Driven from Low Impedance)	BW		100		kHz	6
Operating Temperature						
	T_{OP}	See Ordering Table			$^{\circ}C$	1,3
Package Size						
		9.0 x 14.0 x 4.5			mm	

Table Notes:

1. See Standard Frequencies and Ordering Information
2. Parameters are tested with production test circuit
3. Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
4. Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5. Output levels are standard 100K PECL compatible and measured from 20% to 80% of a full output swing (Fig 1).
6. Not tested in production, guaranteed by design, verified at qualification.
7. Integrated across 12 kHz to 20 MHz, or 50 kHz to 80 MHz per GR-253-CORE Issue3.
8. Tested with $V_c = 0.3V$ to 3V for 3.3V supply, $V_c = 0.5V$ to 4.5 V for 5V supply, $V_c = 0.5V$ to 11.5V for 12V supply
9. Maximum frequency occurs at room temperature

Table 2. Typical Single Side-Band Phase Noise (dBc/Hz) for Sinewave Output

Output Frequency	100 Hz Offset	1 kHz Offset	10 kHz Offset	100 kHz Offset	1 MHz Offset
640 MHz	-75	-110	-135	-150	-160
1000 MHz	-65	-95	-125	-150	-155

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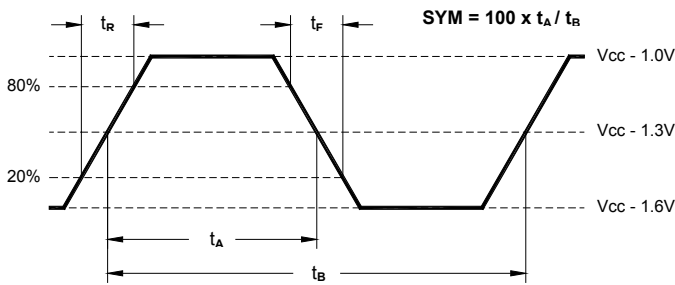
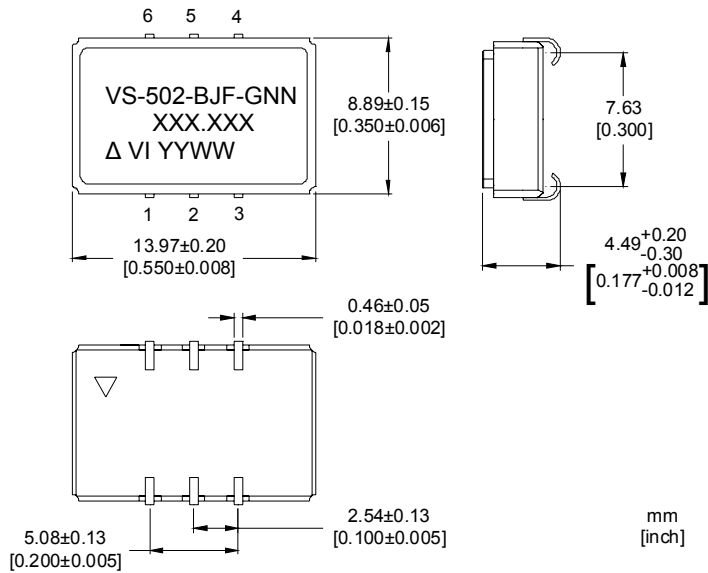


Figure 1. 100K PECL Waveform

Outline Diagram



Pad Layout

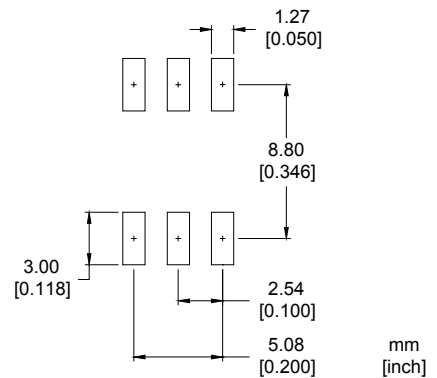


Table 3. Pin Out – PECL Option

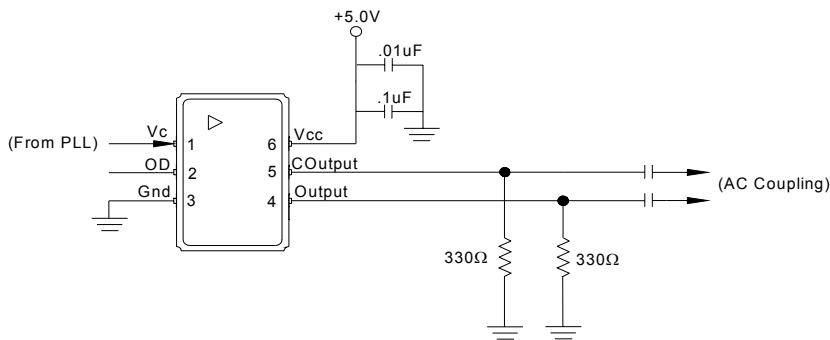
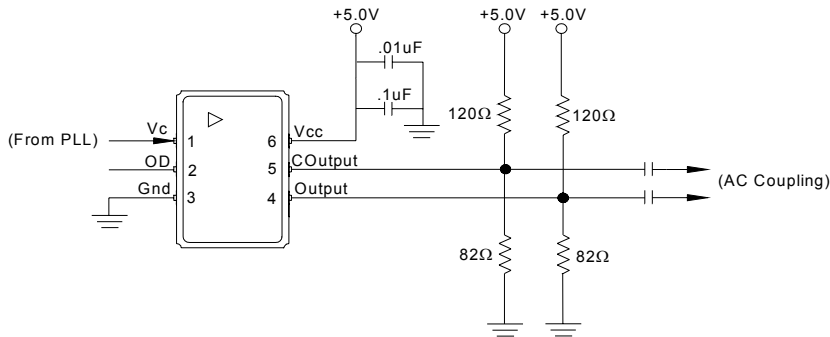
Pin	Symbol	Function
1	V _c	VCSO Control Voltage
2	OD	N/C or Output Disable ¹
3	GND	Case and Electrical Ground
4	Output	VCSO Output
5	COutput	VCSO Complementary Output
6	V _{cc}	Power Supply Voltage

Table Notes:

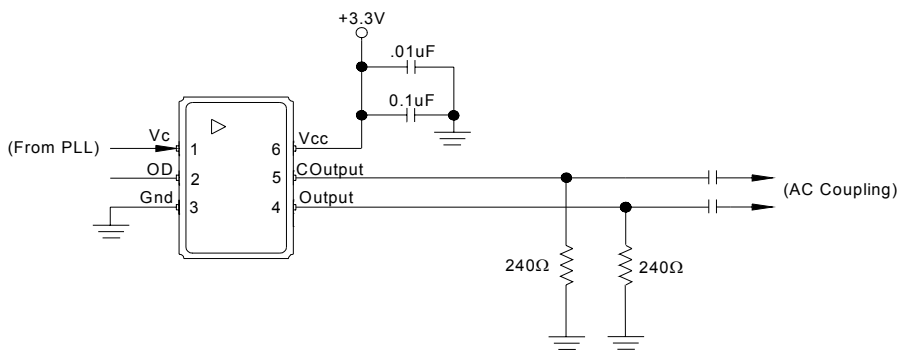
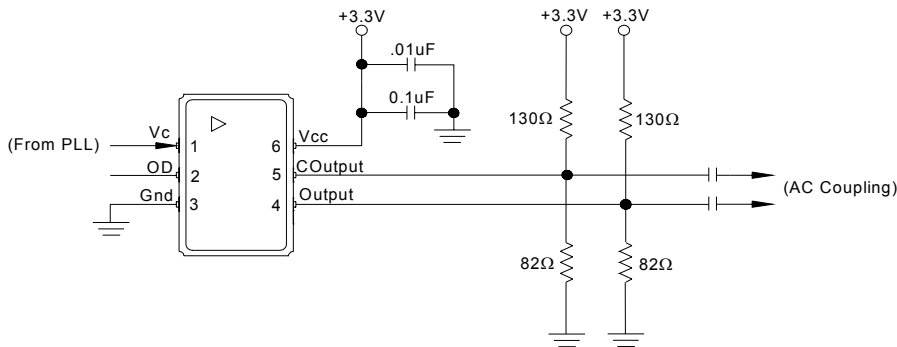
- By setting Output Disable pin high, the RF output is disabled and pin 4 is held high, pin 5 is held low. The threshold for Output Disable is 2.3V above pin 3. Output disable pin can be left floating for normal operation

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Suggested Output Load Configurations – PECL Operation



Suggested Output Load Configurations – LVPECL Operation



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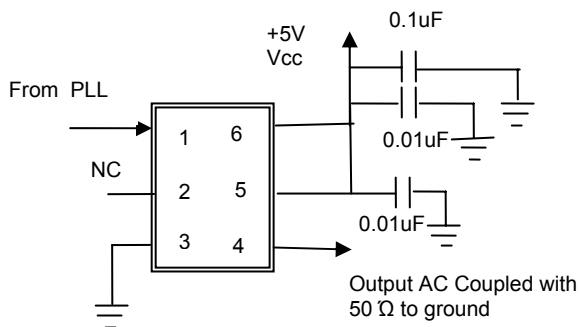
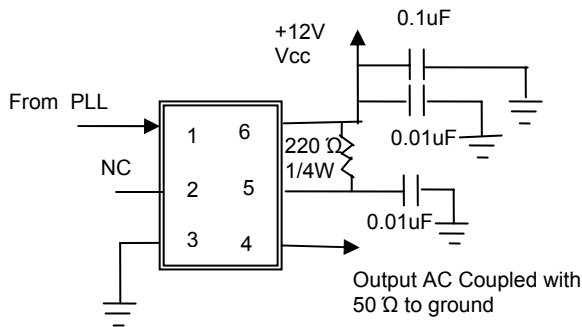
Table 4. Pin Out – Sinewave Option

Pin	Symbol	Function
1	V_c	VCSO Control Voltage
2	-	N/C
3	V_{EE}	Ground
4	Output	VCSO Sinewave Output
5	V_{CC}	V_{CC2}^1
6	V_{CC}	V_{CC1}

Table Notes:

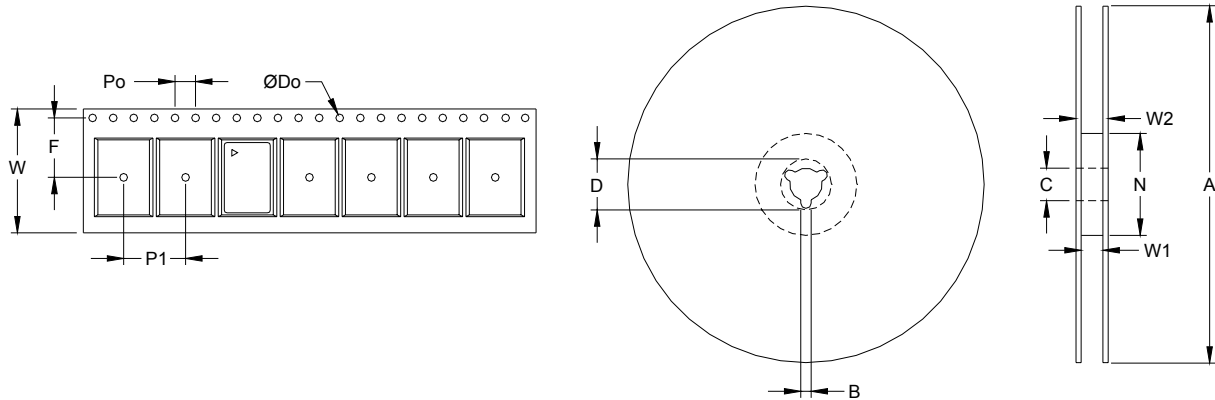
1. If V_{CC1} is +12V and a separate 5V is not applied to pin 5 then pin 5 must be connected through a 220Ω 1/4W external resistor.

Suggested Output Load Configurations – SINEWAVE Operation



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Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm)

Reel Dimensions (mm)

Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VS-502	24	11.5	1.5	4	12	330	1.5	13	20.2	100	24.4	30.4	200

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	$V_{CC} + 1.0V$	V
Voltage Control Range	V_C	-0.5 to $V_{CC} + 0.5V$	V
Storage Temperature	T_S	-55 to $+125$	$^{\circ}C$
Soldering Temp/Time	T_{LS}	$+260/40$	$^{\circ}C/sec$

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Reliability

The VS-502 family is capable of meeting the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

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Handling Precautions

Although ESD protection circuitry has been designed into the VS-502 proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings

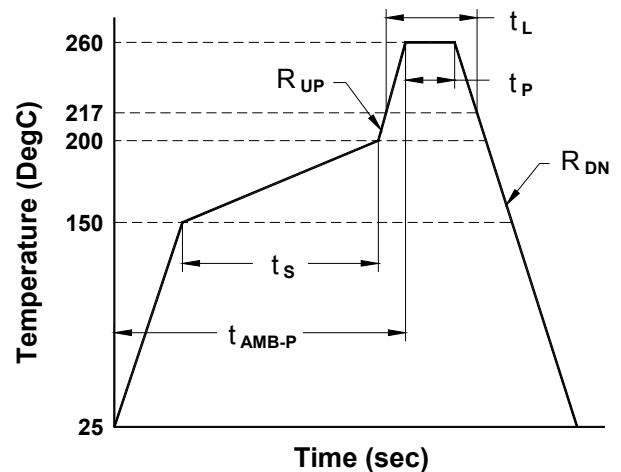
Model	Minimum	Conditions
Human Body Model	1500 V	MIL-STD 883, Method 3015
Charged Device Model	1000 V	JESD 22-C101

Reflow Profile (IPC/JEDEC J-STD-020)

Parameter	Symbol	Value
PreHeat Time	t_s	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device is designed to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VS-502 device is hermetically sealed so an aqueous wash is not an issue.

Termination Plating: Electroless Gold Plate over Nickel Plate



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Available Standard Frequencies (MHz)

480	622.08	640	672.1627	696.4215	938
970	983.04	1000	1090	1200	1330
1344.3256					

Other Frequencies Available Upon Request.

Ordering Information

VS – 502 - B J C - G N N – xxxx.xxxx

Product Family

VS: VCSO

Package

502: 9 x 14 x 4.5 mm

Input

D: 3.3 V

C: 5.0 V

B: 12.0 V

Output

F: PECL

G: Sine \geq 0 dBm

H: Sine \geq 3 dBm

J: Sine \geq 7 dBm

K: Sine \geq 10 dBm

Operating Temperature

C: 0°C to +70 °C

D: -20°C to +70 °C

F: -40°C to +85 °C

Frequency (See Above)

300 – 1350 MHz

Other (Future Use)

N: N/A

Other (Future Use)

N: N/A

Absolute Pull Range

G: \pm 50 ppm

F: \pm 32 ppm

C: \pm 20 ppm

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