NEC Electronics Inc.

CMOS-5 1.2-MICRON CMOS GATE ARRAYS

PRELIMINARY

April 1988

Description

The CMOS-5 gate arrays are low-power, high-speed integrated circuits featuring 1.2-micron silicon-gate CMOS technology. The basic cell on the gate array chip consists of six transistors, three p-channel and three n-channel. See figures 1 and 2.

These application-specific integrated circuits (ASICs) have part numbers in the μPD65000 series. They are available in a variety of sizes (2,000 to 45,000 gates) and packages.

Other NEC publications associated with this data sheet are listed below.

General Design Manual (stock no. 700210)
1.2-Micron CMOS Design Manual (in process)
1.2-Micron CMOS Block Library (in process)
ASIC Package Drawings (stock no. 700348)

Features

- ☐ Technology: 1.2-micron, silicon-gate CMOS; two or three metal layers
- ☐ High speed
  - — Input buffer: 1.2 ns (F/O = 1, L = 0 mm)
  - — Internal gate: 1 ns (F/O = 3, L = 3 mm)
  - — Power gate: 0.7 ns (F/O = 3, L = 3 mm)
  - — Output buffer: 2.5 ns (C_L = 15 pF)
- ☐ Low power
  - — Internal cell: 12 μW/MHz
  - — Output buffer: 1.5 mW/MHz (C_L = 15 pF)
- ☐ Output current: 3, 6, 12 or 17.5 mA
- ☐ Single + 5-volt power supply
  - — CMOS level: 4.5 to 5.5 V
  - — TTL level: 4.75 to 5.25 V
- ☐ Ambient temperature:
  - — CMOS level: −40 to +85°C
  - — TTL level: 0 to +70°C
- ☐ Block library with more than 140 macros
- ☐ Input buffers
  - — CMOS level
  - — TTL level
  - — Schmitt trigger
  - — With pull-up or pull-down resistor
- ☐ Output buffers
  - — Normal
  - — Open-drain
  - — Three-state
  - — Bidirectional
- ☐ I/O interface: CMOS or TTL compatible
- ☐ Packages
  - — Plastic DIP: 24- to 64-pin
  - — Plastic flatpack: 44- to 160-pin
  - — Plastic LCC: 24- to 84-pin
  - — Plastic PGA: 72- to 280-pin
  - — Ceramic PGA: 72- to 280-pin
- ☐ Supported by advanced CAD tools
  - — Schematic capture
  - — Design rule check
  - — Logic and timing simulation before and after placement and routing
  - — Racing check, setup and hold time check, before and after placement and routing
  - — Automatic placement and routing
  - — Test vector generation if NEC scan path design methodology is used
  - — Test program generation
- ☐ Direct access to NEC design centers through communication network or telephone dial-up
- ☐ Quick turnaround time

Figure 1. CMOS Gate Array Chip Layout

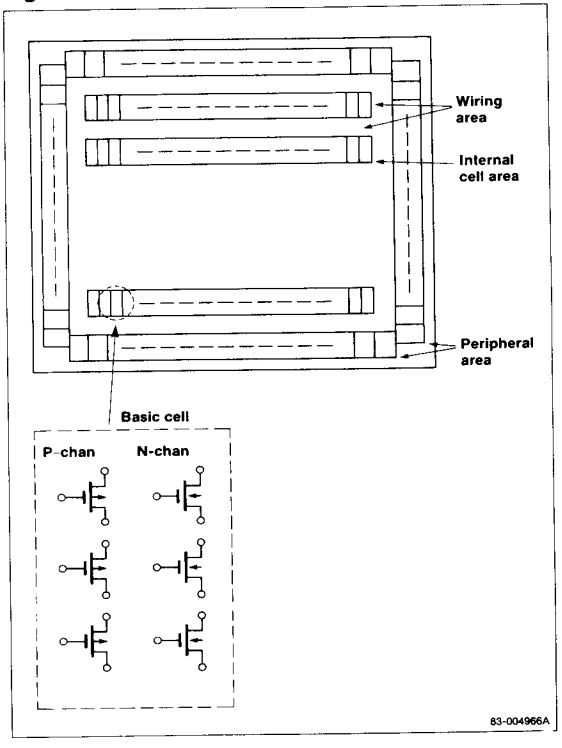
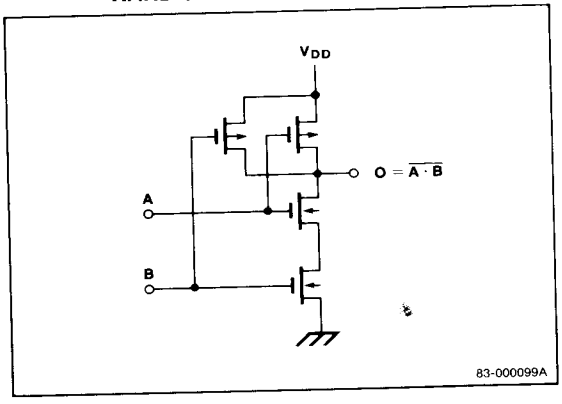


Figure 2. Cell Configured as a Two-Input NAND Gate



Development Procedure

The semicustom approach of gate arrays offers a unique and effective method of manufacturing ICs at reduced cost and development time. NEC makes this possible by stocking wafers that are completely fabricated except for the final step of interconnection. This provides a designer the freedom of interconnecting the uncommitted components to achieve a unique circuit configuration.

Essential Documents

- ☐ Contract and nondisclosure agreement
- ☐ Circuit diagram based on the NEC Block Library
- ☐ Interconnection data file (LOGINC)
- ☐ Test data pattern file (LOGPAT)
- ☐ Pin assignment (if required)
- ☐ Critical path identification (if required)

Absolute Maximum Ratings

$T_A = +25°C$

Power supply voltage, V_{DD}	−0.5 to +6.5 V
Input voltage, V_I	−0.5 V to V_{DD} + 0.5 V
Input current, I_I	40 mA
Output current, I_O	40 mA
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the Recommended Operating Conditions.

Recommended Operating Conditions

		CMOS Level		TTL Level		
Parameter	Symbol	Min	Max	Min	Max	Unit
Power supply voltage	V_{DD}	4.5	5.5	4.75	5.25	V
Ambient temperature	T_A	−40	+85	0	+70	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	0	0.8	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	2.2	V_{DD}	V
Input rise or fall time	t_R, t_F	0	200	0	200	ns
Positive Schmitt trigger voltage (1)	V_P	1.8	4.0	1.2	2.4	V
Negative Schmitt trigger voltage (1)	V_N	0.6	3.1	0.6	1.8	V
Hysteresis voltage (1)	V_H	0.3	1.5	0.3	1.5	V

Notes:

(1) $V_{DD} = 5.0$ V

DC Characteristics

$V_{DD} = 5$ V ±10%; $T_A = -40$ to +85°C

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Quiescent current	I_L		0.1	200	μA	$V_I = V_{DD}$ or GND
Input leakeage current	I_I			10	μA	
Off-state output leakage current	I_{OZ}			10	μA	$V_O = V_{DD}$ or GND
Low-level output current						
Type 1 buffer	I_{OL}	3.0			mA	$V_{OL} = 0.4$ V
Type 2 buffer	I_{OL}	6.0			mA	
Type 3 buffer	I_{OL}	12.0			mA	
Type 4 buffer	I_{OL}	17.5			mA	
High-level output current						
Type 1 buffer	I_{OH}			−1.6	mA	$V_{OH} = V_{DD} - 0.4$ V
Type 2 buffer	I_{OH}			−3.2	mA	
Type 3 buffer	I_{OH}			−6.4	mA	
Type 4 buffer	I_{OH}			−9.4	mA	
Low-level output voltage	V_{OL}			0.1	V	$I_O = 0$ mA
High-level output voltage	V_{OH}	$V_{DD} - 0.1$			V	

AC Characteristics

V_{DD} = 5 V ±10%; T_A = −40 to +85 °C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Toggle frequency	f_{TOG}	100	250		MHz	F/O = 1
Delay time, internal gate						
Single	t_{PD}		0.7		ns	F/O = 2; L = 2 mm
Power	t_{PD}		0.55		ns	
Delay time, buffer						
Input	t_{PD}		1.8		ns	F/O = 2; L = 2 mm
Output	t_{PD}		3.0		ns	C_L = 15 pF
Output rise time	t_R		3.0		ns	C_L = 15 pF
Output fall time	t_F		2.0		ns	C_L = 15 pF

Input/Output Capacitance

Terminal	Symbol	Limits Typ	Max	Unit	Test Conditions
Input	C_{IN}	10	25	pF	$V_{DD} = V_I = 0$ V; f = 1 MHz
Output	C_{OUT}	10	25	pF	
I/O	$C_{I/O}$	10	25	pF	

Gate Array Sizes

μPD	Gates	Cells	Signal Pads
65025	2016	1344	88
65032	3366	2244	106
65044	4440	2960	120
65051	5292	3528	132
65061	6348	4232	144
65071	7500	5000	156
65082	8748	5832	164
65103	10,800	7200	180
65140	14,256	9504	212
65180	18,144	12,096	244
65240	24,000	16,000	284
65300	30,600	20,400	280
65450	45,012	30,008	334

Notes:

(1) Each signal pad can be used as an input, output, bidirectional, or three-state port.

(2) μPD65300 and μPD65450 have three metal layers.

Figure 3. Example of a Circuit Diagram

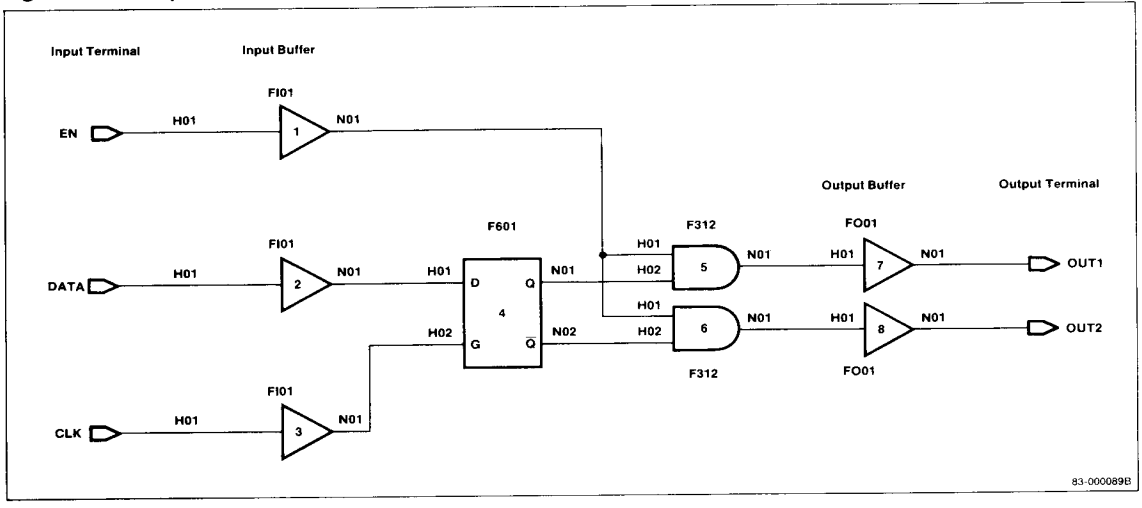
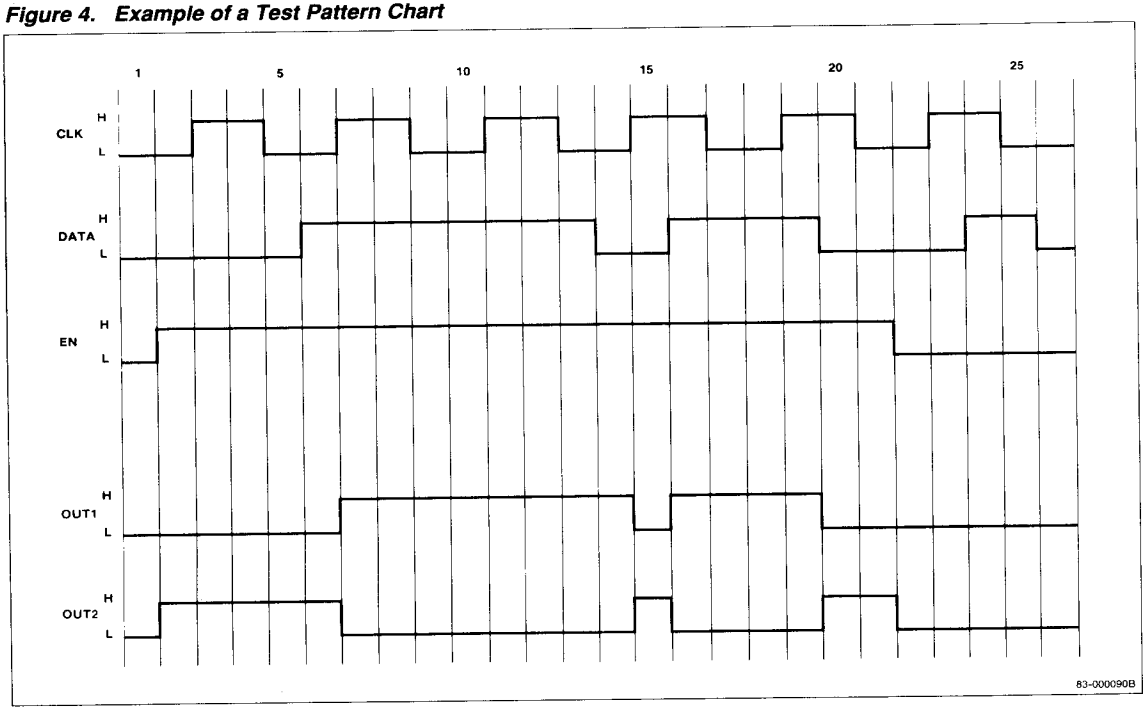
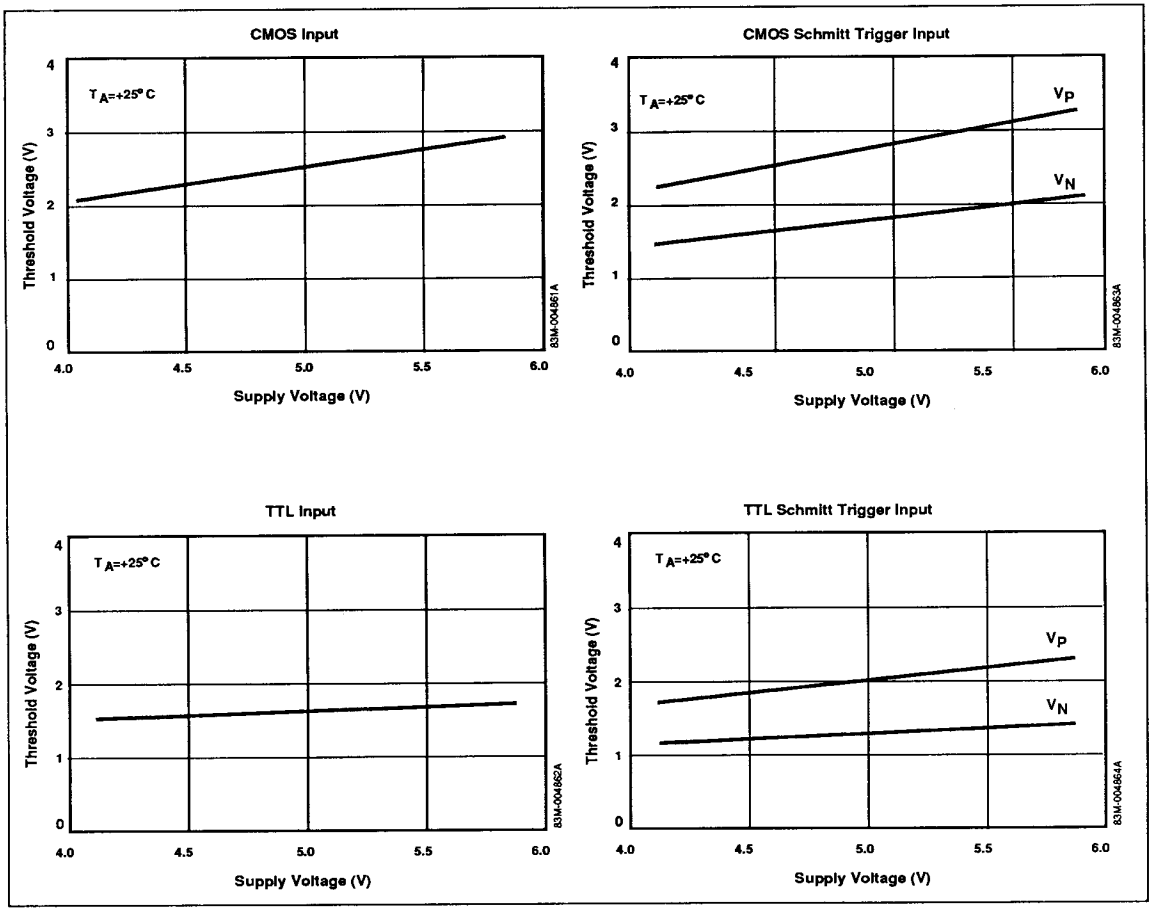


Figure 4. Example of a Test Pattern Chart



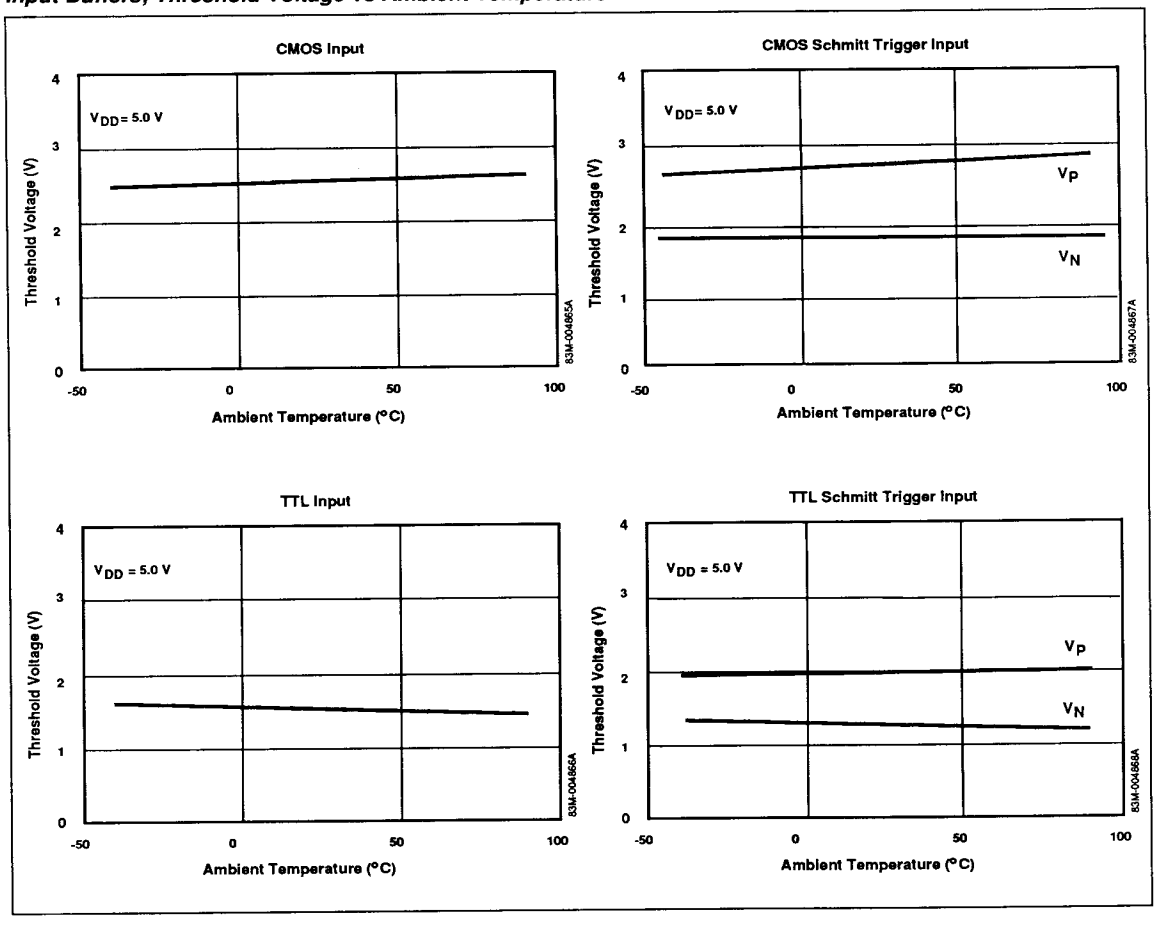
Operating Characteristics

Input Buffers; Threshold Voltage vs Supply Voltage



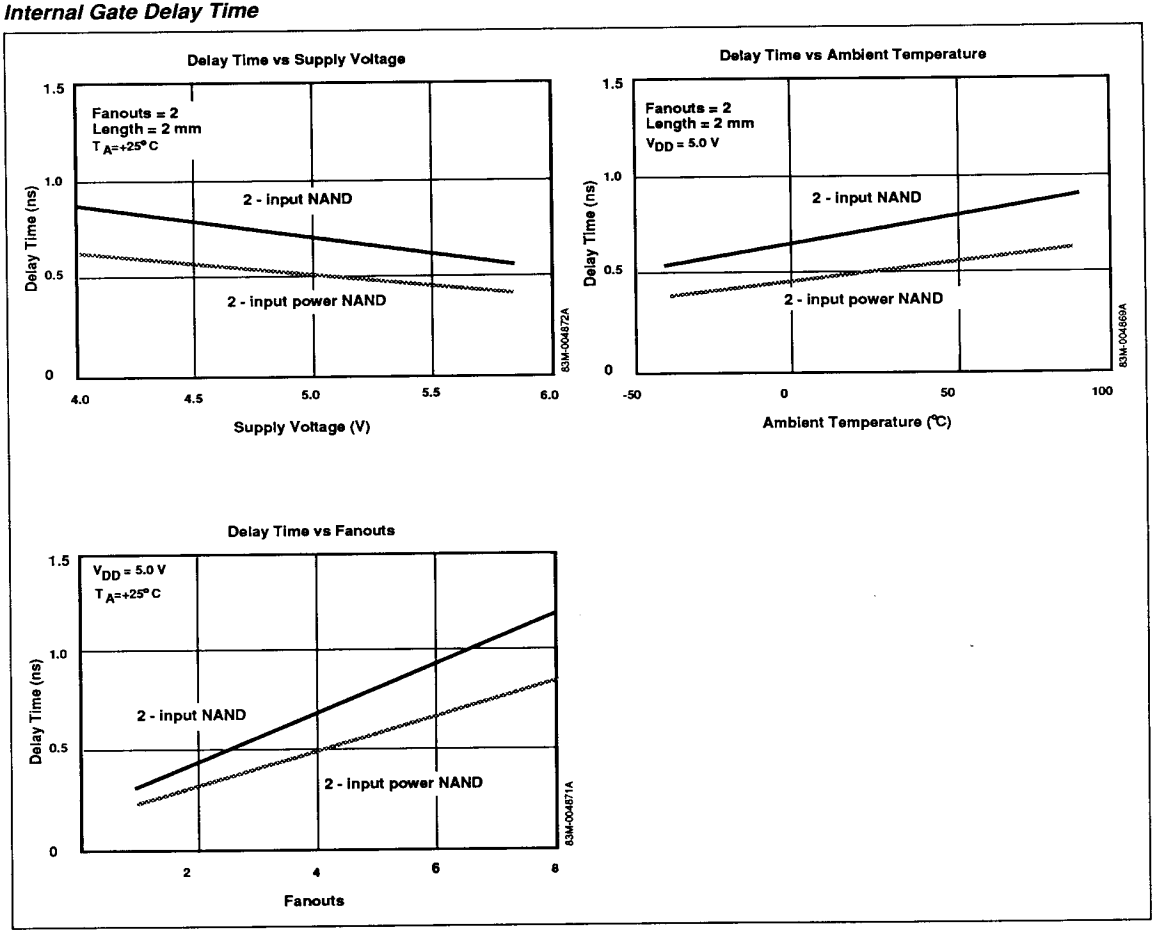
Operating Characteristics (cont)

Input Buffers; Threshold Voltage vs Ambient Temperature



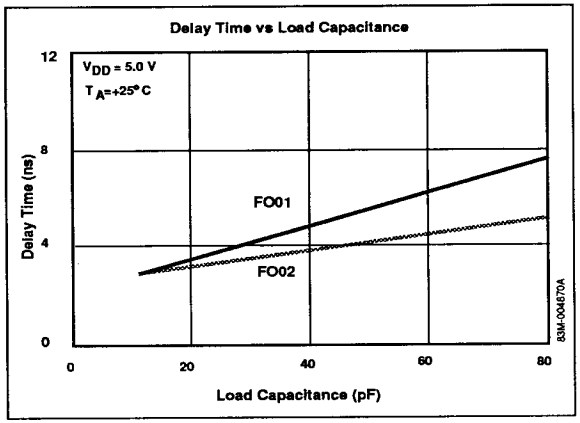
Operating Characteristics (cont)

Internal Gate Delay Time

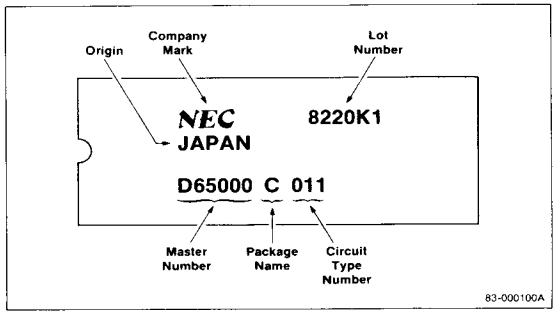


Operating Characteristics (cont)

Output Buffers



Typical Package Marking



Package Availability

	μPD65xxx				μPD65xxx				μPD65xxx				
	025	032	044	051	061	071	082	103	140	180	240	300	450
Plastic DIP													
24-pin (300 mil)	U	U											
28-pin (600 mil)	U	U	U										
40-pin (600 mil)	U	U	U	U	U	U	U						
48-pin (600 mil)	U	U	U	U	U	U	U						
Plastic Shrink DIP													
64-pin (750 mil)	A	A	A	U	U	U	U	U					
Plastic Flatpack													
44-pin	U	U	U										
52-pin	U	U	U										
64-pin	U	U	U	U	U	U	U						
80-pin		U	U	U	U	U	U						
100-pin			U	U	U	U	U						
120-pin							U	U	U	U	U	U	
136-pin								U	U	U	U	U	
160-pin										U	U	U	
Plastic Leaded Chip Carrier (PLCC)													
28-pin	U	U	U										
44-pin	U	U	U										
52-pin	U	U	U										
68-pin			U	U	U	U	U	U					
84-pin			U	U	U	U	U	U					
Ceramic Pin Grid Array (PGA)													
72-pin	U	U	U	U	U	U	U	U	U				
132-pin		U	U	U	U	U	U	U	U	A	A	U	
176-pin								U	U	A	U	U	U
208-pin									U	A	U	U	U
280-pin											U	U	U
Plastic Pin Grid Array (PPGA)													
72-pin	U	U	U	U	U	U	U		U				
120-pin		U	U	U	U	U	U		U	U	U	U	
132-pin				U	U	U	U		U	U	U	U	
144-pin									U	U	U	U	
176-pin									U	U	U	U	U
208-pin										U	U	U	U

U = under development; please consult your nearest NEC ASIC design center for scheduled availability.

A = available

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