



# Half-Bridge N-Channel Programmable 1-A MOSFET Driver for DC/DC Conversion with Adjustable High Side Propagation Delay

## FEATURES

- 8-V or 12-V Low-Side Gate Drive
- Undervoltage Lockout
- Internal Bootstrap Diode
- Adaptive Shoot-Through Protection
- Synchronous MOSFET Disable
- Shutdown Control
- Adjustable High-Side Propagation Delay
- Switching Frequency Up to 1 MHz
- Drive MOSFETs In 5- to 48-V Systems



## APPLICATIONS

- Multi-Phase DC/DC Conversion
- High Current Synchronous Buck Converters
- High Frequency Synchronous Buck Converters
- Asynchronous-to-Synchronous Adaptations
- Mobile Computer DC/DC Converters
- Desktop Computer DC/DC Converters

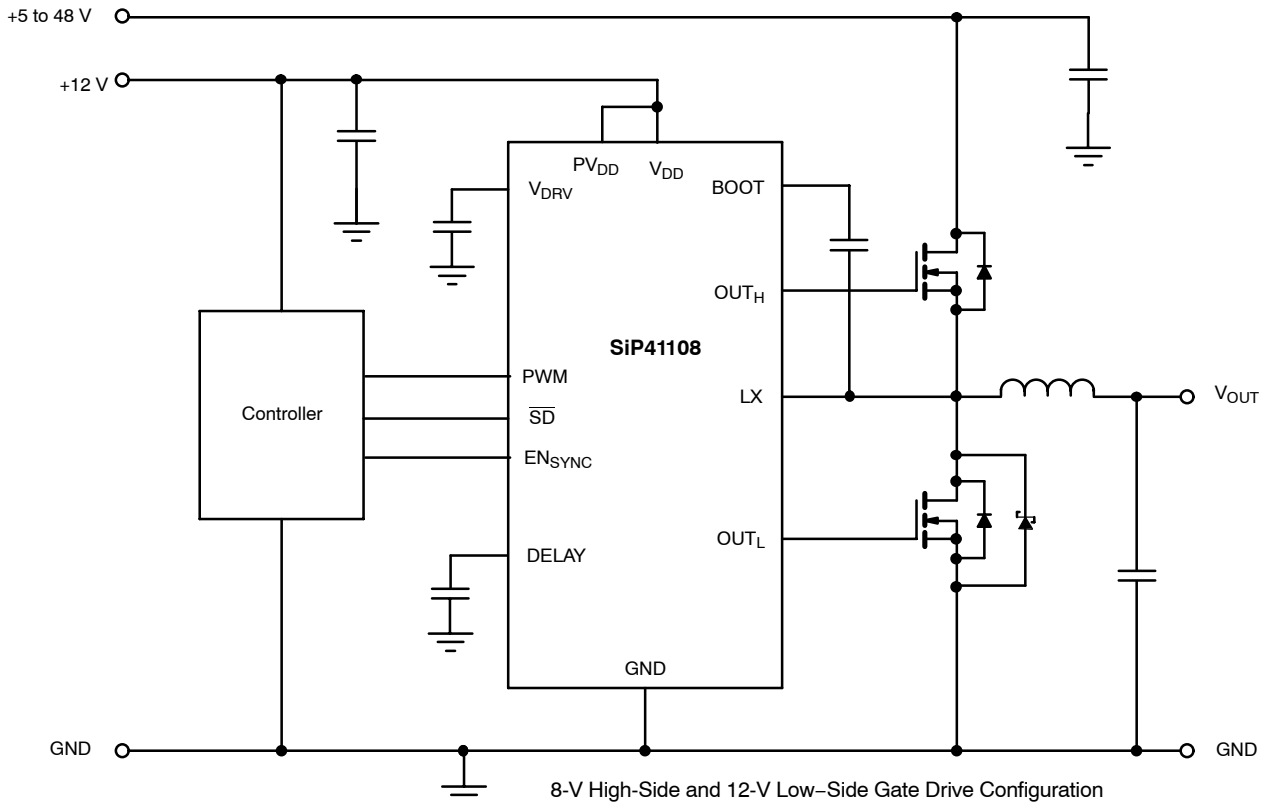
## DESCRIPTION

SiP41108 is a high-speed half-bridge MOSFET driver with adaptive shoot-through protection for use in high frequency, high current, multiphase dc-to-dc synchronous rectifier buck power supplies. It is designed to operate at switching frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving n-channel MOSFETs. SiP41108 comes with adaptive shoot-through protection to prevent simultaneous conduction of the external MOSFETs.

The high-side turn on delay is programmable via an external capacitor. The 8-V regulator sets the high-side gate drive. The low-side driver supply,  $PV_{DD}$ , must be externally connected to either  $V_{DRV}$  or  $V_{DD}$  for 8-V or 12-V gate drive respectively.

The SiP41108 is assembled in a lead (Pb)-free PowerPAK® TSSOP-16 package and is specified to operate over the industrial operating range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

## FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)**

$V_{DD}$ , PWM, EN <sub>SYNC</sub> , DELAY	-0.3 to 15 V	Power Dissipation <sup>a,b</sup>	
LX, BOOT	-0.3 to 55 V	TSSOP-16 PowerPAK	2.6 W
BOOT to LX	-0.3 to 15 V	Thermal Impedance ( $\theta_{JA}$ ) <sup>a,b</sup>	
Storage Temperature	-40 to 150°C	TSSOP-16 PowerPAK	38°C/W
Operating Junction Temperature	125°C	Notes	
		a. Device mounted with all leads soldered or welded to PC board.	
		b. Derate 26.3 mW/°C	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)**

$V_{DD}$	10.8 V to 13.2 V	$V_{BOOT-LX}$	8 V
$V_{LX}$	48 V	Operating Temperature Range	-40 to 85°C
$C_{BOOT}$	100 nF to 1 $\mu$ F		

SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 12\text{ V}$ , $V_{BOOT} - V_{LX} = 8\text{ V}$ , $T_A = -40\text{ to }85^\circ\text{C}$		Limits			Unit
				Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>Power Supplies</b>							
Supply Voltage	$V_{DD}$			10.8		13.2	V
Quiescent Current	$I_{DDQ}$	PWM Non-Switching			5.0	8.5	mA
Supply Current	$I_{DD}$	$f_{PWM} = 100\text{ kHz}$ , $C_{LOAD} = 3\text{ nF}$	$PV_{DD} = V_{DD}$		11.5		
			$PV_{DD} = V_{DRV}$		10.0		
Shutdown Current	$I_{SD}$	$\overline{SD} = 0\text{ V}$ , $T_A = 25^\circ\text{C}$			0.1	1	$\mu$ A
		$\overline{SD} = 0\text{ V}$			0.8	5	
<b>Reference Voltage</b>							
Break-Before-Make	$V_{BBM}$				2.5		V
<b>PWM Input</b>							
Input High	$V_{IH}$			4.0		$V_{DD}$	V
Input Low	$V_{IL}$					1.0	
Bias Current	$I_B$				$\pm 0.3$	$\pm 1$	$\mu$ A
<b>EN<sub>SYNC</sub>, <math>\overline{SD}</math> Inputs</b>							
Input High	$V_{IH}$			4.0		$V_{DD}$	V
Input Low	$V_{IL}$					1.0	
Bias Current (EN <sub>SYNC</sub> )	$I_B$					$\pm 1$	$\mu$ A
Bias Current ( $\overline{SD}$ )	$I_B$	$\overline{SD} = V_{DD}$				15	
<b>Bootstrap Diode</b>							
Forward Voltage	$V_F$	$I_F = 40\text{ mA}$ , $T_A = 25^\circ\text{C}$		0.7	0.85	1.0	V
<b>MOSFET Drivers</b>							
High-Side Drive Current	$I_{PKH}(\text{source})$	$V_{BOOT} - V_{LX} = 8\text{ V}$			0.8		A
	$I_{PKH}(\text{sink})$				1.0		
Low-Side Drive Current	$I_{PKL}(\text{source})$	$V_{DRV} = 8\text{ V}$	$PV_{DD} = V_{DRV}$		0.9		
	$I_{PKL}(\text{sink})$				1.2		
	$I_{PKL}(\text{source})$	$V_{DRV} = 12\text{ V}$	$PV_{DD} = V_{DD}$		1.4		
	$I_{PKL}(\text{sink})$				1.8		

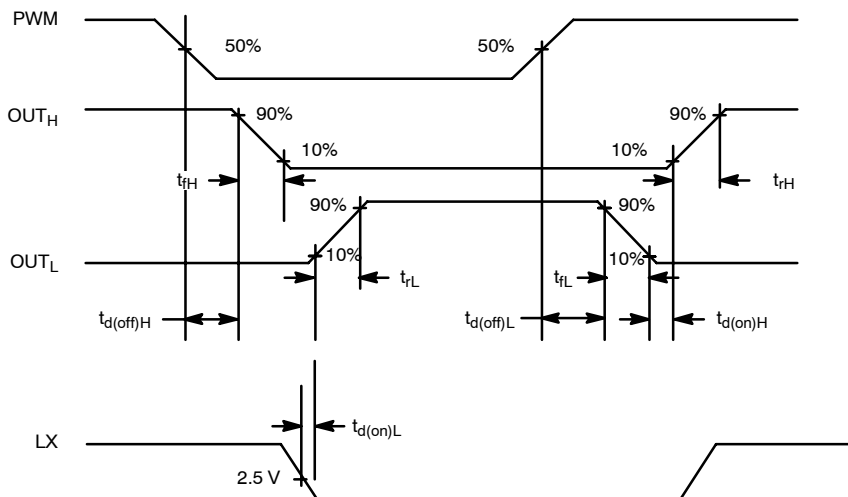


SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 12\text{ V}, V_{BOOT} - V_{LX} = 8\text{ V}, T_A = -40\text{ to }85^\circ\text{C}$		Limits			Unit
				Min <sup>a</sup>	Typ <sup>b</sup>	Max <sup>a</sup>	
<b>MOSFET Drivers</b>							
High-Side Driver Impedance	$R_{DH(source)}$	$V_{BOOT} - V_{LX} = 8\text{ V}, LX = GND$			2.3	4.2	$\Omega$
	$R_{DH(sink)}$				1.9	3.5	
Low-Side Driver Impedance	$R_{DL(source)}$	$V_{DRV} = 8\text{ V}$	$P_{VDD} = V_{DRV}$		2.9	5.2	
	$R_{DL(sink)}$				1.3	2.4	
	$R_{DL(source)}$	$V_{DRV} = 12\text{ V}$	$P_{VDD} = V_{DD}$		2.4	4.3	
	$R_{DL(sink)}$				1.2	2.2	
High-Side Rise Time	$t_{rH}$	10% - 90%, $V_{BOOT} - V_{LX} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$			45		
High-Side Fall Time	$t_{fH}$				35		
High-Side Rise Time Bypass		10% - 90%, $V_{BOOT} - V_{LX} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$			45		
High-Side Fall Time Bypass					35		
High-Side Propagation Delay	$t_{d(off)H}$	See Timing Waveforms			20		
	$t_{d(on)H}$				30		
Low-Side Rise Time	$t_{rL}$	10% - 90%, $V_{BOOT} - V_{LX} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$	$P_{VDD} = V_{DRV}$		65		
		10% - 90%, $V_{BOOT} - V_{LX} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$	$P_{VDD} = V_{DD}$		65		
Low-Side Fall Time	$t_{fL}$	10% - 90%, $V_{BOOT} - V_{LX} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$	$P_{VDD} = V_{DRV}$		30		
		10% - 90%, $V_{BOOT} - V_{LX} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$	$P_{VDD} = V_{DD}$		30		
Low-Side Propagation Delay	$t_{d(off)L}$	See Timing Waveforms			15		
	$t_{d(on)L}$				20		
<b>LX Timer</b>							
PHASE Falling Time-out	$t_{LX}$				380		ns
<b>V<sub>DRV</sub> Regulator</b>							
Output Voltage	$V_{DRV}$			7.6	8	8.4	V
Output Current	$I_{DRV}$				80	100	mA
Current Limit	$I_{LIM}$	$V_{DRV} = 0\text{ V}$		120	200	280	
Line Regulation	LNR	$V_{CC} = 10.8\text{ V to }13.2\text{ V}$			0.05	0.5	%/V
Load Regulation	LDR	5 mA to 80 mA			0.1	1.0	%
<b>V<sub>DRV</sub> Regulator UVLO</b>							
V <sub>DRV</sub> Rising	$V_{UVLO2}$	$V_{DRV} = V_{DD}$			6.7	7.2	V
V <sub>DRV</sub> Falling		$V_{DRV} = V_{DD}$			6.4	6.9	
Hysteresis	Hyst			100	300	500	mV
<b>High-Side Undervoltage Lockout</b>							
Threshold	$V_{UVHS}$	LX Falling		2.5	3.35	4.0	V
<b>V<sub>DD</sub> Undervoltage Lockout</b>							
Threshold	$V_{UVLO1}$			5.0	5.3	5.6	V
Power on Reset Time	POR				2.5		ms
<b>Thermal Shutdown</b>							
Temperature	$T_{SD}$	Temperature Rising			165		°C
Hysteresis	$T_H$	Temperature Falling			25		

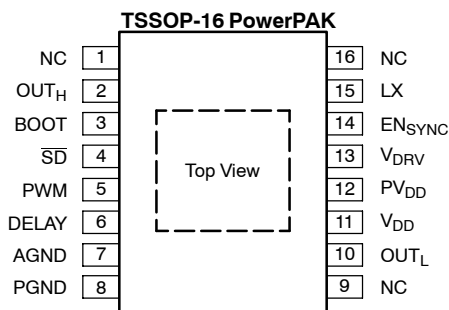
Notes

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (-40° to 85°C).
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at  $V_{DD} = 12\text{ V}$  unless otherwise noted.

**TIMING WAVEFORMS**



**PIN CONFIGURATION AND TRUTH TABLE**



TRUTH TABLE				
PWM	SD	EN <sub>SYNC</sub>	OUT <sub>H</sub>	OUT <sub>L</sub>
L	H	L	L	L
H	H	L	H	L
L	H	H	L	H
H	H	H	H	L
X	L	X	L	L

**ORDERING INFORMATION**

Part Number	Temperature Range	Marking
SiP41108DQP-T1-E3	-40 to 85°C	41108

**Eval Kit      Temperature Range**

SiP41108DB	-40 to 85°C
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**PIN DESCRIPTION**

Pin Number	Name	Function
1, 9, 16	NC	No Connection
2	OUT <sub>H</sub>	8-V High-side MOSFET gate drive
3	BOOT	Bootstrap supply for high-side driver. A capacitor connects between BOOT and LX.
4	$\overline{SD}$	Shuts down the driver IC
5	PWM	Input signal for the MOSFET drivers
6	DELAY	Connection for the highside delay adjustment capacitor.
7	AGND	Analog ground. Exposed pad is connected to AGND.
8	PGND	Power ground
10	OUT <sub>L</sub>	Synchronous or low-side MOSFET gate drive
11	V <sub>DD</sub>	12-V supply. Connect a bypass capacitor $\geq 1 \mu F$ from here to ground.
12	PV <sub>DD</sub>	Low side driver supply. Connect to V <sub>DRV</sub> for 8-V Gate Drive or to V <sub>DD</sub> for 12-V drive.
13	V <sub>DRV</sub>	8-V Voltage Regulator Output. Connect a bypass capacitor $\geq 1 \mu F$ from here to ground
14	EN <sub>SYNC</sub>	Enables OUT <sub>L</sub> , the driver for the synchronous MOSFET
15	LX	Connection to source of high-side MOSFET, drain of the low-side MOSFET, and the inductor

**FUNCTIONAL BLOCK DIAGRAM**

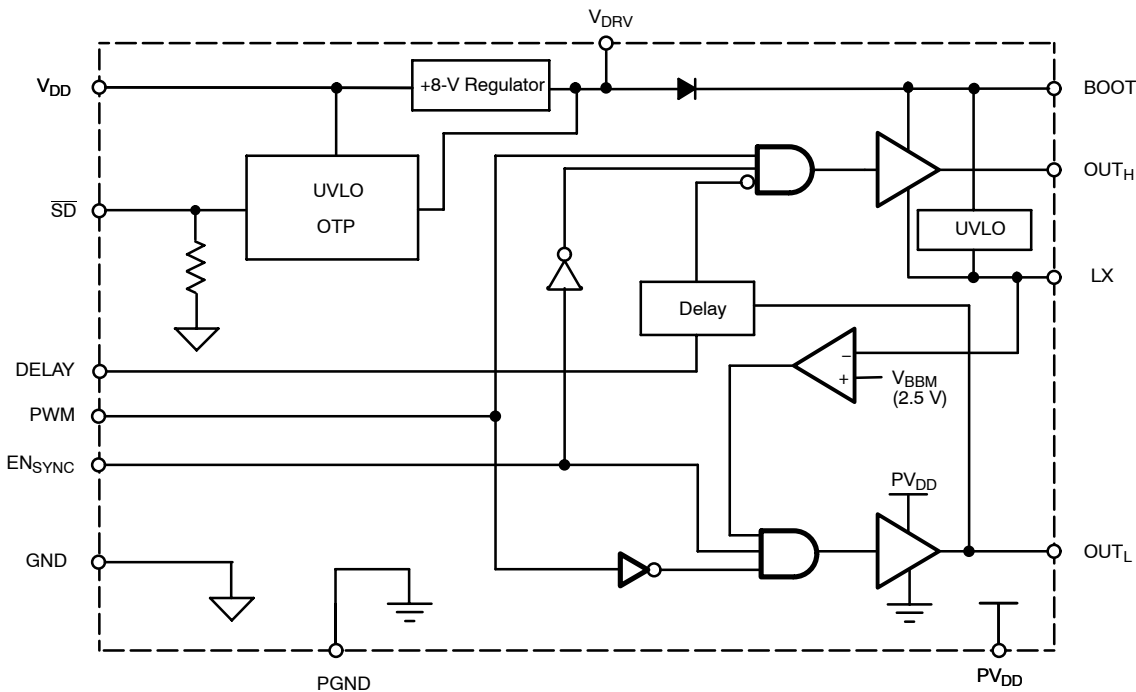


Figure 1.

**DETAILED OPERATION**

**PWM**

The PWM pin controls the switching of the external MOSFETs. The driver logic operates in a noninverting configuration. The PWM input stage should be driven by a signal with fast transition times, like those provided by a PWM controller or logic gate, (<200 ns). The PWM input functions as a logic input and is not intended for applications where a slow changing input voltage is used to generate a switching output when the input switching threshold voltage is reached. The PWM amplitude is 5 V but can go up to  $V_{DD}$ .

**Low-Side Driver**

The supplies for the low-side driver are  $V_{DD}$  and GND. During shutdown,  $OUT_L$  is held low.

**High-Side Driver**

The high-side driver is isolated from the substrate to create a floating high-side driver so that an n-channel MOSFET can be

used for the high-side switch. The supplies for the high-side driver are  $BOOT$  and  $LX$ . The voltage is supplied by a floating bootstrap capacitor, which is continually recharged by the switching action of the output. During shutdown  $OUT_H$  is held low.

**Gate Drive Voltage ( $V_{DRV}$ ) Regulator**

An integrated 80-mA, 8-V regulator supplies voltage to the  $V_{DRV}$  pin and it current limits at 200-mA typical when the output of the regulator is shorted to ground. A capacitor (1  $\mu$ F minimum) must be connected to the  $V_{DRV}$  pin to stabilize the regulator output, and the voltage on  $V_{DRV}$  is supplied to the integrated bootstrap diode.  $V_{DRV}$  is used to recharge the bootstrap capacitor and can be used to power the low-side driver. The  $V_{DRV}$  can be externally connected to  $V_{DD}$  to bypass the 8-V regulator and allow 12-V high-side gate drive. If  $V_{DRV}$  is connected to  $V_{DD}$  the system voltage should not exceed 43 V.

### Bootstrap Circuit

The internal bootstrap diode and a bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode replaces the external Schottky diode needed for the bootstrap circuit; only a capacitor is necessary to complete the bootstrap circuit. The bootstrap capacitor is sized according to,

$$C_{BOOT} = (Q_{GATE}/\Delta V_{BOOT-LX}) \times 10$$

where  $Q_{GATE}$  is the gate charge needed to turn on the high-side MOSFET and  $\Delta V_{BOOT-LX}$  is the amount of droop allowed in the bootstrapped supply voltage when the high-side MOSFET is driven high. The bootstrap capacitor value is typically 0.1  $\mu$ F to 1  $\mu$ F. The bootstrap capacitor voltage rating must be greater than  $V_{DD} + 12$  V to withstand transient spikes and ringing.

### Shoot-Through Protection

The external MOSFETs are prevented from conducting at the same time during transitions. Break-before-make circuits monitor the voltages on the LX pin and the  $OUT_L$  pin and control the switching as follows: When the signal on PWM goes low,  $OUT_H$  will go low after an internal propagation delay. After the voltage on LX falls below 2.5 V by the inductor action, the low-side driver is enabled and  $OUT_L$  goes high after some delay. When the signal on PWM goes high,  $OUT_L$  will go low after an internal propagation delay. After the voltage on  $OUT_L$  drops below 2.5 V, the high-side driver is enabled and  $OUT_H$  will go high after an internal propagation delay. If LX does not drop below 2.5 V within 380 ns after  $OUT_H$  goes low,  $OUT_L$  is forced high until the next PWM transition.

### Delay

The addition of a capacitor between DELAY and GND will increase the propagation delay time for  $OUT_H$  going high. Delay capacitance may be added to prevent shoot through current in the low-side MOSFET due to the finite time between  $OUT_L$  going low and the continuing conduction of the low-side

MOSFET. Choose a MOSFET with lower gate resistance to reduce this effect. If necessary, choose a capacitor value that prevents MOSFET conduction under worst-case temperature and manufacturing conditions. Propagation delay is increased according to the ratio of 1 ns/pF.

### Synchronous MOSFET Enable

Under light load conditions, efficiency can be increased by disabling the synchronous MOSFET, thus avoiding the gate charge losses of the synchronous MOSFET. When  $EN_{SYNC}$  is low,  $OUT_L$  is forced low. When high, the low-side driver operates normally.  $EN_{SYNC}$  should be driven by a 5-V signal but can go up to  $V_{DD}$ .

### Shutdown

The driver enters shutdown mode when  $\overline{SD}$  goes low. Both  $OUT_L$  and  $OUT_H$  go low during shutdown. Shutdown current is less than 1  $\mu$ A.

### $V_{DD}$ Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1- $\mu$ F ceramic capacitor as close as practical between the  $V_{DD}$  and GND pins.

### Undervoltage Lockout

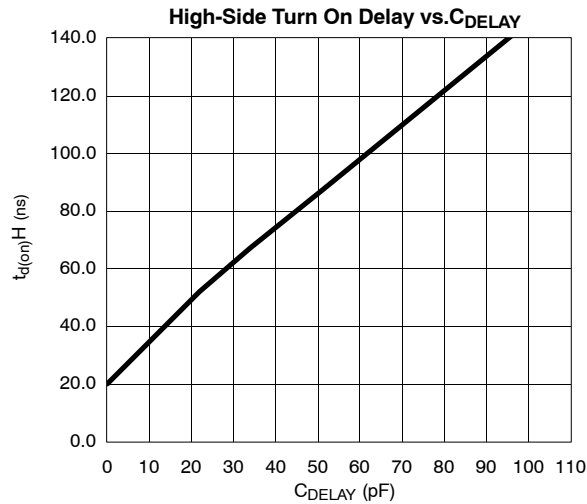
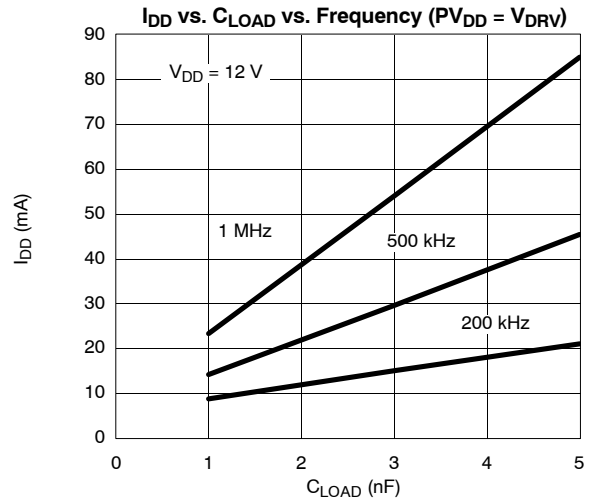
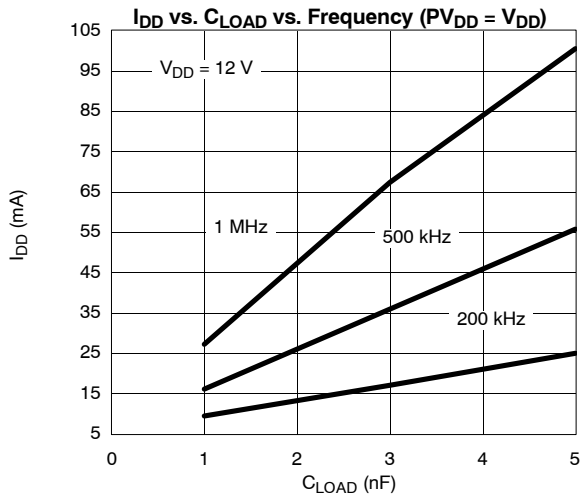
Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces  $OUT_L$  and  $OUT_H$  to low when  $V_{DD}$  is below its specified voltage. A separate UVLO forces  $OUT_H$  low when the voltage between BOOT and LX is below the specified voltage.

### Thermal Protection

If the die temperature rises above 165°C, the thermal protection disables the drivers. The drivers are re-enabled after the die temperature has decreased below 140°C.



**TYPICAL CHARACTERISTICS**



**TYPICAL WAVEFORMS**

Figure 2. PWM Signal vs. HS Gate, LS Gate and LX (Rising)

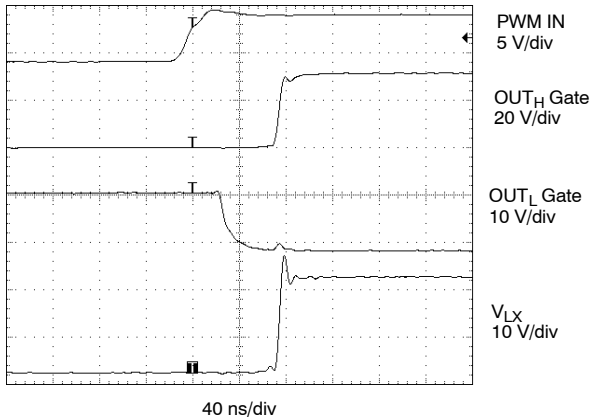
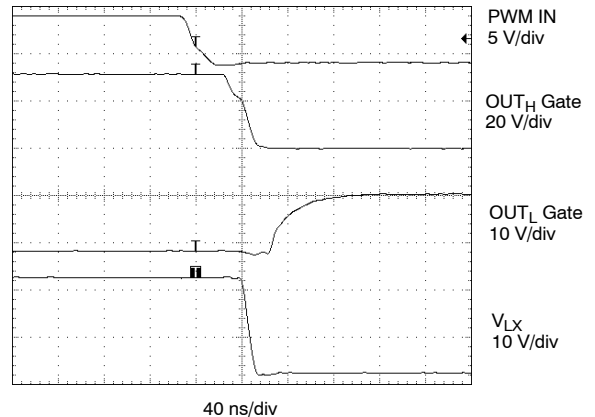


Figure 3. PWM Signal vs. HS Gate, LS Gate and LX (Falling)



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