LTM9011-14/ LTM9010-14/LTM9009-14

14-Bit, 125Msps/105Msps/ 80Msps Low Power Octal ADCs

FEATURES

- **8-Channel Simultaneous Sampling ADC**
- **73.1dB SNR**
- **88dB SFDR**
- Low Power: 140mW/113mW/94mW per Channel
- Single 1.8V Supply
- Serial LVDS Outputs: 1 or 2 Bits per Channel
- Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$
- 800MHz Full Power Bandwidth S/H
- Shutdown and Nap Modes
- Serial SPI Port for Configuration
- Internal Bypass Capacitance, No External Components
- 140-Pin (9mm × 11.25mm) BGA Package

APPLICATIONS

- Communications
- Cellular Base Stations
- Software Defined Radios
- Portable Medical Imaging
- Multichannel Data Acquisition
- Nondestructive Testing

DESCRIPTION

The LTM®9011-14/LTM9010-14/LTM9009-14 are 8-channel, simultaneous sampling 14-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. AC performance includes 73.1dB SNR and 88dB spurious free dynamic range (SFDR). Low power consumption per channel reduces heat in high channel count applications. Integrated bypass capacitance and flow-through pinout reduces overall board space requirements.

DC specs include ±1LSB INL (typ), ±0.3LSB DNL (typ) and no missing codes over temperature. The transition noise is a low $1.2LSB_{RMS}$.

The digital outputs are serial LVDS to minimize the number of data lines. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode).

The ENC+ and ENC− inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL, or CMOS inputs. An internal clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

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TYPICAL APPLICATION

9009101114 TA01
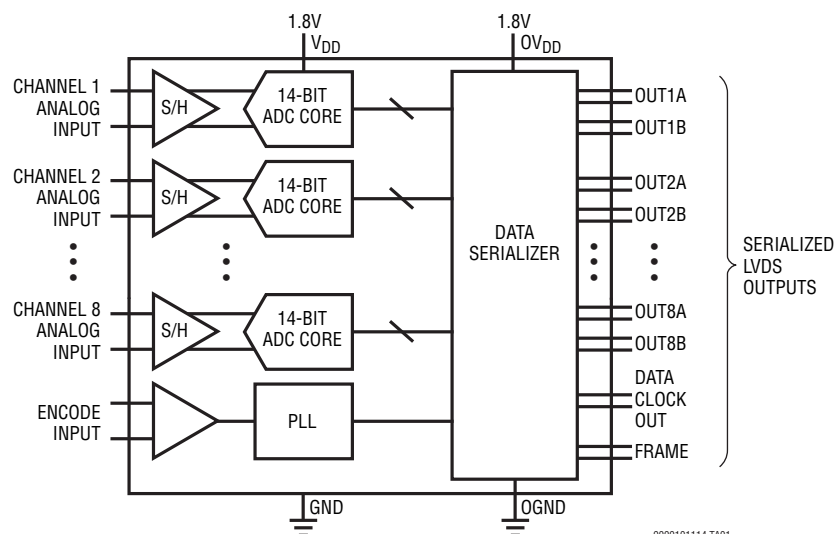
LTM9011-14, 125Msps, 2-Tone FFT, f_{IN} = 70MHz and 75MHz

9009101114 TA01b

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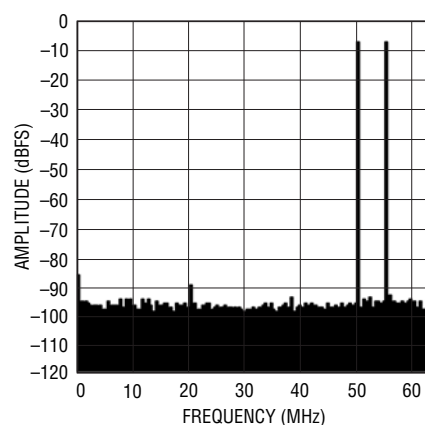
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages

V_{DD}, OV_{DD}.. –0.3V to 2V

Analog Input Voltage (A_{IN}^+, A_{IN}^-,

PAR/$\overline{SER}$, SENSE) (Note 3)...........–0.3V to (V_{DD} + 0.2V)

Digital Input Voltage (ENC$^+$, ENC$^-$, $\overline{CS}$,

SDI, SCK) (Note 4).................................... –0.3V to 3.9V

SDO (Note 4) .... –0.3V to 3.9V

Digital Output Voltage .... –0.3V to (OV_{DD} + 0.3V)

Operating Temperature Range

LTM9011C, 9010C, 9009C .... 0°C to 70°C

LTM9011I, 9010I, 9009I .... –40°C to 85°C

Storage Temperature Range.................... –65°C to 150°C

PIN CONFIGURATION

TOP VIEW

BGA PACKAGE
140-LEAD (11.25mm × 9.00mm × 2.72mm)

T_{JMAX} = 150°C, θ_{JA} = 28°C/W
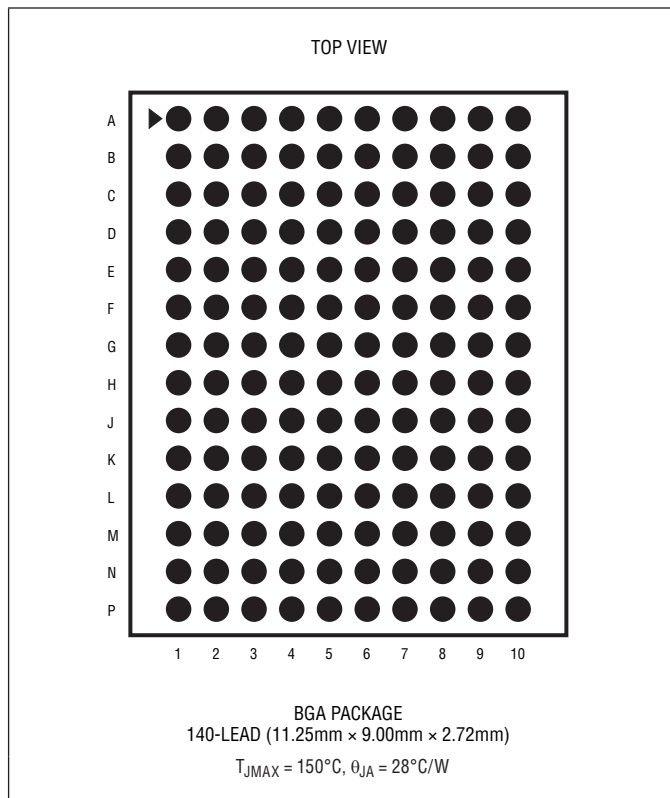
ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM9011CY-14#PBF	LTM9011CY-14#PBF	LTM9011Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	0°C to 70°C
LTM9011IY-14#PBF	LTM9011IY-14#PBF	LTM9011Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	–40°C to 85°C
LTM9010CY-14#PBF	LTM9010CY-14#PBF	LTM9010Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	0°C to 70°C
LTM9010IY-14#PBF	LTM9010IY-14#PBF	LTM9010Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	–40°C to 85°C
LTM9009CY-14#PBF	LTM9009CY-14#PBF	LTM9009Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	0°C to 70°C
LTM9009IY-14#PBF	LTM9009IY-14#PBF	LTM9009Y14	140-Lead (11.25mm × 9mm × 2.72mm) BGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

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CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		LTM9011-14 MIN	TYP	MAX	LTM9010-14 MIN	TYP	MAX	LTM9009-14 MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			14			14			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	−4.1	±1.2	4.1	−3.25	±1	3.25	−2.75	±1	2.75	LSB
Differential Linearity Error	Differential Analog Input	●	−0.9	±0.3	0.9	−0.8	±0.3	0.8	−0.8	±0.3	0.8	LSB
Offset Error	(Note 7)	●	−12	±3	12	−12	±3	12	−12	±3	12	mV
Gain Error	Internal Reference External Reference	●	−2.6	−1.3 −1.3	0	−2.6	−1.3 −1.3	0	−2.6	−1.3 −1.3	0	%FS %FS
Offset Drift				±20			±20			±20		µV/°C
Full-Scale Drift	Internal Reference External Reference			±35 ±25			±35 ±25			±35 ±25		ppm/°C ppm/°C
Gain Matching	External Reference			±0.2			±0.2			±0.2		%FS
Offset Matching				±3			±3			±3		mV
Transition Noise	External Reference			1.2			1.2			1.2		LSB$_{RMS}$

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ − A_{IN}^-$)	1.7V < V_{DD} < 1.9V	●		1 to 2		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Analog Input (Note 8)	●	V_{CM} − 100mV	V_{CM}	V_{CM} + 100mV	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
I_{INCM}	Analog Input Common Mode Current	Per Pin, 125Msps Per Pin, 105Msps Per Pin, 80Msps			155 130 100		µA µA µA
I_{IN1}	Analog Input Leakage Current No Encode	0 < A_{IN}^+, A_{IN}^- < V_{DD},	●	−1		1	µA
I_{IN2}	PAR/$\overline{SER}$ Input Leakage Current	0 < PAR/$\overline{SER}$ < V_{DD}	●	−3		3	µA
I_{IN3}	SENSE Input Leakage Current	0.625 < SENSE < 1.3V	●	−6		6	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter				0.15		ps$_{RMS}$
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
BW-3B	Full-Power Bandwidth	Figure 6 Test Circuit			800		MHz

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DYNAMIC ACCURACY
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = −1dBFS. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTM9011-14 MIN	TYP	MAX	LTM9010-14 MIN	TYP	MAX	LTM9009-14 MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input 70MHz Input 140MHz Input	●	71.1	73.1 73 72.6		70.7	73 72.9 72.6		70.9	73 72.9 72.5		dBFS dBFS dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input 70MHz Input 140MHz Input	●	75	88 85 82		75	88 85 82		77	88 85 82		dBFS dBFS dBFS
	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input 70MHz Input 140MHz Input	●	84	90 90 90		84	90 90 90		85	90 90 90		dBFS dBFS dBFS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input 70MHz Input 140MHz Input	●	69.6	73 72.6 72		70.2	73 72.6 72		70.4	72.9 72.6 72		dBFS dBFS dBFS
	Crosstalk, Near Channel	10MHz Input (Note 12)			−90			−90			−90		dBc
	Crosstalk, Far Channel	10MHz Input (Note 12)			−105			−105			−105		dBc

INTERNAL REFERENCE CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = −1dBFS. (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	$0.5 \cdot V_{DD} - 25mV$	$0.5 \cdot V_{DD}$	$0.5 \cdot V_{DD} + 25mV$	V
V_{CM} Output Temperature Drift			±25		ppm/°C
V_{CM} Output Resistance	−600µA < I_{OUT} < 1mA		4		Ω
V_{REF} Output Voltage	I_{OUT} = 0	1.225	1.250	1.275	V
V_{REF} Output Temperature Drift			±25		ppm/°C
V_{REF} Output Resistance	−400µA < I_{OUT} < 1mA		7		Ω
V_{REF} Line Regulation	1.7V < V_{DD} < 1.9V		0.6		mV/V

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC⁺, ENC⁻)							
Differential Encode Mode (ENC⁻ Not Tied to GND)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set			1.2		V
		Externally Set (Note 8)	●	1.1		1.6	V
V_{IN}	Input Voltage Range	ENC⁺, ENC⁻ to GND	●	0.2		3.6	V
R_{IN}	Input Resistance	(See Figure 10)			10		kΩ
C_{IN}	Input Capacitance				3.5		pF
Single-Ended Encode Mode (ENC⁻ Tied to GND)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
V_{IN}	Input Voltage Range	ENC⁺ to GND	●	0		3.6	V
R_{IN}	Input Resistance	(See Figure 11)			30		kΩ
C_{IN}	Input Capacitance				3.5		pF
DIGITAL INPUTS ($\overline{CS}$, SDI, SCK in Serial or Parallel Programming Mode. SDO in Parallel Programming Mode)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	−10		10	µA
C_{IN}	Input Capacitance				3		pF
SDO OUTPUT (Serial Programming Mode. Open-Drain Output. Requires 2kΩ Pull-Up Resistor if SDO Is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	−10		10	µA
C_{OUT}	Output Capacitance				3		pF
DIGITAL DATA OUTPUTS							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode	●	247	350	454	mV
		100Ω Differential Load, 1.75mA Mode	●	125	175	250	mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode	●	1.125	1.250	1.375	V
		100Ω Differential Load, 1.75mA Mode	●	1.125	1.250	1.375	V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

POWER REQUIREMENTS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		LTM9011-14 MIN	TYP	MAX	LTM9010-14 MIN	TYP	MAX	LTM9009-14 MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
I_{VDD}	Analog Supply Current	Sine Wave Input	●		566	610		448	486		368	400	mA
I_{OVDD}	Digital Supply Current	2-Lane Mode, 1.75mA Mode 2-Lane Mode, 3.5mA Mode	● ●		54 98	62 108		52 96	62 106		50 94	58 104	mA mA
P_{DISS}	Power Dissipation	2-Lane Mode, 1.75mA Mode 2-Lane Mode, 3.5mA Mode	● ●		1116 1196	1210 1292		900 980	986 1066		752 832	824 908	mW mW
P_{SLEEP}	Sleep Mode Power				2			2			2		mW
P_{NAP}	Nap Mode Power				170			170			170		mW
$P_{DIFFCLK}$	Power Increase With Differential Encode Mode Enabled (No Increase for Sleep Mode)				40			40			40		mW

TIMING CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTM9011-14 MIN	TYP	MAX	LTM9010-14 MIN	TYP	MAX	LTM9009-14 MIN	TYP	MAX	UNITS
f_S	Sampling Frequency	(Notes 10,11)	●	5		125	5		105	5		80	MHz
t_{ENCL}	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	100 100	4.52 2	4.76 4.76	100 100	5.93 2	6.25 6.25	100 100	ns ns
t_{ENCH}	ENC High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2	4 4	100 100	4.52 2	4.76 4.76	100 100	5.93 2	6.25 6.25	100 100	ns ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				0			0			0		ns

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Data Outputs (R_{TERM} = 100Ω Differential, C_L = 2pF to GND on Each Output)							
t_{SER}	Serial Data Bit Period	2-Lanes, 16-Bit Serialization 2-Lanes, 14-Bit Serialization 2-Lanes, 12-Bit Serialization 1-Lane, 16-Bit Serialization 1-Lane, 14-Bit Serialization 1-Lane, 12-Bit Serialization			$1/(8 \cdot f_S)$ $1/(7 \cdot f_S)$ $1/(6 \cdot f_S)$ $1/(16 \cdot f_S)$ $1/(14 \cdot f_S)$ $1/(12 \cdot f_S)$		s s s s s s
t_{FRAME}	FR to DCO Delay	(Note 8)	●	$0.35 \cdot t_{SER}$	$0.5 \cdot t_{SER}$	$0.65 \cdot t_{SER}$	s
t_{DATA}	DATA to DCO Delay	(Note 8)	●	$0.35 \cdot t_{SER}$	$0.5 \cdot t_{SER}$	$0.65 \cdot t_{SER}$	s
t_{PD}	Propagation Delay	(Note 8)	●	$0.7n + 2 \cdot t_{SER}$	$1.1n + 2 \cdot t_{SER}$	$1.5n + 2 \cdot t_{SER}$	s
t_R	Output Rise Time	Data, DCO, FR, 20% to 80%			0.17		ns
t_F	Output Fall Time	Data, DCO, FR, 20% to 80%			0.17		ns
	DCO Cycle-Cycle Jitter	t_{SER} = 1ns			60		ps_{P-P}
	Pipeline Latency				6		Cycles

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TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Port Timing (Note 8)							
t_{SCK}	SCK Period	Write Mode Read Back Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Setup Time		●	5			ns
t_H	SCK to $\overline{CS}$ Setup Time		●	5			ns
t_{DS}	SDI Setup Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Read Back Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●			125	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 125MHz (LTM9011), 105MHz (LTM9010), or 80MHz (LTM9009), 2-lane output mode, differential ENC+/ENC− = 2V_{P-P} sine wave, input range = 2V_{P-P} with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Offset error is the offset voltage measured from −0.5 LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111 in 2's complement output mode.

Note 8: Guaranteed by design, not subject to test.

Note 9: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 125MHz (LTM9011), 105MHz (LTM9010), or 80MHz (LTM9009), 2-lane output mode, ENC+ = single-ended 1.8V square wave, ENC− = 0V, input range = 2V_{P-P} with differential drive, unless otherwise noted. The supply current and power dissipation specifications are totals for the entire chip, not per channel.

Note 10: Recommended operating conditions.

Note 11: The maximum sampling frequency depends on the speed grade of the part and also which serialization mode is used. The maximum serial data rate is 1000Mbps so t_{SER} must be greater than or equal to 1ns.

Note 12: Near-channel crosstalk refers to Ch. 1 to Ch.2, and Ch.7 to Ch.8. Far-channel crosstalk refers to Ch.1 to Ch.7, Ch.1 to Ch.8, Ch.2 to Ch.7, and Ch.2 to Ch.8.

TIMING DIAGRAMS

2-Lane Output Mode, 16-Bit Serialization*

SAMPLE N-6   SAMPLE N-5   SAMPLE N-4

*SEE THE DIGITAL OUTPUTS SECTION

9009101114 TD01

2-Lane Output Mode, 14-Bit Serialization

SAMPLE N-6   SAMPLE N-5   SAMPLE N-4   SAMPLE N-3

9009101114 TD02
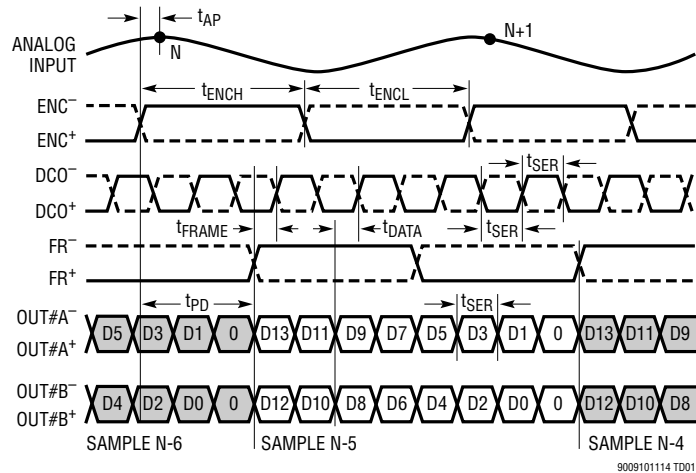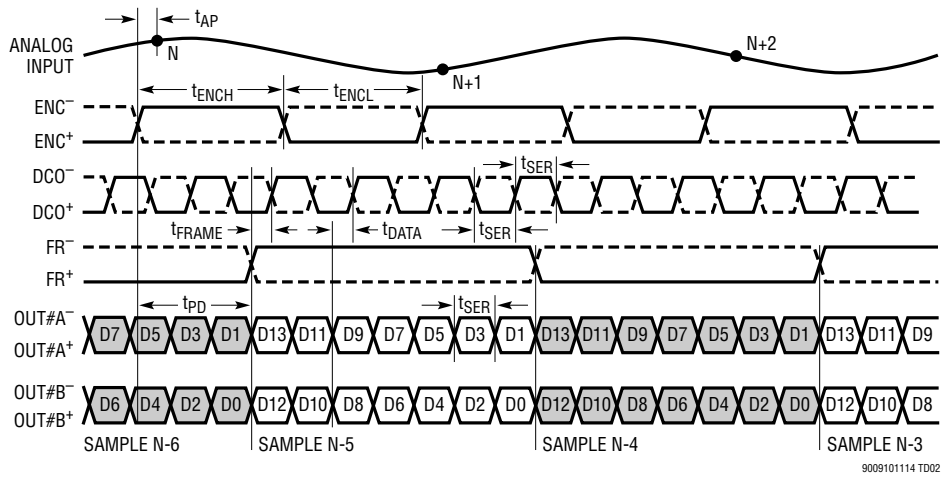
NOTE THAT IN THIS MODE FR⁺/FR⁻ HAS TWO TIMES THE PERIOD OF ENC⁺/ENC⁻

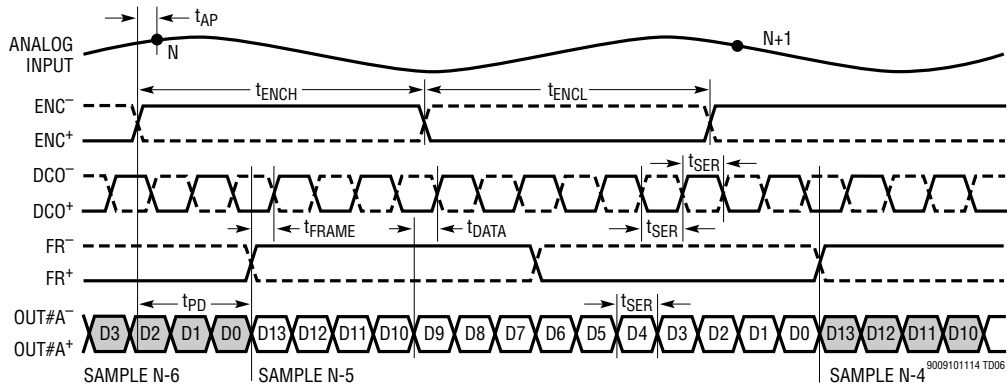# TIMING DIAGRAMS

2-Lane Output Mode, 12-Bit Serialization

9009101114 TD03
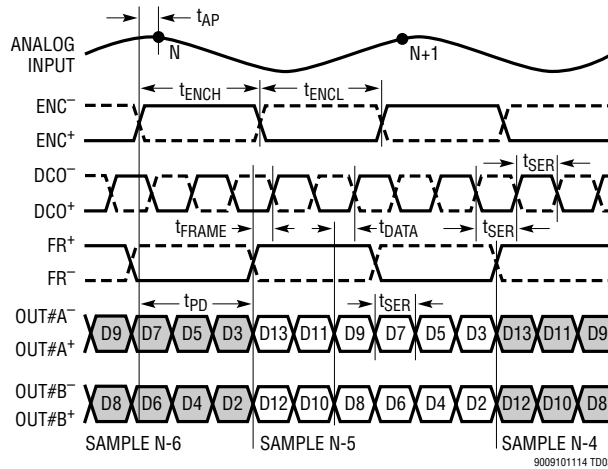
1-Lane Output Mode, 16-Bit Serialization

9009101114 TD(
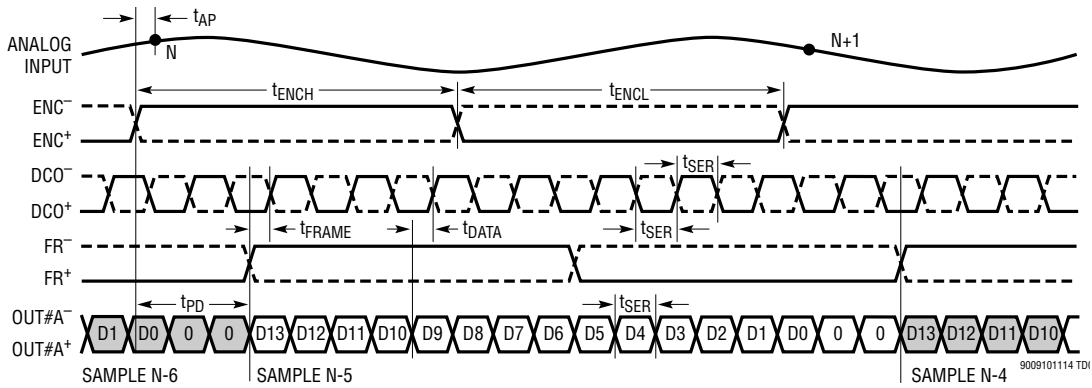
OUT#B⁺, OUT#B⁻ ARE DISABLED

TIMING DIAGRAMS

One-Lane Output Mode, 14-Bit Serialization

OUT#B$^+$, OUT#B$^-$ ARE DISABLED

One-Lane Output Mode, 12-Bit Serialization

OUT#B$^+$, OUT#B$^-$ ARE DISABLED

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TIMING DIAGRAMS

SPI Port Timing (Readback Mode)
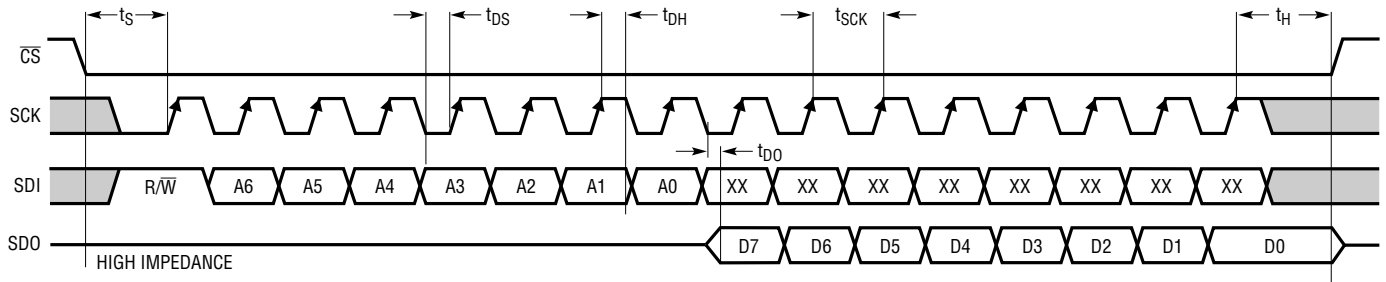
SPI Port Timing (Write Mode)
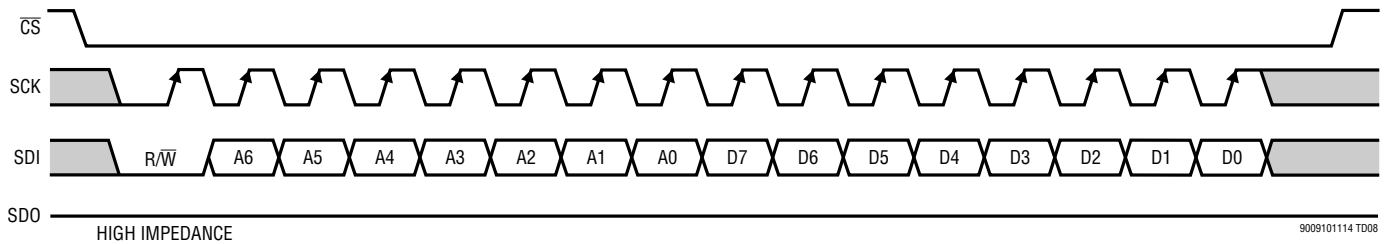
9009101114 TD08

TYPICAL PERFORMANCE CHARACTERISTICS

LTM9011-14: Integral Nonlinearity (INL)

PLACEHOLDER
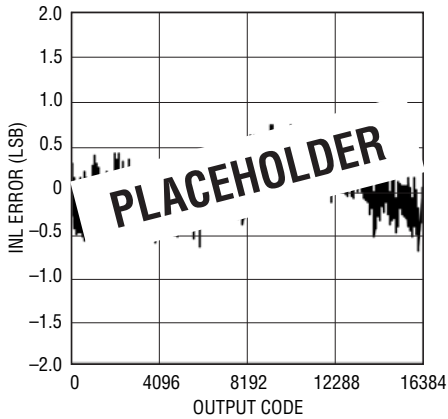
217514 G01

LTM9011-14: Differential Nonlinearity (DNL)

PLACEHOLDER
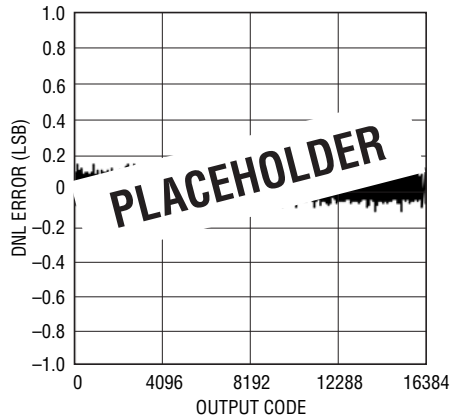
217514 G02

LTM9011-14: 8k Point FFT, f_{IN} = 5MHz −1dBFS, 125Msps

PLACEHOLDER
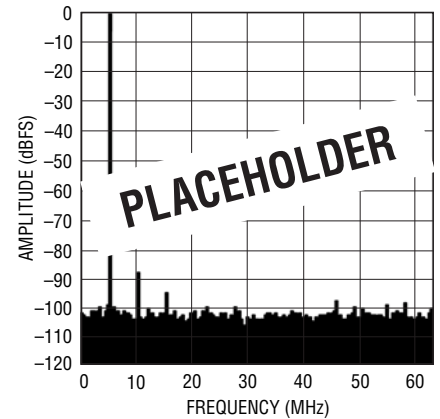
217514 G03

LTM9011-14: 8k Point FFT, f_{IN} = 30MHz −1dBFS, 125Msps

PLACEHOLDER
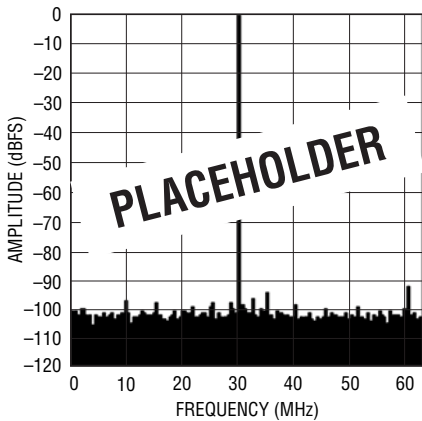
217514 G04

LTM9011-14: 8k Point FFT, f_{IN} = 70MHz −1dBFS, 125Msps

PLACEHOLDER
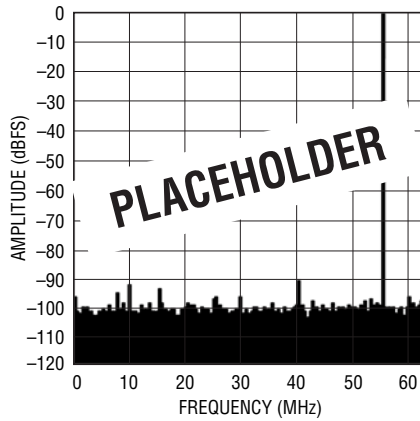
217514 G05

LTM9011-14: 8k Point FFT, f_{IN} = 140MHz −1dBFS, 125Msps

PLACEHOLDER
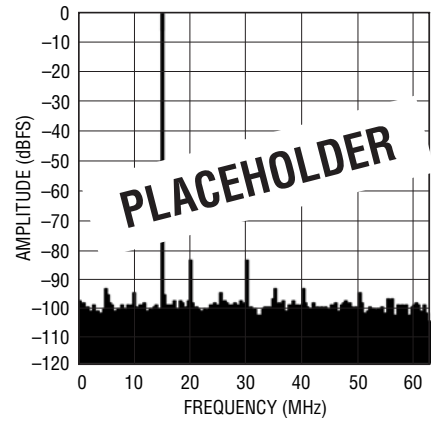
217514 G06

LTM9011-14: 8k Point 2-Tone FFT, f_{IN} = 70MHz, 75MHz, −1dBFS, 125Msps

PLACEHOLDER
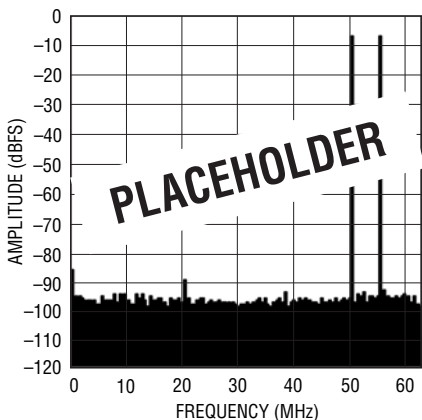
217514 G07

LTM9011-14: Shorted Input Histogram

PLACEHOLDER
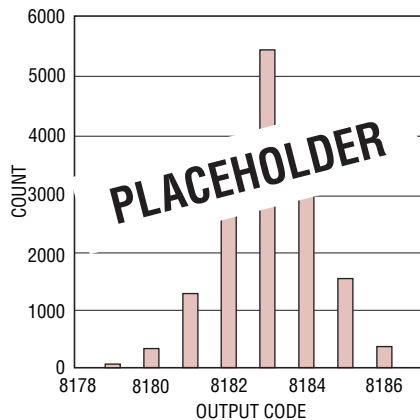
217514 G08

LTM9011-14: SNR vs Input Frequency, −1dB, 2V Range, 125Msps

PLACEHOLDER

217514 G09

9009101114p
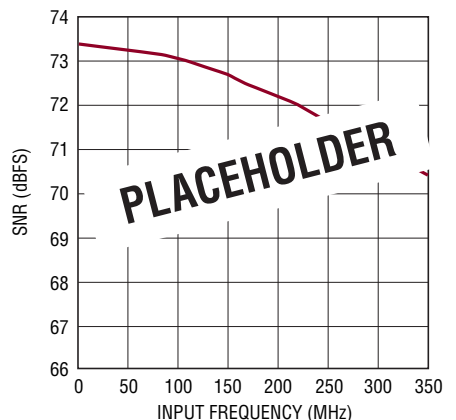
TYPICAL PERFORMANCE CHARACTERISTICS

LTM9011-14: SFDR vs Input Frequency, –1dB, 2V Range, 125Msps
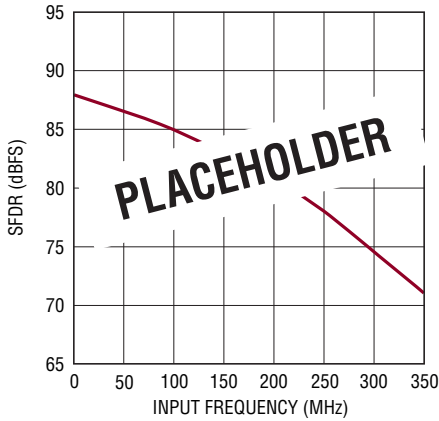
LTM9011-14: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 125Msps
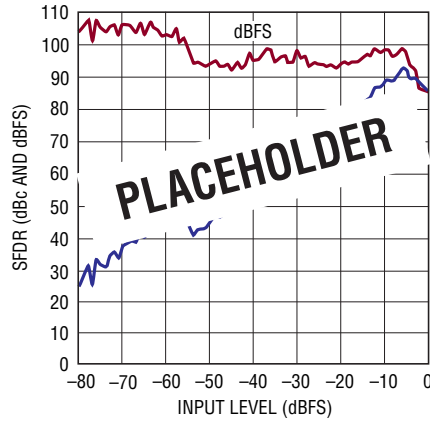
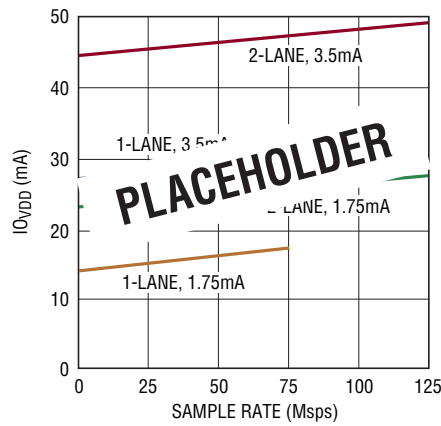**LTM9011-14: SNR vs Input Level, f_{IN} = 70MHz, 2V Range, 125Msps**
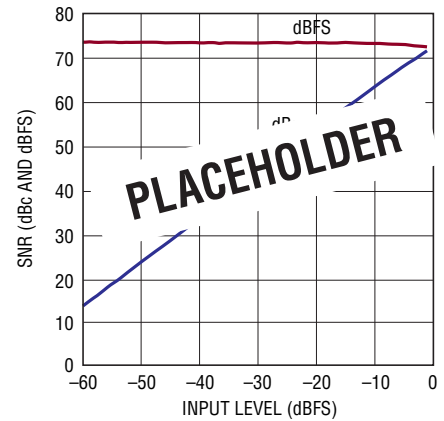
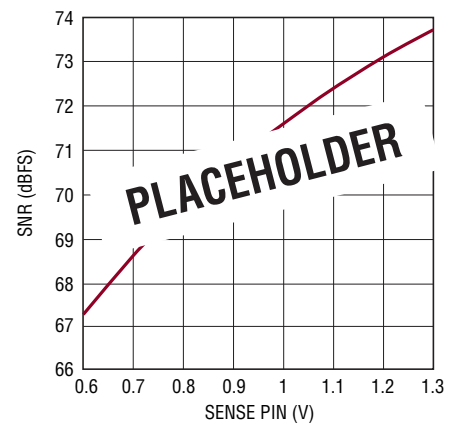**LTM9011-14: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB**
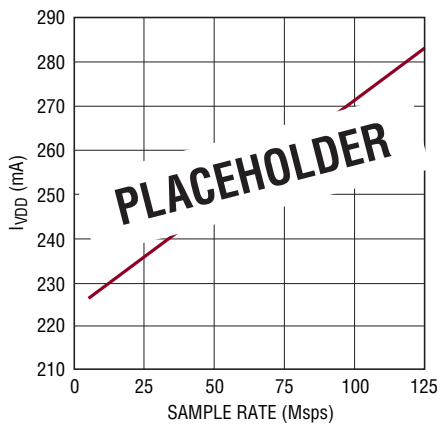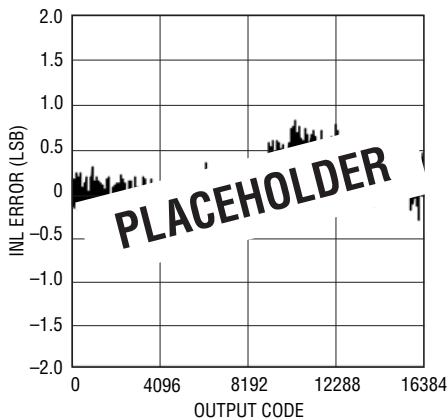
IO_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB

LTM9011-14: SNR vs SENSE, f_{IN} = 5MHz, –1dB

LTM9010-14: Integral Nonlinearity (INL)

LTM9010-14: Differential Nonlinearity (DNL)
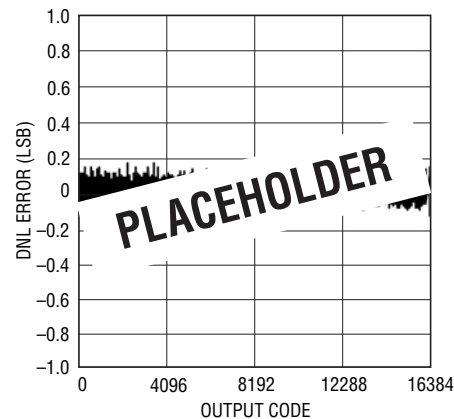
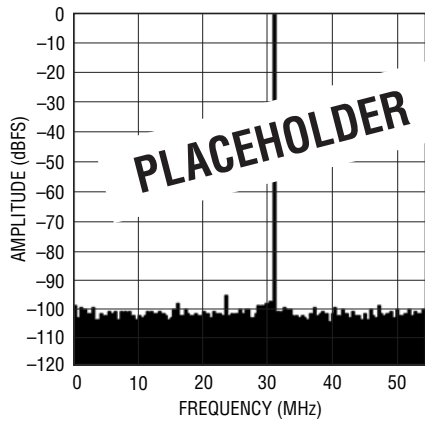**LTM9010-14: 8k Point FFT, f_{IN} = 5MHz –1dBFS, 105Msps**
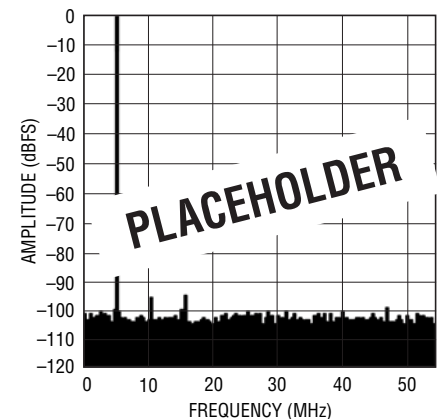
TYPICAL PERFORMANCE CHARACTERISTICS

LTM9010-14: 8k Point FFT, f$_{IN}$ = 30MHz –1dBFS, 105Msps

AMPLITUDE (dBFS) vs FREQUENCY (MHz)

PLACEHOLDER

217514 G17

LTM9010-14: 8k Point FFT, f$_{IN}$ = 70MHz –1dBFS, 105Msps

AMPLITUDE (dBFS) vs FREQUENCY (MHz)

PLACEHOLDER

217514 G18

LTM9010-14: 8k Point FFT, f$_{IN}$ = 140MHz –1dBFS, 105Msps

AMPLITUDE (dBFS) vs FREQUENCY (MHz)

PLACEHOLDER
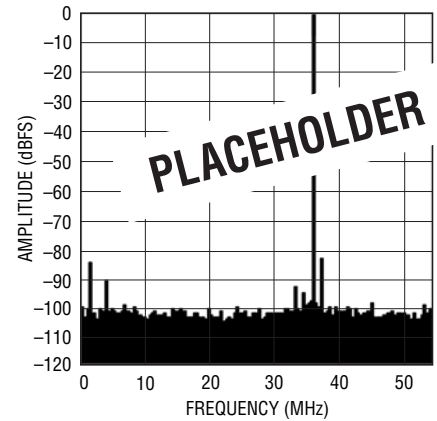
217514 G19

LTM9010-14: 8k Point 2-Tone FFT, f$_{IN}$ = 70MHz, 75MHz, –1dBFS, 105Msps

AMPLITUDE (dBFS) vs FREQUENCY (MHz)

PLACEHOLDER
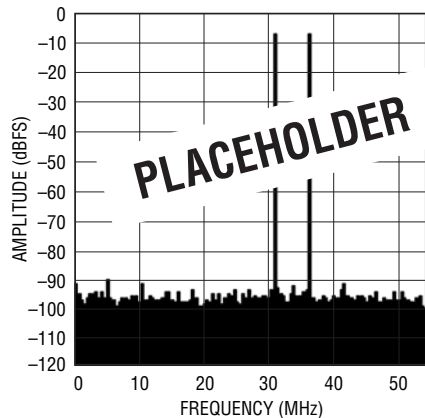
217514 G20

LTM9010-14: Shorted Input Histogram

COUNT vs OUTPUT CODE

PLACEHOLDER
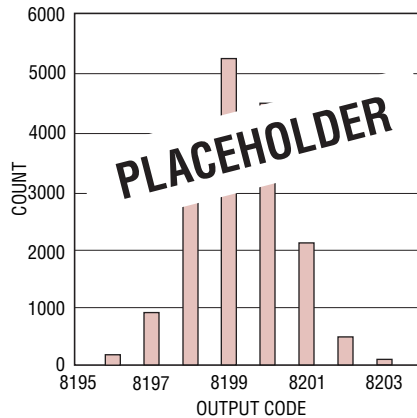
217514 G21

LTM9010-14: SNR vs Input Frequency, –1dB, 2V Range, 105Msps

SNR (dBFS) vs INPUT FREQUENCY (MHz)

PLACEHOLDER
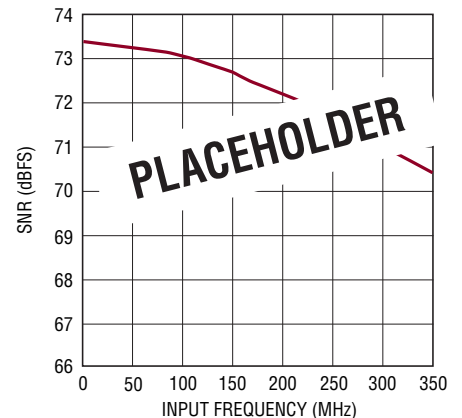
217514 G22

LTM9010-14: SFDR vs Input Frequency, –1dB, 2V Range, 105Msps

SFDR (dBFS) vs INPUT FREQUENCY (MHz)

PLACEHOLDER
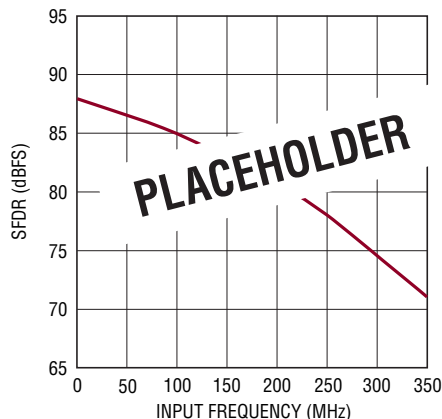
217514 G23

LTM9010-14: SFDR vs Input Level, f$_{IN}$ = 70MHz, 2V Range, 105Msps

SFDR (dBc AND dBFS) vs INPUT LEVEL (dBFS)

dBFS

PLACEHOLDER

217514 G24

LTM9010-14: I$_{VDD}$ vs Sample Rate, 5MHz Sine Wave Input, –1dB

I$_{VDD}$ (mA) vs SAMPLE RATE (Msps)

PLACEHOLDER

217514 G54
9009101114p

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TYPICAL PERFORMANCE CHARACTERISTICS

LTM9010-14: SNR vs SENSE, f_{IN} = 5MHz, –1dB
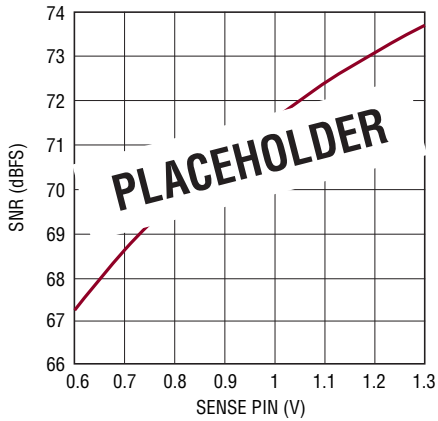
217514 G25

LTM9009-14: Integral Nonlinearity (INL)
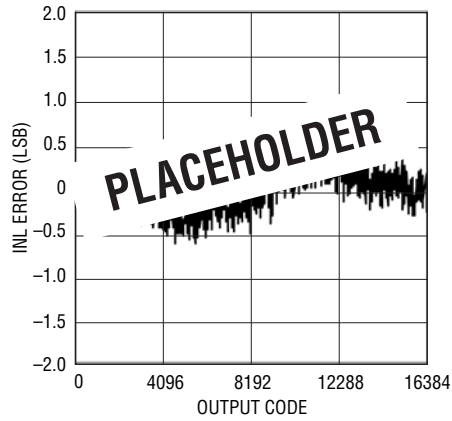
217514 G26

LTM9009-14: Differential Nonlinearity (DNL)
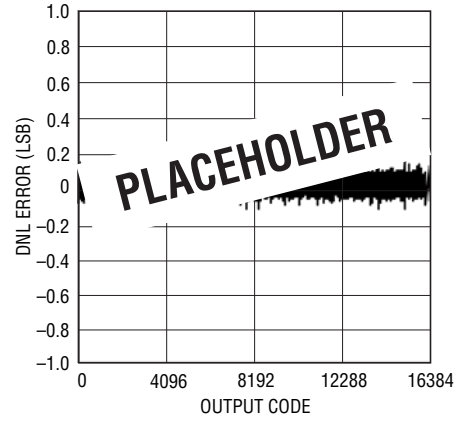
217514 G27

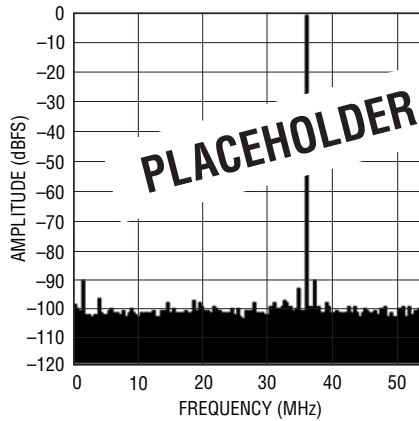**LTM9009-14: 8k Point FFT, f_{IN} = 5MHz –1dBFS, 80Msps**
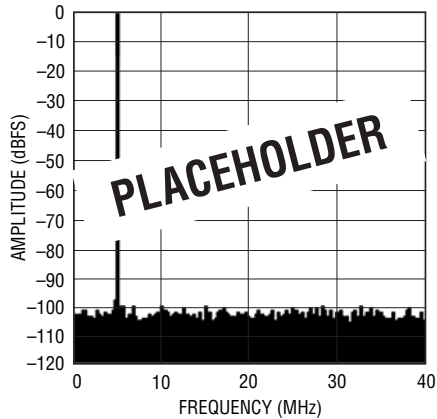
217514 G28

LTM9009-14: 8k Point FFT, f_{IN} = 30MHz –1dBFS, 80Msps
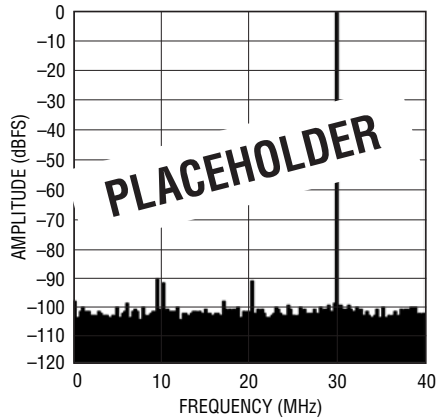
217514 G29

LTM9009-14: 8k Point FFT, f_{IN} = 70MHz –1dBFS, 80Msps
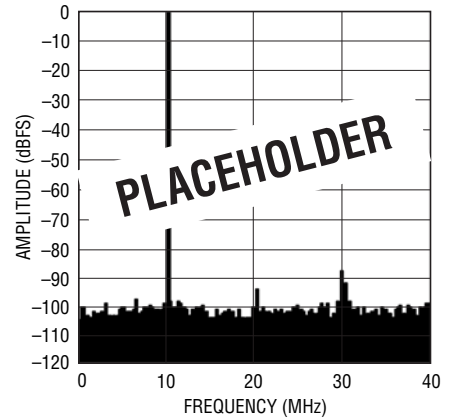
217514 G30

LTM9009-14: 8k Point FFT, f_{IN} = 140MHz –1dBFS, 80Msps
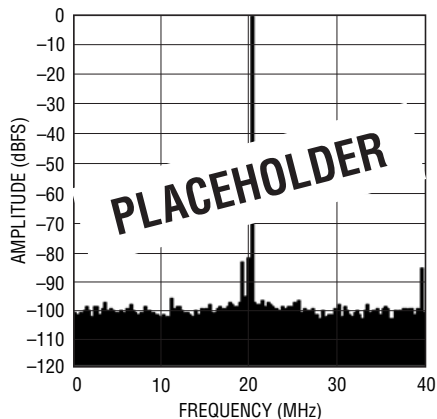
217514 G31

LTM9009-14: 8k Point 2-Tone FFT, f_{IN} = 70MHz, 75MHz, –1dBFS, 80Msps
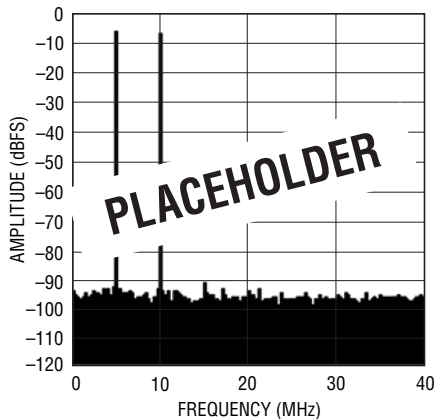
217514 G32

LTM9009-14: Shorted Input Histogram

217514 G33
9009101114p

15
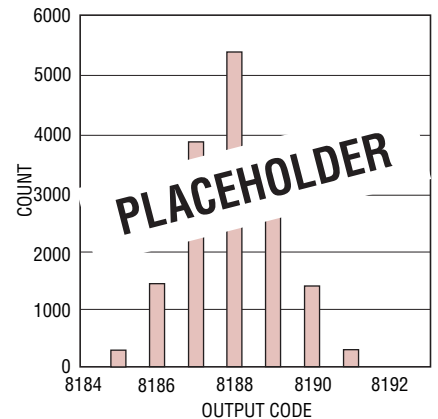
LTM9011-14/
LTM9010-14/LTM9009-14

TYPICAL PERFORMANCE CHARACTERISTICS

LTM9009-14: SNR vs Input
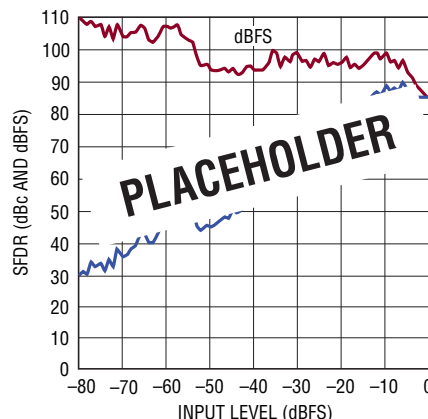Frequency, −1dB, 2V Range,
80Msps

PLACEHOLDER
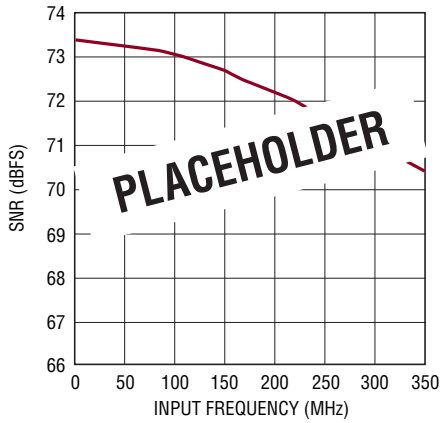
217514 G34

LTM9009-14: SFDR vs Input
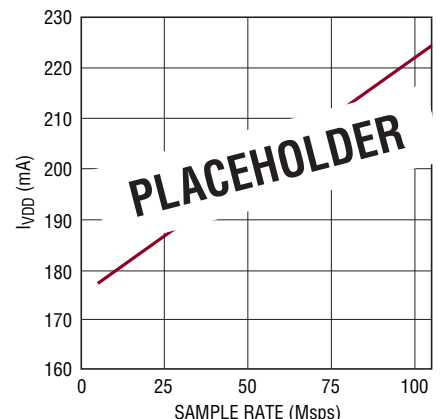Frequency, −1dB, 2V Range,
80Msps

PLACEHOLDER
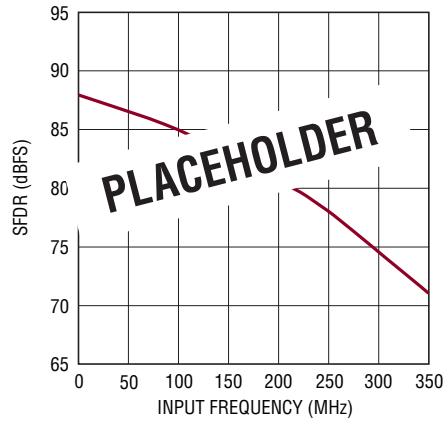
217514 G35

LTM9009-14: SFDR vs Input Level,
f_{IN} = 70MHz, 2V Range, 80Msps

PLACEHOLDER
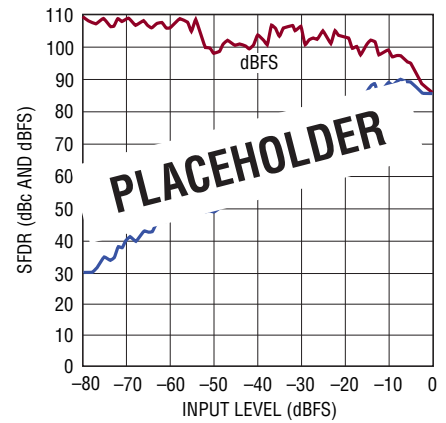
217514 G36

LTM9009-14: I_{VDD} vs Sample Rate,
5MHz Sine Wave Input, −1dB

PLACEHOLDER

217514 G55

LTM9009-14: SNR vs SENSE,
f_{IN} = 5MHz, −1dB

PLACEHOLDER

217514 G37

DCO Cycle-Cycle Jitter vs Serial
Data Rate

PLACEHOLDER

217514 G52

9009101114p

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PIN FUNCTIONS

A_{IN1}^+ **(B2):** Channel 1 Positive Differential Analog Input.

A_{IN1}^- **(B1):** Channel 1 Negative Differential Analog Input.

V_{CM12} **(B3):** Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 1 and 2. V_{CM} is internally bypassed to ground with a 0.1µF ceramic capacitor. No external capacitance is required.

A_{IN2}^+ **(C2):** Channel 2 Positive Differential Analog Input.

A_{IN2}^- **(C1):** Channel 2 Negative Differential Analog Input.

A_{IN3}^+ **(E2):** Channel 3 Positive Differential Analog Input.

A_{IN3}^- **(E1):** Channel 3 Negative Differential Analog Input.

V_{CM34} **(F3):** Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 3 and 4. V_{CM} is internally bypassed to ground with a 0.1µF ceramic capacitor. No external capacitance is required.

A_{IN4}^+ **(G2):** Channel 4 Positive Differential Analog Input.

A_{IN4}^- **(G1):** Channel 4 Negative Differential Analog Input.

A_{IN5}^+ **(H1):** Channel 5 Positive Differential Analog Input.

A_{IN5}^- **(H2):** Channel 5 Negative Differential Analog Input.

V_{CM56} **(J3):** Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 5 and 6. V_{CM} is internally bypassed to ground with a 0.1µF ceramic capacitor. No external capacitance is required.

A_{IN6}^+ **(K1):** Channel 6 Positive Differential Analog Input.

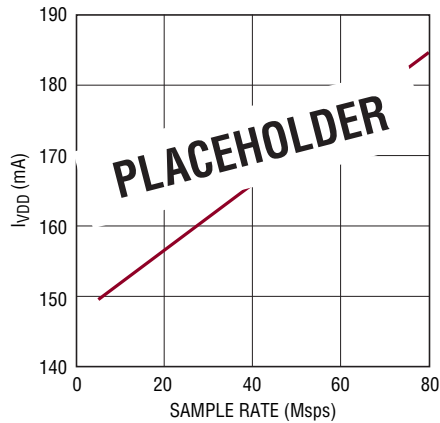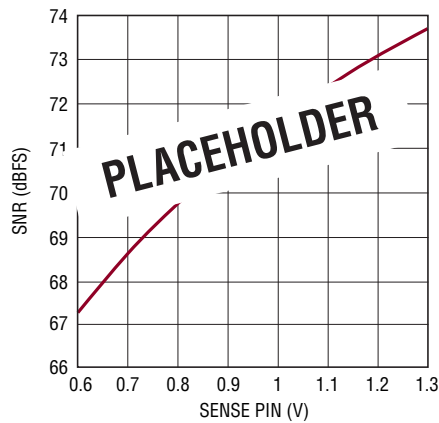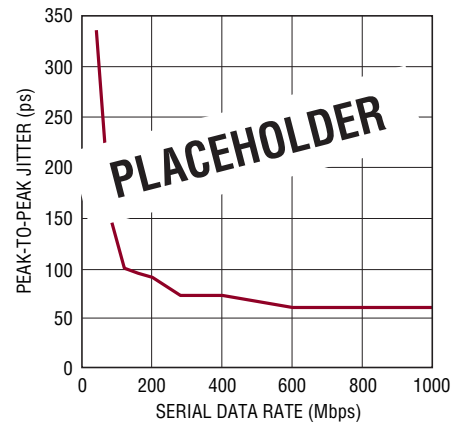A_{IN6}^- **(K2):** Channel 6 Negative Differential Analog Input.

A_{IN7}^+ **(M1):** Channel 7 Positive Differential Analog Input.

A_{IN7}^- **(M2):** Channel 7 Negative Differential Analog Input.

V_{CM78} **(N3):** Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs of channels 7 and 8. V_{CM} is internally bypassed to ground with a 0.1µF ceramic capacitor. No external capacitance is required.

A_{IN8}^+ **(N1):** Channel 8 Positive Differential Analog Input.

A_{IN8}^- **(N2):** Channel 8 Negative Differential Analog Input

V_{DD} **(D3, D4, E3, E4, K3, K4, L3, L4):** 1.8V Analog Power Supply. V_{DD} is internally bypassed to ground with 0.1µF ceramic capacitors.

ENC⁺ (P5): Encode Input. Conversion starts on the rising edge.

ENC⁻ (P6): Encode Complement Input. Conversion starts on the falling edge.

$\overline{CSA}$ (L5): In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CSA}$ is the serial interface chip select input for registers controlling channels 1, 4, 5 and 8. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ selects 2-lane or 1-lane output mode. $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

$\overline{CSB}$ (M5): In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CSB}$ is the serial interface chip select input for registers controlling channels 2, 3, 6 and 7. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ selects 2-lane or 1-lane output mode. $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

SCK (L6): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SCK is the serial interface clock input. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK selects 3.5mA or 1.75mA LVDS output currents. SCK can be driven with 1.8V to 3.3V logic.

SDI (M6): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDI is the serial interface data Input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDI can be used to power down the part. SDI can be driven with 1.8V to 3.3V logic.

GND (See Pin Configuration Table): ADC Power Ground. Use multiple vias close to pins.

PIN FUNCTIONS

OV$_{DD}$ (G9, G10): Output Driver Supply. OV$_{DD}$ is internally bypassed to ground with a 0.1µF ceramic capacitor.

SDOA (E6): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDOA is the optional serial interface data output for registers controlling channels 1 through 4. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain N-channel MOSFET output that requires an external 2k pull-up resistor from 1.8V to 3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In parallel programming mode (PAR/$\overline{SER}$ = V$_{DD}$), SDOA is an input that enables internal 100Ω termination resistors on the digital outputs of channels 1, 4, 5 and 8. When used as an input, SDO can be driven with 1.8V to 3.3V logic through a 1k series resistor.

SDOB (D6): Serial Data Output Pin for Channels 2, 3, 6 and 7. See description for SDOA.

PAR/$\overline{SER}$ (A7): Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. $\overline{CSA}$, $\overline{CSB}$, SCK, SDI, SDOA and SDOB become a serial interface that control the A/D operating modes. Connect to V$_{DD}$ to enable parallel programming mode where $\overline{CSA}$, $\overline{CSB}$, SCK, SDI, SDOA and SDOB become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{SER}$ should be connected directly to ground or the V$_{DD}$ of the part and not be driven by a logic signal.

V$_{REF}$ (B6): Reference Voltage Output. V$_{REF}$ is internally bypassed to ground with a 1µF ceramic capacitor, nominally 1.25V.

SENSE (C5): Reference Programming Pin. Connecting SENSE to V$_{DD}$ selects the internal reference and a ±1V input range. Connecting SENSE to ground selects the internal reference and a ±0.5V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of ±0.8 • V$_{SENSE}$. SENSE is internally bypassed to ground with a 0.1µF ceramic capacitor.

LVDS Outputs

All pins in this section are differential LVDS outputs. The output current level is programmable. There is an optional internal 100Ω termination resistor between the pins of each LVDS output pair.

OUT1A⁻/OUT1A⁺, OUT1B⁻/OUT1B⁺ (E7/E8, C8/D8): Serial Data Outputs for Channel 1. In 1-lane output mode only OUT1A⁻/OUT1A⁺ are used.

OUT2A⁻/OUT2A⁺, OUT2B⁻/OUT2B⁺ (B8/A8, D7/C7): Serial Data Outputs for Channel 2. In 1-lane output mode only OUT2A⁻/OUT2A⁺ are used.

OUT3A⁻/OUT3A⁺, OUT3B⁻/OUT3B⁺ (D10/D9, E10/E9): Serial Data Outputs for Channel 3. In 1-lane output mode only OUT3A⁻/OUT3A⁺ are used.

OUT4A⁻/OUT4A⁺, OUT4B⁻/OUT4B⁺ (C9/C10, F7/F8): Serial Data Outputs for Channel 4. In 1-lane output mode only OUT4A⁻/OUT4A⁺ are used.

OUT5A⁻/OUT5A⁺, OUT5B⁻/OUT5B⁺ (J8/J7, K8/K7): Serial Data Outputs for Channel 5. In 1-lane output mode only OUT5A⁻/OUT5A⁺ are used.

OUT6A⁻/OUT6A⁺, OUT6B⁻/OUT6B⁺ (K9/K10, L9/L10): Serial Data Outputs for Channel 6. In 1-lane output mode only OUT6A⁻/OUT6A⁺ are used.

OUT7A⁻/OUT7A⁺, OUT7B⁻/OUT7B⁺ (M7/L7, P8/N8): Serial Data Outputs for Channel 7. In 1-lane output mode only OUT7A⁻/OUT7A⁺ are used.

OUT8A⁻/OUT8A⁺, OUT8B⁻/OUT8B⁺ (L8/M8, M10/M9): Serial Data Outputs for Channel 8. In 1-lane output mode only OUT8A⁻/OUT8A⁺ are used.

FRA⁻/FRA⁺ (H7/H8): Frame Start Outputs for Channels 1, 4, 5 and 8.

FRB⁻/FRB⁺ (J9/J10): Frame Start Outputs for Channels 2, 3, 6 and 7.

DCOA⁻/DCOA⁺ (G8/G7): Data Clock Outputs for Channels 1, 4, 5 and 8.

DCOB⁻/DCOB⁺ (F10, F9): Data Clock Outputs for Channels 2, 3, 6 and 7.

PIN CONFIGURATION TABLE

	1	2	3	4	5	6	7	8	9	10
A	GND	GND	GND	GND	GND	GND	PAR/$\overline{SER}$	O2A$^+$	OGND	OGND
B	$A_{IN1}{}^-$	$A_{IN1}{}^+$	V_{CM12}	GND	GND	V_{REF}	GND	O2A$^-$	OGND	OGND
C	$A_{IN2}{}^-$	$A_{IN2}{}^+$	GND	GND	SENSE	GND	O2B$^+$	O1B$^-$	O4A$^-$	O4A$^+$
D	GND	GND	V_{DD}	V_{DD}	GND	SDOB	O2B$^-$	O1B$^+$	O3A$^+$	O3A$^-$
E	$A_{IN3}{}^-$	$A_{IN3}{}^+$	V_{DD}	V_{DD}	GND	SDOA	O1A$^-$	O1A$^+$	O3B$^+$	O3B$^-$
F	GND	GND	V_{CM34}	GND	GND	GND	O4B$^-$	O4B$^+$	DCOB$^+$	DCOB$^-$
G	$A_{IN4}{}^-$	$A_{IN4}{}^+$	GND	GND	GND	GND	DCOA$^+$	DCOA$^-$	OV$_{DD}$	OV$_{DD}$
H	$A_{IN5}{}^+$	$A_{IN5}{}^-$	GND	GND	GND	GND	FRA$^-$	FRA$^+$	OGND	OGND
J	GND	GND	V_{CM56}	GND	GND	GND	O5A$^+$	O5A$^-$	FRB$^-$	FRB$^+$
K	$A_{IN6}{}^+$	$A_{IN6}{}^-$	V_{DD}	V_{DD}	GND	GND	O5B$^+$	O5B$^-$	O6A$^-$	O6A$^+$
L	GND	GND	V_{DD}	V_{DD}	$\overline{CSA}$	SCK	O7A$^+$	O8A$^-$	O6B$^-$	O6B$^+$
M	$A_{IN7}{}^+$	$A_{IN7}{}^-$	GND	GND	$\overline{CSB}$	SDI	O7A$^-$	O8A$^+$	O8B$^+$	O8B$^-$
N	$A_{IN8}{}^+$	$A_{IN8}{}^-$	V_{CM78}	GND	GND	GND	GND	O7B$^+$	OGND	OGND
P	GND	GND	GND	GND	CLK$^+$	CLK$^-$	GND	O7B$^-$	OGND	OGND

Top View of BGA Package (Looking Through Component).

FUNCTIONAL BLOCK DIAGRAM
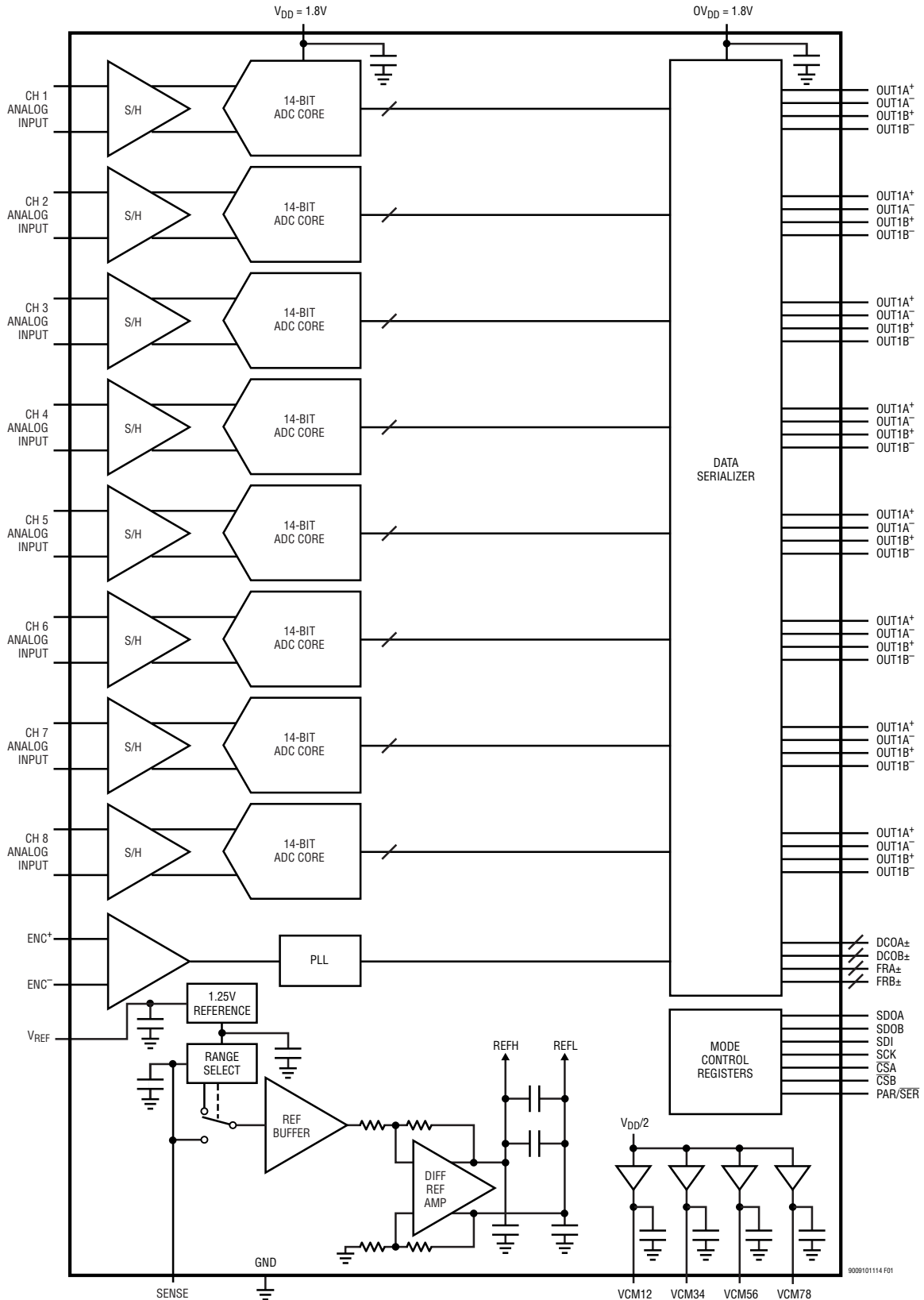
Figure 1. Functional Block Diagram

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APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTM9011-14/LTM9010-14/LTM9009-14 are low power, 8-channel, 14-bit, 125Msps/105Msps/80Msps A/D converters that are powered by a single 1.8V supply. The analog inputs should be driven differentially. The encode input can be driven differentially for optimal jitter performance, or single-ended for lower power consumption. The digital outputs are serial LVDS to minimize the number of data lines. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). Many additional features can be chosen by programming the mode control registers through a serial SPI port.

ANALOG INPUT

The analog inputs are differential CMOS sample-and-hold circuits (Figure 2). The inputs should be driven differentially around a common mode voltage set by the appropriate V_{CM} output pins, which are nominally $V_{DD}/2$. For the 2V input range, the inputs should swing from $V_{CM} - 0.5V$ to $V_{CM} + 0.5V$. There should be 180° phase difference between the inputs.

The eight channels are simultaneously sampled by a shared encode circuit (Figure 2).
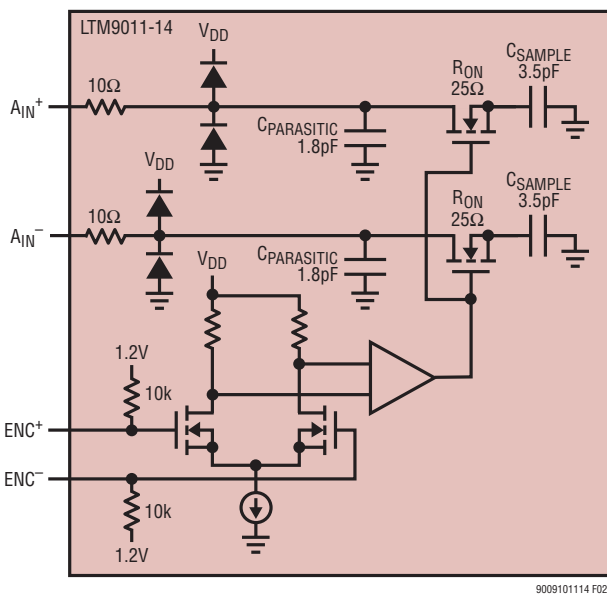
Figure 2. Equivalent Input Circuit. Only One of the Eight Analog Channels Is Shown

INPUT DRIVE CIRCUITS

Input Filtering

If possible, there should be an RC low pass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wideband noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's input frequency.

Transformer Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with a center-tapped secondary. The center tap is biased with V_{CM}, setting the A/D input at its optimal DC level. At higher input frequencies a transmission line balun transformer (Figures 4 to 6) has better balance, resulting in lower A/D distortion.
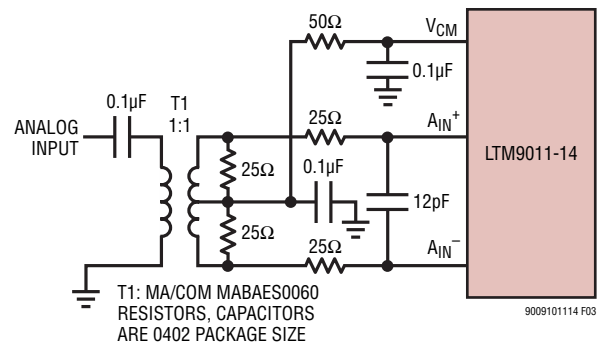
Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

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Amplifier Circuits

Figure 7 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC-coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 4 to 6) should convert the signal to differential before driving the A/D.

Reference

The LTM9011-14/LTM9010-14/LTM9009-14 has an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference,
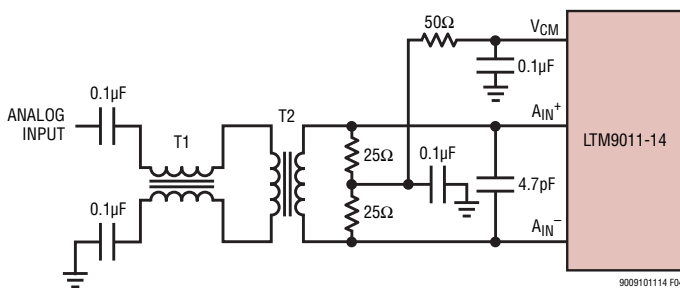
T1: MA/COM MABA-007159-000000
T2: MA/COM MABAES0060
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 4. Recommended Front End Circuit for Input Frequencies from 70MHz to 170MHz
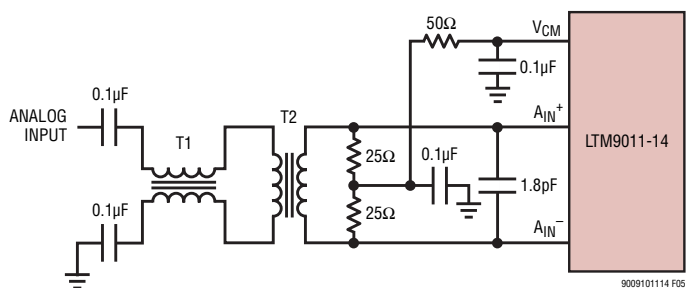
T1: MA/COM MABA-007159-000000
T2: COILCRAFT WBC1-1LB
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 5. Recommended Front End Circuit for Input Frequencies from 170MHz to 300MHz
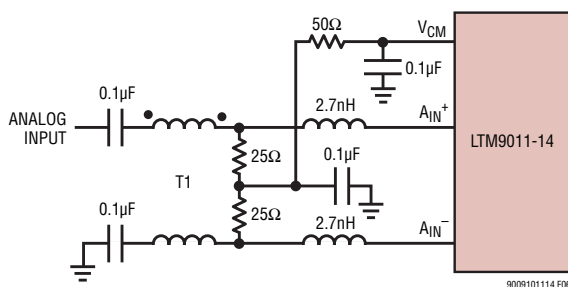
T1: MA/COM ETC1-1-13
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 6. Recommended Front End Circuit for Input Frequencies Above 300MHz
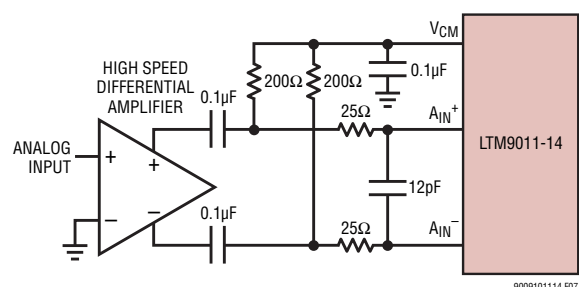
Figure 7. Front End Circuit Using a High Speed Differential Amplifier

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apply a 1.25V reference voltage to SENSE (Figure 9).

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be 1.6 • V_{SENSE}. The reference is shared by all eight ADC channels, so it is not possible to independently adjust the input range of individual channels.

The V_{REF}, REFH and REFL pins are internally bypassed, as shown in Figure 8.

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 10), and the single-ended encode mode (Figure 11).
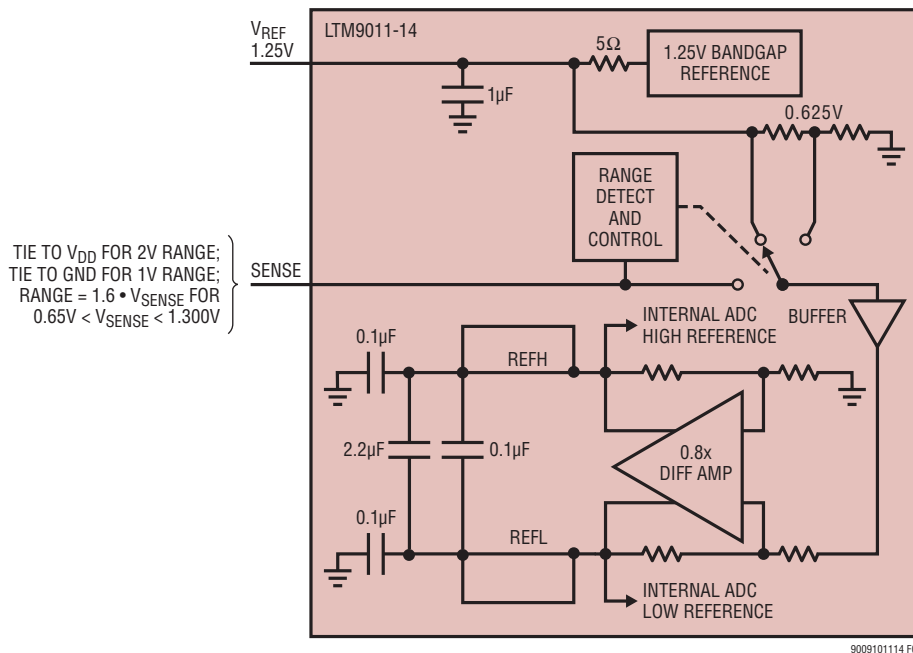
Figure 8. Reference Circuit
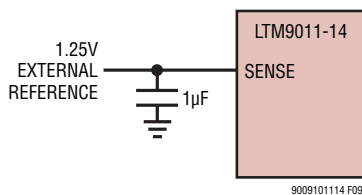
Figure 9. Using an External 1.25V Reference
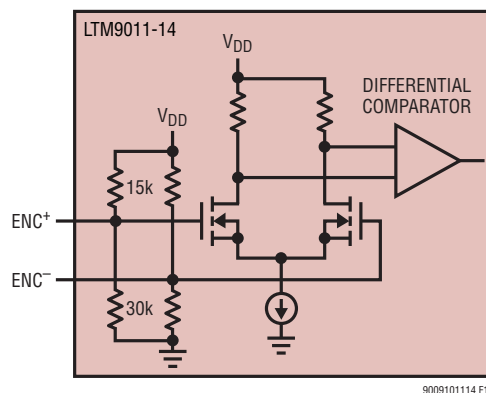
Figure 10. Equivalent Encode Input Circuit for Differential Encode Mode
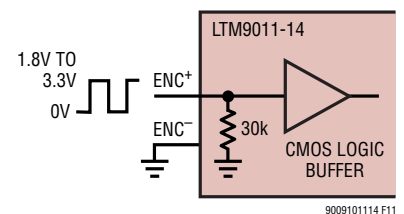
Figure 11. Equivalent Encode Input Circuit for Single-Ended Encode Mode

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The differential encode mode is recommended for sinusoidal, PECL, or LVDS encode inputs (Figures 12 and 13). The encode inputs are internally biased to 1.2V through 10k equivalent resistance. The encode inputs can be taken above V_{DD} (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC⁻ should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance ENC⁺ should have fast rise and fall times.

The single-ended encode mode should be used with CMOS encode inputs. To select this mode, ENC⁻ is connected to ground and ENC⁺ is driven with a square wave encode input. ENC⁺ can be taken above V_{DD} (up to 3.6V) so 1.8V to 3.3V CMOS logic levels can be used. The ENC⁺ threshold is 0.9V. For good jitter performance ENC⁺ should have fast

rise and fall times.

Clock PLL and Duty Cycle Stabilizer

The encode clock is multiplied by an internal phase-locked loop (PLL) to generate the serial digital output data. If the encode signal changes frequency or is turned off, the PLL requires 25µs to lock onto the input clock.

A clock duty cycle stabilizer circuit allows the duty cycle of the applied encode signal to vary from 30% to 70%. In the serial programming mode it is possible to disable the duty cycle stabilizer, but this is not recommended. In the parallel programming mode the duty cycle stabilizer is always enabled.

T1 = MA/COM ETC1-1-13
RESISTORS AND CAPACITORS
ARE 0402 PACKAGE SIZE
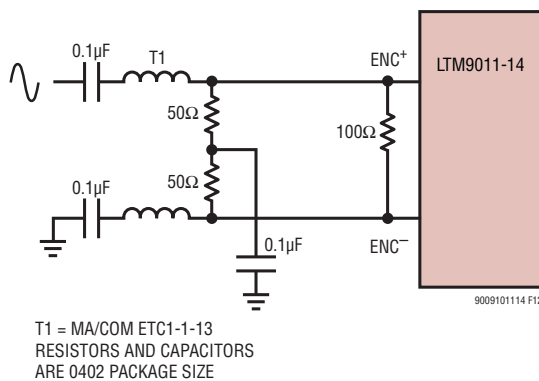
Figure 12. Sinusoidal Encode Drive
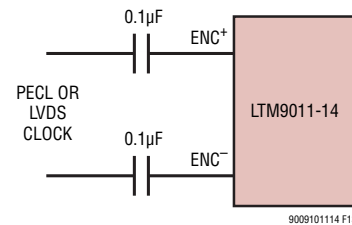
Figure 13. PECL or LVDS Encode Drive

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DIGITAL OUTPUTS

The digital outputs of the LTM9011-14/LTM9010-14/LTM9009-14 are serialized LVDS signals. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). The data can be serialized with 16, 14, or 12-bit serialization (see timing diagrams for details). Note that with 12-bit serialization the two LSBs are not available—this mode is included for compatibility with the 12-bit versions of these parts.

The output data should be latched on the rising and falling edges of the data clock out (DCO). A data frame output (FR) can be used to determine when the data from a new conversion result begins. In the 2-lane, 14-bit serialization mode, the frequency of the FR output is halved.

The maximum serial data rate for the data outputs is 1Gbps, so the maximum sample rate of the ADC will depend on the serialization mode as well as the speed grade of the ADC (see Table 1). The minimum sample rate for all serialization modes is 5Msps.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground.

Programmable LVDS Output Current

The default output driver current is 3.5mA. This current can be adjusted by control register A2 in the serial programming mode. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA. In the parallel programming mode the SCK pin can select either 3.5mA or 1.75mA.

Optional LVDS Driver Internal Termination

In most cases using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A2. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is doubled to maintain the same output voltage swing. In the parallel programming mode the SDO pin enables internal termination. Internal termination should only be used with 1.75mA, 2.1mA or 2.5mA LVDS output current modes.

Table 1. Maximum Sampling Frequency for All Serialization Modes. Note That These Limits Are for the LTM9011-14. The Sampling Frequency for the Slower Speed Grades Cannot Exceed 105MHz (LTM9010-14) or 80MHz (LTM9009-14).

SERIALIZATION MODE		MAXIMUM SAMPLING FREQUENCY, f_S (MHz)	DCO FREQUENCY	FR FREQUENCY	SERIAL DATA RATE
2-Lane	16-Bit Serialization	125	$4 \cdot f_S$	f_S	$8 \cdot f_S$
2-Lane	14-Bit Serialization	125	$3.5 \cdot f_S$	$0.5 \cdot f_S$	$7 \cdot f_S$
2-Lane	12-Bit Serialization	125	$3 \cdot f_S$	f_S	$6 \cdot f_S$
1-Lane	16-Bit Serialization	62.5	$8 \cdot f_S$	f_S	$16 \cdot f_S$
1-Lane	14-Bit Serialization	71.4	$7 \cdot f_S$	f_S	$14 \cdot f_S$
1-Lane	12-Bit Serialization	83.3	$6 \cdot f_S$	f_S	$12 \cdot f_S$

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DATA FORMAT

Table 2 shows the relationship between the analog input voltage and the digital data output bits. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A1.

Table 2. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (2V RANGE)	D13-D0 (OFFSET BINARY)	D13-D0 (2's COMPLEMENT)
>1.000000V	11 1111 1111 1111	01 1111 1111 1111
+0.999878V	11 1111 1111 1111	01 1111 1111 1111
+0.999756V	11 1111 1111 1110	01 1111 1111 1110
+0.000122V	10 0000 0000 0001	00 0000 0000 0001
+0.000000V	10 0000 0000 0000	00 0000 0000 0000
−0.000122V	01 1111 1111 1111	11 1111 1111 1111
−0.000244V	01 1111 1111 1110	11 1111 1111 1110
−0.999878V	00 0000 0000 0001	10 0000 0000 0001
−1.000000V	00 0000 0000 0000	10 0000 0000 0000
<−1.000000V	00 0000 0000 0000	10 0000 0000 0000

Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is randomized by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied —an exclusive-OR operation is applied between the LSB and all other bits. The FR and DCO outputs are not affected. The output randomizer is enabled by serially programming mode control register A1.

Digital Output Test Pattern

To allow in-circuit testing of the digital interface to the A/D, there is a test mode that forces the A/D data outputs (D13-D0) of all channels to known values. The digital output test patterns are enabled by serially programming mode control registers A3 and A4. When enabled, the test patterns override all other formatting modes: 2's complement and randomizer.

Output Disable

The digital outputs may be disabled by serially programming mode control register A2. The current drive for all digital outputs including DCO and FR are disabled to save power or enable in-circuit testing. When disabled the common mode of each output pair becomes high impedance, but the differential impedance may remain low.

Sleep and Nap Modes

The A/D may be placed in sleep or nap modes to conserve power. In sleep mode the entire device is powered down, resulting in 2mW power consumption. Sleep mode is enabled by mode control register A1 (serial programming mode), or by SDI (parallel programming mode). The time required to recover from sleep mode is about 2ms.

In nap mode any combination of A/D channels can be powered down while the internal reference circuits and the PLL stay active, allowing faster wakeup than from sleep mode. Recovering from nap mode requires at least 100 clock cycles. If the application demands very accurate DC settling then an additional 50µs should be allowed so the on-chip references can settle from the slight temperature shift caused by the change in supply current as the A/D leaves nap mode. Nap mode is enabled by mode control register A1 in the serial programming mode.

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DEVICE PROGRAMMING MODES

The operating modes of the LTM9011-14/LTM9010-14/LTM9009-14 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}. The $\overline{CS}$, SCK, SDI and SDO pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V, or 3.3V CMOS logic. When used as an input, SDO should be driven through a 1k series resistor. Table 3 shows the modes set by $\overline{CS}$, SCK, SDI and SDO.

Table 3. Parallel Programming Mode Control Bits (PAR/$\overline{SER}$ = V_{DD})

Pin	DESCRIPTION
$\overline{CS}$	**2-Lane / 1-Lane Selection Bit**
	0 = 2-Lane, 16-Bit Serialization Output Mode
	1 = 1-Lane, 14-Bit Serialization Output Mode
SCK	**LVDS Current Selection Bit**
	0 = 3.5mA LVDS Current Mode
	1 = 1.75mA LVDS Current Mode
SDI	**Power Down Control Bit**
	0 = Normal Operation
	1 = Sleep Mode
SDO	**Internal Termination Selection Bit**
	0 = Internal Termination Disabled
	1 = Internal Termination Enabled

Serial Programming Mode

To use the serial programming mode, PAR/$\overline{SER}$ should be tied to ground. The $\overline{CS}$, SCK, SDI and SDO pins become a serial interface that program the A/D mode control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the Timing Diagrams sections). During a read back command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and read back is not needed, then SDO can be left floating and no pull-up resistor is needed. Table 4 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to logic 0. To perform a software reset, bit D7 in the reset register is written with a logic 1. After the reset is complete, bit D7 is automatically set back to zero.

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Table 4. Serial Programming Mode Register Map (PAR/$\overline{\text{SER}}$ = GND)

REGISTER A0: RESET REGISTER (ADDRESS 00h)

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Note That $\overline{\text{CSA}}$ Controls Channels 1, 4, 5 and 8, $\overline{\text{CSB}}$ Controls Channels 2, 3, 6 and 7.

Bit 7	**RESET**	Software Reset Bit

0 = Not Used
1 = Software Reset. All Mode Control Registers Are Reset to 00h. The ADC Is Momentarily Placed in SLEEP Mode. This Bit Is Automatically Set Back to Zero After the Reset Is Complete

Bits 6-0   Unused, Don't Care Bits.

REGISTER A1 ($\overline{\text{CSA}}$): FORMAT AND POWER-DOWN REGISTER (ADDRESS 01h with $\overline{\text{CSA}}$ = GND)

D7	D6	D5	D4	D3	D2	D1	D0
DCSOFF	RAND	TWOSCOMP	SLEEP	NAP_8	NAP_5	NAP_4	NAP_1

Note That $\overline{\text{CSA}}$ Controls Channels 1, 4, 5 and 8, $\overline{\text{CSB}}$ Controls Channels 2, 3, 6 and 7.

Bit 7   **DCSOFF**   Clock Duty Cycle Stabilizer Bit
0 = Clock Duty Cycle Stabilizer On
1 = Clock Duty Cycle Stabilizer Off. This Is Not Recommended.

Bit 6   **RAND**   Data Output Randomizer Mode Control Bit
0 = Data Output Randomizer Mode Off
1 = Data Output Randomizer Mode On

Bit 5   **TWOSCOMP**   Two's Complement Mode Control Bit
0 = Offset Binary Data Format
1 = Two's Complement Data Format

Bits 4-0   **SLEEP: NAP_X**   Sleep/Nap Mode Control Bits
00000 = Normal Operation
0XXX1 = Channel 1 in Nap Mode
0XX1X = Channel 4 in Nap Mode
0X1XX = Channel 5 in Nap Mode
01XXX = Channel 8 in Nap Mode
1XXXX = Sleep Mode. Channels 1, 4, 5 and 8 Are Disabled
Note: Any Combination of Channels Can Be Placed in Nap Mode.

REGISTER A1 ($\overline{\text{CSB}}$): FORMAT AND POWER-DOWN REGISTER (ADDRESS 01h with $\overline{\text{CSB}}$ = GND)

D7	D6	D5	D4	D3	D2	D1	D0
DCSOFF	RAND	TWOSCOMP	SLEEP	NAP_7	NAP_6	NAP_3	NAP_2

Note That $\overline{\text{CSA}}$ Controls Channels 1, 4, 5 and 8, $\overline{\text{CSB}}$ Controls Channels 2, 3, 6 and 7.

Bit 7   **DCSOFF**   Clock Duty Cycle Stabilizer Bit
0 = Clock Duty Cycle Stabilizer On
1 = Clock Duty Cycle Stabilizer Off. This Is Not Recommended.

Bit 6   **RAND**   Data Output Randomizer Mode Control Bit
0 = Data Output Randomizer Mode Off
1 = Data Output Randomizer Mode On

Bit 5   **TWOSCOMP**   Two's Complement Mode Control Bit
0 = Offset Binary Data Format
1 = Two's Complement Data Format

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Bits 4-0   **SLEEP: NAP_4:NAP_1**   Sleep/Nap Mode Control Bits
00000 = Normal Operation
0XXX1 = Channel 2 in Nap Mode
0XX1X = Channel 3 in Nap Mode
0X1XX = Channel 6 in Nap Mode
01XXX = Channel 7 in Nap Mode
1XXXX = Sleep Mode. Channels 2, 3, 6 and 7 Are Disabled
Note: Any Combination of Channels Can Be Placed in Nap Mode.

REGISTER A2: OUTPUT MODE REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTMODE2	OUTMODE1	OUTMODE0

Note That $\overline{CSA}$ Controls Channels 1, 4, 5 and 8, $\overline{CSB}$ Controls Channels 2, 3, 6 and 7.

Bits 7-5   **ILVDS2:ILVDS0**   LVDS Output Current Bits
000 = 3.5mA LVDS Output Driver Current
001 = 4.0mA LVDS Output Driver Current
010 = 4.5mA LVDS Output Driver Current
011 = Not Used
100 = 3.0mA LVDS Output Driver Current
101 = 2.5mA LVDS Output Driver Current
110 = 2.1mA LVDS Output Driver Current
111 = 1.75mA LVDS Output Driver Current

Bit 4   **TERMON**   LVDS Internal Termination Bit
0 = Internal Termination Off
1 = Internal Termination On. LVDS Output Driver Current Is 2x the Current Set by ILVDS2:ILVDS0. Internal Termination Should Only Be Used with 1.75mA, 2.1mA or 2.5mA LVDS Output Current Modes.

Bit 3   **OUTOFF**   Output Disable Bit
0 = Digital Outputs Are Enabled.
1 = Digital Outputs Are Disabled.

Bits 2-0   **OUTMODE2:OUTMODE0**   Digital Output Mode Control Bits
000 = 2-Lanes, 16-Bit Serialization
001 = 2-Lanes, 14-Bit Serialization
010 = 2-Lanes, 12-Bit Serialization
011 = Not Used
100 = Not Used
101 = 1-Lane, 14-Bit Serialization
110 = 1-Lane, 12-Bit Serialization
111 = 1-Lane, 16-Bit Serialization

REGISTER A3: TEST PATTERN MSB REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
OUTTEST	X	TP13	TP12	TP11	TP10	TP9	TP8

Note That $\overline{CSA}$ Controls Channels 1, 4, 5 and 8, $\overline{CSB}$ Controls Channels 2, 3, 6 and 7.

Bit 7   **OUTTEST**   Digital Output Test Pattern Control Bit
0 = Digital Output Test Pattern Off
1 = Digital Output Test Pattern On

Bit 6   Unused, Don't Care Bit.

Bit 5-0   **TP13:TP8**   Test Pattern Data Bits (MSB)
TP13:TP8 Set the Test Pattern for Data Bit 13 (MSB) Through Data Bit 8.

REGISTER A4: TEST PATTERN LSB REGISTER (ADDRESS 04h)

D7	D6	D5	D4	D3	D2	D1	D0
TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0

Note That $\overline{CSA}$ Controls Channels 1, 4, 5 and 8, $\overline{CSB}$ Controls Channels 2, 3, 6 and 7.

Bit 7-0   **TP7:TP0**   Test Pattern Data Bits (LSB)
TP7:TP0 Set the Test Pattern for Data Bit 7 Through Data Bit 0 (LSB).

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GROUNDING AND BYPASSING

The LTM9011-14/LTM9010-14/LTM9009-14 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane in the first layer beneath the ADC is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

Bypass capacitors are integrated inside the package; additional capacitance is optional.

The analog inputs, encode signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

The pin assignments of the LTM9011-14/LTM9010-14/LTM9009-14 allow a flow-through layout that makes it possible to use multiple parts in a small area when a large number of ADC channels are required. The LTM9011 module has similar layout rules to other BGA packages. The layout can be implemented with 6mil blind vias and 5mil traces. The pinout has been designed to minimize the space required to route the analog and digital traces. The analog and digital traces can essentially be routed within the width of the package. This allows multiple packages to be located close together for high channel count applications. Trace lengths for the analog inputs and digital outputs should be matched as well as possible. Table 5 lists the trace lengths for the analog inputs and digital outputs inside the package from the die pad to the package pad. These should be added to the PCB trace lengths for best matching.

HEAT TRANSFER

Most of the heat generated by the LTM9011-14/LTM9010-14/LTM9009-14 is transferred from the die through the bottom of the package onto the printed circuit board. The ground pins should be connected to the internal ground planes by multiple vias.

Table 5. Internal Trace Lengths

PIN	NAME	LENGTH (mm)	PIN	NAME	LENGTH (mm)	PIN	NAME	LENGTH (mm)	PIN	NAME	LENGTH (mm)
E7	01A$^-$	1.775	K8	05B$^-$	0.379	E1	A_{IN3}^-	2.491	F10	DCOB$^-$	1.811
E8	01A$^+$	1.947	K7	05B$^+$	0.528	E2	A_{IN3}^+	2.505	F9	DCOB$^+$	1.812
C8	01B$^-$	1.847	K9	06A$^-$	1.866	G1	A_{IN4}^-	3.376	H7	FRA$^-$	1.117
D8	01B$^+$	1.850	K10	06A$^+$	1.865	G2	A_{IN4}^+	3.372	H8	FRA$^+$	1.038
B8	02A$^-$	3.233	L9	06B$^-$	2.268	H2	A_{IN5}^-	3.301	J9	FRB$^-$	1.644
A8	02A$^+$	3.246	L10	06B$^+$	2.267	H1	A_{IN5}^+	3.346	J10	FRB$^+$	1.643
D7	02B$^-$	0.179	M7	07A$^-$	1.089	K2	A_{IN6}^-	2.506	A7	PAR/SER	3.838
C7	02B$^+$	1.127	L7	07A$^+$	0.179	K1	A_{IN6}^+	2.533	L6	SCK	0.240
D10	03A$^-$	2.126	P8	07B$^-$	3.281	M2	A_{IN7}^-	3.198	E6	SDOA	0.453
D9	03A$^+$	2.177	N8	07B$^+$	3.149	M1	A_{IN7}^+	3.214	D6	SDOB	0.274
E10	03B$^-$	1.811	L8	08A$^-$	1.862	N2	A_{IN8}^-	4.726	M6	SDI	1.069
E9	03B$^+$	1.812	M8	08A$^+$	1.847	N1	A_{IN8}^+	4.691	B3	V_{CM12}	3.914
C9	04A$^-$	3.199	M10	08B$^-$	4.021	P6	CLK$^-$	4.106	F3	V_{CM34}	0.123
C10	04A$^+$	3.196	M9	08B$^+$	4.016	P5	CLK$^+$	4.106	J3	V_{CM56}	0.079
F7	04B$^-$	0.706	B1	A_{IN1}^-	4.689	L5	$\overline{CSA}$	0.919	N3	V_{CM78}	3.915
F8	04B$^+$	0.639	B2	A_{IN1}^+	4.709	M5	$\overline{CSB}$	1.162			
J8	05A$^-$	0.392	C1	A_{IN2}^-	4.724	G8	DCOA$^-$	1.157			
J7	05A$^+$	0.436	C2	A_{IN2}^+	4.769	G7	DCOA$^+$	1.088			

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TYPICAL APPLICATIONS

Silkscreen Top

Top Side

GRAPHIC
PENDING

GRAPHIC
PENDING

TYPICAL APPLICATIONS

Inner Layer 2 GND

GRAPHIC
PENDING

Inner Layer 3

GRAPHIC
PENDING

Inner Layer 4

GRAPHIC
PENDING

Inner Layer 5 Power

GRAPHIC
PENDING

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TYPICAL APPLICATIONS

Bottom Side

GRAPHIC
PENDING

Silkscreen Bottom

GRAPHIC
PENDING

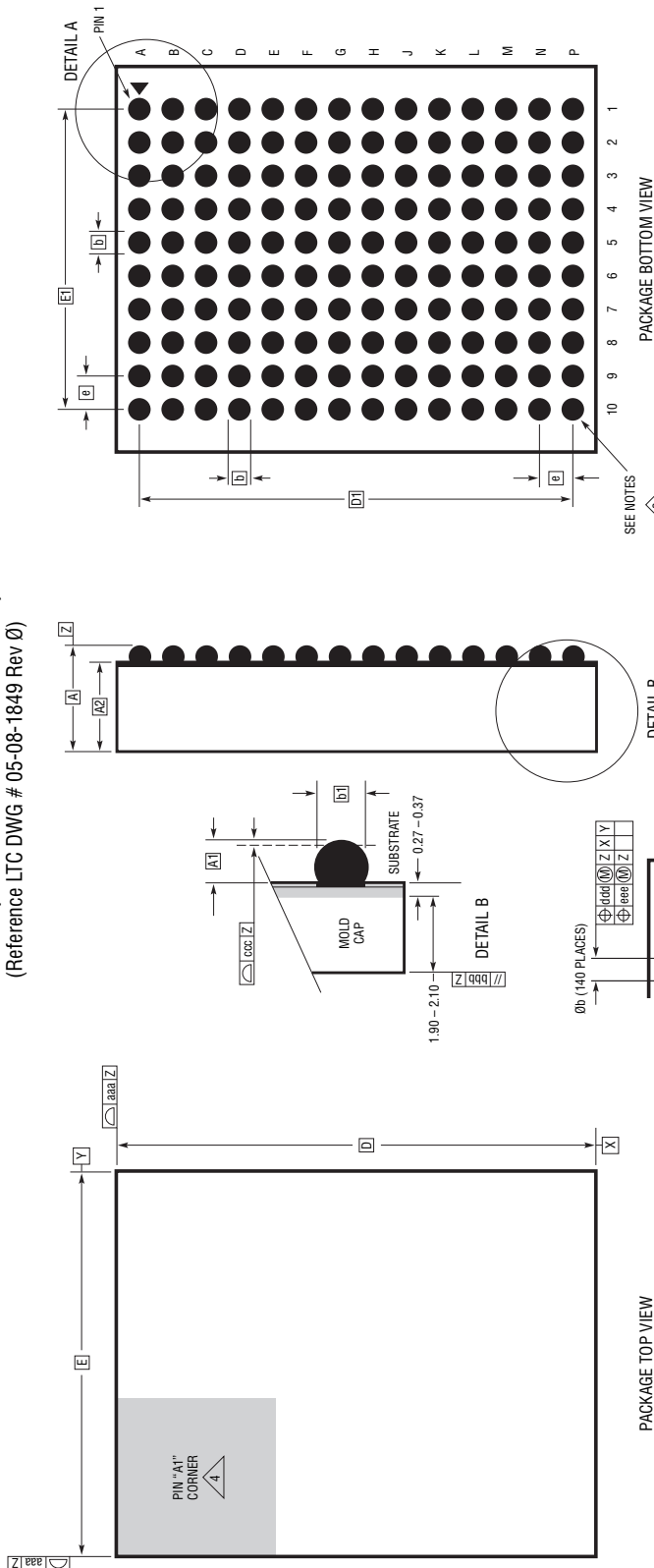## TYPICAL APPLICATIONS

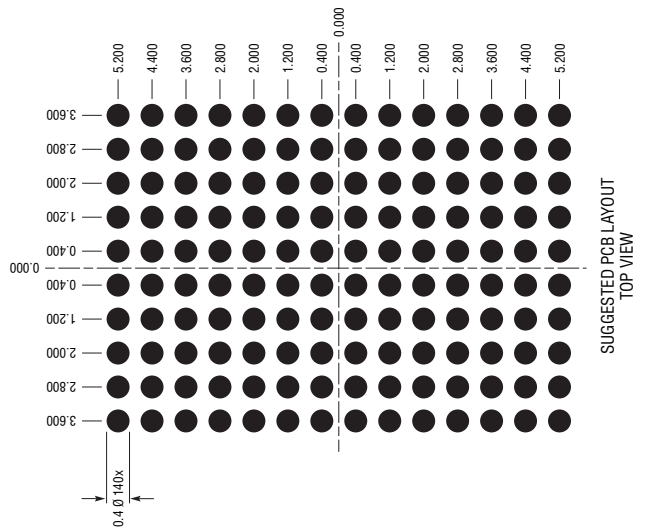**LTM9009-14 Schematic**

GRAPHIC
PENDING

PACKAGE DESCRIPTION

BGA Package
140-Lead (11.25mm × 9.00mm × 2.72mm)
(Reference LTC DWG # 05-08-1849 Rev Ø)

PACKAGE BOTTOM VIEW

DETAIL A
PIN 1

DETAIL B
PACKAGE SIDE VIEW

DETAIL A

DETAIL B

SUBSTRATE

MOLD CAP

Øb (140 PLACES)

0.27 – 0.37

1.90 – 2.10

PACKAGE TOP VIEW

PIN "A1" CORNER

SUGGESTED PCB LAYOUT
TOP VIEW

0.4 Ø 140x

PACKAGE IN TRAY LOADING ORIENTATION

COMPONENT PIN "A1"

TRAY PIN 1 BEVEL

LTMXXXXX
µModule

LINEAR TECHNOLOGY

BGA 140 0709 REV Ø

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
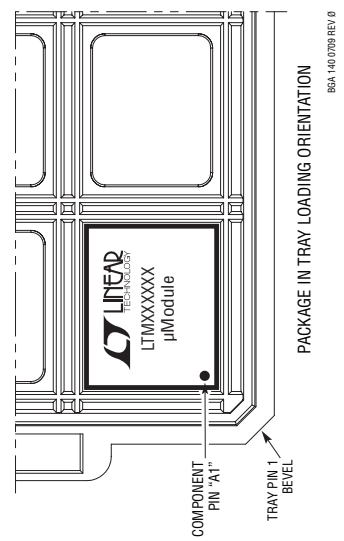
SYMBOL	DIMENSIONS			NOTES
	MIN	NOM	MAX	
A	2.47	2.72	2.97	
A1	0.30	0.40	0.50	
A2	2.17	2.32	2.47	
b	0.45	0.50	0.55	
b1	0.45	0.50	0.55	
D		11.25		
E		9.0		
e		0.80		
D1		10.40		
E1		7.2		
aaa			0.15	
bbb			0.10	
ccc			0.12	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 140				

5.200 4.400 3.600 2.800 2.000 1.200 0.400 0.000 0.400 1.200 2.000 2.800 3.600 4.400 5.200

3.600 2.800 2.000 1.200 0.400 0.000 0.400 1.200 2.000 2.800 3.600

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TYPICAL APPLICATION

Single-Ended to Differential Conversion Using LTC6409 and 50MHz Lowpass Filter (Only One Channel Shown)

9009101114 TA02
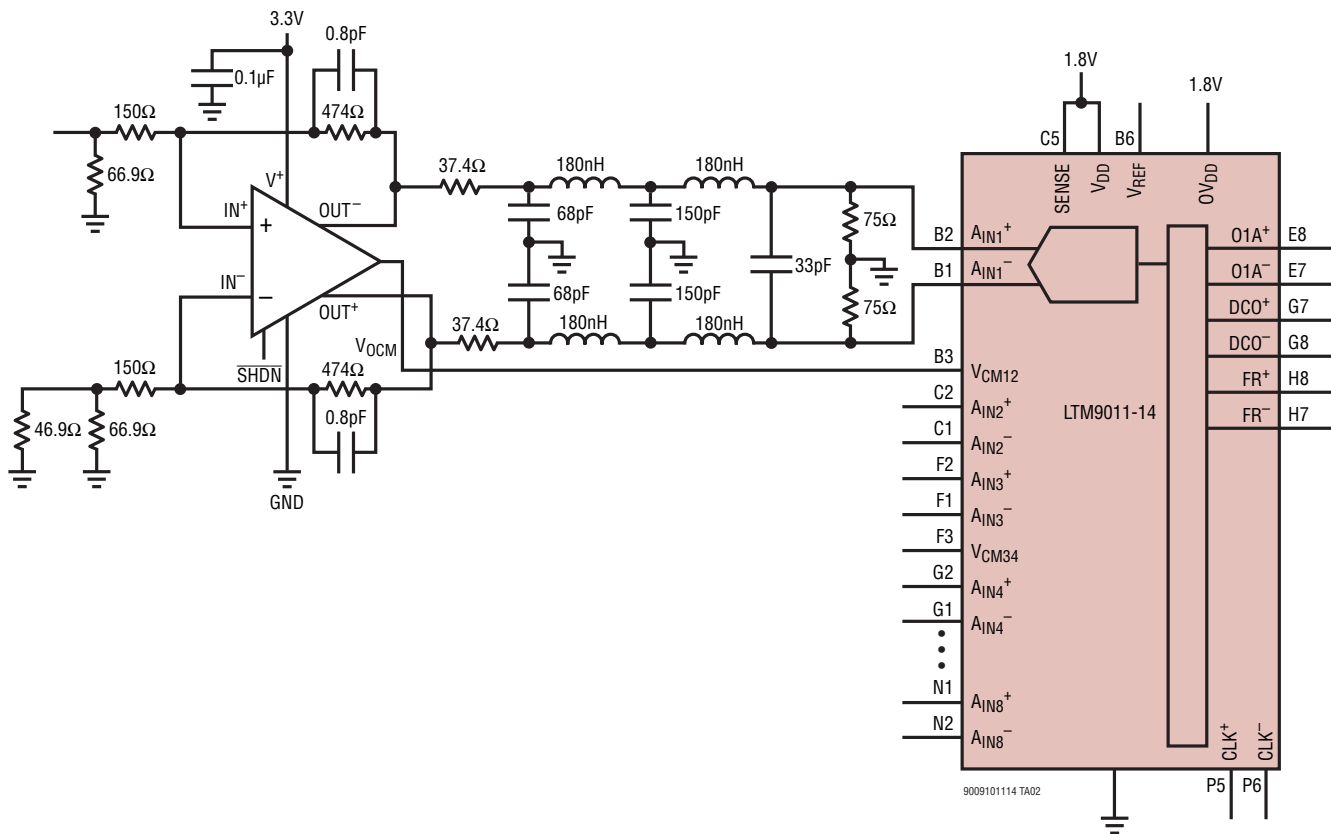
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2170-14/LTC2171-14/LTC2172-14	14-Bit, 25Msps/40Msps/65Msps 1.8V Quad ADCs, Ultralow Power	178mW/234mW/360mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
LTC2170-12/LTC2171-12/LTC2172-12	12-Bit, 25Msps/40Msps/65Msps 1.8V Quad ADCs, Ultralow Power	178mW/234mW/360mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
LTC2173-12/LTC2174-12/LTC2175-12	12-Bit, 80Msps/105Msps/125Msps 1.8V Quad ADCs, Ultralow Power	412mW/481mW/567mW, 70.5dB SNR, 85dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
LTC2173-14/LTC2174-14/LTC2175-14	14-Bit, 80Msps/105Msps/125Msps 1.8V Quad ADCs, Ultralow Power	412mW/481mW/567mW, 73.4dB SNR, 85dB SFDR, Serial LVDS Outputs, 7mm × 8mm QFN-52
Amplifiers/Filters		
LTC6412	800MHz, 31dB Range, Analog-Controlled Variable Gain Amplifier	Continuously Adjustable Gain Control, 35dBm OIP3 at 240MHz, 10dB Noise Figure, 4mm × 4mm QFN-24
LTC6420-20	1.8GHz Dual Low Noise, Low Distortion Differential ADC Drivers for 300MHz IF	Fixed Gain 10V/V, 1nV/$\sqrt{Hz}$ Total Input Noise, 80mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6421-20	1.3GHz Dual Low Noise, Low Distortion Differential ADC Drivers	Fixed Gain 10V/V, 1nV/$\sqrt{Hz}$ Total Input Noise, 40mA Supply Current per Amplifier, 3mm × 4mm QFN-20
LTC6605-7/ LTC6605-10/ LTC6605-14	Dual Matched 7MHz/10MHz/14MHz Filters with ADC Drivers	Dual Matched 2nd Order Lowpass Filters with Differential Drivers, Pin-Programmable Gain, 6mm × 3mm DFN-22
LTM9002	14-Bit Dual Channel IF/Baseband Receiver Subsystem	Integrated High Speed ADC, Passive Filters and Fixed Gain Differential Amplifiers

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36 **Linear Technology Corporation**
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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