**CY7C1354B**

**CY7C1356B**

# 9-Mb (256K x 36/512K x 18) Pipelined SRAM with NoBL™ Architecture

## Features

- **Pin-compatible and functionally equivalent to ZBT**
- **Supports 225-MHz bus operations with zero wait states**
  - **— Available speed grades are 225, 200, and 166 MHz**
- **Internally self-timed output buffer control to eliminate the need to use asynchronous OE**
- **Fully registered (inputs and outputs) for pipelined operation**
- **Byte Write capability**
- **Separate $V_{DDQ}$ for 3.3V or 2.5V I/O**
- **Single 3.3V power supply**
- **Fast clock-to-output times**
  - **— 2.8 ns (for 225-MHz device)**
  - **— 3.2ns (for 200-MHz device)**
  - **— 3.5 ns (for 166-MHz device)**
- **Clock Enable ($\overline{CEN}$) pin to suspend operation**
- **Synchronous self-timed writes**
- **Available in 100 TQFP, 119 BGA, and 165 fBGA packages**
- **IEEE 1149.1 JTAG Boundary Scan**
- **Burst capability–linear or interleaved burst order**
- **"ZZ" Sleep Mode option and Stop Clock option**

## Functional Description

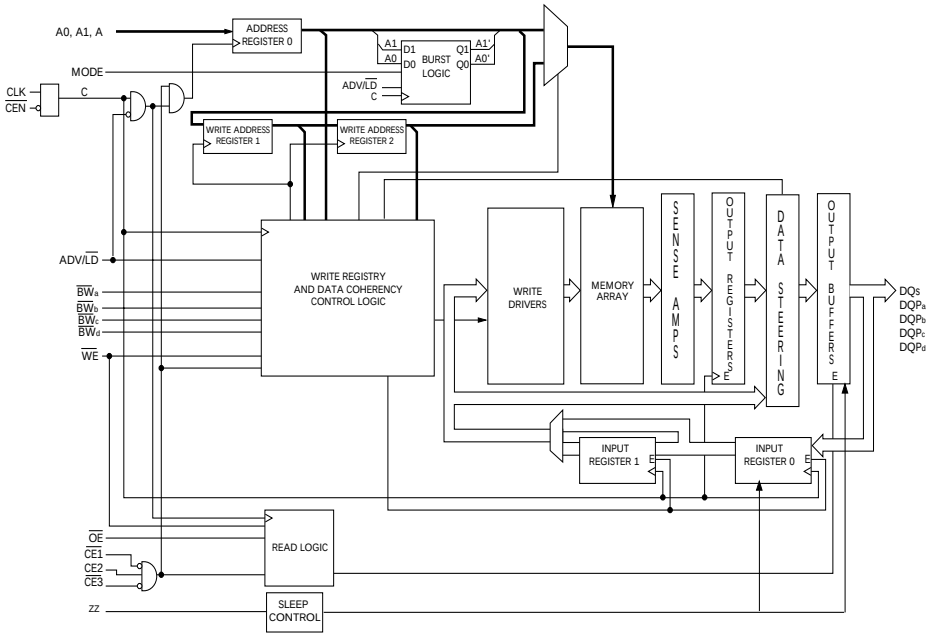
The CY7C1354B and CY7C1356B are 3.3V, 256K x 36 and 512K x 18 Synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back Read/Write operations with no wait states. The CY7C1354B and CY7C1356B are equipped with the advanced (NoBL) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent Write/Read transitions. The CY7C1354B and CY7C1356B are pin compatible and functionally equivalent to ZBT devices.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle.

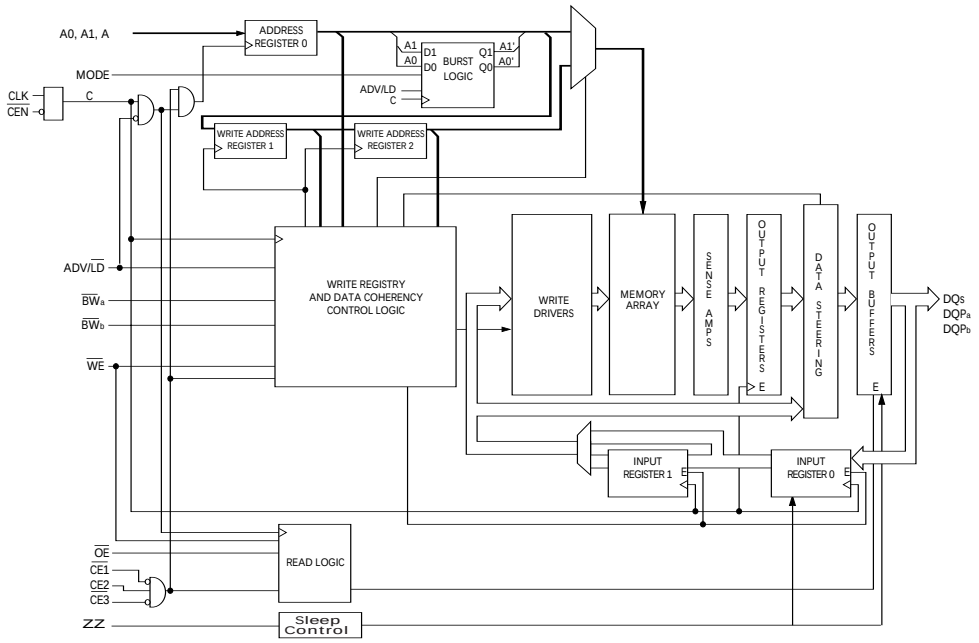
Write operations are controlled by the Byte Write Selects ($\overline{BW_a}$–$\overline{BW_d}$ for CY7C1354B and $\overline{BW_a}$–$\overline{BW_b}$ for CY7C1356B) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, $CE_2$, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to avoid bus contention, the output drivers are synchronously three-stated during the data portion of a write sequence.

## Logic Block Diagram-CY7C1354B (256K x 36)



## Logic Block Diagram-CY7C1356B (512K x 18)



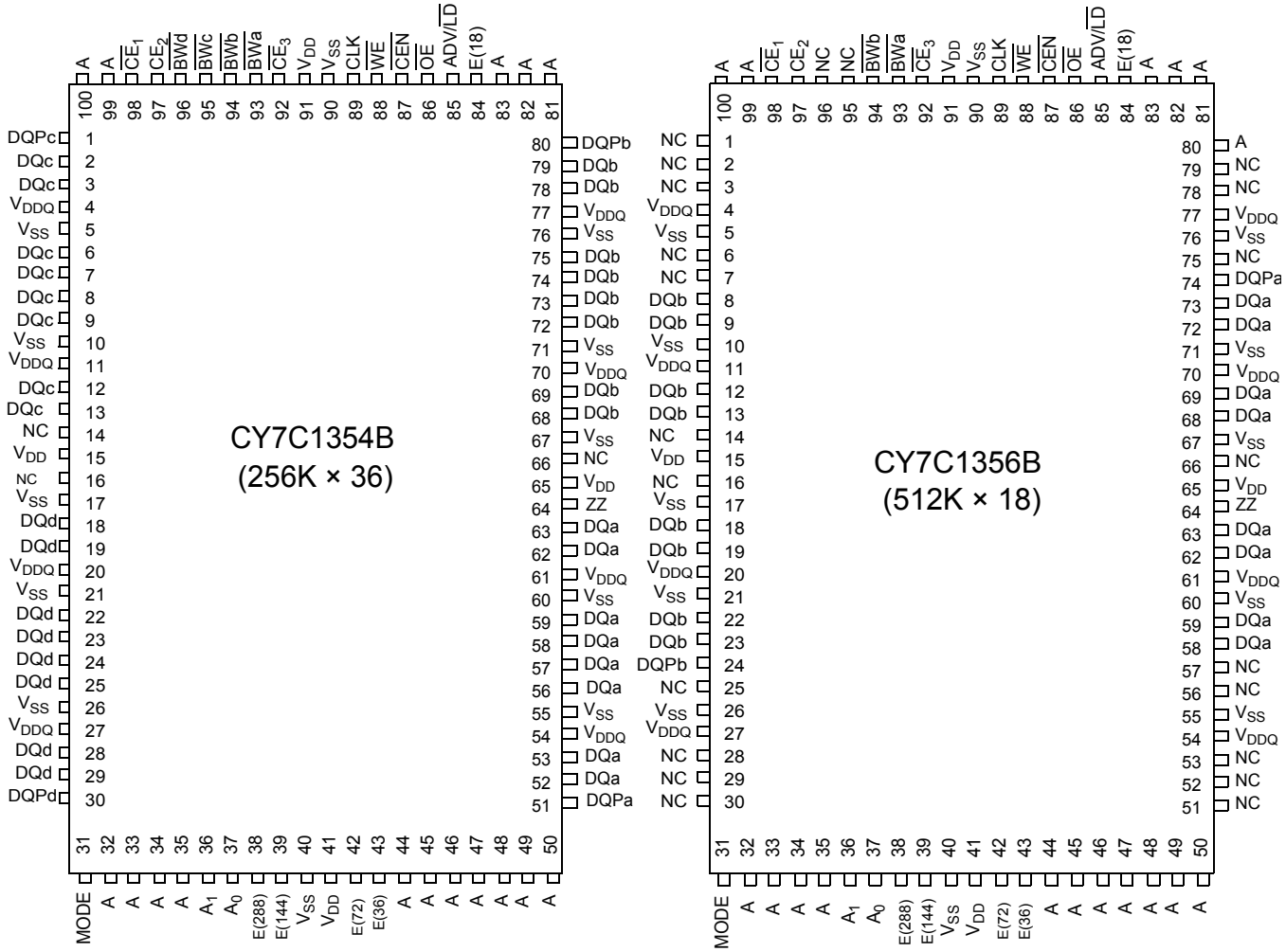

## Selection Guide

| | CY7C1354B-225<br>CY7C1356B-225 | CY7C1354B-200<br>CY7C1356B-200 | CY7C1354B-166<br>CY7C1356B-166 | Unit |
|---|---|---|---|---|
| Maximum Access Time | 2.8 | 3.2 | 3.5 | ns |
| Maximum Operating Current | 250 | 220 | 180 | mA |
| Maximum CMOS Standby Current | 35 | 35 | 35 | mA |

Shaded areas contain advance information.
Please contact your local Cypress sales representative for availability of these parts.

## Pin Configurations

**100-pin TQFP Packages**



**Pin Configurations** (continued)

**119-ball BGA Pinout**
**CY7C1354B (256K × 36) – 14 × 22 BGA**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | A | A | E(18) | A | A | $V_{DDQ}$ |
| **B** | NC | $CE_2$ | A | ADV/$\overline{LD}$ | A | $\overline{CE_3}$ | NC |
| **C** | NC | A | A | $V_{DD}$ | A | A | NC |
| **D** | $DQ_c$ | $DQP_c$ | $V_{SS}$ | NC | $V_{SS}$ | $DQP_b$ | $DQ_b$ |
| **E** | $DQ_c$ | $DQ_c$ | $V_{SS}$ | $\overline{CE_1}$ | $V_{SS}$ | $DQ_b$ | $DQ_b$ |
| **F** | $V_{DDQ}$ | $DQ_c$ | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | $DQ_b$ | $V_{DDQ}$ |
| **G** | $DQ_c$ | $DQ_c$ | $\overline{BW_c}$ | A | $\overline{BW_b}$ | $DQ_b$ | $DQ_b$ |
| **H** | $DQ_c$ | $DQ_c$ | $V_{SS}$ | $\overline{WE}$ | $V_{SS}$ | $DQ_b$ | $DQ_b$ |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | $DQ_d$ | $DQ_d$ | $V_{SS}$ | CLK | $V_{SS}$ | $DQ_a$ | $DQ_a$ |
| **L** | $DQ_d$ | $DQ_d$ | $\overline{BW_d}$ | NC | $\overline{BW_a}$ | $DQ_a$ | $DQ_a$ |
| **M** | $V_{DDQ}$ | $DQ_d$ | $V_{SS}$ | $\overline{CEN}$ | $V_{SS}$ | $DQ_a$ | $V_{DDQ}$ |
| **N** | $DQ_d$ | $DQ_d$ | $V_{SS}$ | A1 | $V_{SS}$ | $DQ_a$ | $DQ_a$ |
| **P** | $DQ_d$ | $DQP_d$ | $V_{SS}$ | A0 | $V_{SS}$ | $DQP_a$ | $DQ_a$ |
| **R** | NC | A | MODE | $V_{DD}$ | NC | A | NC |
| **T** | NC | E(72) | A | A | A | E(36) | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**CY7C1356B (512K x 18)–14 x 22 BGA**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| **A** | $V_{DDQ}$ | A | A | E(18) | A | A | $V_{DDQ}$ |
| **B** | NC | $CE_2$ | A | ADV/$\overline{LD}$ | A | $\overline{CE_3}$ | NC |
| **C** | NC | A | A | $V_{DD}$ | A | A | NC |
| **D** | $DQ_b$ | NC | $V_{SS}$ | NC | $V_{SS}$ | $DQP_a$ | NC |
| **E** | NC | $DQ_b$ | $V_{SS}$ | $\overline{CE_1}$ | $V_{SS}$ | NC | $DQ_a$ |
| **F** | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{OE}$ | $V_{SS}$ | $DQ_a$ | $V_{DDQ}$ |
| **G** | NC | $DQ_b$ | $\overline{BW_b}$ | A | $V_{SS}$ | NC | $DQ_a$ |
| **H** | $DQ_b$ | NC | $V_{SS}$ | $\overline{WE}$ | $V_{SS}$ | $DQ_a$ | NC |
| **J** | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| **K** | NC | $DQ_b$ | $V_{SS}$ | CLK | $V_{SS}$ | NC | $DQ_a$ |
| **L** | $DQ_b$ | NC | $V_{SS}$ | NC | $\overline{BW_a}$ | $DQ_a$ | NC |
| **M** | $V_{DDQ}$ | $DQ_b$ | $V_{SS}$ | $\overline{CEN}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| **N** | $DQ_b$ | NC | $V_{SS}$ | A1 | $V_{SS}$ | $DQ_a$ | NC |
| **P** | NC | $DQP_b$ | $V_{SS}$ | A0 | $V_{SS}$ | NC | $DQ_a$ |
| **R** | NC | A | MODE | $V_{DD}$ | NC | A | NC |
| **T** | E(72) | A | A | E(36) | A | A | ZZ |
| **U** | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

**Pin Configurations** (continued)

**165-Ball fBGA Pinout**

**CY7C1354B (256K × 36) – 13 × 15 fBGA**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | E(288) | A | $\overline{CE}_1$ | $\overline{BW}_c$ | $\overline{BW}_b$ | $\overline{CE}_3$ | $\overline{CEN}$ | ADV/$\overline{LD}$ | A | A | NC |
| **B** | NC | A | CE2 | $\overline{BW}_d$ | $\overline{BW}_a$ | CLK | $\overline{WE}$ | $\overline{OE}$ | E(18) | A | E(144) |
| **C** | $DQP_c$ | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_b$ |
| **D** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **E** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **F** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **G** | $DQ_c$ | $DQ_c$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_b$ | $DQ_b$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **K** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **L** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **M** | $DQ_d$ | $DQ_d$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | $DQ_a$ |
| **N** | $DQP_d$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | NC | NC | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_a$ |
| **P** | NC | E(72) | A | A | TDI | A1 | TDO | A | A | A | NC |
| **R** | MODE | E(36) | A | A | TMS | A0 | TCK | A | A | A | A |

**CY7C1356B (512K × 18) – 13 × 15 fBGA**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | E(288) | A | $\overline{CE}_1$ | $\overline{BW}_b$ | NC | $\overline{CE}_3$ | $\overline{CEN}$ | ADV/$\overline{LD}$ | A | A | A |
| **B** | NC | A | CE2 | NC | $\overline{BW}_a$ | CLK | $\overline{WE}$ | $\overline{OE}$ | E(18) | A | E(144) |
| **C** | NC | NC | $V_{DDQ}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DDQ}$ | NC | $DQP_a$ |
| **D** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **E** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **F** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **G** | NC | $DQ_b$ | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | NC | $DQ_a$ |
| **H** | NC | NC | NC | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | NC | NC | ZZ |
| **J** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **K** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **L** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **M** | $DQ_b$ | NC | $V_{DDQ}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DDQ}$ | $DQ_a$ | NC |
| **N** | $DQP_b$ | NC | $V_{DDQ}$ | $V_{SS}$ | NC | NC | NC | $V_{SS}$ | $V_{DDQ}$ | NC | NC |
| **P** | NC | E(72) | A | A | TDI | A1 | TDO | A | A | A | NC |
| **R** | MODE | E(36) | A | A | TMS | A0 | TCK | A | A | A | A |

## Pin Definitions

| Pin Name | I/O Type | Pin Description |
|---|---|---|
| A0<br>A1<br>A | Input-Synchronous | **Address Inputs used to select one of the address locations**. Sampled at the rising edge of the CLK. |
| $\overline{BW_a}$<br>$\overline{BW_b}$<br>$\overline{BW_c}$<br>$\overline{BW_d}$ | Input-Synchronous | **Byte Write Select Inputs, active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW_a}$ controls $DQ_a$ and $DQP_a$, $\overline{BW_b}$ controls $DQ_b$ and $DQP_b$, $\overline{BW_c}$ controls $DQ_c$ and $DQP_c$, $\overline{BW_d}$ controls $DQ_d$ and $DQP_d$. |
| $\overline{WE}$ | Input-Synchronous | **Write Enable Input, active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence. |
| $\overline{ADV/LD}$ | Input-Synchronous | **Advance/Load Input used to advance the on-chip address counter or load a new address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ should be driven LOW in order to load a new address. |
| CLK | Input-Clock | **Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW. |
| $\overline{CE_1}$ | Input-Synchronous | **Chip Enable 1 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $CE_2$ and $\overline{CE_3}$ to select/deselect the device. |
| $CE_2$ | Input-Synchronous | **Chip Enable 2 Input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device. |
| $\overline{CE_3}$ | Input-Synchronous | **Chip Enable 3 Input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $CE_2$ to select/deselect the device. |
| $\overline{OE}$ | Input-Asynchronous | **Output Enable, active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a Write sequence, during the first clock when emerging from a deselected state and when the device has been deselected. |
| $\overline{CEN}$ | Input-Synchronous | **Clock Enable Input, active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required. |
| $DQ_a$<br>$DQ_b$<br>$DQ_c$<br>$DQ_d$ | I/O-Synchronous | **Bidirectional Data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by addresses during the previous clock rise of the Read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, $DQ_a$–$DQ_d$ are placed in a three-state condition. The outputs are automatically three-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$. |
| $DQP_a$<br>$DQP_b$<br>$DQP_c$<br>$DQP_d$ | I/O-Synchronous | **Bidirectional Data Parity I/O lines**. Functionally, these signals are identical to $DQ_{[a:d]}$. During write sequences, DQPa is controlled by BWa, DQPb is controlled by BWb, DQPc is controlled by BWc, and DQPd is controlled by BWd. |
| MODE | Input Strap Pin | **Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order. |
| TDO | JTAG serial output Synchronous | **Serial data-out to the JTAG circuit**. Delivers data on the negative edge of TCK. |
| TDI | JTAG serial input Synchronous | **Serial data-In to the JTAG circuit**. Sampled on the rising edge of TCK. |
| TMS | Test Mode Select Synchronous | **This pin controls the Test Access Port state machine**. Sampled on the rising edge of TCK. |
| TCK | JTAG-Clock | **Clock input to the JTAG circuitry**. |
| $V_{DD}$ | Power Supply | **Power supply inputs to the core of the device**. |
| $V_{DDQ}$ | I/O Power Supply | **Power supply for the I/O circuitry**. |
| $V_{SS}$ | Ground | **Ground for the device**. Should be connected to ground of the system. |

## Pin Definitions (continued)

| Pin Name | I/O Type | Pin Description |
|---|---|---|
| NC | – | **No connects**. This pin is not connected to the die. |
| E(18,36, 72, 144, 288) | – | **These pins are not connected**. They will be used for expansion to the 18M, 36M, 72M, 144M and 288M densities. |
| ZZ | Input-Asynchronous | **ZZ "sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin can be connected to $V_{SS}$ or left floating. |

## Introduction

### Functional Overview

The CY7C1354B and CY7C1356B are synchronous-pipelined Burst NoBL SRAMs designed specifically to eliminate wait states during Write/Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal ($\overline{CEN}$). If $\overline{CEN}$ is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with $\overline{CEN}$. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ($t_{CO}$) is 2.8 ns (225-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE_1}$, $CE_2$, $\overline{CE_3}$) active at the rising edge of the clock. If Clock Enable ($\overline{CEN}$) is active LOW and ADV/$\overline{LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a Read or Write operation, depending on the status of the Write Enable ($\overline{WE}$). $BW_{[d:a]}$ can be used to conduct Byte Write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All Writes are simplified with on-chip synchronous self-timed Write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, $CE_2$, $\overline{CE_3}$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (Reads, Writes, and Deselects) are pipelined. ADV/$\overline{LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

*Single Read Accesses*

A read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$ are ALL asserted active, (3) the Write Enable input signal $\overline{WE}$ is deasserted HIGH, and (4) ADV/$\overline{LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 2.8 ns (225-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (Read/Write/Deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will three-state following the next clock rise.

*Burst Read Accesses*

The CY7C1354B and CY7C1356B have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four Reads without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the Single Read Access section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap around when incremented sufficiently. A HIGH input on ADV/$\overline{LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (Read or Write) is maintained throughout the burst sequence.

*Single Write Accesses*

Write access are initiated when the following conditions are satisfied at clock rise: (1) $\overline{CEN}$ is asserted LOW, (2) $\overline{CE_1}$, $CE_2$, and $\overline{CE_3}$ are ALL asserted active, and (3) the Write signal $\overline{WE}$ is asserted LOW. The address presented to $A_0 \angle A_{16}$ is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically three-stated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354B and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356B). In addition, the address for the subsequent access (Read/Write/Deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354B and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356B) (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the Write is complete.

The data written during the Write operation is controlled by $\overline{BW}$ ($\overline{BW_{a,b,c,d}}$ for CY7C1354B and $\overline{BW_{a,b}}$ for CY7C1356B) signals. The CY7C1354B/56B provides Byte Write capability that is described in the Write Cycle Description table. Asserting the Write Enable input ($\overline{WE}$) with the selected Byte Write Select ($\overline{BW}$) input will selectively write to only the desired bytes. Bytes not selected during a Byte Write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the Write operations. Byte Write capability has been included in order to greatly simplify

Read/Modify/Write sequences, which can be reduced to simple Byte Write operations.

Because the CY7C1354B and CY7C1356B are common I/O devices, data should not be driven into the device while the outputs are active. The Output Enable (OE) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354B and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356B) inputs. Doing so will three-state the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1354B and $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1356B) are automatically three-stated during the data portion of a write cycle, regardless of the state of OE.

*Burst Write Accesses*

The CY7C1354B/56B has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four WRITE operations without reasserting the address inputs. ADV/LD must be driven LOW in order to load the initial address, as described in the Single Write Access section above. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables ($CE_1$, $CE_2$, and $CE_3$) and WE inputs are ignored and the burst counter is incremented. The correct BW ($BW_{a,b,c,d}$ for CY7C1354B and $BW_{a,b}$ for CY7C1356B) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

*Sleep Mode*

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $CE_1$, $CE_2$, and $CE_3$, must remain inactive for the duration of $t_{ZZREC}$ after the ZZ input returns LOW.

## Interleaved Burst Address Table (MODE = Floating or $V_{DD}$)

| First Address | Second Address | Third Address | Fourth Address |
|---|---|---|---|
| A1,A0 | A1,A0 | A1,A0 | A1,A0 |
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

## Linear Burst Address Table (MODE = GND)

| First Address | Second Address | Third Address | Fourth Address |
|---|---|---|---|
| A1,A0 | A1,A0 | A1,A0 | A1,A0 |
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

## ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min. | Max | Unit |
|---|---|---|---|---|---|
| $I_{DDZZ}$ | Sleep mode standby current | ZZ $\geq V_{DD} - 0.2V$ | | 35 | mA |
| $t_{ZZS}$ | Device operation to ZZ | ZZ $\geq V_{DD} - 0.2V$ | | $2t_{CYC}$ | ns |
| $t_{ZZREC}$ | ZZ recovery time | ZZ $\leq 0.2V$ | $2t_{CYC}$ | | ns |
| $t_{ZZI}$ | ZZ active to sleep current | This parameter is sampled | | $2t_{CYC}$ | ns |
| $t_{RZZI}$ | ZZ Inactive to exit sleep current | This parameter is sampled | 0 | | ns |

## Truth Table[1, 2, 3, 4, 5, 6, 7]

| Operation | Address Used | $\overline{CE}$ | ZZ | $\overline{ADV/LD}$ | $\overline{WE}$ | $\overline{BWx}$ | $\overline{OE}$ | $\overline{CEN}$ | CLK | DQ |
|---|---|---|---|---|---|---|---|---|---|---|
| Deselect Cycle | None | H | L | L | X | X | X | L | L-H | Three-State |
| Continue Deselect Cycle | None | X | L | H | X | X | X | L | L-H | Three-State |
| Read Cycle (Begin Burst) | External | L | L | L | H | X | L | L | L-H | Data Out (Q) |
| Read Cycle (Continue Burst) | Next | X | L | H | X | X | L | L | L-H | Data Out (Q) |
| NOP/Dummy Read (Begin Burst) | External | L | L | L | H | X | H | L | L-H | Three-State |
| Dummy Read (Continue Burst) | Next | X | L | H | X | X | H | L | L-H | Three-State |
| Write Cycle (Begin Burst) | External | L | L | L | L | L | X | L | L-H | Data In (D) |
| Write Cycle (Continue Burst) | Next | X | L | H | X | L | X | L | L-H | Data In (D) |
| NOP/WRITE ABORT (Begin Burst) | None | L | L | L | L | H | X | L | L-H | Three-State |
| WRITE ABORT (Continue Burst) | Next | X | L | H | X | H | X | L | L-H | Three-State |
| IGNORE CLOCK EDGE (Stall) | Current | X | L | X | X | X | X | H | L-H | - |
| Sleep MODE | None | X | H | X | X | X | X | X | X | Three-State |

**Notes:**
1. X = "Don't Care", 1 = Logic HIGH, 0 = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BW}$x = 0 signifies at least one Byte Write Select is active, $\overline{BW}$x = Valid signifies that the desired Byte Write Selects are asserted, see Write Cycle Description table for details.
2. Write is defined by $\overline{WE}$ and $\overline{BW}_{[a:d]}$. See Write Cycle Description table for details.
3. When a write cycle is detected, all I/Os are three-stated, even during Byte Writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal.
5. $\overline{CEN}$ = H inserts wait states.
6. Device will power-up deselected and the I/Os in a three-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and $DQP_{[a:d]}$ = Three-state when $\overline{OE}$ is inactive or when the device is deselected, and DQs = data when $\overline{OE}$ is active.

## Partial Write Cycle Description[1, 2, 3, 8]

| Function (CY7C1354B) | $\overline{WE}$ | $\overline{BW_d}$ | $\overline{BW_c}$ | $\overline{BW_b}$ | $\overline{BW_a}$ |
|---|---|---|---|---|---|
| Read | H | X | X | X | X |
| Write –No bytes written | L | H | H | H | H |
| Write Byte a– ($DQ_a$ and $DQP_{a)}$ | L | H | H | H | L |
| Write Byte b – ($DQ_b$ and $DQP_{b)}$ | L | H | H | L | H |
| Write Bytes b, a | L | H | H | L | L |
| Write Byte c – ($DQ_c$ and $DQP_{c)}$ | L | H | L | H | H |
| Write Bytes c, a | L | H | L | H | L |
| Write Bytes c, b | L | H | L | L | H |
| Write Bytes c, b, a | L | H | L | L | L |
| Write Byte d – ($DQ_d$ and $DQP_{d)}$ | L | L | H | H | H |
| Write Bytes d, a | L | L | H | H | L |
| Write Bytes d, b | L | L | H | L | H |
| Write Bytes d, b, a | L | L | H | L | L |
| Write Bytes d, c | L | L | L | H | H |
| Write Bytes d, c, a | L | L | L | H | L |
| Write Bytes d, c, b | L | L | L | L | H |
| Write All Bytes | L | L | L | L | L |

**Note:**
8. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_{[a:d]}$ is valid. Appropriate write will be done based on which byte write is active.

| Function (CY7C1356B) | $\overline{WE}$ | $\overline{BW_b}$ | $\overline{BW_a}$ |
|---|---|---|---|
| Read | H | x | x |
| Write – No Bytes Written | L | H | H |
| Write Byte a – ($DQ_a$ and $DQP_{a)}$ | L | H | L |
| Write Byte b – ($DQ_b$ and $DQP_{b)}$ | L | L | H |
| Write Both Bytes | L | L | L |

## IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1354B/CY7C1354B incorporates a serial boundary scan Test Access Port (TAP) in the BGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 3.3V I/O logic levels.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ($V_{SS}$) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to $V_{DD}$ through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

### Test Access Port–Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

### Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

### Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

### Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State

Diagram). The output changes on the falling edge of TCK. TDO is connected to the Least Significant Bit (LSB) of any register.

### Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ($V_{DD}$) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

### TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

#### *Instruction Register*

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

#### *Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ($V_{SS}$) when the BYPASS instruction is executed.

#### *Boundary Scan Register*

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The ×36 configuration has a 69-bit-long register, and the ×18 configuration has a 69-bit-long register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

#### *Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

### TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data, or control signals into the SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the Inputs and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

#### *EXTEST*

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

#### *IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

#### *SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

#### *SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times ($t_{CS}$ and $t_{CH}$). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and $\overline{CK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

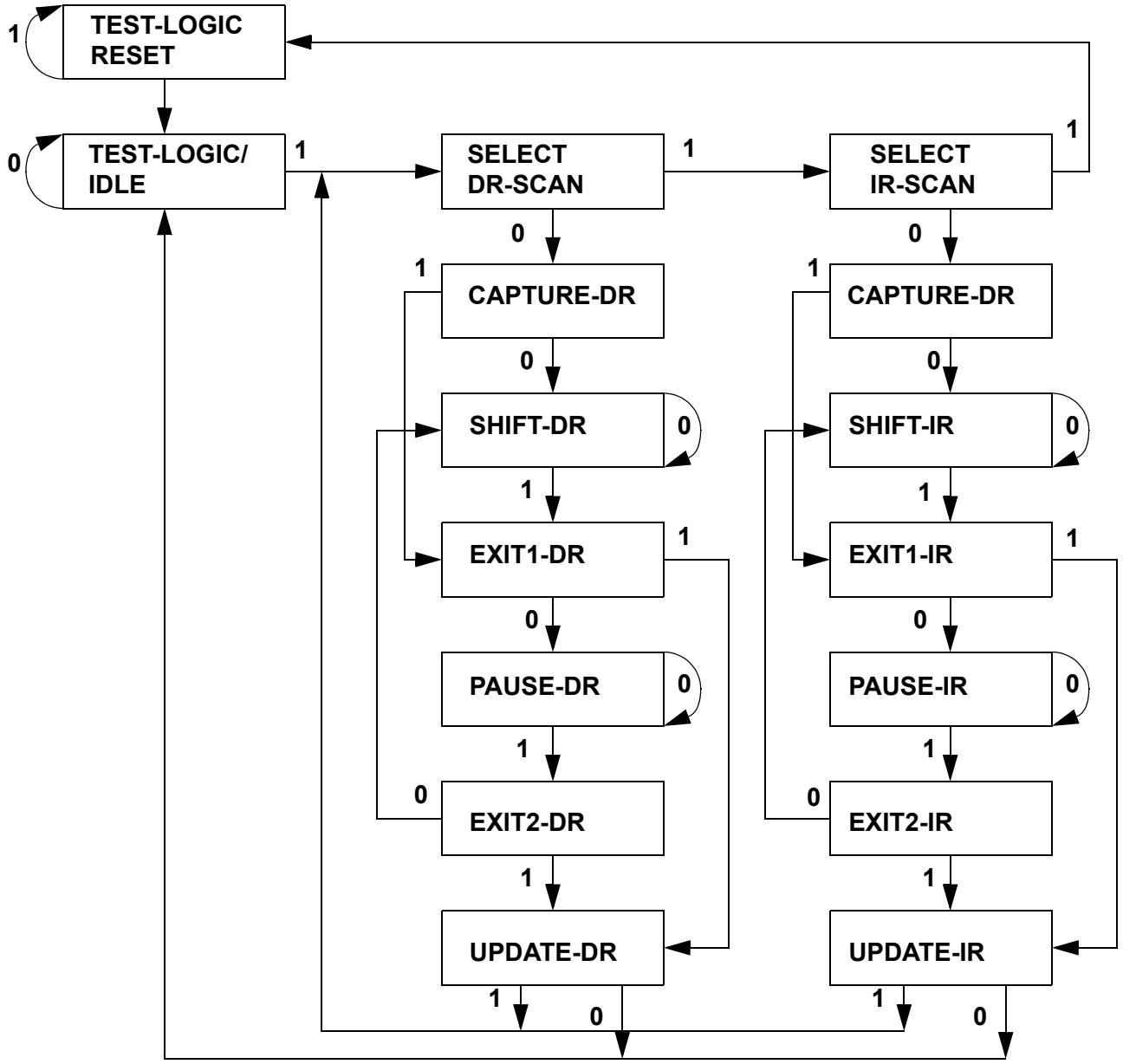
*Bypass*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

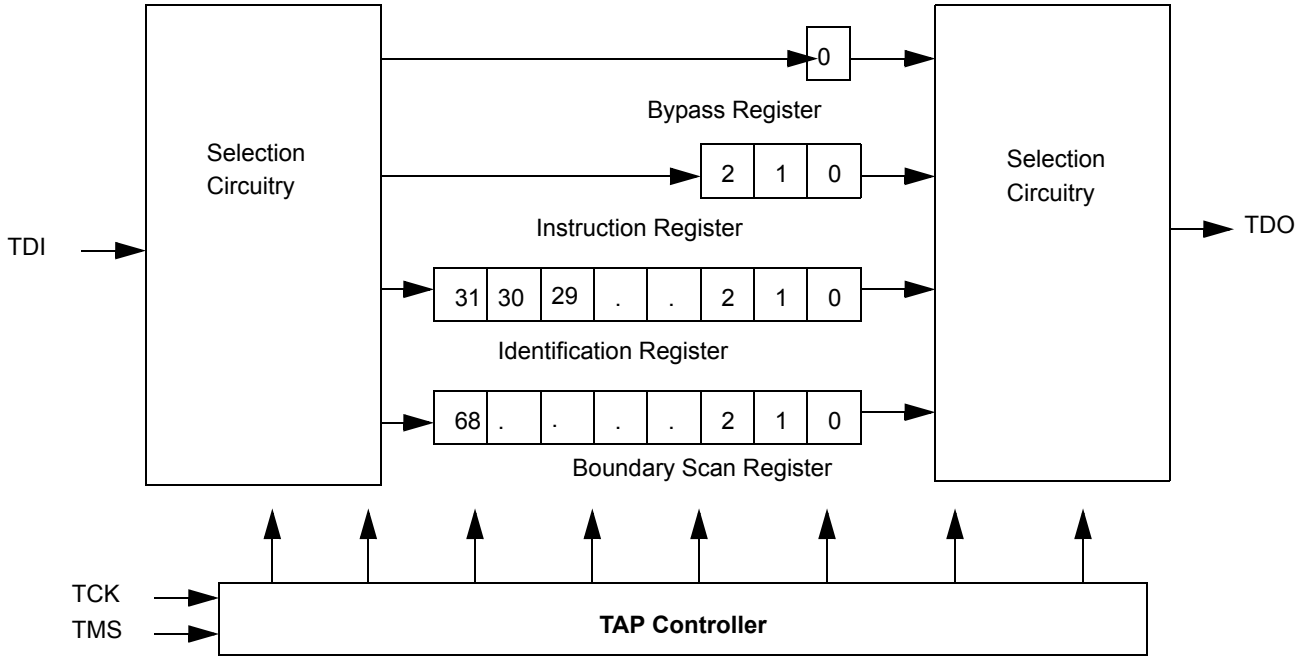
*Reserved*

These instructions are not implemented but are reserved for future use. Do not use these instructions.

**TAP Controller State Diagram**




**Note:**
9. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.




## TAP Electrical Characteristics Over the Operating Range[10, 11]

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH1}$ | Output HIGH Voltage | $I_{OH}$ = 2.0 mA, $V_{DDQ}$ = 3.3V | 2.0 | | V |
| | | $I_{OH}$ = 2.0 mA, $V_{DDQ}$ = 2.5V | 1.7 | | V |
| $V_{OH2}$ | Output HIGH Voltage | $I_{OH}$ = 100 µA, $V_{DDQ}$ = 3.3V | 2.0 | | V |
| | | $I_{OH}$ = 100 µA, $V_{DDQ}$ = 2.5V | 2.0 | | V |
| $V_{OL1}$ | Output LOW Voltage | $I_{OL}$ = 2.0 mA | | 0.7 | V |
| $V_{OL2}$ | Output LOW Voltage | $I_{OL}$ = 100 µA | | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | 1.7 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | –0.3 | 0.7 | V |
| $I_X$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{DDQ}$ | –30 | 30 | µA |
| $I_X$ | Input Load Current TMS and TDI | GND ≤ $V_I$ ≤ $V_{DDQ}$ | –30 | 30 | µA |

## TAP AC Switching Characteristics Over the Operating Range [12, 13]

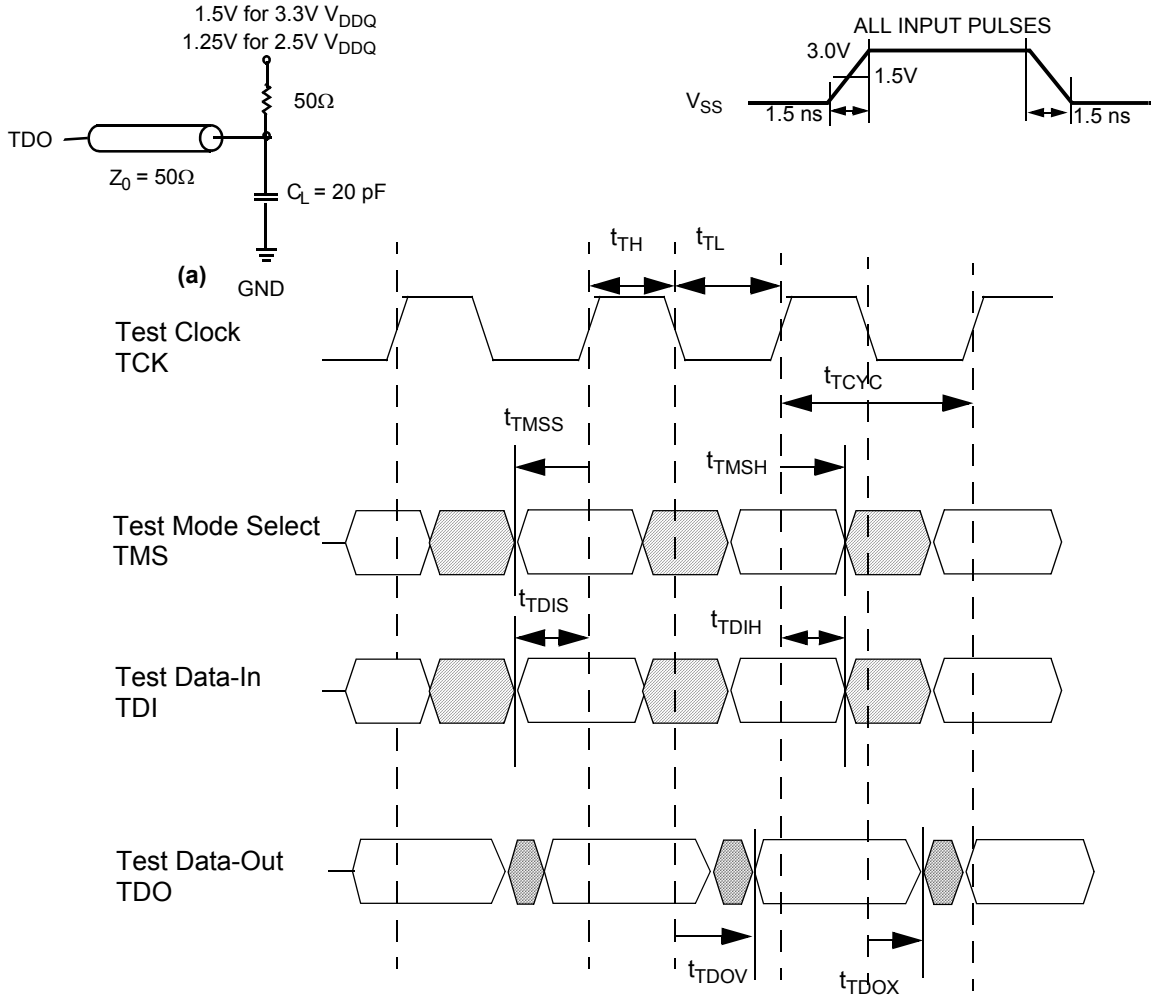
| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{TCYC}$ | TCK Clock Cycle Time | 100 | | ns |
| $t_{TF}$ | TCK Clock Frequency | | 10 | MHz |
| $t_{TH}$ | TCK Clock HIGH | 40 | | ns |
| $t_{TL}$ | TCK Clock LOW | 40 | | ns |
| **Set-up Times** | | | | |
| $t_{TMSS}$ | TMS Set-up to TCK Clock Rise | 10 | | ns |
| $t_{TDIS}$ | TDI Set-up to TCK Clock Rise | 10 | | ns |
| $t_{CS}$ | Capture Set-up to TCK Rise | 10 | | ns |

**Notes:**
10. All voltage referenced to ground.
11. Overshoot: $V_{IH}(AC) \le V_{DD} + 1.5V$ for $t \le t_{TCYC}/2$; undershoot: $V_{IL}(AC) \ge -0.5V$ for $t \le t_{TCYC}/2$.
12. $t_{CS}$ and $t_{CH}$ refer to the set-up and hold time requirements of latching data from the boundary scan register.
13. Test conditions are specified using the load in TAP AC test conditions. $t_R/t_F$ = 1 ns.

## TAP AC Switching Characteristics Over the Operating Range (continued)[12, 13]

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| **Hold Times** | | | | |
| $t_{TMSH}$ | TMS Hold after TCK Clock Rise | 10 | | ns |
| $t_{TDIH}$ | TDI Hold after Clock Rise | 10 | | ns |
| $t_{CH}$ | Capture Hold after clock rise | 10 | | ns |
| **Output Times** | | | | |
| $t_{TDOV}$ | TCK Clock LOW to TDO Valid | | 20 | ns |
| $t_{TDOX}$ | TCK Clock LOW to TDO Invalid | 0 | | ns |

## TAP Timing and Test Conditions




## Identification Register Definitions

| Instruction Field | CY7C1354B | CY7C1356B | Description |
|---|---|---|---|
| Revision Number (31:29) | 001 | 001 | Reserved for version number. |
| Cypress Device ID (28:12) | 01010001000100110 | 01010001000010110 | Reserved for future use. |
| Cypress JEDEC ID (11:1) | 00000110100 | 00000110100 | Allows unique identification of SRAM vendor. |
| ID Register Presence (0) | 1 | 1 | Indicate the presence of an ID register. |

## Scan Register Sizes

| Register Name | Bit Size |
|---|---|
| Instruction | 3 |
| Bypass | 1 |
| ID | 32 |
| Boundary Scan | 69 |

## Identification Codes

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant. |
| IDCODE | 001 | Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation. |
| SAMPLE Z | 010 | Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state. |
| RESERVED | 011 | Do Not Use: This instruction is reserved for future use. |
| SAMPLE/PRELOAD | 100 | Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant. |
| RESERVED | 101 | Do Not Use: This instruction is reserved for future use. |
| RESERVED | 110 | Do Not Use: This instruction is reserved for future use. |
| BYPASS | 111 | Places the bypass register between TDI and TDO. This operation does not affect SRAM operation. |

## Boundary Scan Exit Order (×36)

| Bit # | 119-Ball ID | 165-Ball ID |
|---|---|---|
| 1 | K4 | B6 |
| 2 | H4 | B7 |
| 3 | M4 | A7 |
| 4 | F4 | B8 |
| 5 | B4 | A8 |
| 6 | G4 | A9 |
| 7 | C3 | B10 |
| 8 | B3 | A10 |
| 9 | D6 | C11 |
| 10 | H7 | E10 |
| 11 | G6 | F10 |
| 12 | E6 | G10 |
| 13 | D7 | D10 |
| 14 | E7 | D11 |
| 15 | F6 | E11 |
| 16 | G7 | F11 |
| 17 | H6 | G11 |
| 18 | T7 | H11 |
| 19 | K7 | J10 |
| 20 | L6 | K10 |
| 21 | N6 | L10 |
| 22 | P7 | M10 |
| 23 | N7 | J11 |

## Boundary Scan Exit Order (×36) (continued)

| Bit # | 119-Ball ID | 165-Ball ID |
|---|---|---|
| 24 | M6 | K11 |
| 25 | L7 | L11 |
| 26 | K6 | M11 |
| 27 | P6 | N11 |
| 28 | T4 | R11 |
| 29 | A3 | R10 |
| 30 | C5 | P10 |
| 31 | B5 | R9 |
| 32 | A5 | P9 |
| 33 | C6 | R8 |
| 34 | A6 | P8 |
| 35 | P4 | R6 |
| 36 | N4 | P6 |
| 37 | R6 | R4 |
| 38 | T5 | P4 |
| 39 | T3 | R3 |
| 40 | R2 | P3 |
| 41 | R3 | R1 |
| 42 | P2 | N1 |
| 43 | P1 | L2 |
| 44 | L2 | K2 |
| 45 | K1 | J2 |
| 46 | N2 | M2 |

## Boundary Scan Exit Order (×36) (continued)

| Bit # | 119-Ball ID | 165-Ball ID |
|---|---|---|
| 47 | N1 | M1 |
| 48 | M2 | L1 |
| 49 | L1 | K1 |
| 50 | K2 | J1 |
| 51 | Not Bonded (Preset to 1) | Not Bonded (Preset to 1) |
| 52 | H1 | G2 |
| 53 | G2 | F2 |
| 54 | E2 | E2 |
| 55 | D1 | D2 |
| 56 | H2 | G1 |
| 57 | G1 | F1 |
| 58 | F2 | E1 |
| 59 | E1 | D1 |
| 60 | D2 | C1 |
| 61 | C2 | B2 |
| 62 | A2 | A2 |
| 63 | E4 | A3 |
| 64 | B2 | B3 |
| 65 | L3 | B4 |
| 66 | G3 | A4 |
| 67 | G5 | A5 |
| 68 | L5 | B5 |
| 69 | B6 | A6 |

## Boundary Scan Exit Order (×18)

| Bit # | 119-Ball ID | 165-Ball ID |
|---|---|---|
| 1 | K4 | B6 |
| 2 | H4 | B7 |
| 3 | M4 | A7 |
| 4 | F4 | B8 |
| 5 | B4 | A8 |
| 6 | G4 | A9 |
| 7 | C3 | B10 |
| 8 | B3 | A10 |
| 9 | T2 | A11 |
| 10 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 11 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 12 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 13 | D6 | C11 |
| 14 | E7 | D11 |
| 15 | F6 | E11 |

## Boundary Scan Exit Order (×18) (continued)

| Bit # | 119-Ball ID | 165-Ball ID |
|---|---|---|
| 16 | G7 | F11 |
| 17 | H6 | G11 |
| 18 | T7 | H11 |
| 19 | K7 | J10 |
| 20 | L6 | K10 |
| 21 | N6 | L10 |
| 22 | P7 | M10 |
| 23 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 24 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 25 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 26 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 27 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 28 | T6 | R11 |
| 29 | A3 | R10 |
| 30 | C5 | P10 |
| 31 | B5 | R9 |
| 32 | A5 | P9 |
| 33 | C6 | R8 |
| 34 | A6 | P8 |
| 35 | P4 | R6 |
| 36 | N4 | P6 |
| 37 | R6 | R4 |
| 38 | T5 | P4 |
| 39 | T3 | R3 |
| 40 | R2 | P3 |
| 41 | R3 | R1 |
| 42 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 43 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 44 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 45 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 46 | P2 | N1 |
| 47 | N1 | M1 |
| 48 | M2 | L1 |
| 49 | L1 | K1 |
| 50 | K2 | J1 |
| 51 | Not Bonded (Preset to 1) | Not Bonded (Preset to 1) |
| 52 | H1 | G2 |

**Boundary Scan Exit Order (×18)** (continued)

| Bit # | 119-Ball ID | 165-Ball ID |
|---|---|---|
| 53 | G2 | F2 |
| 54 | E2 | E2 |
| 55 | D1 | D2 |
| 56 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 57 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 58 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 59 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 60 | Not Bonded (Preset to 0) | Not Bonded (Preset to 0) |
| 61 | C2 | B2 |
| 62 | A2 | A2 |
| 63 | E4 | A3 |
| 64 | B2 | B3 |
| 65 | Not Bonded (Preset to 0 | Not Bonded (Preset to 0) |
| 66 | G3 | Not Bonded (Preset to 0) |
| 67 | Not Bonded (Preset to 0 | A4 |
| 68 | L5 | B5 |
| 69 | B6 | A6 |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on $V_{DD}$ Relative to GND..... –0.5V to +4.6V

DC to Outputs in Three-State..... –0.5V to $V_{DDQ}$ + 0.5V

DC Input Voltage.....–0.5V to $V_{DD}$ + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

## Operating Range

| Range | Ambient Temperature | $V_{DD}$ | $V_{DDQ}$ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 3.3V – 5%/+10% | 2.5V – 5% to $V_{DD}$ |
| Industrial | –40°C to +85°C | | |

## Electrical Characteristics Over the Operating Range[14, 15]

| Parameter | Description | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | | | 3.135 | 3.6 | V |
| $V_{DDQ}$ | I/O Supply Voltage | $V_{DDQ}$ = 3.3V | | 3.135 | $V_{DD}$ | V |
| | | $V_{DDQ}$ = 2.5V | | 2.375 | 2.625 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = –4.0 mA, $V_{DDQ}$ = 3.3V | | 2.4 | | V |
| | | $V_{DD}$ = Min., $I_{OH}$ = –1.0 mA, $V_{DDQ}$ = 2.5V | | 2.0 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$= 8.0 mA, $V_{DDQ}$ = 3.3V | | | 0.4 | V |
| | | $V_{DD}$ = Min., $I_{OL}$= 1.0 mA, $V_{DDQ}$ = 2.5V | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{DDQ}$ = 3.3V | | 2.0 | $V_{DD}$ + 0.3V | V |
| | | $V_{DDQ}$ = 2.5V | | 1.7 | $V_{DD}$ + 0.3V | V |
| $V_{IL}$ | Input LOW Voltage[14] | $V_{DDQ}$ = 3.3V | | –0.3 | 0.8 | V |
| | | $V_{DDQ}$ = 2.5V | | –0.3 | 0.7 | V |
| $I_X$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{DDQ}$ | | –5 | 5 | µA |
| | Input Current of MODE | | | –30 | 30 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{DDQ}$, Output Disabled | | –5 | 5 | µA |
| $I_{DD}$ | $V_{DD}$ Operating Supply | $V_{DD}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{CYC}$ | 4.4-ns cycle, 225 MHz | | 250 | mA |
| | | | 5-ns cycle, 200 MHz | | 220 | mA |
| | | | 6-ns cycle, 166 MHz | | 180 | mA |
| $I_{SB1}$ | Automatic CE Power-down Current—TTL Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ = $1/t_{CYC}$ | All speed grades | | 50 | mA |
| $I_{SB2}$ | Automatic CE Power-down Current—CMOS Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN}$ ≤ 0.3V or $V_{IN}$ ≥ $V_{DDQ}$ – 0.3V, f = 0 | All speed grades | | 35 | mA |
| $I_{SB3}$ | Automatic CE Power-down Current—CMOS Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN}$ ≤ 0.3V or $V_{IN}$ ≥ $V_{DDQ}$ – 0.3V, f = $f_{MAX}$ = $1/t_{CYC}$ | All speed grades | | 50 | mA |
| $I_{SB4}$ | Automatic CE Power-down Current—TTL Inputs | Max. $V_{DD}$, Device Deselected, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = 0 | All speed grades | | 40 | mA |

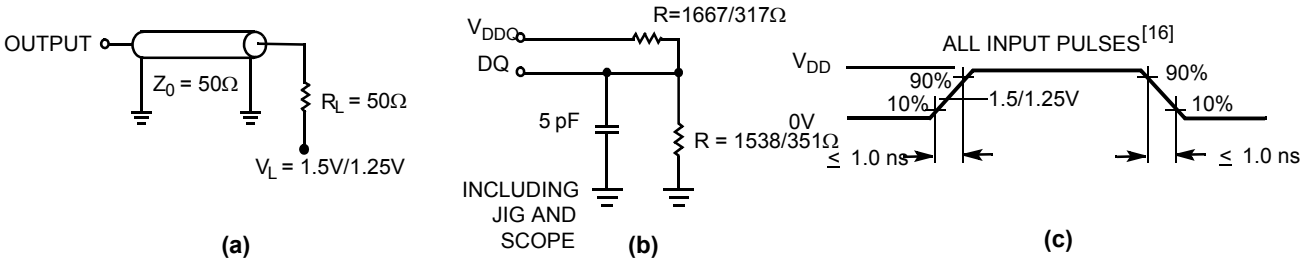
Shaded areas contain advance information.

**Notes:**
14. Overshoot: $V_{IH}(AC) < V_{DD} + 1.5V$ (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL}(AC) > –2V$ (Pulse width less than $t_{CYC}/2$).
15. $T_{Power\text{-}up}$: Assumes a linear ramp from 0V to $V_{DD}$ (min.) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} < V_{DD}$.

## Capacitance[16]

| Parameter | Description | Test Conditions | BGA Max. | fBGA Max. | TQFP Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 3.3V $V_{DDQ}$ = 2.5V | 5 | 5 | 5 | pF |
| $C_{CLK}$ | Clock Input Capacitance | | 5 | 5 | 5 | pF |
| $C_{I/O}$ | Input/Output Capacitance | | 7 | 7 | 5 | pF |

## AC Test Loads and Waveforms




## Thermal Resistance[16]

| Parameters | Description | Test Conditions | BGA Typ. | fBGA Typ. | TQFP Typ. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51. | 25 | 27 | 25 | °C/W | 17 |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 6 | 6 | 9 | °C/W | 17 |

## Switching Characteristics Over the Operating Range [21, 22]

| Parameter | Description | -225 | | -200 | | -166 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{Power}$[17] | $V_{CC}$ (typical) to the First Access Read or Write | 1 | | 1 | | 1 | | ms |
| **Clock** | | | | | | | | |
| $t_{CYC}$ | Clock Cycle Time | 4.4 | | 5 | | 6 | | ns |
| $F_{MAX}$ | Maximum Operating Frequency | | 225 | | 200 | | 166 | MHz |
| $t_{CH}$ | Clock HIGH | 1.8 | | 2.0 | | 2.4 | | ns |
| $t_{CL}$ | Clock LOW | 1.8 | | 2.0 | | 2.4 | | ns |
| **Output Times** | | | | | | | | |
| $t_{CO}$ | Data Output Valid after CLK Rise | | 2.8 | | 3.2 | | 3.5 | ns |
| $t_{EOV}$ | $\overline{OE}$ LOW to Output Valid | | 2.8 | | 3.2 | | 3.5 | ns |
| $t_{DOH}$ | Data Output Hold after CLK Rise | 1.25 | | 1.5 | | 1.5 | | ns |
| $t_{CHZ}$ | Clock to High-Z[18, 19, 20] | 1.25 | 2.8 | 1.5 | 3.2 | 1.5 | 3.5 | ns |
| $t_{CLZ}$ | Clock to Low-Z[18, 19, 20] | 1.25 | | 1.5 | | 1.5 | | ns |
| $t_{EOHZ}$ | $\overline{OE}$ HIGH to Output High-Z[18, 19, 20] | | 2.8 | | 3.2 | | 3.5 | ns |
| $t_{EOLZ}$ | $\overline{OE}$ LOW to Output Low-Z[18, 19, 20] | 0 | | 0 | | 0 | | ns |

Shaded areas contain advance information.

**Notes:**

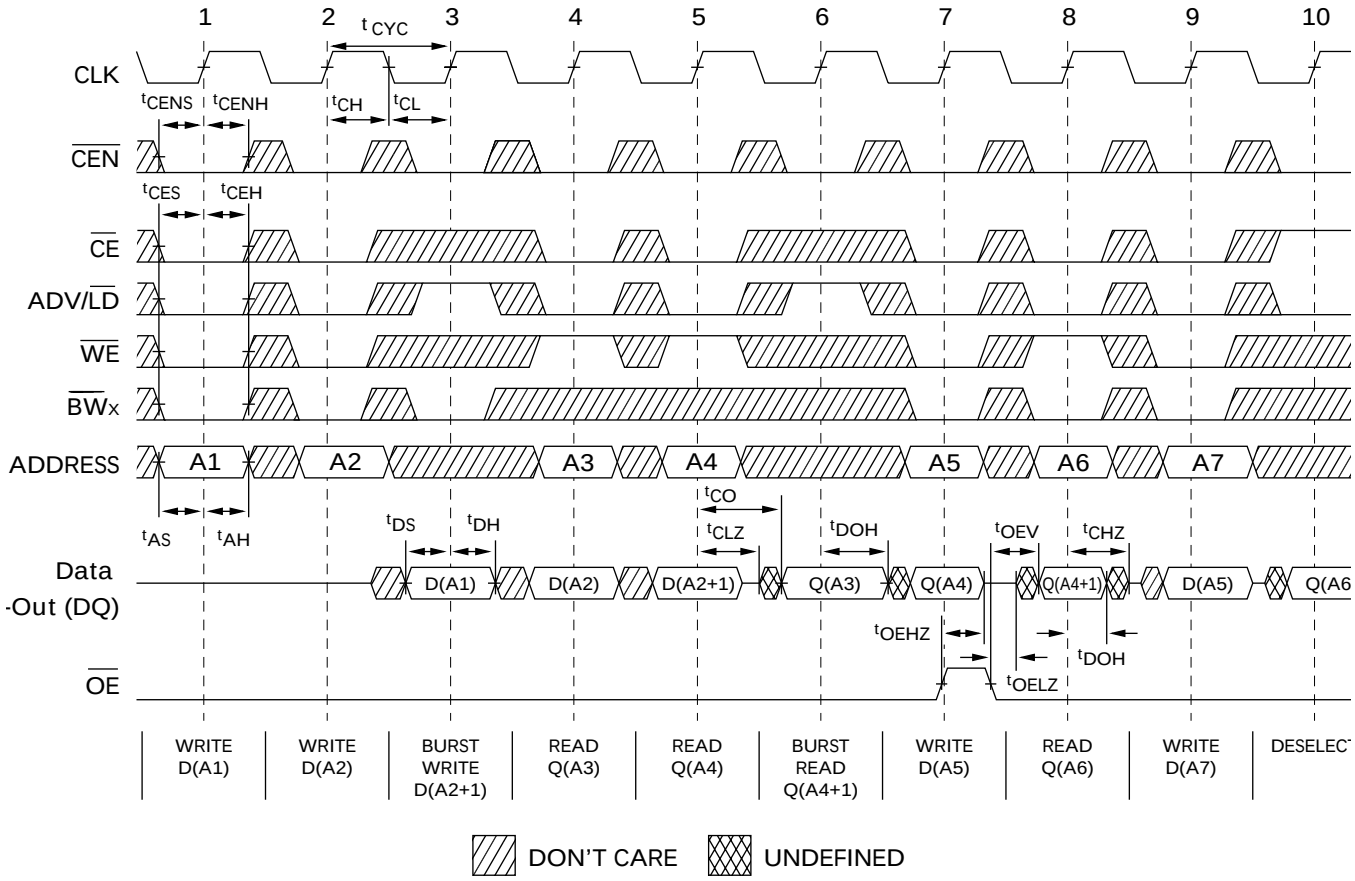
16. Tested initially and after any design or process changes that may affect these parameters.
17. This part has a voltage regulator internally; $t_{power}$ is the time power needs to be supplied above $V_{DD}$ minimum initially, before a Read or Write operation can be initiated.
18. $t_{CHZ}$, $t_{CLZ}$, $t_{EOLZ}$, and $t_{EOHZ}$ are specified with AC test conditions shown in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
19. At any given voltage and temperature, $t_{EOHZ}$ is less than $t_{EOLZ}$ and $t_{CHZ}$ is less than $t_{CLZ}$ to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z prior to Low-Z under the same system conditions.
20. This parameter is sampled and not 100% tested.
21. Timing reference level is 1.5V when $V_{DDQ}$ = 3.3V and is 1.25V when $V_{DDQ}$ = 2.5V.
22. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

**Switching Characteristics** Over the Operating Range (continued)[21, 22]

| Parameter | Description | -225 | | -200 | | -166 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Set-up Times** | | | | | | | | |
| $t_{AS}$ | Address Set-up before CLK Rise | 1.4 | | 1.5 | | 1.5 | | ns |
| $t_{DS}$ | Data Input Set-up before CLK Rise | 1.4 | | 1.5 | | 1.5 | | ns |
| $t_{CENS}$ | $\overline{CEN}$ Set-up before CLK Rise | 1.4 | | 1.5 | | 1.5 | | ns |
| $t_{WES}$ | $\overline{WE}$, $\overline{BW}_x$ Set-up before CLK Rise | 1.4 | | 1.5 | | 1.5 | | ns |
| $t_{ALS}$ | ADV/$\overline{LD}$ Set-up before CLK Rise | 1.4 | | 1.5 | | 1.5 | | ns |
| $t_{CES}$ | Chip Select Set-up | 1.4 | | 1.5 | | 1.5 | | ns |
| $t_{AH}$ | Address Hold after CLK Rise | 0.4 | | 0.5 | | 0.5 | | ns |
| **Hold Times** | | | | | | | | |
| $t_{DH}$ | Data Input Hold after CLK Rise | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{CENH}$ | $\overline{CEN}$ Hold after CLK Rise | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{WEH}$ | $\overline{WE}$, $\overline{BW}_x$ Hold after CLK Rise | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{ALH}$ | ADV/$\overline{LD}$ Hold after CLK Rise | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{CEH}$ | Chip Select Hold after CLK Rise | 0.4 | | 0.5 | | 0.5 | | ns |

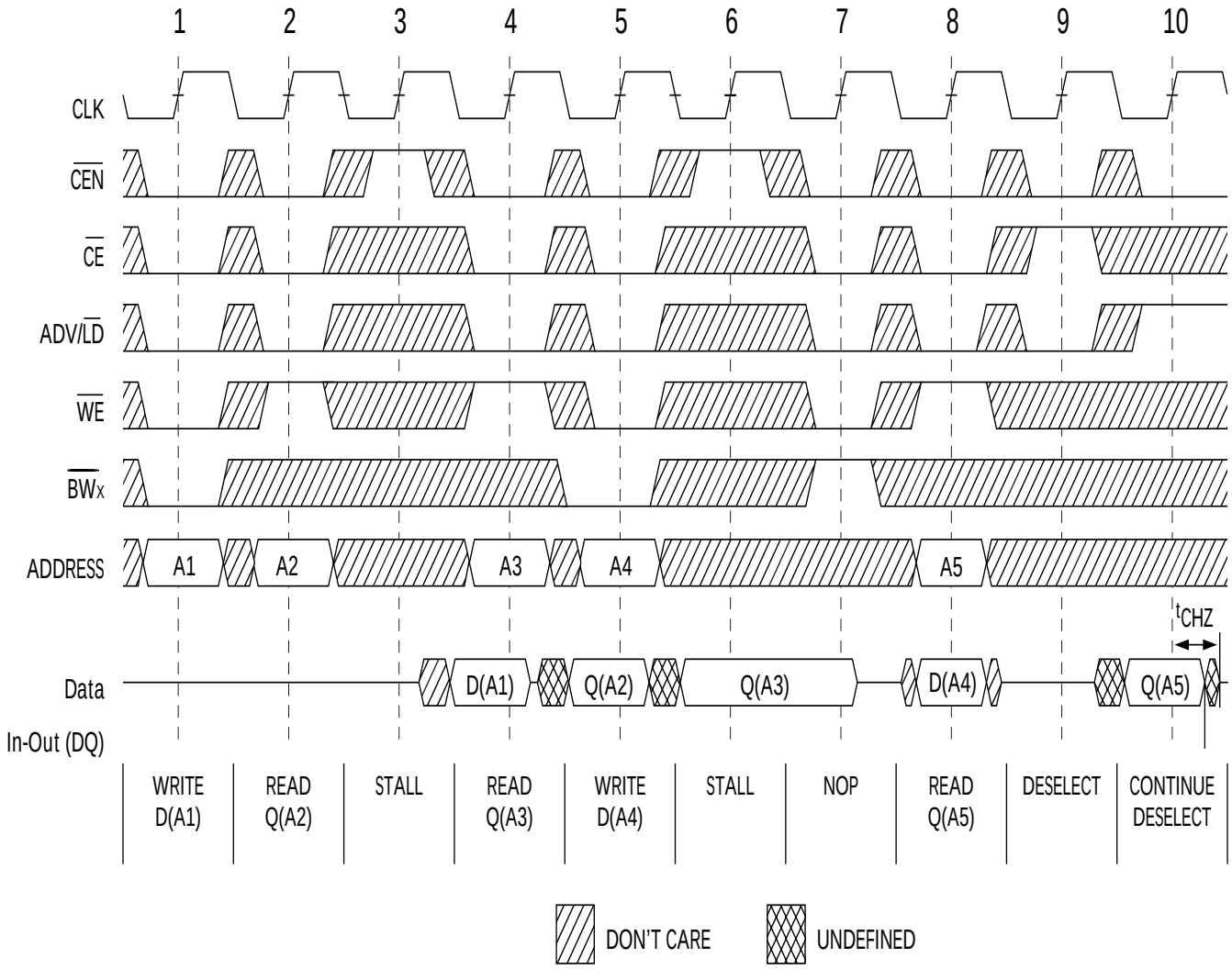
## Switching Waveforms

### Read/WriteTiming[23,24,25]



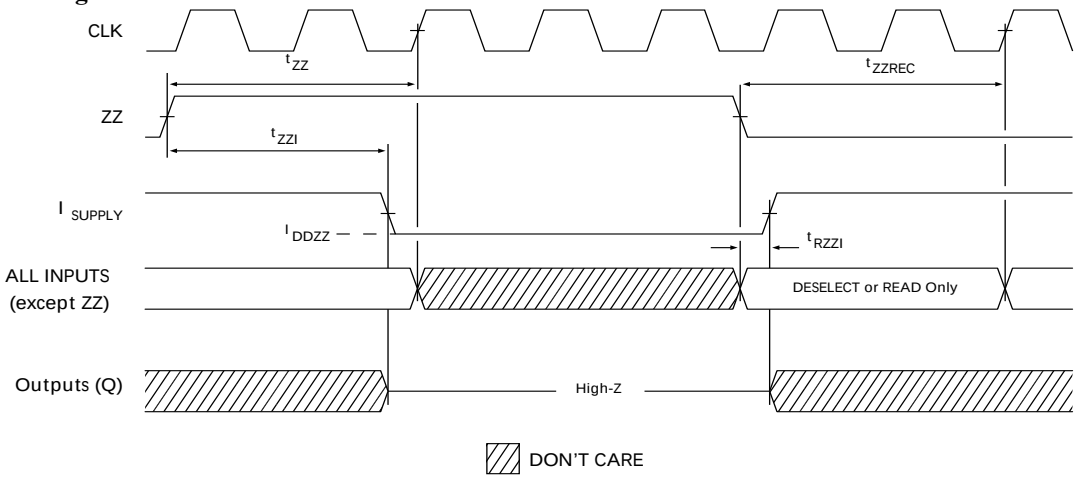
**Switching Waveforms** (continued)

**NOP,STALL AND DESELECT CYCLES[23,24,26]**



## Switching Waveforms (continued)

### ZZ Mode Timing [27,28]




**Note:**
23. For this waveform ZZ is tied low.
24. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, $CE_2$ is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH,$\overline{CE}_1$ is HIGH or $CE_2$ is LOW or $\overline{CE}_3$ is HIGH.
25. Order of the Burst sequence is determined by the status of the MODE (0=Linear, 1=Interleaved).Burst operations are optional.
26. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle
27. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
28. I/Os are in High-Z when exiting ZZ sleep mode..

## Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 225 | CY7C1354B-225AC | A101 | 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) | Commercial |
| | CY7C1356B-225AC | | | |
| | CY7C1354B-225AI | A101 | 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) | Industrial |
| | CY7C1356B-225AI | | | |
| | CY7C1354B-225BGC | BG119 | 119-ball Ball Grid Array (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1356B-225BGC | | | |
| | CY7C1354B-225BGI | BG119 | 119-ball Ball Grid Array (14 x 22 x 2.4 mm) | Industrial |
| | CY7C1356B-225BGI | | | |
| | CY7C1354B-225BZC | BB165A | 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm) | Commercial |
| | CY7C1356B-225BZC | | | |
| | CY7C1354B-225BZI | BB165A | 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm) | Industrial |
| | CY7C1356B-225BZI | | | |

## Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 200 | CY7C1354B-200AC<br>CY7C1356B-200AC | A101 | 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) | Commercial |
| | CY7C1354B-200AI<br>CY7C1356B-200AI | A101 | 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) | Industrial |
| | CY7C1354B-200BGC<br>CY7C1356B-200BGC | BG119 | 119-ball Ball Grid Array (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1354B-200BGI<br>CY7C1356B-200BGI | BG119 | 119-ball Ball Grid Array (14 x 22 x 2.4 mm) | Industrial |
| | CY7C1354B-200BZC<br>CY7C1356B-200BZC | BB165A | 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm) | Commercial |
| | CY7C1354B-200BZI<br>CY7C1356B-200BZI | BB165A | 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm) | Industrial |
| 166 | CY7C1354B-166AC<br>CY7C1356B-166AC | A101 | 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) | Commercial |
| | CY7C1354B-166AI<br>CY7C1356B-166AI | A101 | 100-lead Thin Quad Flat Pack (14 x 20 x 1.4 mm) | Industrial |
| | CY7C1354B-166BGC<br>CY7C1356B-166BGC | BG119 | 119-ball Ball Grid Array (14 x 22 x 2.4 mm) | Commercial |
| | CY7C1354B-166BGI<br>CY7C1356B-166BGI | BG119 | 119-ball Ball Grid Array (14 x 22 x 2.4 mm) | Industrial |
| | CY7C1354B-166BZC<br>CY7C1356B-166BZC | BB165A | 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm) | Commercial |
| | CY7C1354B-166BZI<br>CY7C1356B-166BZI | BB165A | 165-ball Fine Pitch Ball Grid Array (13 x 15 x 1.2 mm) | Industrial |

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.



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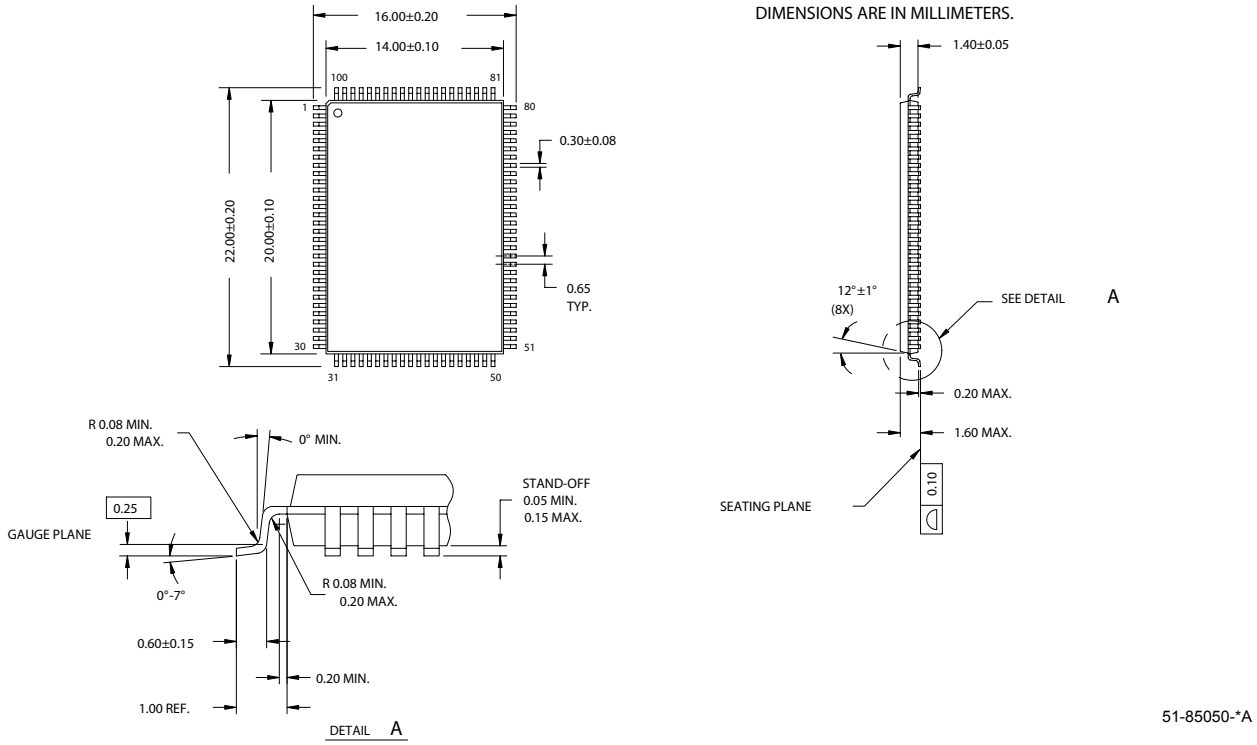
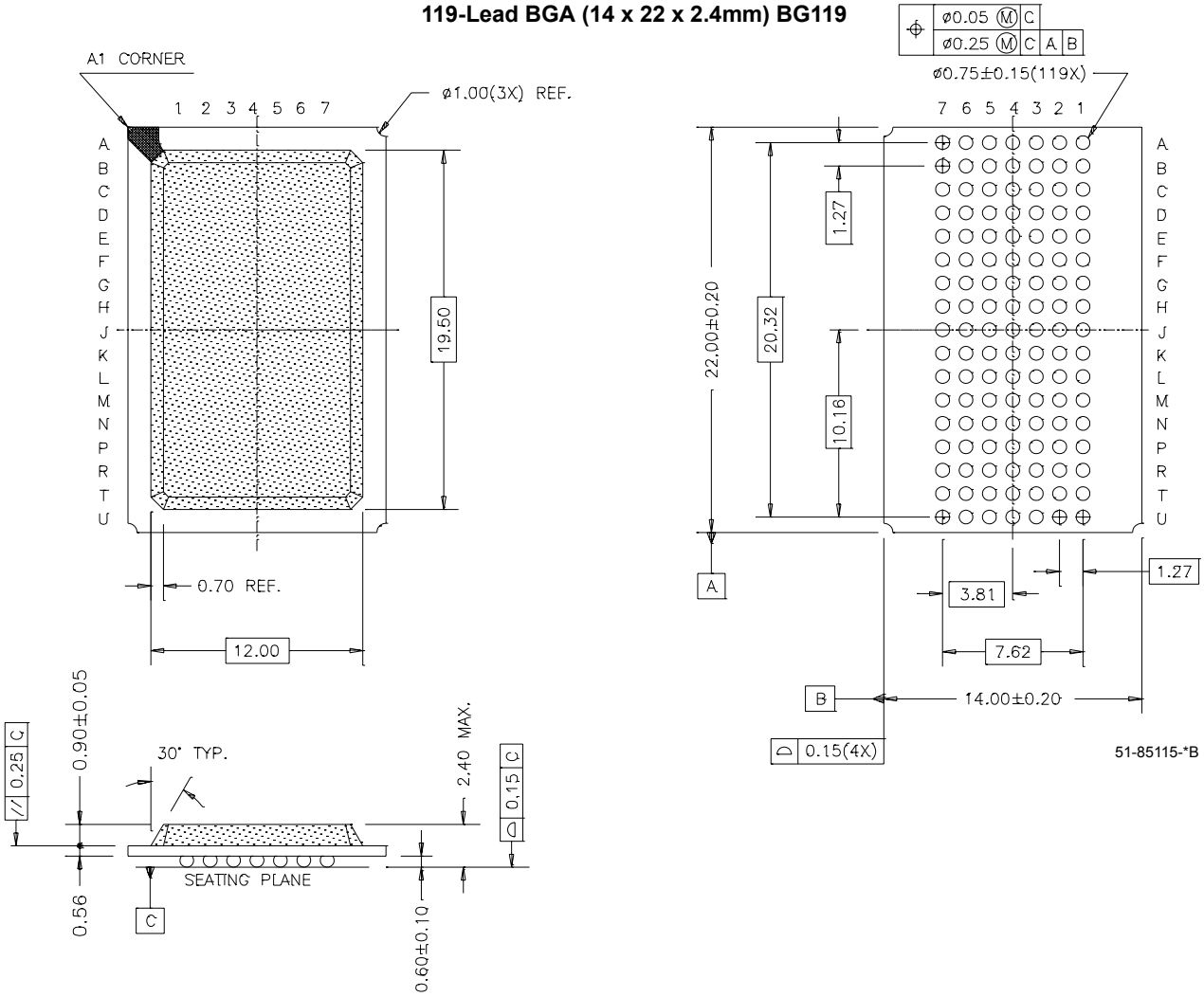
## Package Diagrams

**100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101**



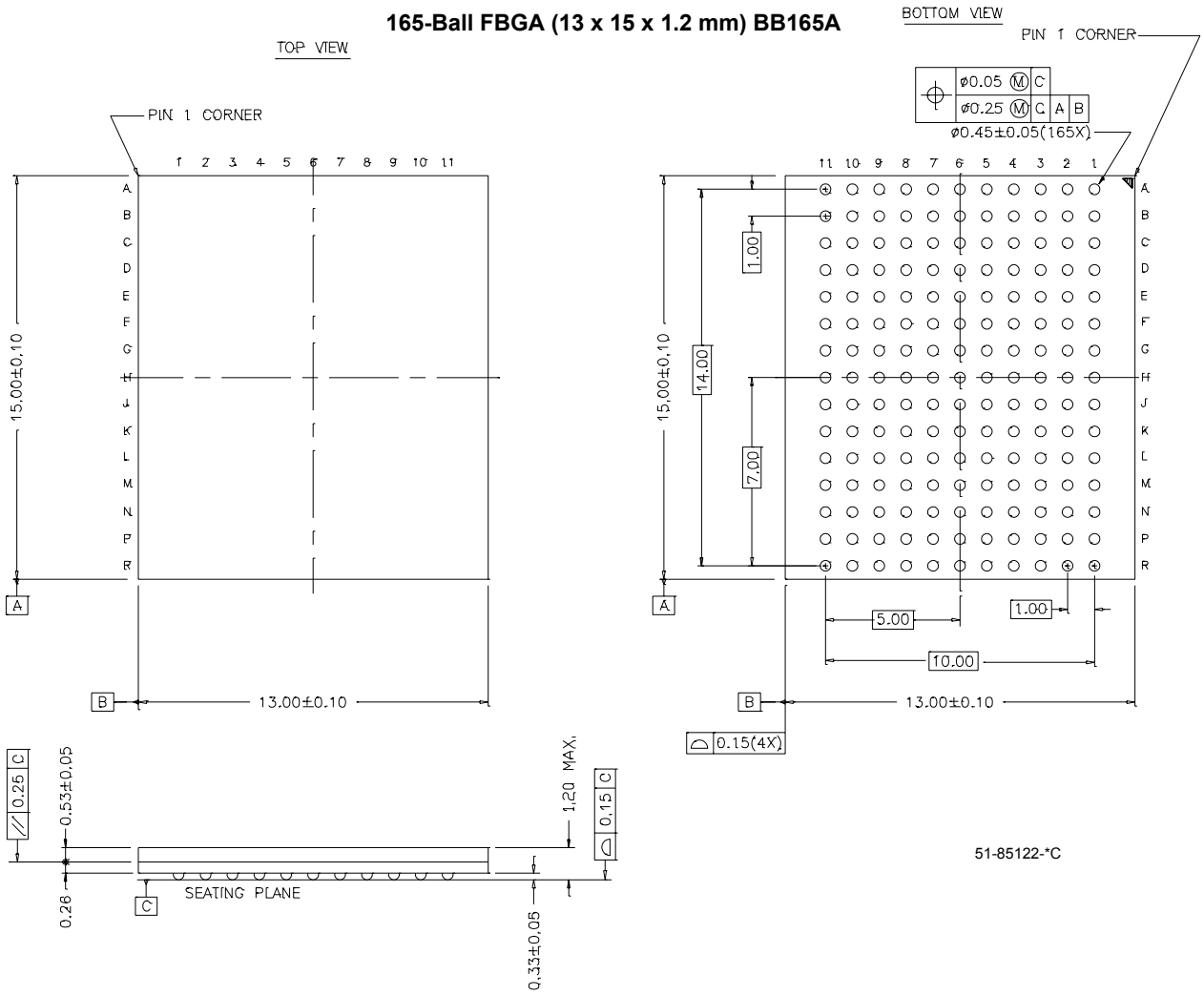
**Package Diagrams** (continued)

**119-Lead BGA (14 x 22 x 2.4mm) BG119**



**Package Diagrams** (continued)

**165-Ball FBGA (13 x 15 x 1.2 mm) BB165A**

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## Document History Page

| Document Title: CY7C1354B/CY7C1356B 9-Mb (256K x 36/512K x 18) Pipelined SRAM with NoBL™ Architecture<br>Document Number: 38-05114 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 117904 | 08/28/02 | RCS | New Data Sheet |
| *A | 126207 | 08/27/03 | DPM | Removed Preliminary status<br>Removed 250-MHz Speed bin<br>Added 225-MHz speed bin<br>Increased $T_{CO}$, $T_{EOV}$, $T_{CHZ}$, $T_{EOHZ}$ for 200 MHz to 3.2 ns from 3.0 ns<br>Updated JTAG revision number and device depth<br>Updated JTAG boundary scan orders<br>Added $t_{Power}$ specification<br>Changed footnotes ordering<br>Added Industrial operating range<br>Changed Capacitance table to have TQFP, BGA, and fBGA columns. |
| *B | 205060 | See ECN | NJY | Removed footnote 13 “Minimum voltage equals –2.0V for pulse durations of less than 20 ns.”<br>Removed footnote 14 “TA is the case temperature.”<br>Changed footnote 15 from “Overshoot: $V_{IH}(AC) < V_{DD} + 1.5V$ for $t < t_{TCYC}/2$; undershoot: $V_{IL}(AC) < 0.5V$ for t < tTCYC/2; power-up: VIH < 2.6V and VDD < 2.4V and VDDQ < 1.4V for t < 200 ms. “to footnote 13“Overshoot: VIH(AC) < VDD +1.5V (Pulse width less than tCYC/2), undershoot: VIL(AC)> -2V (Pulse width less than tCYC/2). “<br>Added footnote 14 “$T_{Power-up}$: Assumes a linear ramp from 0V to $V_{DD}$ (min.) within 200ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} < V_{DD}$. “<br>Added footnote 20 “Timing reference level is 1.5V when $V_{DDQ}$ = 3.3V and is 1.25V when $V_{DDQ}$ = 2.5V.”<br>Changed footnote 21 from “Test conditions shown in (a), (b) and (c) of AC Test Loads. “to “Test conditions shown in (a) of AC Test Loads unless otherwise noted. “<br>Updated ZZ Mode Electrical Characteristics.<br>Updated $I_{SB1}$ and $I_{SB3}$ currents in Electrical Characteristics table.<br>Modified functional block diagram.<br>Modified Truth Table and Write Cycle Descriptions.<br>Updated Ordering Information. |
| *C | 230388 | See ECN | VBL | Modified ID code<br>Changed balls B4 and A5 from $\overline{BW}_d$ and $\overline{BW}_b$ to NC and ball A4 from $\overline{BW}_c$ to $\overline{BW}_b$ for 165-ball FBGA package for CY7C1356B<br>Changed balls C11 from DQPb to DQPa and balls D11,E11,F11 and G11 from DQb to DQa for CY7C1356B.<br>Update Ordering Info section: changed BZC to BZI in Industrial part |