PRELIMINARY **CY7B333B**

CYPRESS SEMICONDUCTOR

General-Purpose Synchronous BiCMOS PLD

Features

- 16 I/O macrocells, each having:
  - Choice of combinatorial or registered output
  - Registers programmable to T-type or D-type
  - Emulation of RS and JK flip-flop
  - Independent (product term) output enable
  - Synchronous clock input and product term controlled asynchronous reset product term for each bank of 8 macrocells
  - Programmable output polarity control
  - Up to 8 macrocell registers may be buried while preserving the use of the associated pins as inputs and without using additional product terms
  - 8 product terms per output
- 146 product terms total
- 2 clock inputs that can also be logic inputs
- High performance
  - 10 ns maximum propagation delay
- Centered power and ground pins for low noise operation
- Advanced BiCMOS technology
- Available in 28-pin, 300-mil PDIP, cerDIP, PLCC, and LCC packages
- Programmable security bit

Functional Description

The CY7B333B is a 28-pin, general-purpose, high-performance PLD with seven dedicated inputs, two clock inputs, and sixteen I/O macrocells (two banks of eight I/O macrocells). These are connected to a logic array of 146 product terms and 50 input terms. The CY7B333B has centered power and ground pins for low noise operation.

The CY7B333B uses an 8-wide sum of product terms distribution scheme. Each one of the 16 I/O macrocells has as its input an 8-wide sum of product terms. There are two asynchronous reset product terms (one product term per bank of eight I/O macrocells).

CLK1 provides the synchronous clock input for one bank of macrocells, and CLK2 provides the synchronous clock input for the other bank of macrocells. If no synchronous clock inputs are needed, the CLK1 and CLK2 inputs can function as standard logic inputs. Output enable is controlled with one dedicated product term per macrocell. An asynchronous reset product term is provided for each bank of macrocells.

Each macrocell has a register that can be programmed to be a T-type or D-type. RS-type and JK-type registers can be emulated. The macrocell architecture also allows up to one half of the macrocell registers to be buried without sacrificing any I/O pins and without using additional product terms.

The CY7B333B is available in a wide variety of packages including 28-pin, 300-mil plastic DIP and ceramic DIP, 28-pin square plastic leaded chip carrier (PLCC), 28-pin square J-leaded hermetic ceramic chip and, for military only, standard opaque ceramic leadless chip carrier (LCC).

Pin Configuration

LCC/PLCC
Top View

B333–2

Logic Block Diagram

B333–1

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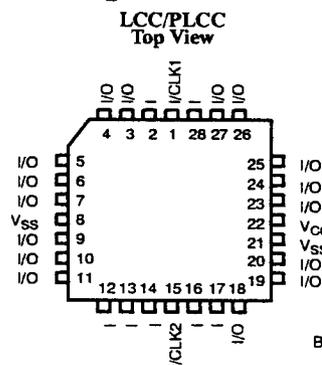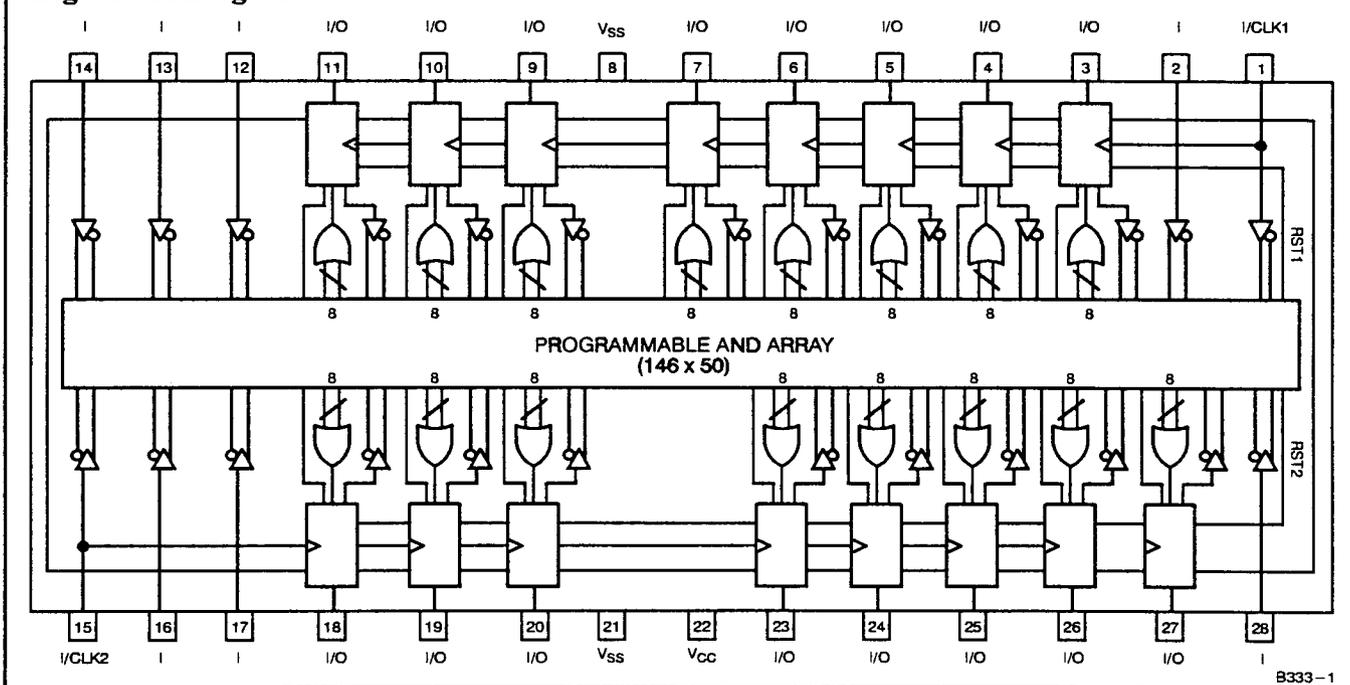
Selection Guide

		7B333B−10	7B333B−12	7B333B−15
I_{CC1} (mA)	Commercial	150	150	
	Military		170	170
t_{PD} (ns)	Commercial	10	12	
	Military		12	15
t_s (ns)	Commercial	8	10	
	Military		10	12
t_{CO1} (ns)	Commercial	8	10	
	Military		10	12

Macrocell Description

The control bits in each macrocell allow independant selection of combinatorial or registered output and polarity. There are five configuration bits ($C_0 - C_4$) in each I/O macrocell. The clock sources for the two groups of eight registers on the left and right side of the package are CLK1 and CLK2, respectively.

The one-of-three feedback multiplexer in the macrocell allows a choice of three feedback sources: (1) register output, (2) macrocell I/O pin, and (3) adjacent macrocell I/O pin. This is done by programming the C_3 and C_4 configuration bits. The choice of either of two I/O pins as input source allows registers to be buried (internal feedback path selected with output buffer three-stated) while preserving the use of the associated I/O pin as an input by routing the input pin to the array through the adjacent output macrocell-feedback multiplexer.

This approach allows up to one half of the registers to be buried without sacrifice of any I/O pins and is accomplished with no increase in array size or the accompanying degradation of die cost or speed performance.

The three-state output buffer of each macrocell is controlled by an individual product term.

The CY7B333B has a single asynchronous reset product term for each group of eight macrocells.

Control Bit Description

Each I/O macrocell has one register that may be configured by the dedicated configuration bit, C_0, as T-type or D-type register. The T-type register may also be used to implement an RS or JK register. If $C_0 = 0$ (default) then the output register will be D type. On the other hand, setting $C_0 = 1$ will configure a T-type register. C_1 controls whether the input is registered or combinatorial. C_2 controls output polarity. C_3 and C_4 select feedback from register output, macrocell I/O pin, or adjacent macrocell I/O pin. The default configuration ($C_4, C_3, C_2, C_1, C_0 = 0$) is an inverted combinational output with I/O pin feedback. *Table 1* describes the various macrocell configurations and the corresponding values of $C_4 - C_0$.

Table 1. Macrocell Configuration Bits

C_4	C_3	C_2	C_1	C_0	Configuration
0	0	0	0	X	Combinatorial, Inverted, I/O Feedback
0	0	0	1	0	D Register, Inverted, I/O Feedback
0	0	0	1	1	T Register, Inverted, I/O Feedback
0	0	1	0	X	Combinatorial, Noninverted, I/O Feedback
0	0	1	1	0	D Register, Noninverted, I/O Feedback
0	0	1	1	1	T Register, Noninverted, I/O Feedback
1	0	X	X	X	Illegal
0	1	0	0	X	Combinatorial, Inverted, Registered Feedback
0	1	0	1	0	D Register, Inverted, Registered Feedback
0	1	0	1	1	T Register, Inverted, Registered Feedback
0	1	1	0	X	Combinatorial, Noninverted, Registered Feedback
0	1	1	1	0	D Register, Noninverted, Registered Feedback
0	1	1	1	1	T Register, Noninverted, Registered Feedback
1	1	0	0	X	Combinatorial, Inverted, Adjacent I/O Feedback
1	1	0	1	0	D Register, Inverted, Adjacent I/O Feedback
1	1	0	1	1	T Register, Inverted, Adjacent I/O Feedback
1	1	1	0	X	Combinatorial, Noninverted, Adjacent I/O Feedback
1	1	1	1	0	D Register, Noninverted, Adjacent I/O Feedback
1	1	1	1	1	T Register, Noninverted, Adjacent I/O Feedback

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... $-65°C$ to $+150°C$

Ambient Temperature with
Power Applied .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs
in High Z State .... $-0.5V$ to V_{CC} Max.

DC Input Voltage .... $-0.5V$ to $(V_{CC} + 0.5V)$

DC Input Current .... -30 mA to $+5$ mA
(except during programming)

DC Program Voltage 9.5V

Static Discharge Voltage .... >500V
(per MIL–STD–883, Method 3015)

Operating Range (per MIL-STD-883, Method 3015)

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[1]	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -4$ mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4$ mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs		2.2		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[2]			0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max.		-250	50	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$		-100	100	μA
I_{SC}	Output Short Circuit Current[5]	V_{CC} = Max., $V_{OUT} = 0.5V$[3]		-30	-130	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IH} = GND, Outputs Open	Com'l		150	mA
			Mil		170	
I_{CC2}	Power Supply Current at Frequency[4,5]	V_{CC} = Max., Outputs Disabled (in High Z State), Device Operating at f_{MAX3}	Com'l		170	mA
			Mil		190	

Notes:
2. T_A is the "instant on" case temperature.
3. Minimum DC input voltage is -0.3 volts. During transitions, the inputs may undershoot to -2.0 volts for periods less than 20 ns.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT} = 0.5V$ has been chosen to avoid test problems caused by ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.
5. Measured with the device configured as a 16-bit counter.

Capacitance[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0V$ at f = 1 MHz	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0V$ at f = 1 MHz	10	pF

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AC Test Loads and Waveforms

+5V

R1 819 Ω

OUTPUT

C = 35 pF   R2 335 Ω

0V   0V

(a) Normal Load (Load 1)

B333-8

R = 237 Ω

OUTPUT

C = 35 pF V_{TH} = 1.45V

0V   0V

(b) Thévenin Equivalent (Load 1)

B333-9

R = 237 Ω

OUTPUT

C = 5 pF V_X

0V   0V

(c) Three-state Delay Load (Load 2)

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ALL INPUT PULSES

3.0V
90%
GND
10%
≤ 2 ns   ≤ 2 ns

(d)
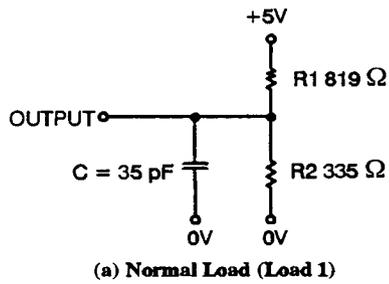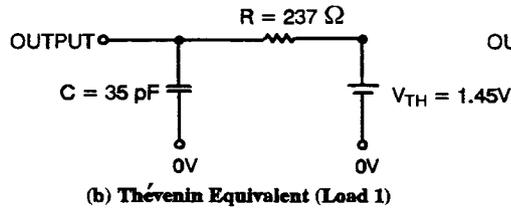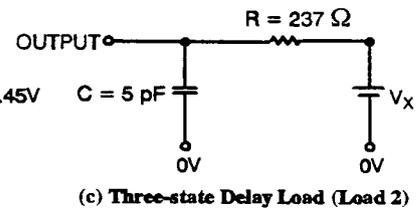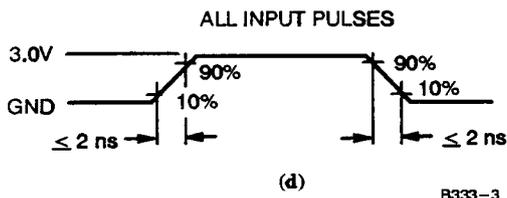
B333-3

Parameter	V_X	Output Waveform—Measurement Level	
t_{ER} (−)	1.5V	V_{OH} 0.5V V_X	B333-4
t_{ER} (+)	2.6V	V_{OL} 0.5V V_X	B333-5
t_{EA} (+)	V_{TH}	V_X 0.5V V_{OH}	B333-6
t_{EA} (−)	V_{TH}	V_X 0.5V V_{OL}	B333-7

Switching Waveform

INPUTS I/O, REGISTERED FEEDBACK SYNCHRONOUS PRESET

t_S t_H t_{WH} t_{WL}

CLK

t_{SPR} t_P

t_{AW} t_{AR}

t_{OH}

ASYNCHRONOUS RESET

t_{CO} t_{AP}

REGISTERED OUTPUTS

t_{ER}[7] t_{EA}

t_{PD} t_{ER}[7] t_{EA}

COMBINATORIAL OUTPUTS
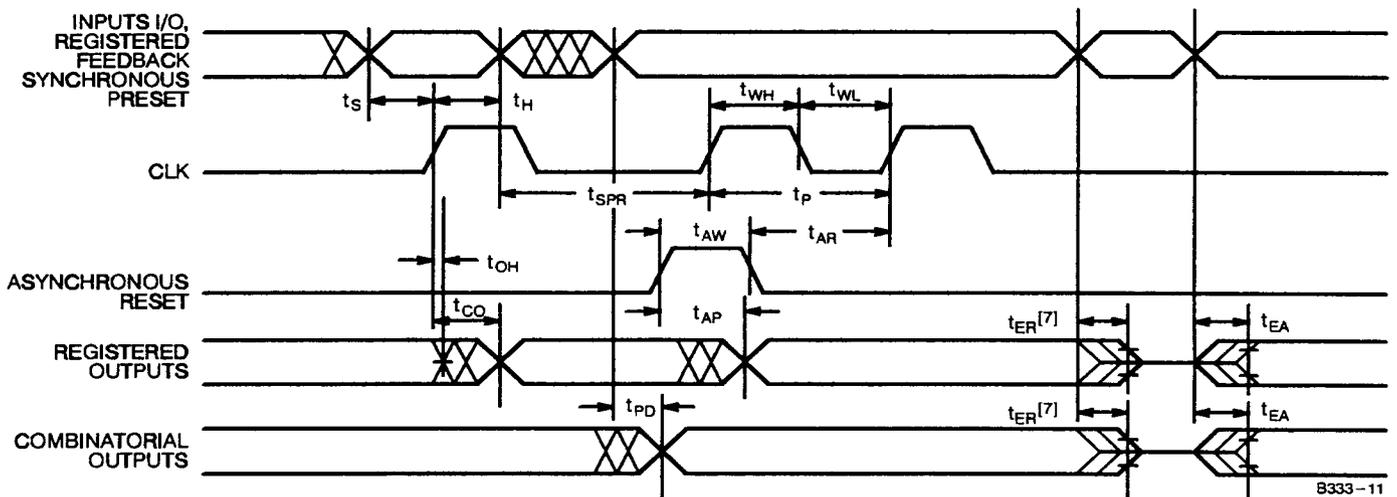
B333-11

Power-Up Reset Waveform
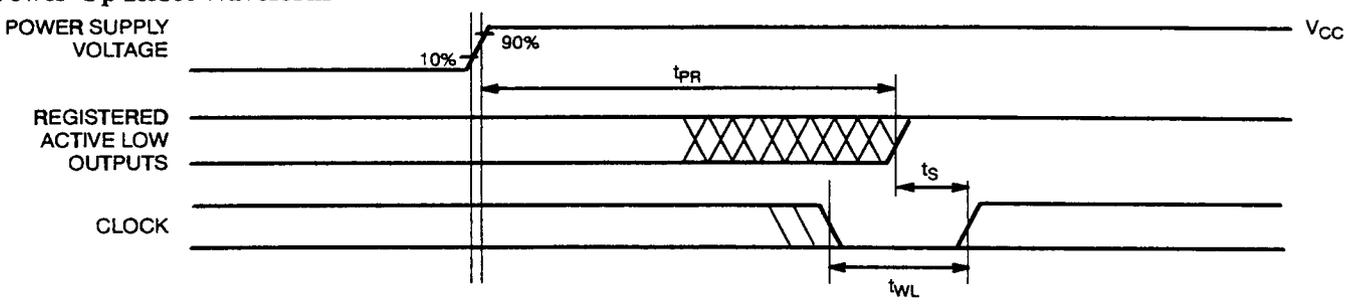
Switching Characteristics[6]

Parameter	Description		7B333B−10		7B333B−12		7B333B−15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]	Com'l		10		12			ns
		Mil				12		15	
t_{EA}	Input to Output Enable Delay[7]	Com'l		12		14			ns
		Mil				14		16	
t_{ER}	Input to Output Disable Delay[7, 8]	Com'l		12		14			ns
		Mil				14		16	
t_{CO1}	Clock to Output Delay[7]	Com'l		8		10			ns
		Mil				10		12	
t_{CO2}	Clock to Registered Feedback to Combinatorial Output Delay[5, 7, 9]	Com'l		17		20			ns
		Mil				20		25	
t_{OH}	Output Data Stable Time from Input Clock	Com'l	1		1				ns
		Mil			1		1		
t_S	Input or Feedback Set-Up Time	Com'l	8		10				ns
		Mil			10		12		
t_H	Input Hold Time	Com'l	0		0				ns
		Mil			0		0		
t_P	External Clock Period (t_{CO1} + t_S)[10, 7]	Com'l	16		20				ns
		Mil			20		24		
t_{WH}	Clock Width HIGH[5]	Com'l	6		9				ns
		Mil			9		10		
t_{WL}	Clock Width LOW[5]	Com'l	6		9				ns
		Mil			9		10		
f_{MAX1}	External Maximum Frequency (1/(t_{CO1} + t_S))[7, 10, 11]	Com'l	62.5		50				MHz
		Mil			50		41.6		
f_{MAX2}	Data Path Maximum Frequency (1/(t_{WH} + t_{WL}))[5, 10]	Com'l	83.3		55.5				MHz
		Mil			55.5		50		
f_{MAX3}	Internal Feedback Maximum Frequency (1/(t_{CF} + t_S))[5, 12]	Com'l	80		58				MHz
		Mil			58		48		
t_{CF}	Register Clock to Feedback Input[13]	Com'l		5		7			ns
		Mil				7		9	
t_{AW}	Asynchronous Reset Width[5, 7]	Com'l	8		10				ns
		Mil			10		12		
t_{AR}	Asynchronous Reset Recovery Time[5]	Com'l	10		12				ns
		Mil			12		15		
t_{AP}	Asynchronous Reset to Registered Output Delay[7]	Com'l		12		14			ns
		Mil				14		17	
t_{PR}	Power-Up Reset Time[5]	Com'l		1.0		1.0			μs
		Mil				1.0		1.0	

Programming

The 7B333B can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG, and other programmers. Design for the CY7B333B can be implemented using Cypress Semiconductor's *Warp2* VHDL compiler, and also with Data I/O's ABEL, Logical Device's CUPL, and other compilers. Please contact your local Cypress representative for further information.

Synchronous I/O Macrocell
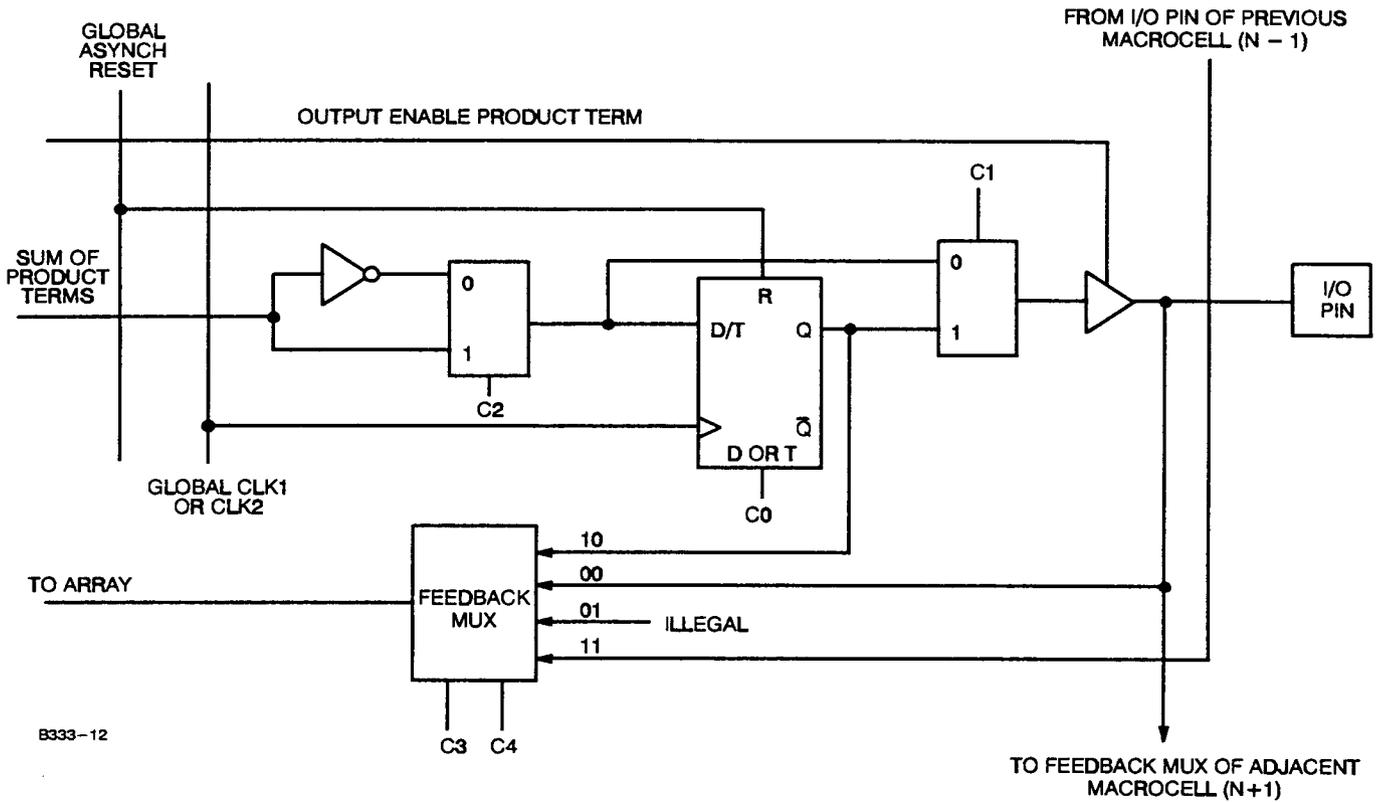
B333-12

Notes:

5. AC test load (Load 1) used for all parameters except where noted.

7. This specification is guaranteed for eight or fewer devices outputs changing state in a given access cycle.

7. This parameter is measured as the time after the output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max. (See Load 2.)

9. Delay measured from clock of registered macrocell to feedback through logic array to second macrocell output configured as a combinatorial path.

10. This is a calculated parameter and is not directly tested.

11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.

12. This spec indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.

13. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 7) minus t_S and is not directly tested.

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Block Diagram

B333-13

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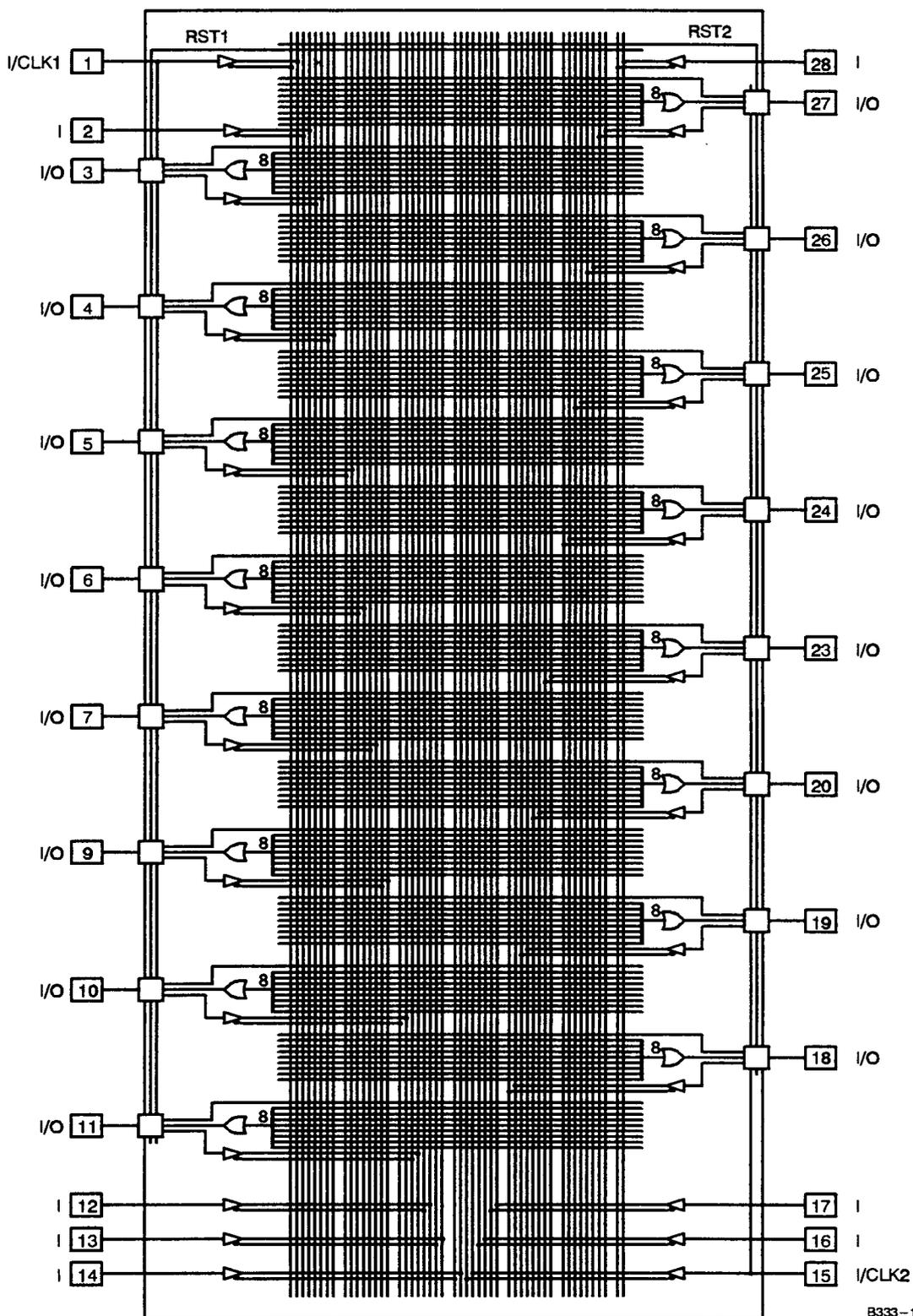
MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO1}	9, 10, 11
t_{EA}	9, 10, 11
t_{ER}	9, 10, 11
t_{OH}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type	Operating Range
150	10	83.3	CY7B333B−10DC	D22	Commercial
			CY7B333B−10JC	J64	
			CY7B333B−10PC	P21	
	12	55.5	CY7B333B−12DC	D22	Commercial
			CY7B333B−12JC	J64	
			CY7B333B−12PC	P21	
170	12	55.5	CY7B333B−12DMB	D22	Military
			CY7B333B−12LMB	L64	
	15	50	CY7B333B−15DMB	D22	Military
			CY7B333B−15LMB	L64	

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PRELIMINARY　　　　　　CY7B333B

Package Diagrams

28-Lead (300-Mil) CerDIP D22
MIL−STD−1835 D−15 Config. A
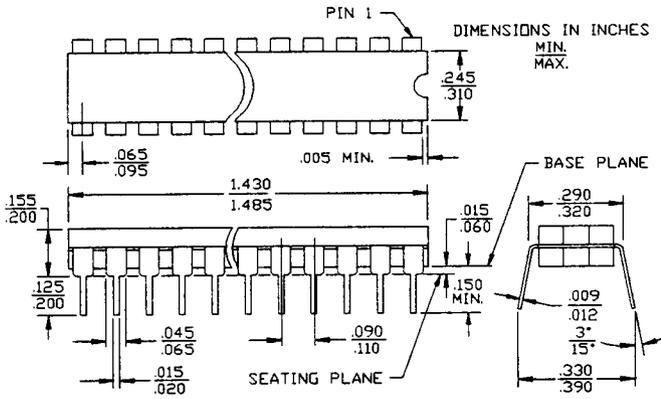
28-Square Leadless Chip Carrier L64
MIL−STD−1835 C−4
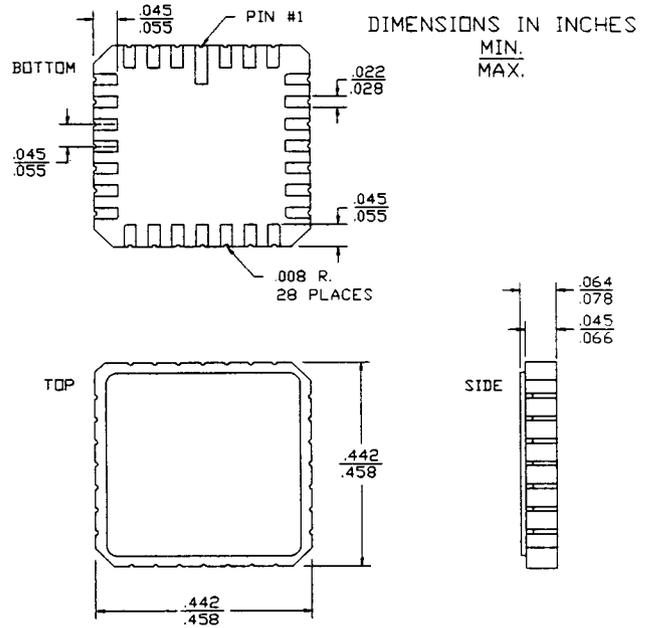
### 28-Lead Plastic Leaded Chip Carrier J64

CYPRESS SEMICONDUCTOR

PRELIMINARY   **CY7B333B**
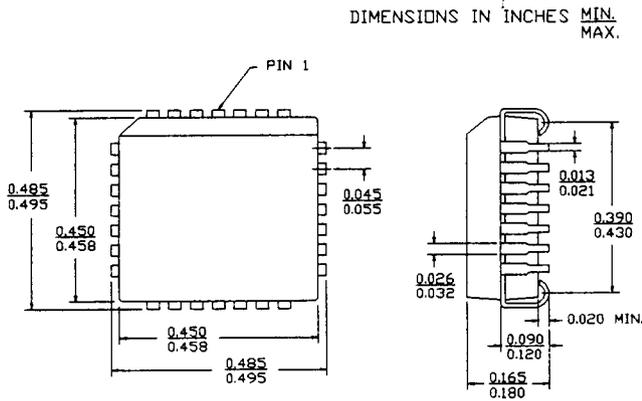
Package Diagrams (continued)

28-Lead (300-Mil) Molded DIP P21

PIN 1

DIMENSIONS IN INCHES MIN.
MAX.

0.250 / 0.270

0.030 / 0.080

1.370 / 1.425

SEATING PLANE

0.140 / 0.190

0.120 / 0.140

0.115 / 0.160

0.015 / 0.060

0.280 / 0.325

0.009 / 0.012

3° MIN.

0.090 / 0.110

0.055 / 0.065

0.015 / 0.020

0.310 / 0.385