μPD485505
Line Buffer for Communications Systems

Preliminary Information

Description

The μPD485505 is a 5048-word by 8-bit dual-port line buffer fabricated with a silicon-gate CMOS process. The device is capable of asynchronous read and write operation at high speed and can be used as a time axis converter or a digital delay line of up to 5048 bits (21 bits minimum at maximum frequency).

Applications include image processing in facsimile machines, plain paper copiers, video systems, and other optical scanners; time base correction in video playback systems; and data communication buffering in multiprocessor systems and local area networks.

Features

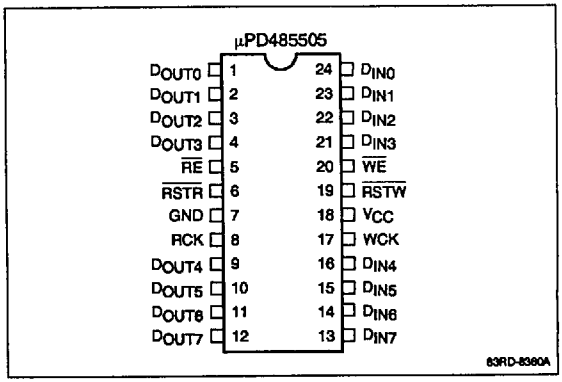
- 5048-word x 8-bit organization
- Fully static operation
- Dual-port operation
- Image processing and data communications applications
- Asynchronous and simultaneous reading/writing
- 1H (5048-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 24-pin plastic SOP and 24-pin plastic ZIP packaging

Ordering Information

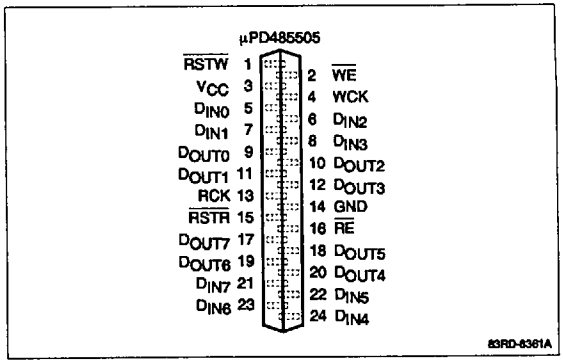
Part No.	Cycle Time (min)	Read Access Time (max)	Package
μPD485505GU-25	25 ns	18 ns	24-pin plastic SOP
GU-35	35 ns	25 ns	
μPD485505V-25	25 ns	18 ns	24-pin plastic ZIP
V-35	35 ns	25 ns	

Pin Configurations

24-Pin Plastic SOP



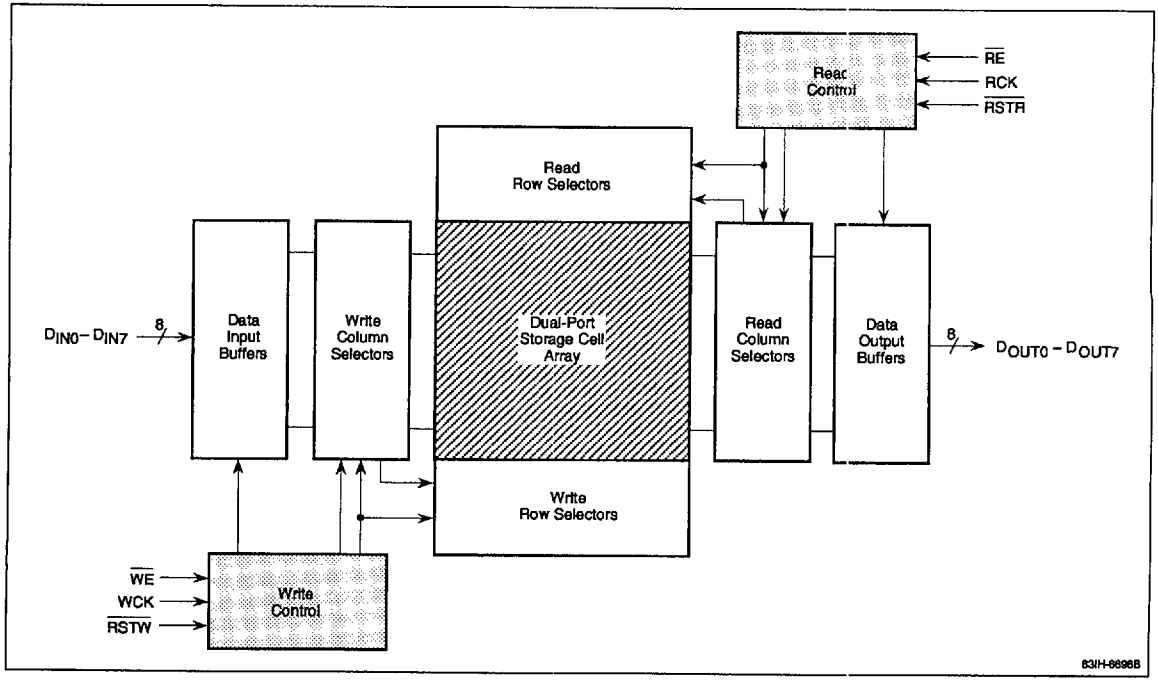
24-Pin Plastic ZIP



Pin Identification

Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
RCK	Read clock input
$\overline{RE}$	Read enable input
$\overline{RSTR}$	Read address reset input
$\overline{RSTW}$	Write address reset input
WCK	Write clock input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



Pin Functions

D_{IN0} - D_{IN7} (Data Inputs). New data is entered on these pins.

D_{OUT0} - D_{OUT7} (Data Outputs). These three-state outputs are used to access stored information. In a simple digital delay line application, a minimum delay of 21 clock cycles is required to move data from the input pins to the output pins.

RCK (Read Clock Input). All read cycle are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are latched by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge.

The internal read address increments with each RCK cycle unless $\overline{RE}$ is high to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 5047 to 0 and begin incrementing again.

$\overline{RE}$ (Read Enable Input). This signal controls read operation. If $\overline{RE}$ is low, all read cycles proceed. If $\overline{RE}$ is at a high level, the data outputs remain valid for that address and the internal read address stops incrementing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

$\overline{RSTR}$ (Read Address Reset Input). This signal is strobed by the rising edge of RCK and resets the internal read address to 0.

$\overline{RSTW}$ (Write Address Reset Input). Bringing this signal low resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

WCK (Write Clock Input). All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle.

The internal write address increments with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 5047 to 0 and begin incrementing again.

$\overline{WE}$ (Write Enable Input). This input is similar to $\overline{RE}$ but controls write operation. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address does not increment. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

Operation

Reset Cycle. The μPD485505 requires the initialization of internal circuits using the $\overline{RSTW}/\overline{RSTR}$ reset signals before starting operation as a time axis converter or a digital delay line.

A reset cycle can be executed at any time and does not depend on the state of $\overline{RE}$ or $\overline{WE}$. However, $\overline{RSTW}$ and $\overline{RSTR}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

Write/Read Cycles. Write and read cycles are synchronized to their respective WCK/RCK inputs and executed individually when WCK or RCK is high and $\overline{WE}$ or $\overline{RE}$ is low. Write data must satisfy setup and hold times as specified from the rising edge of WCK. New data written to a particular address is available for reading after one-half write cycle plus 500 ns (maximum).

The access time of a read cycle is measured from the rising edge of RCK by t_{AC}. Stored data is read nondestructively; data can be read repeatedly because data hold time is infinite.

Time Axis Conversion. To use the μPD485505 as a time axis converter, write and read cycles must be controlled independently. Write and read ports must be initialized separately using the reset signals. Write cycles can then be executed in synchronization with WCK and write data can be stored sequentially from address 0 of this device. Afterward, when a read cycle is executed in synchronization with RCK, stored data can be read sequentially from address 0.

Since write and read cycles can be executed independently, data loaded at one arbitrary drive frequency can be read at another arbitrary drive frequency. In this sense, the μPD485505 functions as a time axis converter.

Digital Delay Line. The μPD485505 can be easily used as a digital delay line of 5048 bits or less. After the internal circuits are initialized using simultaneous $\overline{RSTW}/\overline{RSTR}$ signals, write/read cycles also may be executed simultaneously by supplying the same pulse to the write (WCK) and read (RCK) clocks. Write data is always read after the full 5048-bit delay if neither write nor read operation has been inhibited. This is the essential delay line function.

If either $\overline{WE}$ or $\overline{RE}$ is set at a nonselected (high) level for several cycles while the other is maintained in a selected (low) level, the delay line length can differ from 5048 bits.

For example, if only $\overline{WE}$ is a set to a high level (write disable) for a small number of cycles, read cycles are executed continuously and the delay line length is large. Alternatively, if only $\overline{RE}$ is set to a high level (read disable) for a small number of cycles, write cycles are executed continuously and the delay line length is small. Note that the minimum delay line length is 21 bits (for maximum frequency operation) and the maximum is 5048 bits.

A data delay of 5048 bits or less can also be obtained by applying the $\overline{RSTW}$ and $\overline{RSTR}$ signals at different times. For example, data loaded for "m" cycles after $\overline{RSTW}$ can then be read after supplying $\overline{RSTR}$. In this case, since write data can be read from the beginning after a delay of "m" cycles, the device can be used as an m-bit digital delay line.

The $\overline{RSTW}/\overline{RSTR}$ reset signals can also be simultaneously loaded at every 1H (horizontal line) period. In this case, write data loaded in the previous line cycle is read out from the beginning as read data after the reset. Therefore, a delay line length ranging from 21 to 5048 bits (depending on cycle time) can be obtained according to the length of the reset signals supplied. Refer to the timing waveform for an "n-Bit Delay Line."

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Voltage on any input pin, V_I	−0.5 to V_{CC} + 0.5 V
Voltage on any output pin, V_O	−0.5 to V_{CC} + 0.5 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter *	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_I	5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O	7	pF	D_{OUT0} - D_{OUT7}

* These parameters are sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			80	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD485505-25 Min	μPD485505-25 Max	μPD485505-35 Min	μPD485505-35 Max	Unit	Test Conditions
Access time	t_{AC}		18		25	ns	
Data-in hold time	t_{DH}	3		3		ns	
Data-in setup time	t_{DS}	7		10		ns	
Output disable time	t_{HZ}	5	18	5	25	ns	(Note 4)
Output active time	t_{LZ}	5	18	5	25	ns	(Note 4)
Output hold time	t_{OH}	5		5		ns	
Read clock cycle time	t_{RCK}	25		35		ns	
RCK precharge time	t_{RCP}	9		12		ns	
RCK pulse width	t_{RCW}	9		12		ns	
Read enable hold time	t_{REH}	3		3		ns	(Note 8)
Read enable high delay from RCK	t_{REN1}	3		3		ns	(Note 9)
Read enable low delay to RCK	t_{REN2}	7		10		ns	(Note 9)
Read enable setup time	t_{RES}	7		10		ns	(Note 8)
Read disable pulse width	t_{REW}	0		0		ns	
Reset active hold time	t_{RH}	3		3		ns	(Note 6)
Reset inactive hold time	t_{RN1}	3		3		ns	(Note 7)
Reset inactive setup time	t_{RN2}	7		10		ns	(Note 7)
Reset active setup time	t_{RS}	7		10		ns	(Note 6)
Read reset time	t_{RSTR}	0		0		ns	
Write reset time	t_{RSTW}	0		0		ns	
Transition time	t_T	3	35	3	35	ns	
Write clock cycle time	t_{WCK}	25		35		ns	
WCK precharge time	t_{WCP}	9		12		ns	
WCK pulse width	t_{WCW}	9		12		ns	
Write enable hold time	t_{WEH}	3		3		ns	(Note 8)
Write enable high delay from WCK	t_{WEN1}	3		3		ns	(Note 9)
Write enable low delay to WCK	t_{WEN2}	7		10		ns	(Note 9)
Write enable setup time	t_{WES}	7		10		ns	(Note 8)
Write disable pulse width	t_{WEW}	0		0		ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 1. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

(6) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(7) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(8) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) output disable operations are not guaranteed.

(9) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) output disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 1. Output Loads for Timing Measurements

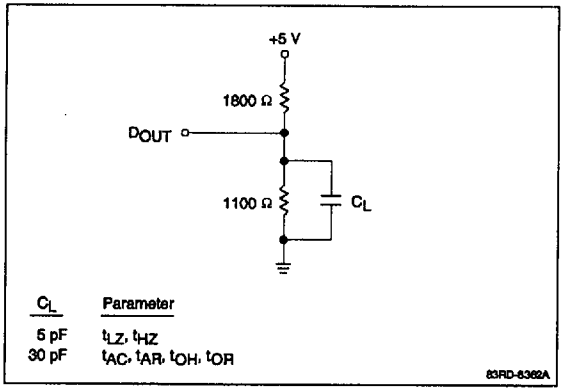
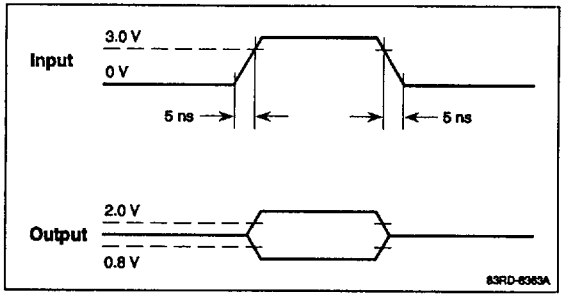
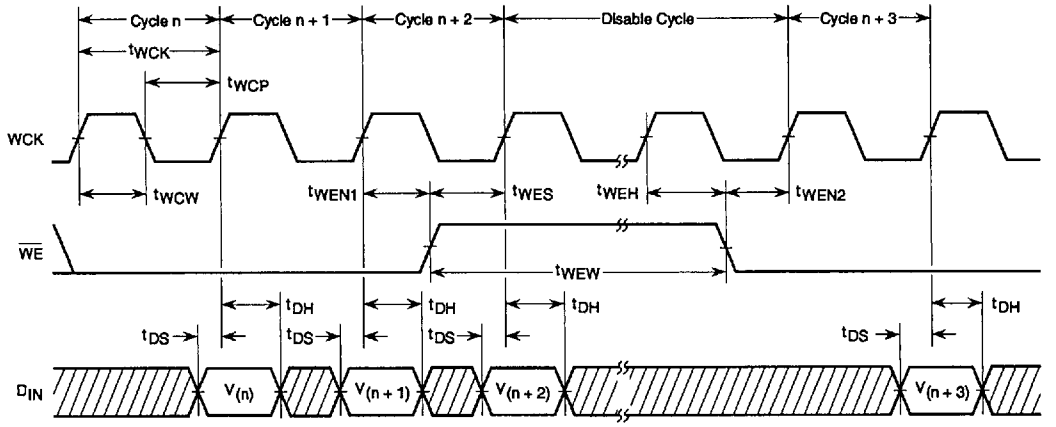


Figure 2. Voltage Thresholds for Timing Measurements



Timing Waveforms

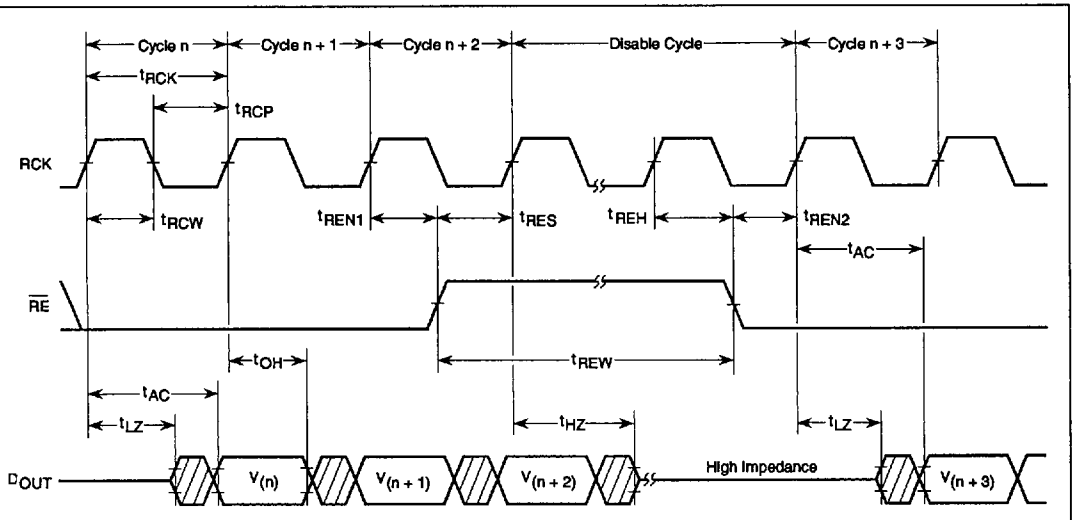
Write Cycle



Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

83IH-67048

Read Cycle

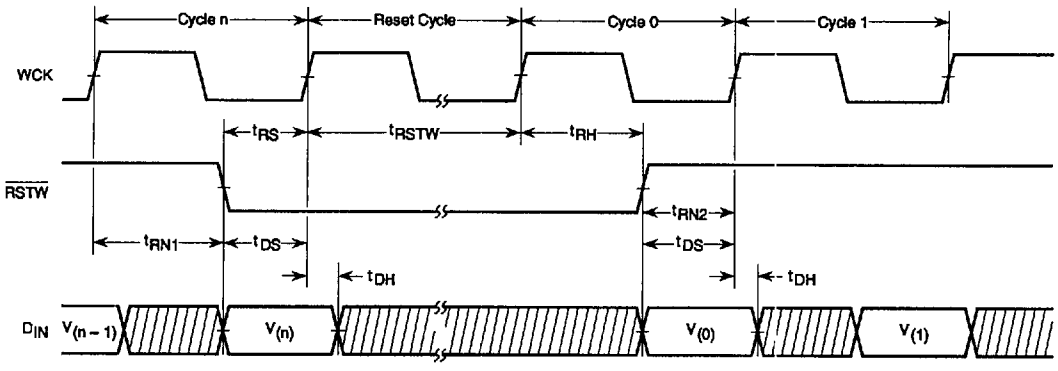


Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

83IH-67058

Timing Waveforms (cont)

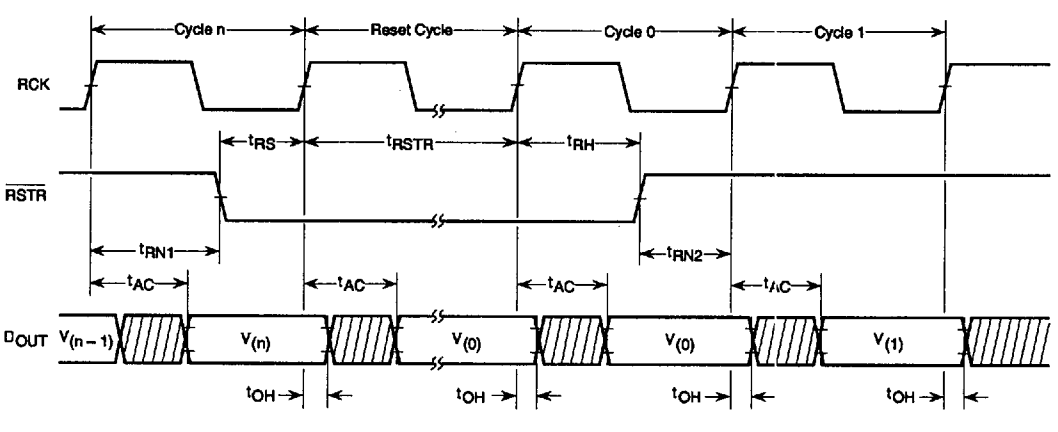
Write Reset Cycle



Notes:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

83IH-6706B

Read Reset Cycle

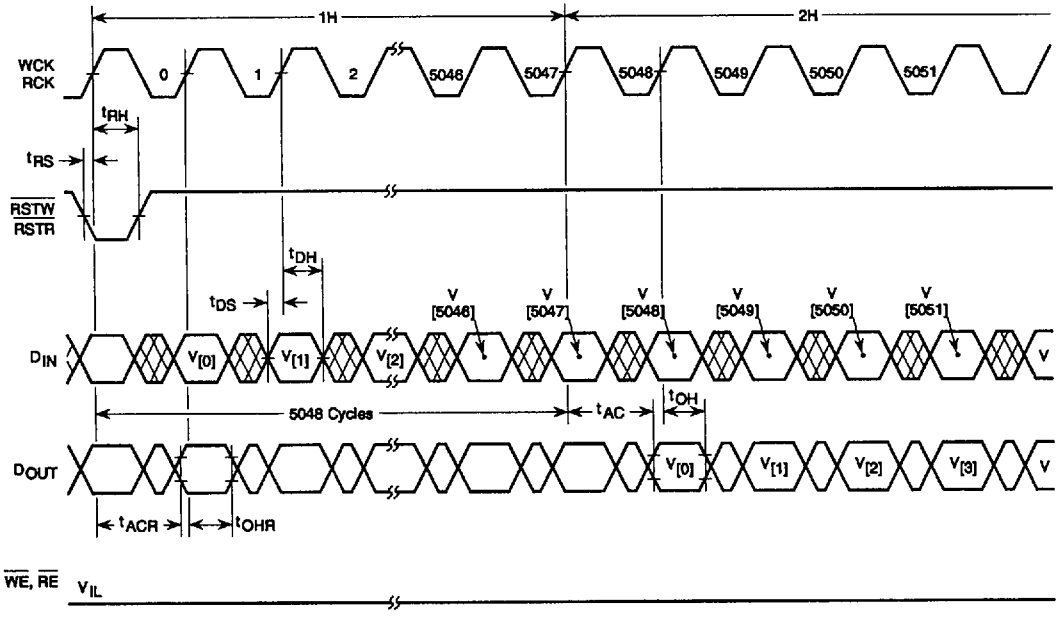


Notes:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

83IH-6707B

Timing Waveforms (cont)

5048-Bit Delay Line Cycle



Notes:

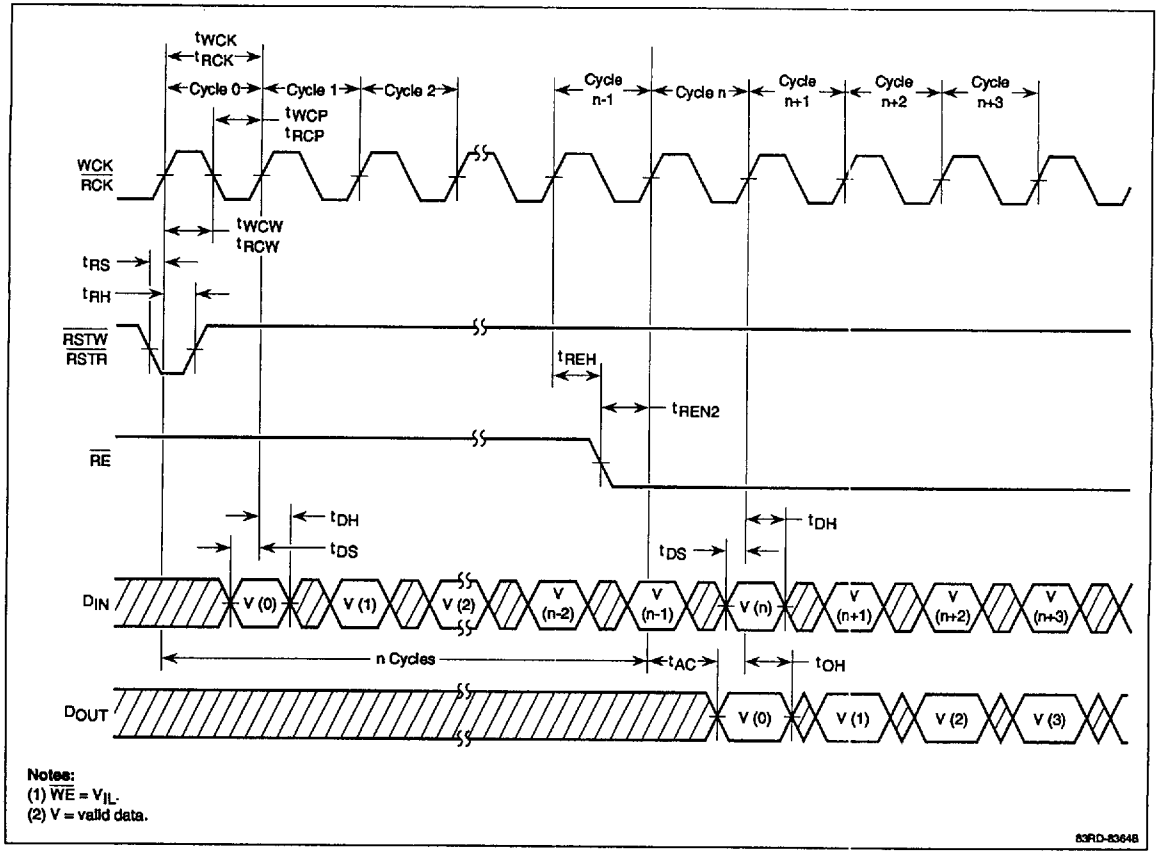
[1] V = valid data.

[2] 1H = the first group of 5048 bits.
2H = the second group of 5048 bits.

83rG-71788

Timing Waveforms (cont)

n-Bit Delay Line Cycle 3

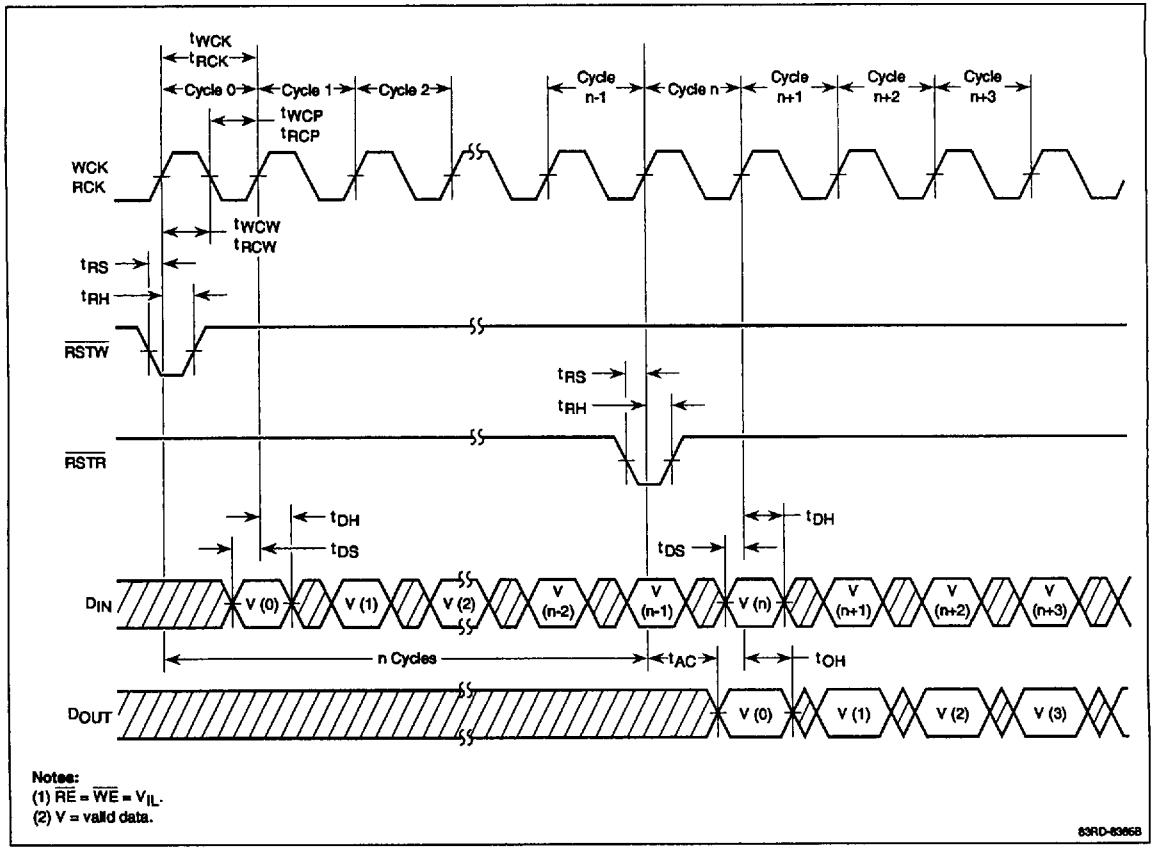


Notes:
(1) $\overline{WE} = V_{IL}$.
(2) V = valid data.

83RD-83648

Timing Waveforms (cont)

n-Bit Delay Line Cycle 2

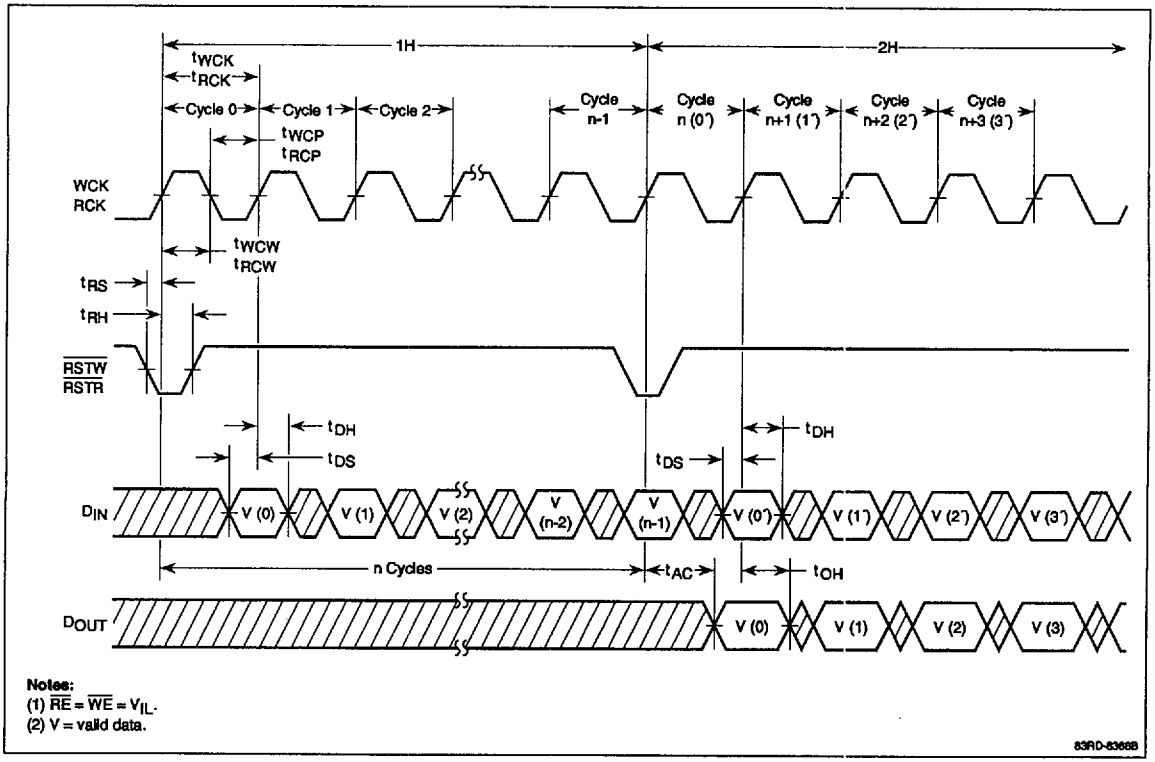


Notes:
(1) $\overline{RE} = \overline{WE} = V_{IL}$.
(2) V = valid data.

83RD-83668

Timing Waveforms (cont)

n-Bit Delay Line Cycle 1

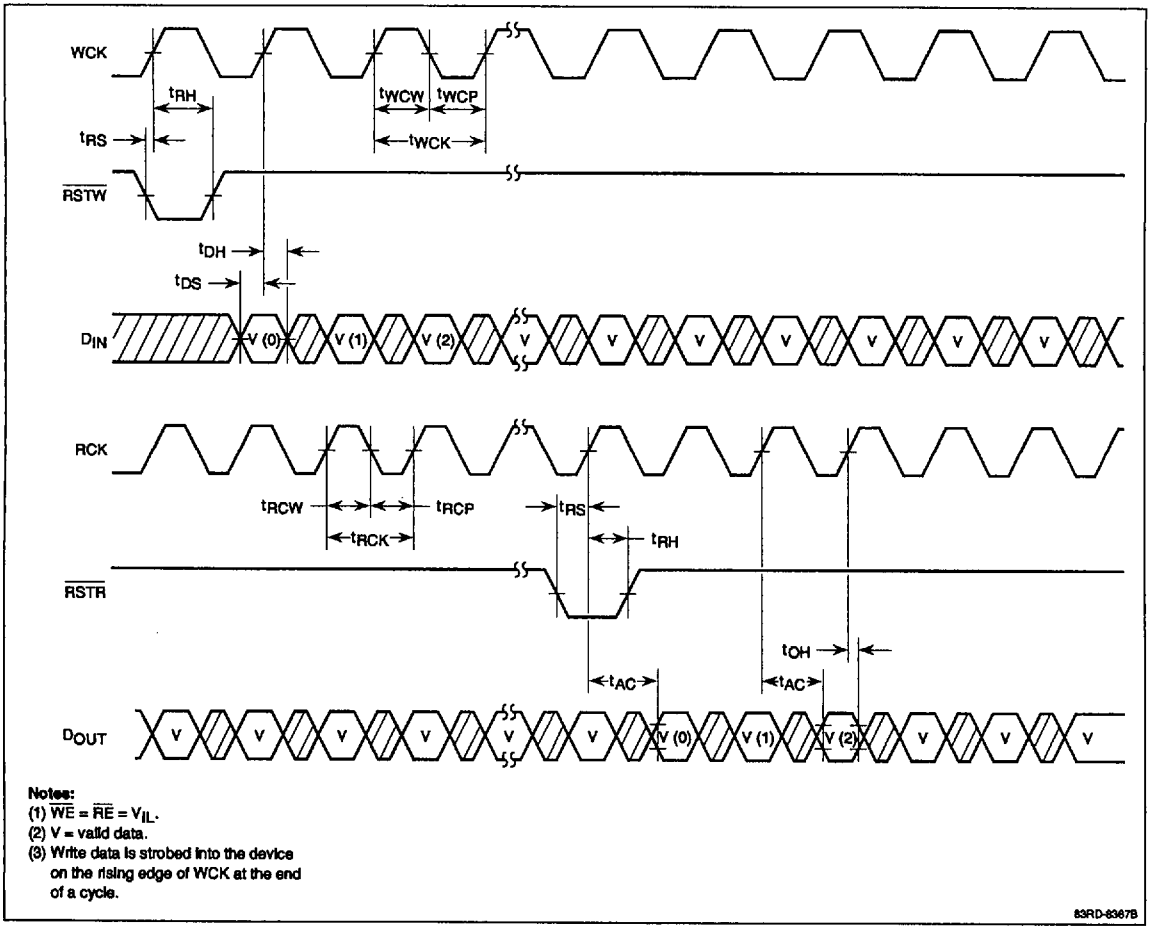


Notes:
(1) $\overline{RE} = \overline{WE} = V_{IL}$.
(2) V = valid data.

83RD-8368B

Timing Waveforms (cont)

Time Axis Conversion Cycle



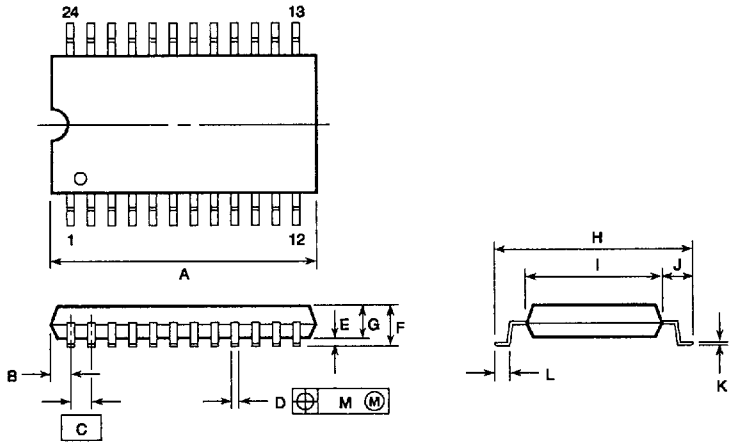
Notes:
(1) $\overline{WE} = \overline{RE} = V_{IL}$.
(2) V = valid data.
(3) Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83RD-8367B

Package Drawings

24-Pin Plastic SOP (450-mil)

Item	Millimeters	Inches
A	16.51 max	.650 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.1 $^{+0.2}_{-0.1}$	.004 $^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	12.2 ± 0.3	.480 $^{+.013}_{-.012}$
I	8.4	.331
J	1.9	.075
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.9 ± 0.2	.035 $^{+.009}_{-.008}$
M	0.12	.005

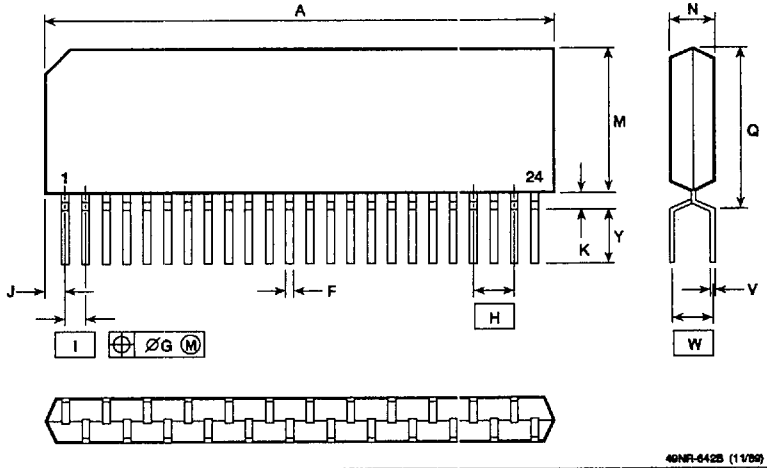


P24GM-50-450A

49NR-513B (6/91)

24-Pin Plastic ZIP (400-mil)

Item	Millimeters	Inches
A	31.75 max	1.250 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020



P24V-254-400A

49NR-642B (11/89)