LCD Segment / Common Driver With Controller

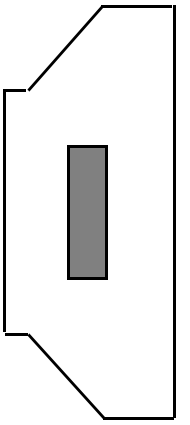
CMOS

SSD1809

SSD1809 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix graphic display system. It consists of 225 high voltage driving output pins for driving 160 Segments, 64 Commons and 1icon driving-Common.

SSD1809 displays data directly from its internal Graphic RAM (160x65). Data/Commands are sent from general MCU through a software selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

SSD1809 embeds a DC-DC Converter, an On-chip Bias Divider and an On-Chip Oscillator which reduce the number of external components. With the special design on minimizing power consumption and package layout, SSD1809 is suitable for any portable battery-driven application requiring a long operation period and a compact size.



SSD1809TR
TAB

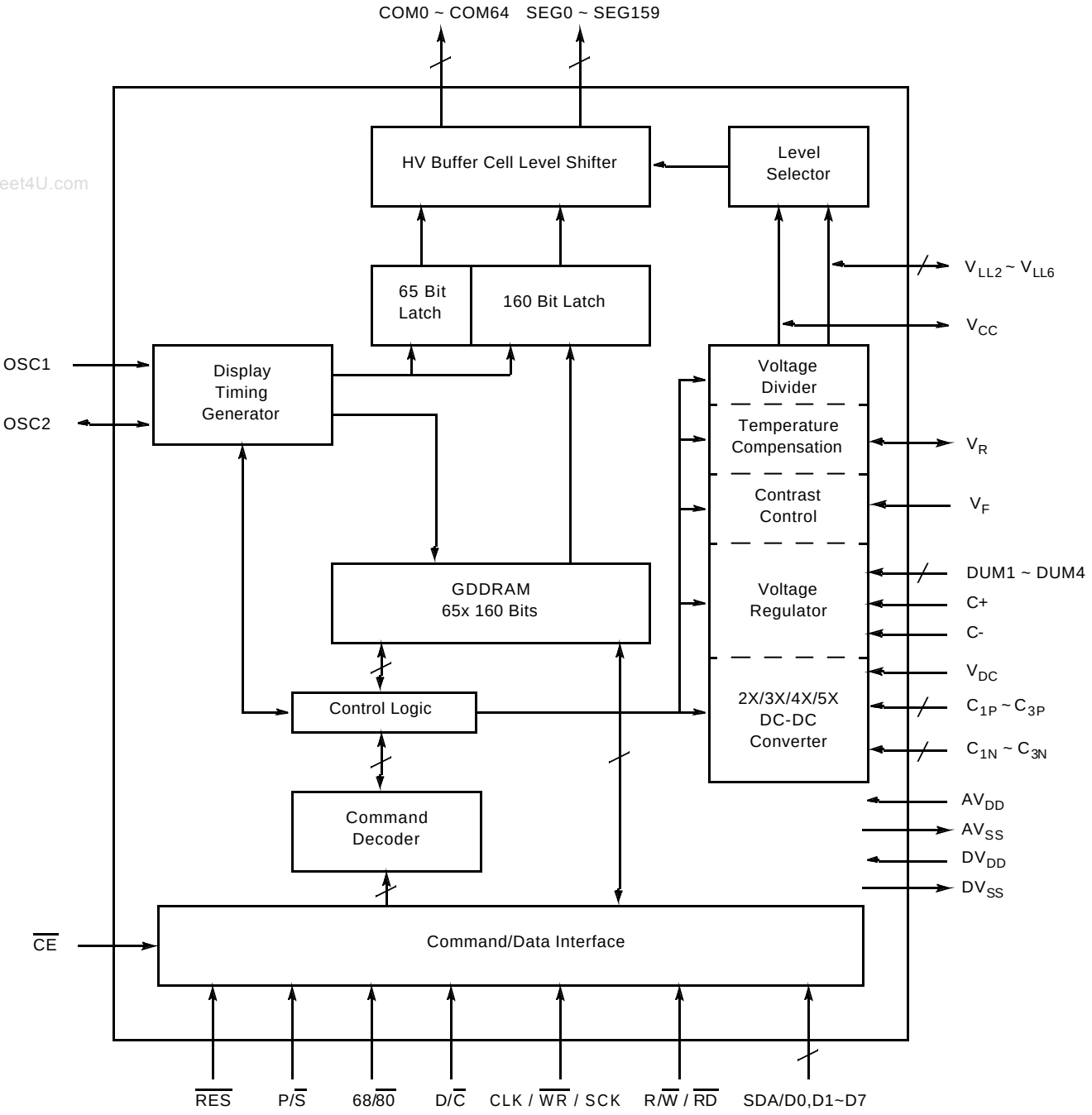
ORDERING INFORMATION

SSD1809TR TAB

- 160x64 Graphic Display with a Icon Line
- Programmable Multiplex Ratio (1 Mux - 65 Mux) [Partial Display]
- Graphic Display Mode Operation / Chinese Character Display Mode Operation
- Supply Operation, 2.2 V - 3.5 V
- Enhanced Low Power Icon Mode (160 icons, <19uA)
- On-Chip Internal DC-DC Converter / External Power Supply
- 2X / 3X / 4X / 5X DC-DC Converter
- On-Chip Oscillator
- On-Chip Bias Voltage Generator
- 1:5 / 1:7 / 1:8 / 1:9 Bias Ratio
- Maximum 16.5V LCD Driving Output Voltage
- 8-bit 6800-Series Parallel Interface, 8-bit 80-Series Parallel Interface and Serial Peripheral Interface (SPI)
- On-Chip 160 x 65 Display Data RAM
- Re-mapping of Row and Column Drivers
- Vertical Scrolling
- Display Masks for implementation of blinking effect
- Programmable Frame Frequency
- Master Clear RAM
- External Contrast Control
- 16 Level Internal Contrast Control
- Selectable LCD Driving Voltage Temperature Coefficients
- Available in TAB (Tape Automated Bonding)

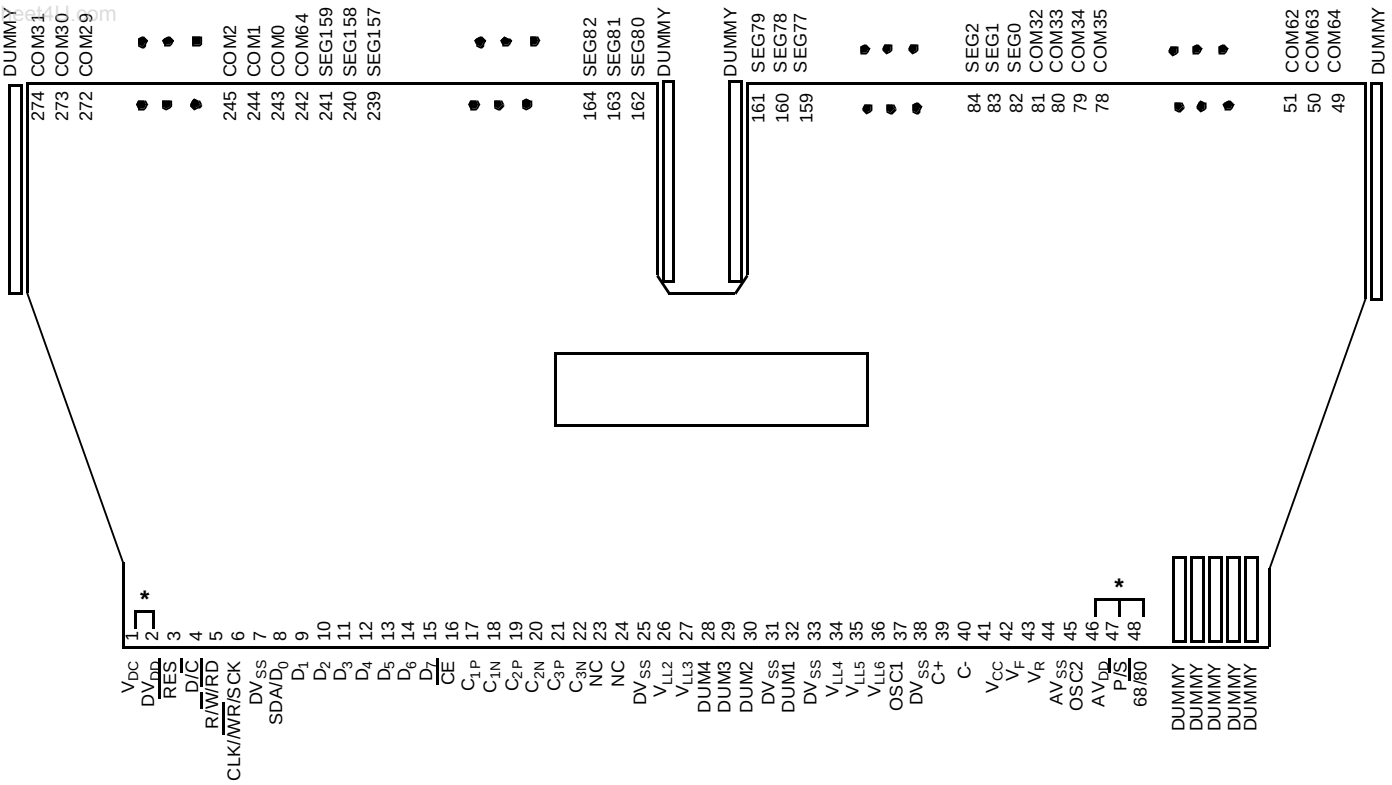
This document contains information on a new product. Specifications and information herein and subject to change without notice.

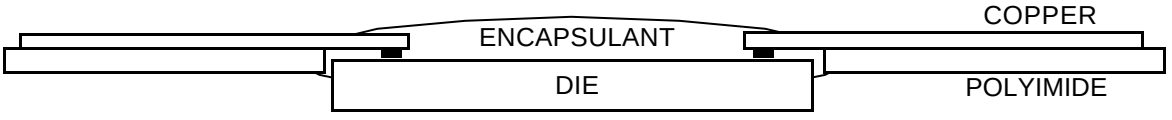
Block Diagram



SSD1809T PIN ASSIGNMENT

(COPPER VIEW)





Normal Design TAB

*Remarks: In the TAB package, pin1(VDC) & pin2(DVDD) are connected to DVDD. Pin46(AVDD), pin47(P/S) & pin48(68/80) are connected to AVDD.

SSD1809T Pin Assignment Table

TAB Pin #	Signal Name	TAB Pin #	Signal Name	TAB Pin #	Signal Name	TAB Pin #	Signal Name	TAB Pin #	Signal Name
1	V_{DC}	61	COM52	121	SEG39	181	SEG99	241	SEG159
2	$\underline{DV_{DD}}$	62	COM51	122	SEG40	182	SEG100	242	COM64
3	$\underline{RES}$	63	COM50	123	SEG41	183	SEG101	243	COM0
4	D/$\overline{C}$	64	COM49	124	SEG42	184	SEG102	244	COM1
5	R/$\overline{W}$ / $\underline{\overline{RD}}$	65	COM48	125	SEG43	185	SEG103	245	COM2
6	CLK/$\underline{\overline{WR}}$/SCK	66	COM47	126	SEG44	186	SEG104	246	COM3
7	DV_{SS}	67	COM46	127	SEG45	187	SEG105	247	COM4
8	SDA/D_0	68	COM45	128	SEG46	188	SEG106	248	COM5
9	D_1	69	COM44	129	SEG47	189	SEG107	249	COM6
10	D_2	70	COM43	130	SEG48	190	SEG108	250	COM7
11	D_3	71	COM42	131	SEG49	191	SEG109	251	COM8
12	D_4	72	COM41	132	SEG50	192	SEG110	252	COM9
13	D_5	73	COM40	133	SEG51	193	SEG111	253	COM10
14	D_6	74	COM39	134	SEG52	194	SEG112	254	COM11
15	$\underline{D_7}$	75	COM38	135	SEG53	195	SEG113	255	COM12
16	$\underline{CE}$	76	COM37	136	SEG54	196	SEG114	256	COM13
17	C_{1P}	77	COM36	137	SEG55	197	SEG115	257	COM14
18	C_{1N}	78	COM35	138	SEG56	198	SEG116	258	COM15
19	C_{2P}	79	COM34	139	SEG57	199	SEG117	259	COM16
20	C_{2N}	80	COM33	140	SEG58	200	SEG118	260	COM17
21	C_{3P}	81	COM32	141	SEG59	201	SEG119	261	COM18
22	C_{3N}	82	SEG0	142	SEG60	202	SEG120	262	COM19
23	NC	83	SEG1	143	SEG61	203	SEG121	263	COM20
24	NC	84	SEG2	144	SEG62	204	SEG122	264	COM21
25	DV_{SS}	85	SEG3	145	SEG63	205	SEG123	265	COM22
26	V_{LL2}	86	SEG4	146	SEG64	206	SEG124	266	COM23
27	V_{LL3}	87	SEG5	147	SEG65	207	SEG125	267	COM24
28	DUM4	88	SEG6	148	SEG66	208	SEG126	268	COM25
29	DUM3	89	SEG7	149	SEG67	209	SEG127	269	COM26
30	DUM2	90	SEG8	150	SEG68	210	SEG128	270	COM27
31	DV_{SS}	91	SEG9	151	SEG69	211	SEG129	271	COM28
32	DUM1	92	SEG10	152	SEG70	212	SEG130	272	COM29
33	DV_{SS}	93	SEG11	153	SEG71	213	SEG131	273	COM30
34	V_{LL4}	94	SEG12	154	SEG72	214	SEG132	274	COM31
35	V_{LL5}	95	SEG13	155	SEG73	215	SEG133		
36	V_{LL6}	96	SEG14	156	SEG74	216	SEG134		
37	OSC1	97	SEG15	157	SEG75	217	SEG135		
38	DV_{SS}	98	SEG16	158	SEG76	218	SEG136		
39	C+	99	SEG17	159	SEG77	219	SEG137		
40	C-	100	SEG18	160	SEG78	220	SEG138		
41	V_{CC}	101	SEG19	161	SEG79	221	SEG139		
42	V_F	102	SEG20	162	SEG80	222	SEG140		
43	V_R	103	SEG21	163	SEG81	223	SEG141		
44	AV_{SS}	104	SEG22	164	SEG82	224	SEG142		
45	OSC2	105	SEG23	165	SEG83	225	SEG143		
46	AV_{DD}	106	SEG24	166	SEG84	226	SEG144		
47	P/$\underline{S}$	107	SEG25	167	SEG85	227	SEG145		
48	68/$\underline{80}$	108	SEG26	168	SEG86	228	SEG146		
49	COM64	109	SEG27	169	SEG87	229	SEG147		
50	COM63	110	SEG28	170	SEG88	230	SEG148		
51	COM62	111	SEG29	171	SEG89	231	SEG149		
52	COM61	112	SEG30	172	SEG90	232	SEG150		
53	COM60	113	SEG31	173	SEG91	233	SEG151		
54	COM59	114	SEG32	174	SEG92	234	SEG152		
55	COM58	115	SEG33	175	SEG93	235	SEG153		
56	COM57	116	SEG34	176	SEG94	236	SEG154		
57	COM56	117	SEG35	177	SEG95	237	SEG155		
58	COM55	118	SEG36	178	SEG96	238	SEG156		
59	COM54	119	SEG37	179	SEG97	239	SEG157		
60	COM53	120	SEG38	180	SEG98	240	SEG158		

MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, T_A=25° C)

Symbol	Parameter	Value	Unit
AV_{DD},DV_{DD},V_{DC}	Supply Voltage	-0.3 to +4.0	V
V_{CC}		V_{SS}-0.3 to V_{SS}+18	V
V_{in}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

V_{SS} = AV_{SS} = DV_{SS} (DV_{SS} = V_{SS} of Digital circuit, AV_{SS} = V_{SS} of Analogue Circuit)

V_{DD} = AV_{DD} = DV_{DD} (DV_{DD} = V_{DD} of Digital circuit, AV_{DD} = V_{DD} of Analogue Circuit)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliability of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.2 to 3.5V, T_A=25° C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DV_{DD}	Logic Circuit Supply Voltage Range	(Absolute value referenced to V_{SS})	2.2	3.0	3.5	V
AV_{DD}	Voltage Generator Circuit Supply Voltage Range		2.2	-	3.5	V
V_{DC}	DC/DC Converter Circuit Supply Voltage Range		2.2	-	3.5	V
I_{AC}	Access Mode Supply Current Drain (AV_{DD} + DV_{DD} + V_{DC} Pins)	V_{DD}=3.0V, Voltage Generator On, 5X Converter Enabled, 65Mux Ratio, R/$\overline{W}$ accessing, T_{cyc}=200kHz, Internal Oscillator Enabled, Frame Freq.=60Hz, Display On.	-	-	450	µA
I_{DP}	Display Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Voltage Generator On, 5X Converter Enabled, 65Mux Ratio, R/$\overline{W}$ Halt, Internal Oscillator Enabled, Frame Freq.=60Hz, Display On.	-	170	270	µA
I_{SB}	Standby Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Display Off, Oscillator Disabled, R/$\overline{W}$ halt.	-	-	1	µA
I_{ICON}	Icon Mode Supply Current Drain (AV_{DD} + DV_{DD} Pins)	V_{DD}=3.0V, Internal Oscillator Enabled, 65Mux Ratio, Display On, Icon Mode C, R/$\overline{W}$ halt, Frame Freq.= 81.25Hz	-	11	19	µA
V_{CC}	LCD Driving Voltage Generator Output (V_{CC} Pin)	Display On, Voltage Generator Enabled, DC/DC Converter Enabled, Frame Freq.=60Hz, Voltage Regulator Enabled, Voltage Divider Enabled.	5	-	16.5	V
V_{LCD}	LCD Driving Voltage Input (V_{CC} Pin)	Voltage Generator Disabled, 1:5 Bias.	5	-	16.5	V
V_{OH1}	Output High Voltage (SDA/D_0-D_7, OSC2)	I_{out}=100mA	0.9*V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (SDA/D_0-D_7, OSC2)	I_{out}=100mA	0	-	0.1*V_{DD}	V
V_{R1}	LCD Driving Voltage Source (V_R Pin)	Voltage Regulator Enabled (V_R voltage depends on TC and Int/Ext Contrast Control)	0	-	V_{CC}-0.5	V
V_{R3}	LCD Driving Voltage Source (V_R Pin)	Regulated DC/DC Converter Mode	-	V_{CC}	-	V
V_{R2}	LCD Driving Voltage Source (V_R Pin)	Voltage Regulator & Regulated DC/DC Disabled.	-	Floating	-	V
V_{CN}	Internal Contrast Control (V_R Output Voltage)	Voltage Regulator Enabled, Internal Contrast control Enabled. (16 Voltage Levels Controlled by Software.)	-5	-	5	%

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.2 to 3.5V, T_A=25° C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH1}	Input high voltage ($\overline{RES}$, OSC2, CLK/$\overline{WR}$/SCK,SDA/D_0-D_7, $\overline{CE}$, R/$\overline{W}$/$\overline{RD}$, D/$\overline{C}$, P/$\overline{S}$, 68/$\overline{80}$, OSC1)		0.8*V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low voltage ($\overline{RES}$, OSC2, CLK/$\overline{WR}$/SCK,SDA/D_0-D_7, $\overline{CE}$, R/$\overline{W}$/$\overline{RD}$, D/$\overline{C}$, P/$\overline{S}$, 68/$\overline{80}$, OSC1)		0	-	0.2*V_{DD}	V
V_{LL6}	LCD Display Voltage Output	Voltage Divider Enabled, 1:5 bias ratio	-	V_R	-	V
V_{LL5}	(V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)		-	4/5*V_R	-	V
V_{LL4}			-	3/5*V_R	-	V
V_{LL3}			-	2/5*V_R	-	V
V_{LL2}			-	1/5*V_R	-	V
V_{LL6}	LCD Display Voltage Output	Voltage Divider Enabled, 1:7 bias ratio	-	V_R	-	V
V_{LL5}	(V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)		-	6/7*V_R	-	V
V_{LL4}			-	5/7*V_R	-	V
V_{LL3}			-	2/7*V_R	-	V
V_{LL2}			-	1/7*V_R	-	V
V_{LL6}	LCD Display Voltage Input	Voltage Divider Enabled, 1:8 bias ratio	-	V_R	-	V
V_{LL5}	(V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)		-	7/8*V_R	-	V
V_{LL4}			-	6/8*V_R	-	V
V_{LL3}			-	2/8*V_R	-	V
V_{LL2}			-	1/8*V_R	-	V
V_{LL6}	LCD Display Voltage Input	Voltage Divider Enabled, 1:9 bias ratio	-	V_R	-	V
V_{LL5}	(V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)		-	8/9*V_R	-	V
V_{LL4}			-	7/9*V_R	-	V
V_{LL3}			-	2/9*V_R	-	V
V_{LL2}			-	1/9*V_R	-	V
V_{LL6}	LCD Display Voltage Input	External Voltage Generator, Voltage Divider Disable	7	-	V_{CC}	V
V_{LL5}	(V_{LL6}, V_{LL5}, V_{LL4}, V_{LL3}, V_{LL2} Pins)		0	-	V_{LL6}	V
V_{LL4}			0	-	V_{LL5}	V
V_{LL3}			0	-	V_{LL4}	V
V_{LL2}			0	-	V_{LL3}	V
I_{OH}	Output High Current Source (SDA/D_0-D_7, OSC2)	V_{out}=V_{DD}-0.4V	50	-	-	µA
I_{OL}	Output Low Current Drain (SDA/D_0-D_7, OSC2)	V_{out}=0.4V	-	-	-50	µA
I_{OZ}	Output Tri-state Current Drain Source (SDA/D_0-D_7, OSC2)		-1	-	1	µA
I_{IL}/I_{IH}	Input Current ($\overline{RES}$, OSC2, CLK/$\overline{WR}$/SCK,SDA/D_0-D_7, $\overline{CE}$, R/$\overline{W}$/$\overline{RD}$, D/$\overline{C}$, P/$\overline{S}$, 68/$\overline{80}$, OSC1)		-1	-	1	µA
R_{on}	Channel resistance between LCD driving signal pins (SEG and COM) and driving voltage input pins (V_{LL2} to V_{LL6})	During Display on, 0.1V apply between two terminals, V_{CC} within operating voltage range	-	-	10	kΩ
V_{SB}	Memory Retention Voltage (DV_{DD})	Standby mode, retain all internal configuration and RAM data	2	-	-	V
C_{IN}	Input Capacitance (OSC1, OSC2, all logic pins)		-	5	7.5	pF
	Temperature Coefficient Compensation*					
PTC0	Flat Temperature Coefficient	TC1=0, TC2=0, Voltage Regulator Disabled	-	0.0	-	%
PTC3	Temperature Coefficient 3*	TC1=1, TC2=1, Voltage Regulator Enabled	-	-0.35	-	%

*The formula for the temperature coefficient (TC) is:

$$TC(\%) = \frac{V_R \text{ at } 50°\text{ C} - V_R \text{ at } 0°\text{ C}}{50°\text{ C} - 0°\text{ C}} \times \frac{1}{V_R \text{ at } 25°\text{ C}} \times 100\%$$

AC ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS}, V_{DD}=2.2 to 3.5V, T_A=25° C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC}	Oscillation Frequency of Display timing generator	Resistor between OSC1 andOSC2 is 900k W Internal Oscillator Enabled	-	50	-	kHz
F_{FRM}	Frame Frequency in Graphic / Character Display Mode	Normal Display Frequency	Fosc / [2 x Mux Ratio x (Frame Freq Register + 1)]			
		Half Display Frequency	Fosc / [4 x Mux Ratio x (Frame Freq Register + 1)]			
	Frame Frequency in Low Power Icon Mode	Icon Mode A and Normal Display Frequency	Fosc / [48 x (Frame Freq Register + 1)]			
		Icon Mode B and Normal Display Frequency	Fosc / [64 x (Frame Freq Register + 1)]			
		Icon Mode C and Normal Display Frequency	Fosc / [96 x (Frame Freq Register + 1)]			
		Icon Mode D and Normal Display Frequency	Fosc / [144 x (Frame Freq Register + 1)]			
		Icon Mode A and Half Display Frequency	Fosc / [96 x (Frame Freq Register +1)]			
		Icon Mode B and Half Display Frequency	Fosc / [128 x (Frame Freq Register + 1)]			
		Icon Mode C and Half Display Frequency	Fosc / [192 x (Frame Freq Register + 1)]			
		Icon Mode D and Half Display Frequency	Fosc / [288 x (Frame Freq Register + 1)]			
OSC	Internal Oscillation Frequency with different value of feedback resistor	Internal Oscillator Enabled, V_{DD} within operation range	See Figure 1 for the relationship			

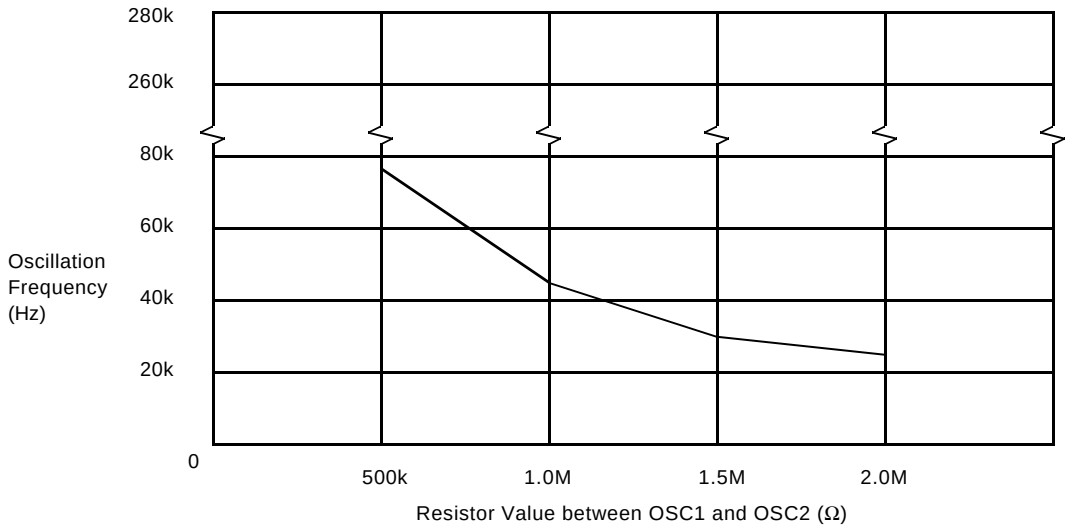


Figure 1 : Internal Oscillator Frequency Relationship with External Resistor Value at V_{DD} = 3V

Table 1 : Timing Characteristics for 6800-Series Parallel Interface (T_A=-30 to 85^{0}C, DV_{DD}=2.2 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	-	500	-	ns
t_{AS}	Address Setup Time	-	200	-	ns
t_{AH}	Address Hold Time	-	250	-	ns
t_{DS}	Data Setup Time for Write Cycle	-	350	-	ns
t_{DHW}	Data Hold Time for Write Cycle	-	250	-	ns
t_{DD}	Data Delay Time for Read Cycle	-	350	-	ns
t_{DHR}	Data Hold Time for Read Cycle	-	100	-	ns

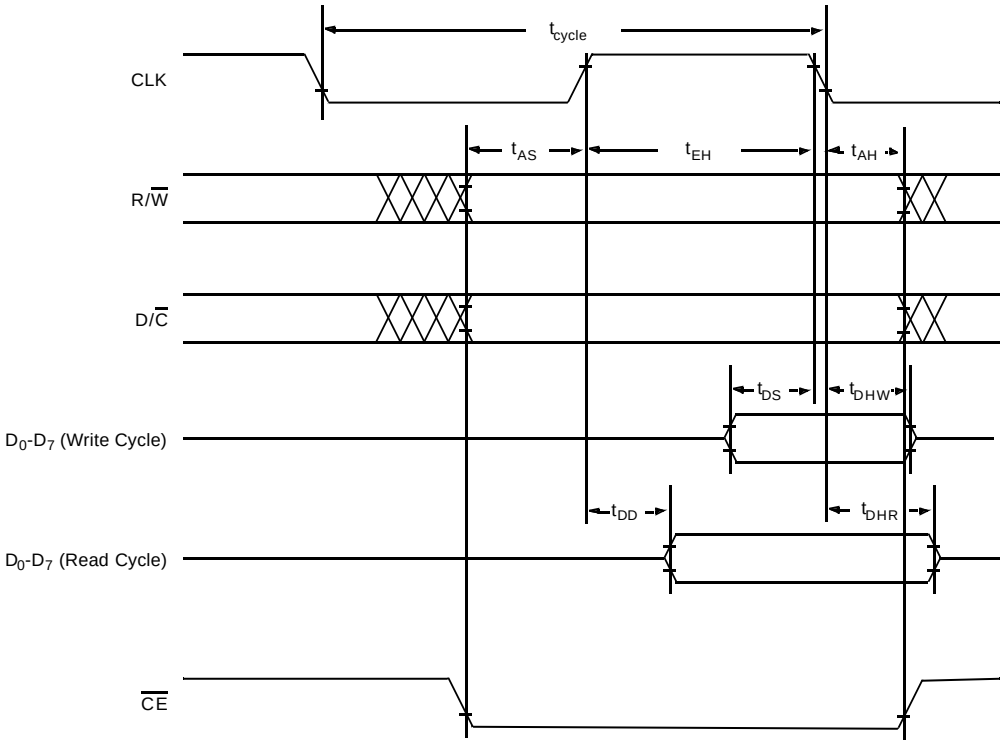


Figure 2 : Timing Characteristics for 6800-Series Parallel Interface

Table 2 : Timing Characteristics for 80-Series Parallel Interface (T_A=-30 to 85°C, DV_{DD}=2.2 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	-	500	-	ns
t_{AS}	Address Setup Time	-	200	-	ns
t_{AH}	Address Hold Time	-	250	-	ns
t_{DS}	Data Setup Time for Write Cycle	-	350	-	ns
t_{DHW}	Data Hold Time for Write Cycle	-	250	-	ns
t_{DD}	Data Delay Time for Read Cycle	-	350	-	ns
t_{DHR}	Data Hold Time for Read Cycle	-	100	-	ns

Note: In Read Cycle, the $\overline{WR}$ pin should be High. In Write Cycle, the $\overline{RD}$ pin should be High.

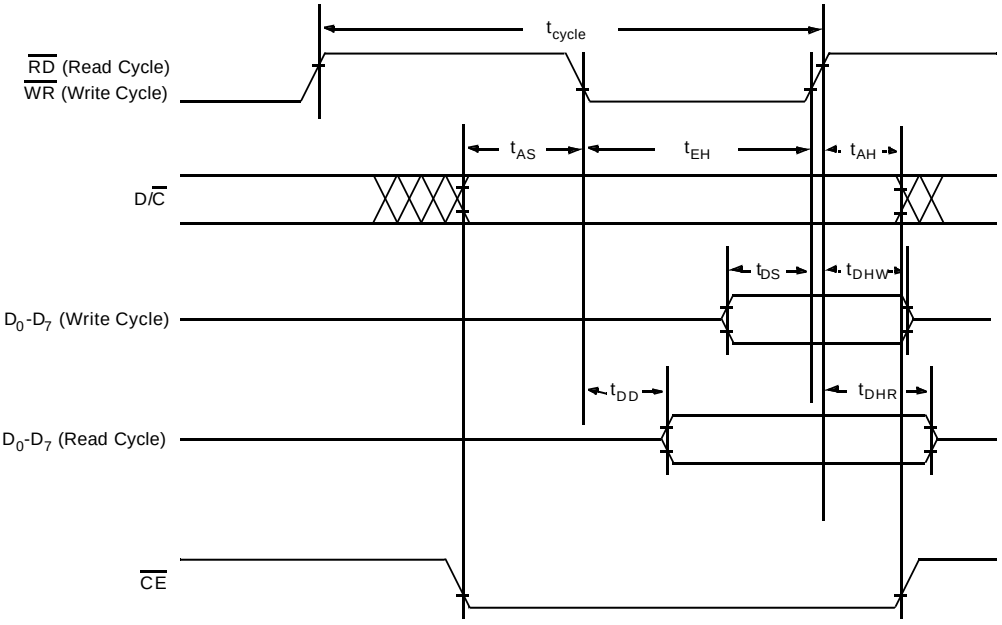


Figure 3 : Timing Characteristics for 80-Series Parallel Interface

Table 3 : Timing Characteristics for Serial Peripheral Interface (SPI) (T_A=-30 to 85°C, DV_{DD}=2.2 to 3.5V, V_{SS}=0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Enable Cycle Time	1000	-	-	ns
t_{EH}	Enable Pulse Width	-	500	-	ns
t_{AS}	Address Setup Time	-	200	-	ns
t_{AH}	Address Hold Time	-	250	-	ns
t_{DS}	Data Setup Time	-	350	-	ns
t_{DH}	Data Hold Time	-	250	-	ns
t_{LEAD}	Enable Lead Time	-	350	-	ns
t_{LAG}	Enable Lag Time	-	100	-	ns

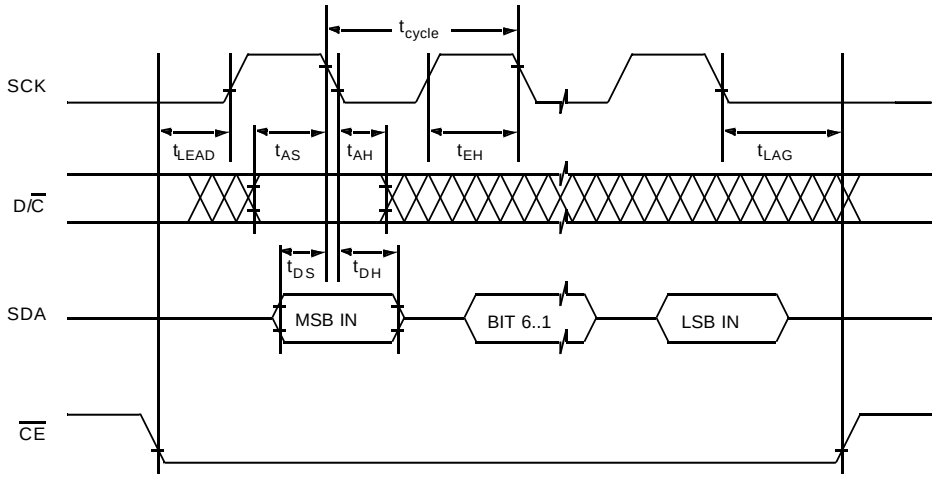


Figure 4 : Timing Characteristics for Serial Peripheral Interface (SPI)

PIN DESCRIPTIONS

P/$\overline{S}$ (Parallel / Serial Interface)

This pin is an input pin which is used to select parallel interface or serial interface. Input High for parallel interface (6800 or 80) while input Low for serial interface (SPI).

68/$\overline{80}$

This pin is an input pin which is used to select 6800 interface or 80 interface. Input High for 6800 interface while input Low for 80 interface.

D/$\overline{C}$ (Data / Command)

This input pin acknowledges the LCD driver that the input at SDA/D_0-D_7 is data or command. Input High for data while input Low for command.

$\overline{CE}$ (Chip Enable)

This pin is an input pin. The chip is enabled when this pin is Low.

CLK/ $\overline{WR}$ / SCK

When 6800-series parallel interface is selected, this input pin is named as CLK which is a clock. Data on SDA/D_0-D_7 are latched at the falling edge of CLK.

When 80-series parallel interface is selected, this input pin is named as $\overline{WR}$ which is a clock in write cycle. It is low enable for write data/command and data on SDA/D_0-D_7 are latched at the rising edge of $\overline{WR}$. In read cycle, this pin should be High.

When SPI is selected, this input pin is named as SCK which is a serial clock. Data on SDA /D_0 is latched at the falling edge of SCK.

$\overline{RES}$ (Reset)

An active Low pulse to this pin reset the internal status of the driver (same as power on reset). The minimum pulse width is 1 µs to initiate the reset process.

SDA / D_0-D_7 (Data)

SDA/D_0-D_7 is a bi-directional bus and is used for data/command transfer. If 6800-series or 80-series parallel interface is selected, D_0-D_7 are connected directly to MCU for data transfer.

When SPI is selected, D_0 is named as SDA which is a serial input of the driver. It receives data/command from MCU to driver and transfers serially. Meanwhile, D_1-D_7 pins can be High or Low.

R/$\overline{W}$ / $\overline{RD}$

When 6800-series parallel interface is selected, this input pin is named as R/$\overline{W}$, Input High will read the display data RAM or the internal status (Busy/Idle) while input Low will write the display data RAM or the internal setup registers.

When 80-series parallel interface is selected, this input pin is named as $\overline{RD}$ and is a clock in read cycle. It is low enable for read data/command and data SDA/D_0-D_7 are latched at the rising edge of $\overline{RD}$. In write cycle, this pin should be High.

When SPI is selected, this input pin can be High or Low.

OSC1 (Oscillator Input)

For internal oscillator mode, this is an input pin for the internal low power RC oscillator circuit. In this mode, an external resistor of certain value should be connected between the OSC1 and OSC2 pins for a range of internal operating frequencies (refer to Figure 1). For external oscillator mode, OSC1 should be left open.

OSC2 (Oscillator Output / External Oscillator Input)

For internal oscillator mode, this is an output for the internal low power RC oscillator circuit. For external oscillator mode, OSC2 will be an input pin for external clock and no external resistor is needed.

V_{LL6} - V_{LL2}

Group of voltage level pins for driving the LCD panel. They can either be connected to external driving circuit for external bias supply or connected internally to built-in divider circuit if internal divider is enable. For internal Voltage Generator enabled, a 1.0µF capacitor to AV_{SS} is required on each pin.

DUM1 - DUM4

If the internal bias voltage levels generator is enabled, a 1µF capacitor to AV_{SS} is required on each pin.

C_{1N} and C_{1P}, C_{2N} and C_{2P}, C_{3N} and C_{3P}

If internal Voltage Generator is enabled with 2X DC-DC converter, a 0.1µF capacitor is required to connect between C_{1N} & C_{1P}.

If internal Voltage Generator is enabled with 3X/4X DC-DC converter, a 0.1µF capacitor is required to connect between C_{1N} & C_{1P} and C_{3N} & C_{3P}.

If internal Voltage Generator is enabled with 5X DC-DC converter, a 0.1µF capacitor is required to connect these three pair of pins.

C+ and C-

If internal divider circuit is enabled, a 1µF capacitor is required to connect between these two pins.

V_R and V_F

This is a feedback path for the gain control (external contrast control) of V_{LL2} to V_{LL6}. For adjusting the LCD driving voltage, it requires a feedback resistor placed between V_R and V_F, a gain control resistor placed between V_F and AV_{SS}, a 4.7µF capacitor placed between V_R and AV_{SS}. (Refer to the Application Circuit)

COM0-COM64 (Row Drivers)

These lines provide the LCD row driving signals to the LCD panel. COM64 also serves as the common driving signal in the icon mode. Output is 0V during display off.

SEG0-SEG159 (Column Drivers)

These 160 pins provide LCD column driving signal to LCD panel. Output is 0V during display off.

AV_{DD} and AV_{SS}

AV_{DD} and AV_{SS} are the positive supply and ground to all of the analog circuit respectively.

V_{CC}

For using the internal Voltage Generator, a 0.1µF capacitor from this pin to AV_{SS} is required. It can also be an external bias input pin if internal Voltage Generator is not used. Power is supplied to the LCD Driving Level Selector and HV Buffer Cell with this pin. Normally, this pin is not intended to be a power supply to other components.

DV_{DD} and DV_{SS}

Power is supplied to the digital control circuit and DC/DC converter of the driver using these two pins. DV_{DD} is power and DV_{SS} is ground.

V_{DC}

V_{DC} is the power supply to the DC/DC converter of the driver.

Remark: In SSD1809T TAB package, V_{DC} pin is connected to DV_{DD} and P/S pin & 68/80 pin are connected to AV_{DD}. Only 6800-parallel interface can be used and DV_{DD} will be the supply of the DC/DC converter in this package.

OPERATION OF LIQUID CRYSTAL DISPLAY DRIVER

Description of Block Diagram Module

Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ is high, data is written to Graphic Display Data RAM (GDDRAM). If D/$\overline{C}$ is low, the input at SDA/D_0-D_7 is interpreted as a Command and it will be decoded and written to the corresponding command register.

Reset is of the same function as Power ON Reset (POR). Once $\overline{RES}$ receives a negative reset pulse of minimium 1µs, all internal circuit will be back to its initial status.

MPU 6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), R/$\overline{W}$, D/$\overline{C}$, $\overline{CE}$, and CLK. R/$\overline{W}$ input High indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register.R/$\overline{W}$ input Low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The chip is enabled when the $\overline{CE}$ is low and the CLK input serves as data latch signal (clock). Refer to Figure 2 showing timing characteristics for 6800-series parallel interface.

MPU 80-Series Parallel Interface

The parallel interface consists of 8 bi-directional data pins (D_0-D_7), $\overline{RD}$, $\overline{WR}$, D/$\overline{C}$, and $\overline{CE}$. $\overline{RD}$ input serves as data read latch signal (clock) provided that $\overline{CE}$ is low. $\overline{WR}$ input serves as data write latch signal(clock) provided that $\overline{CE}$ is low. Whether it is display data or command register write is controlled by D/$\overline{C}$. Refer to Figure 3 showing timing characteristics for 80-series parallel interface.

MPU Serial Peripheral Interface

The serial interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$, and $\overline{CE}$. The chip is enabled when $\overline{CE}$ is low and SDA is shifted into a 8-bit shift register on every falling edge of SCK and data are transferred serially with MSB first and LSB last. D/$\overline{C}$ is sampled on every first clock of each byte cycle and the information is interpreted as Display Data or Command accordingly.

The eight bits information from SDA pin are stored in a buffer shift register. After the next byte information from SDA pin is written into the buffer, the original contents in the buffer will be sent to Display Data RAM or Command Register. A No-Operation (01101000) command could be written to push the last information in the buffer into Display RAM or Command Register.

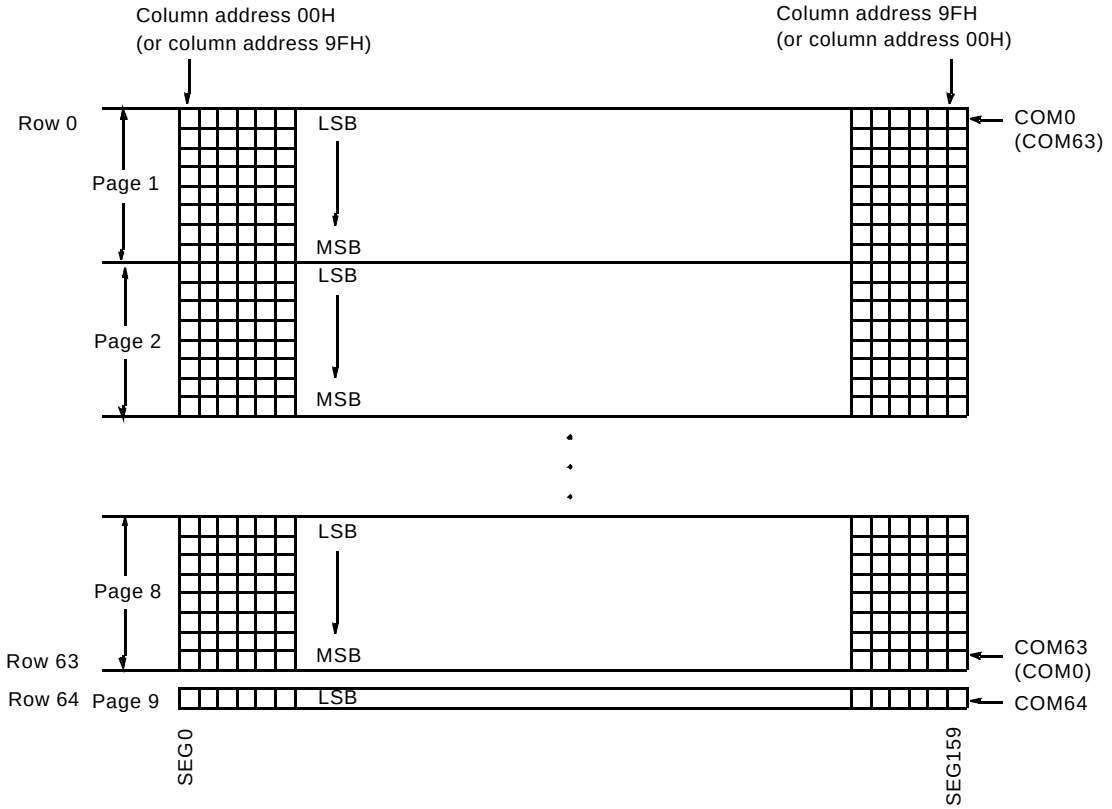
The first bit after the $\overline{CE}$ pin falling edge or the $\overline{RES}$ pin rising edge is always interpreted as MSB.

Refer to Figure 4 showing timing characteristics for Serial Peripheral Interface.

Selection of Interface

Selection of the desired interface is done by putting P/$\overline{S}$ and 68/$\overline{80}$ either high or low as shown in the following table:-

PIN	6800-Series	80-Series	SPI
P/$\overline{S}$	High	High	Low
68/$\overline{80}$	High	Low	High/Low



Note : The configuration in parentheses represent the remapping of Rows and Columns

Figure 5 : Graphic Display Data RAM (GDDRAM) Address Map

Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is determined by number of row times the number of column (160x65 = 10400 bits). Figure 5 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs are provided.

Display Timing Generator

This module is an on chip low power RC oscillator circuitry (Figure 6). The oscillator frequency can be selected in the range of 25kHz to 200kHz by external resistor. One can enable the circuitry by software command. For external clock provided, feed the clock to OSC2 and leave OSC1 open.

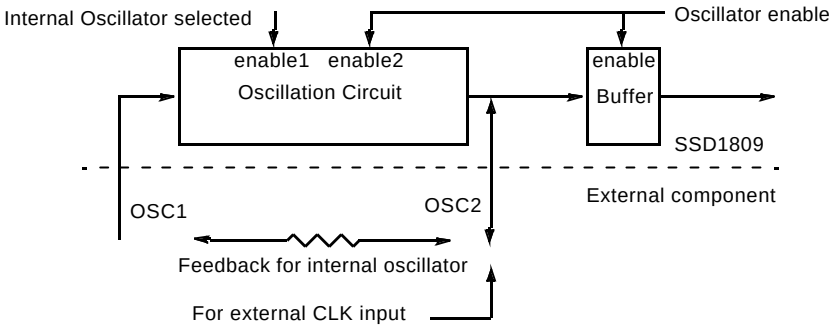


Figure 6 : Oscillator Circuitry

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generate necessary bias voltages. It consists of :

1. 2X, 3X, 4X and 5X DC-DC Converter
   To generate the V_{CC} voltage. 2X, 3X and 4X DC-DC converter are used for LCD panel which needs lower driving voltage for less power consumption. 5X DC-DC converter is used for LCD panel which needs higher driving voltage.
2. Voltage Regulator
   Feedback gain control for initial LCD voltage. it can also be used with external contrast control.
3. Voltage Divider
   Divide the LCD display voltage (V_{LL2}-V_{LL6}) from the regulator output. This is a low power consumption circuit which can save the most display current compare with traditional resistor ladder method.
4. Self adjust temperature compensation circuitry
   Provide 2 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control.
5. Contrast Control Block
   Software control of 16 voltage levels of LCD voltage.
   All blocks can be individually turned off if external voltage generator is employed.

65 Bit Latch / 160 Bit Latch

A 225 bit long register which carries the display signal information. First 65 bits are Common driving signals and other 160 bits are Segment driving signals. Data will be input to the HV-buffer Cell for bumping up to the required level.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell for output signal voltage pump.

HV Buffer Cell (Level Shifter)

HV Buffer Cell works as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

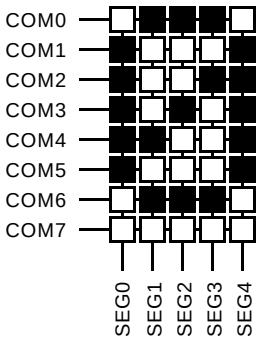


Figure 7a : LCD Display Example " 0"

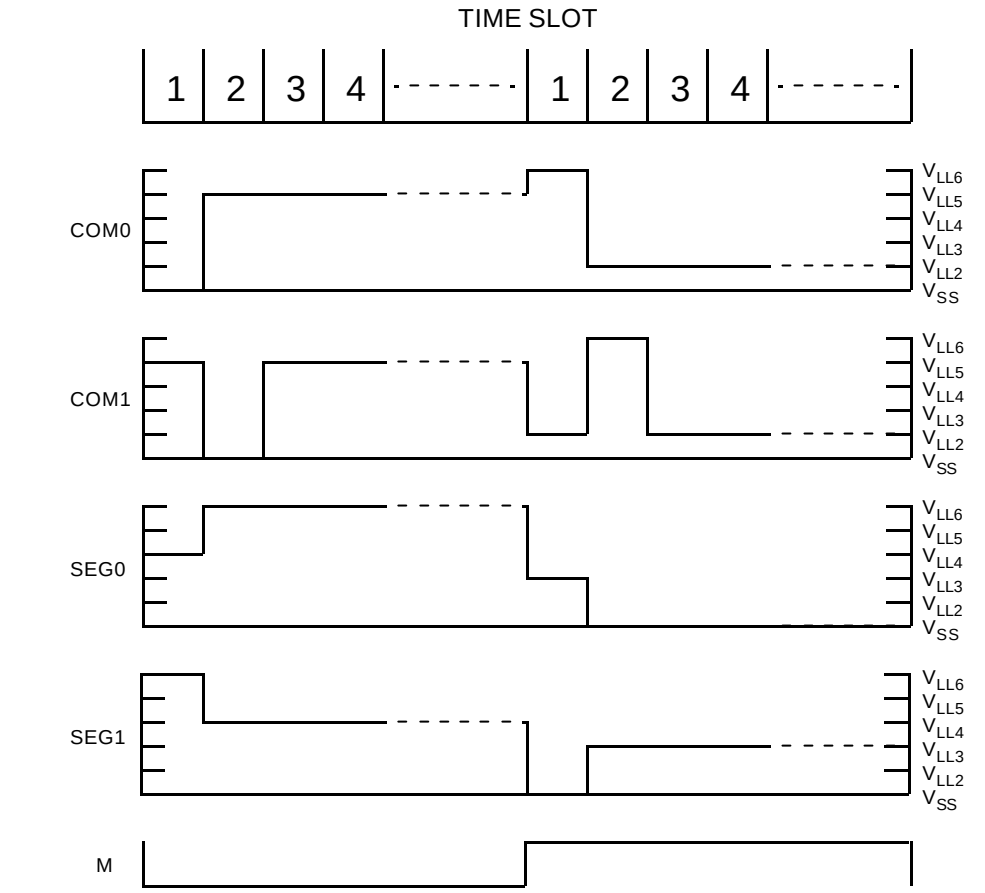


Figure 7b : LCD Driving Signal from SSD1809

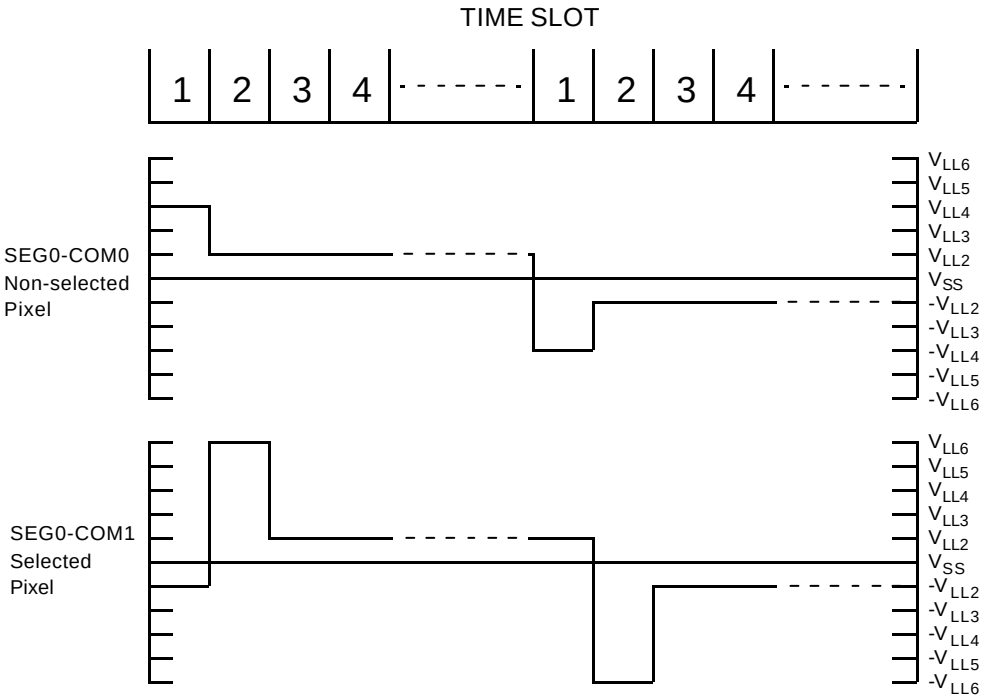


Figure 7c : Effective LCD waveform on LCD pixel

Command Description

Display On (Display Mode)

This command turns the LCD Common and Segment outputs on. This command starts the conversion of data in GDDRAM to necessary waveforms on the Common and Segment driving outputs. The on-chip bias generator is also turned on by this command. (Note : "Oscillator On" command should be sent before "Display On" is selected)

Display Off (Stand-by Mode)

This command turns the display off and the states of the LCD driver are as follow during display off :

1. The Common and Segment outputs are fixed at V_{SS}.
2. The Bias Voltage Generator is turned off.
3. The RAM and content of all registers are retained.
4. IC will accept new commands and data.

The Oscillator is not affected by this command.

Set GDDRAM Column Address

This command positions the address pointer on a column location. The address can be set to location 00H-9FH (160 columns) and the MSB is software set by "set MSB of GDDRAM Column Address". The column address will be increased automatically after a read or write operation. Refer to " Address Increment Table" and command " Set GDDRAM Page Address" for further information.

Set GDDRAM Page Address

This command positions the row address to 1 of 9 possible positions in GDDRAM. Refer to figure 5.

Save / Restore Column Address

Save Column Address command saves a copy of the Column Address of GDDRAM. Restore Column Address command restores the copy obtained from the previous execution of saving column address. This instruction is very useful for writing full graphics characters that are larger than 8 pixels vertically.

Master Clear GDDRAM

This command is to clear the content of the Display Data RAM to zero. Issue this command followed by a dummy write data.

Master Clear Icon RAM

This command is used to clear the content of the Icon Data RAM to zero. Set the page pointer to icon page (page 9) and then issue this command followed by a dummy write data.

Set Page Mask

This command is used to define the page which will be masked. Once the command " Set Page Mask" is issued, the next command will be written to the Page Mask Register which is an 8-bit register. Each bit represents one of the 8 pages: page mask bit 0 represents Page 1, page mask bit 1 represents Page 2, ... etc.

Enable Page Mask

When the Page Mask is enabled, the display of those pages, with page mask bit set, will be cleared. Meanwhile, the data in the display RAM is retained.

Enable Icon Mask

When the Icon Mask is enabled, the display of the icons will be cleared. Meanwhile, the data in the icon display RAM is retained.

Set Logical Page Mask

This command is used to select the page mask type. There are two page mask types 1) Physical page mask and 2)Logical page mask. Physical mask refers to a physical location of the panel which cannot be moved by scrolling, row remap or panel offset. Logical page mask refers to the location of GDDRAM. Therefore a logical mask will keep masking a definite area of GDDRAM content when the contain is moved along the panel by scrolling, row remap or panel offset.

Set Display Mode

This command switches the driver to full display mode or icon display mode. In low power icon mode, only icons (driven by COM64) are displayed. The DC-DC converter, the voltage generator and the regulator are disabled. All V_{CC}, V_{LL}s pins cannot have external bias voltage supply in the low power icon mode. Refer " Set Icon Mode" for further information.

Set Icon Mode

This command is used to select one of 4 smart icon modes.

In smart icon mode A, on-pixels are stressed by a voltage with root-mean-square value of $1xV_{DD}$ whereas off-pixels by $0.58xV_{DD}$.

In smart icon mode B, on-pixels are stressed by a voltage with root-mean-square value of $0.87xV_{DD}$ whereas off-pixels by $0.5xV_{DD}$.

In smart icon mode C, on-pixels are stressed by a voltage with root-mean-square value of $0.71xV_{DD}$ whereas off-pixels by $0.41xV_{DD}$.

In smart icon mode D, on-pixels are stressed by a voltage with root-mean-square value of $0.58xV_{DD}$ whereas off-pixels by $0.33xV_{DD}$.

Remark: Icon Mode cannot be used if external divider is used.

Set Display Frequency

In half display frequency mode, the display frame frequency will be halved. Also, the operation frequency of analog circuitries will be halved as well.

Set Frame Frequency

This command is used to select one of 16 frame frequencies from Fosc/(2 x Mux Ratio) to Fosc/(32 x Mux Ratio). When the " Frame Frequency " command is issued, the following command will be written to the " Frame Frequency Register" which is used to define the desired frame frequencies.

Set Bias Ratio

This command sets the bias of 1:5, 1:7, 1:8 or 1:9 bias for the divider output. The selection should match the characteristic of LCD Panel.

Oscillator Enable

This command is used to either turn on / off Oscillator. For using internal or external oscillator, this command should be executed. The setting for this command is not affected by command " Set Display On/ Off" . See command " Ext/Int Oscillator" for more information

Ext / Int Oscillator

This command is used to select either internal or external oscillator. When internal oscillator is selected, feedback resistor between OSC1 and OSC2 is needed. For external oscillation circuit, feed clock input signal to OSC2 and leave OSC1 open.

Voltage Generator Enable

This command is used to enable the internal Voltage Generator to generate the V_{CC} from AV_{DD}. Disable the voltage generator if external

Vcc is provided.

Set 2X / 3X / 4X / 5X Converter

This command selects the usage of 2X / 3X / 4X / 5X Converter when the internal voltage Generator is enabled.

Set DC/DC Converter Mode

This command sets the DC/DC converter to regulated mode. In regulated mode, V_{CC} voltage equals to V_R voltage.

Voltage Regulator Enable

This command enables regulator which consists of the internal contrast control and temperature compensation circuits.

Internal Voltage Divider Enable

If the internal divider is disabled, external bias can be used for V_{LL6} to $V_{LL2.}$ If the internal divider is enabled, the internal circuit will generated the 1:5 / 1:7 / 1:8 / 1:9 bias driving voltage.

Internal Contrast Control Enable

This command is used to adjust the delta voltage of the bias voltages. With bit option = 1, the software selection for delta bias voltage control is enabled. With bit option = 0, internal contrast control is disabled.

Increase / Decrease Contrast Level

If the internal contrast control is enabled, this command is used to increase or decrease the contrast level within the 16 contrast levels.

Set Contrast Level

This command is used to select one of the 16 contrast levels from 10h to 1Fh when internal contrast control circuitry is in use.

Set Temperature Coefficient

This command can select 2 different LCD driving voltage temperature coefficients to match various liquid crystal temperature grades. Those temperature coefficients are specified in Electrical Characteristics Tables.

Set MUX Ratio / Chinese Character Mode (Partial Display)

This command is used to select the Graphic display mode with different Mux from 2 Mux to 65 Mux or the Chinese character display mode with different character line from 1 line to 3 lines. Figure 8a & 8b in the section " Display Output Description" show the 65 Mux Graphic display mode and 3-line Chinese character display mode respectively.

Set Row Re-Mapping

This instruction selects the mapping of Display Data RAM to Common drivers for mechanical flexibility. There are 2 mappings:

1. Row(0) - Row(Mux ratio-2) of GDDRAM mapped to COM(first display row location) - COM(first display row location+Mux ratio-2). Example is illustrated in figure 8b, the first display row location is COM0 and the Mux ratio is 53, then Row0 of GDDRAM wil be mapped to COM0, Row1 through Row 51 of GDDRAM will be mapped to COM1 to COM51.

2. Row(0) - Row(Mux ratio-2) of GDDRAM mapped to COM(first display row location+Mux ratio-2) - COM(first display row location). Example is illustrated in figure 8c, Row0 - Row51 of GDDRAM is mapped to COM51 - COM0.

Set Column Re-Mapping

This instruction selects the mapping of new Display Data RAM to Segment drivers for mechanical flexibility. There are 2 mappings to select:

1. Column 0 - Column 159 of GDDRAM mapped to SEG0-SEG159 respectively;
2. Column 0 - Column 159 of GDDRAM mapped to SEG159-SEG0 respectively.

Detailed information please refer to Figure 8d in the section " Display Output Description" .

Set Vertical Scroll Value

In Graphic display mode, this command maps the selected GDDRAM rows (00H-3FH) to COM pins. With scroll value equals to 0, Row 0 of GDDRAM is mapped to COM0 and Row 1 through Row 63 are mapped to COM1 through COM63 respectively. With scroll value equal to 1, Row 1 of GDDRAM is mapped to COM0, then Row 2 through Row 63 will be mapped to COM1 through COM62 respectively and Row 0 will be mapped to COM63.

In Chinese character display mode, there are 73 rows of display content including space and icon. This command moves the display content downward equals to the value stored vertical scrolling register.

Set Display Rows Location

This command is used to define the first row location of the display, the first row can be started at COM0 to COM63. Example is given in Figure 8h.

Display Output Description

This is an example of output pattern on the LCD panel. Figure 8a shows the content in GDDRAM and Figure 8b - 8h illustrate the output patterns on the LCD display with a sequence of commands:

1) Set 3-line Chinese character display mode shown in Figure 8b,
2) Enable row re-mapping shown in Figure 8c,
3) Enable column re-mapping & rewrite RAM content shown in Figure 8d,
4) Enable vertical scrolling command with scrolling value of 07h shown in Figure 8e,
5) Disable row re-mapping & column re-mapping and rewrite map content shown in Figure 8f,
6) Enable vertical scrolling command with scrolling value of 3Eh shown in Figure 8g and
7) Set display rows location at 06h shown in Figure 8h.

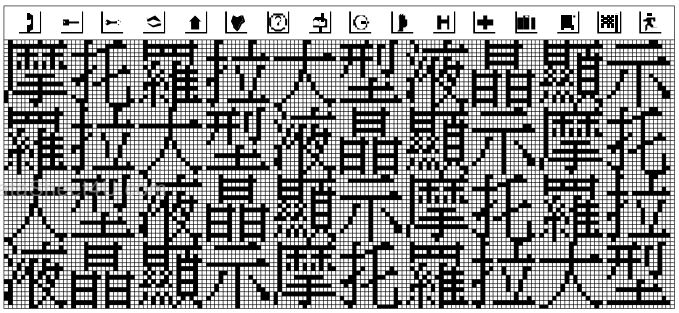


Figure 8a: Content in GDDRAM

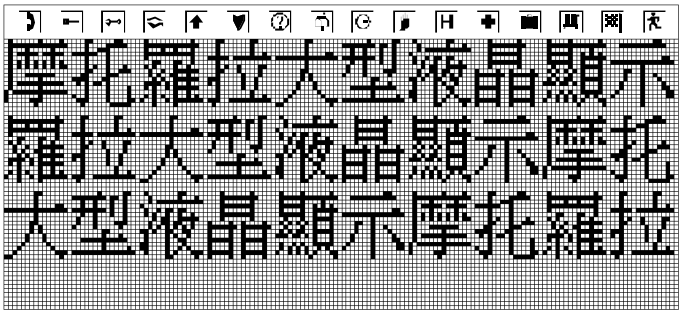


Figure 8b: 3-line Chinese character mode

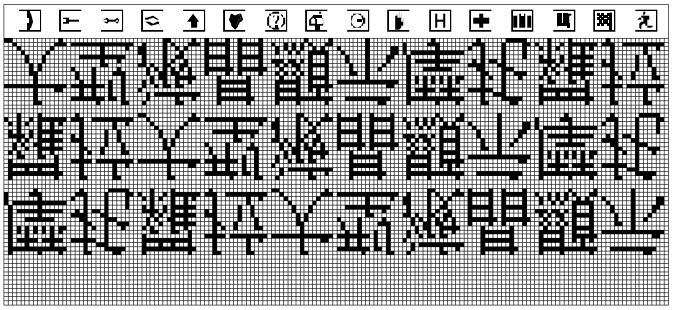


Figure 8c: Row remap enable

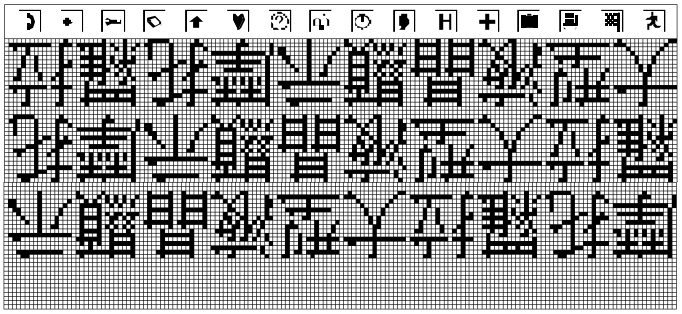


Figure 8d: Column remap enable & Re-write RAM content

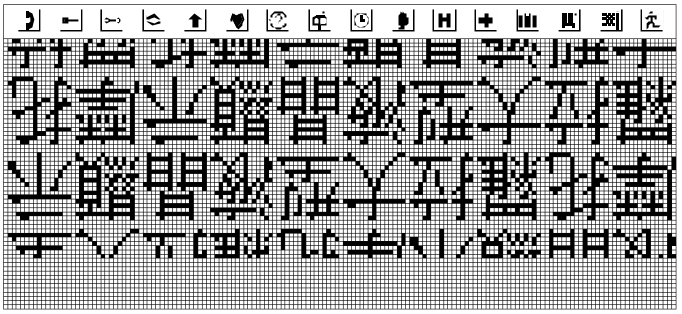


Figure 8e: Vertical scrolling with writing 07h to scrolling register

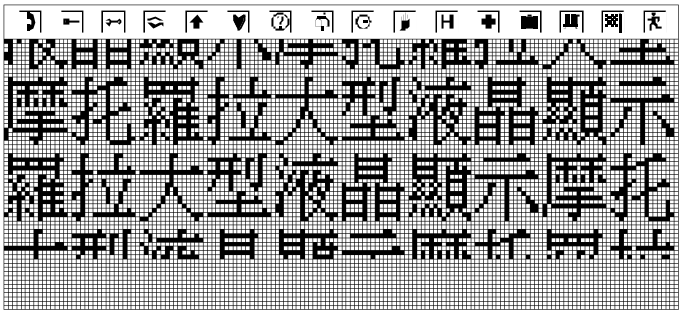


Figure 8f: Disable row re-mapping & column re-mapping and Rewrite map content.

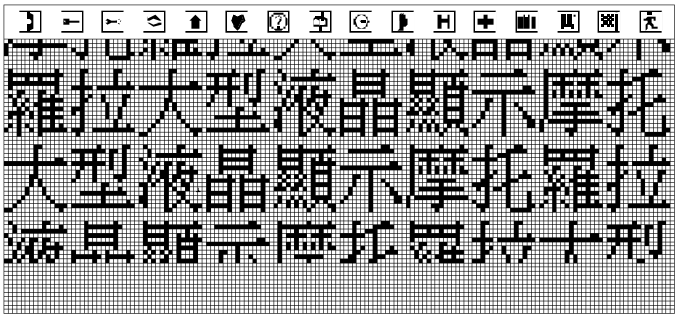


Figure 8g: Vertical scrolling with writing 3Eh to scrolling register

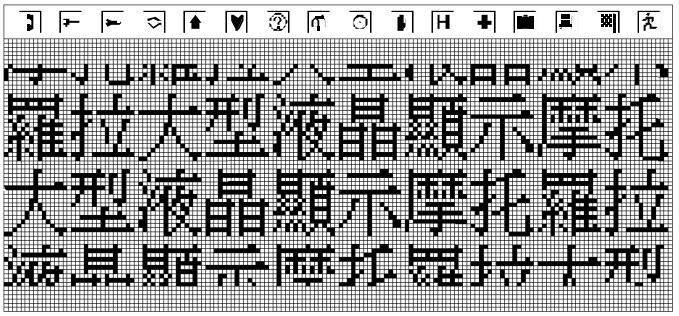


Figure 8h: Centering with display rows locatiion 06h

COMMAND TABLE

Bit Pattern	Command	Comment
$0000X_3X_2X_1X_0$	Set GDDRAM Page Address	Set GDDRAM Page Address using $X_3X_2X_1X_0$ as address bits. $X_3X_2X_1X_0$=0000 : page 1 (POR) $X_3X_2X_1X_0$=0001 : page 2 $X_3X_2X_1X_0$=0010 : page 3 $X_3X_2X_1X_0$=0011 : page 4 $X_3X_2X_1X_0$=0100 : page 5 $X_3X_2X_1X_0$=0101 : page 6 $X_3X_2X_1X_0$=0110 : page 7 $X_3X_2X_1X_0$=0111 : page 8 $X_3X_2X_1X_0$=1000 : page 9
00001001	Set Display Rows Location	Next Command (byte) on D_5 ~ D_0 defines the display rows location. Starts at Row0 - COM0 (POR)
$0000101X_0$	Set 2X/3X DC-DC Converter	X_0=0 : Enable 2X Converter X_0=1 : Enable 3X Converter Remark: This command overrides “Set 4X/5X DC-DC Converter” .
$000011X_1X_0$	Reserved	
00001110	Reserved	
$0001X_3X_2X_1X_0$	Set Contrast Level	Set one of the 16 contrast level values using $X_3X_2X_1X_0$ as data bits. Reset to 0000 during POR.
00001111	Reserved	
$0010000X_0$	Set 4X / 5X DC-DC Converter	X_0=0: Enable 4X Converter (POR) X_0=1: Enable 5X Converter Remark: This command overrides “Set 2X/3X DC-DC Converter” .
$0010001X_0$	Set Segment Re-Mapping	X_0=0 : Column 0 to SEG0 (POR) X_0=1 : Column 0 to SEG159
$0010010X_0$	Set Common Re-Mapping	X_0=0 : Row 0 to Display Row location (POR) X_0=1: Flip the Row-COM mapping.
$0010011X_0$	Set MSB of GDDRAM Column Address	X_0=0: MSB = 0 (POR) X_0=1: MSB = 1
$0010100X_0$	Set Display on/off	X_0=0: Display off (POR) X_0=1: Display on
$0010101X_0$	Voltage Generator Enable	X_0=0: Disable Voltage Generator (POR) X_0=1: Enable Voltage Generator
$0010110X_0$	Voltage Regulator Enable	X_0=0: Disable Regulator (POR) X_0=1: Enable Regulator When application uses a supply with built-in temperature compensation, the regulator should be disabled.
$0010111X_0$	Voltage Divider Enable	X_0=0: Disable Voltage Divider (POR) X_0=1: Enable Voltage Divider When an external bias network is preferred, the voltage divider should be disabled.
$0011000X_0$	Internal Contrast Control Enable	X_0=0: Disable Internal Contrast Control(POR) X_0=1: Enable Internal Contrast Control Internal contrast circuits can be disabled if external contrast circuits is preferred.
$0011001X_0$	Set Display Frequency	X_0=0 : Normal display frequency (POR) X_0=1 : Half display frequency
$0011010X_0$	Save/Restore GDDRAM Column Address	X_0=0 : Restore address X_0=1 : Save address

Bit Pattern	Command	Comment
00110110	Master Clear GDDRAM	Master clear GDDRAM (160 X 64 bits)
00110111	Master Clear Icons RAM	Master Clear of Icons RAM
0011100X_0	Set Bias Ratio 1:9 or 1:7	X_0=0 : bias = 1 : 9 (POR) X_0=1 : bias = 1 : 7 Remark: This command overrides “Set Bias 1:8 or 1:5”.
0011101X_0	Reserved	
0011110X_0	Set Bias Ratio 1:8 or 1:5	X_0=0 : bias = 1 : 8 X_0=1 : bias = 1 : 5 Remark: This command overrides “Set Bias 1:9 or 1:7”.
0011111X_0	Set Display Mode	X_0=0 : Low power icon display mode X_0=1 : Normal display mode (POR)
01000000	Set Vertical Scroll	Next command will be written to vertical scroll register. Scroll register=0 upon POR
01000001	Set Page Mask	Next command (byte) will be written to page mask register. Page mask register=0 upon POR
0100001X_0	Set Logical Page Mask	X_0=0 : Enable Physical Page Mask (POR) X_0=1 : Enable Logical Page Mask
0100010X_0	Enable Page Mask	X_0=0 : Disable page mask (POR) X_0=1 : Enable page mask
0100011X_0	Enable Icon Mask	X_0=0 : Disable icon mask (POR) X_0=1 : Enable icon mask
010010X_1X_0	Reserved	
010011X_1X_0	Reserved	
0101$X_3X_2X_1X_0$	Reserved	
011000X_1X_0	Reserved	
011001X_1X_0	Set Icon Mode	X_1X_0=00 : Icon Mode A X_1X_0=01 : Icon Mode B X_1X_0=10 : Icon Mode C (POR) X_1X_0=11 : Icon Mode D Remark: Icon Mode cannot be used if external divider is used.
0110100X_0	No operation	
01101010	Set Mux Ratio / Chinese Character Mode	Next command (byte) on D_7~D_0 defines the size of panel. D_7=0 : Graphic Mode $D_5D_4D_3D_2D_1D_0$ = 000000 : 1 graphic row (2 Mux) $D_5D_4D_3D_2D_1D_0$ = 000001 : 2 graphic rows (3 Mux) $D_5D_4D_3D_2D_1D_0$ = 000010 : 3 graphic rows (4 Mux) : : : $D_5D_4D_3D_2D_1D_0$ = 111110 : 63 graphic rows (64 Mux) $D_5D_4D_3D_2D_1D_0$ = 111111 : 64 graphic rows (65 Mux) (POR) *D_6 : Don’t care. D_7 = 1 : 16-Point Chinese Character Mode D_1D_0 = 00 - 1 character row (17 Mux) D_1D_0 = 01 - 2 character rows (35 Mux) D_1D_0 = 10 - 3 character rows (53 Mux) *D_6~D_2 : Don’t care.

Bit Pattern	Command	Comment
01101011	Set Frame Frequency	Next command (byte) on D_3~D_0 will be written to the Frame Frequency Register. $D_3D_2D_1D_0$ = 0000 : Frame Frequency Register = 0 $D_3D_2D_1D_0$ = 0001 : Frame Frequency Register = 1 $D_3D_2D_1D_0$ = 0010 : Frame Frequency Register = 2 : : : $D_3D_2D_1D_0$ = 0101 : Frame Frequency Register = 5 (POR) : : : $D_3D_2D_1D_0$ = 1111 : Frame Frequency Register = 15 *D_7~D_4 : Don't care.
011011X_1X_0	Set Temperature Coefficient	X_1X_0=00: 0.00% (POR) X_1X_0=11: -0.35%
0111000X_0	Increase/Decrease Contrast Value	X_0=0: Decrease by one level X_0=1: Increase by one level
0111001X_0	Reserved	
0111010X_0	Set DC-DC Converter Mode	X_0=0 : Normal Mode (POR) X_0=1 : Regulated Mode
0111011X_0	Reserved	
01111000	Reserved	
01111001	Reserved	
0111101X_0	Set External / Internal Oscillator	X_0=0: Internal Oscillator (POR) X_0=1: External Oscillator For internal oscillator mode, place a resistor between OSC1 and OSC2 pins. For external oscillator mode, feed clock input to OSC2 pin.
0111110X_0	Reserved	
0111111X_0	Set Oscillator Enable	X_0=0: Oscillator Master Disable(POR) X_0=1: Oscillator Master Enable This is the master control for oscillator circuitry. This command should be issued after the "External/Internal Oscillator" command.
1$X_6X_5X_4X_3X_2X_1X_0$	Set GDDRAM Column Address	Set GDDRAM Column Address.Use $X_6X_5X_4X_3X_2X_1X_0$ as address bits. MSB of the address set by " Set MSB of GDDRAM column address command.

Data Read / Write

6800-Series Parallel Interface

To read data from the GDDRAM, input High to R/$\overline{W}$ pin and D/$\overline{C}$ pin. Data are valid at the falling edge of CLK. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input Low to R/$\overline{W}$ pin and High to D/$\overline{C}$ pin. Data which fulfil the data setup time, are input to the LCD driver at the falling edge of CLK. And the GDDRAM column address pointer will be increased by one automatically.

80-Series Parallel Interface

To read data from the GDDRAM, input High to $\overline{WR}$ pin and D/$\overline{C}$ pin and $\overline{RD}$ is used as a clock input. Data are valid at the rising edge of $\overline{RD}$. And the GDDRAM column address pointer will be increased by one automatically.

To write data to the GDDRAM, input High to $\overline{RD}$ pin and D/$\overline{C}$ pin and $\overline{WR}$ pin is used as a clock input. Data which fulfil the data setup time, are input to the LCD driver at the rising edge of $\overline{WR}$. And the GDDRAM column address pointer will be increased by one automatically.

SPI Interface

Input High to D/$\overline{C}$ pin to write data to the GDDRAM. Data which fulfil the data setup time, are input to the LCD driver at the falling edge of SCK. And the GDDRAM column address pointer will be increased by one automatically.

Read data from GDDRAM is not available.

No auto address pointer increment will be performed for the Dummy Write Data after Master Clear GDDRAM. (Refer to the "Commands Required for R/W Actions on RAM" Table)

Address Increment Table (Automatic)

Comment	Address Increment	Remarks
Write Command	No	
Read Command	No (invalid mode)	*1
Write Data	Yes	*2, *3
Read Data	Yes	*3

Address Increment is done automatically data read write. The column address pointer of GDDRAM*3 is affected.

Remarks : *1. Only data is read from RAM.

*2. If write data is issued after Command Clear RAM, Address increase is not applied.

*3. Column Address will be wrapped round when overflow.

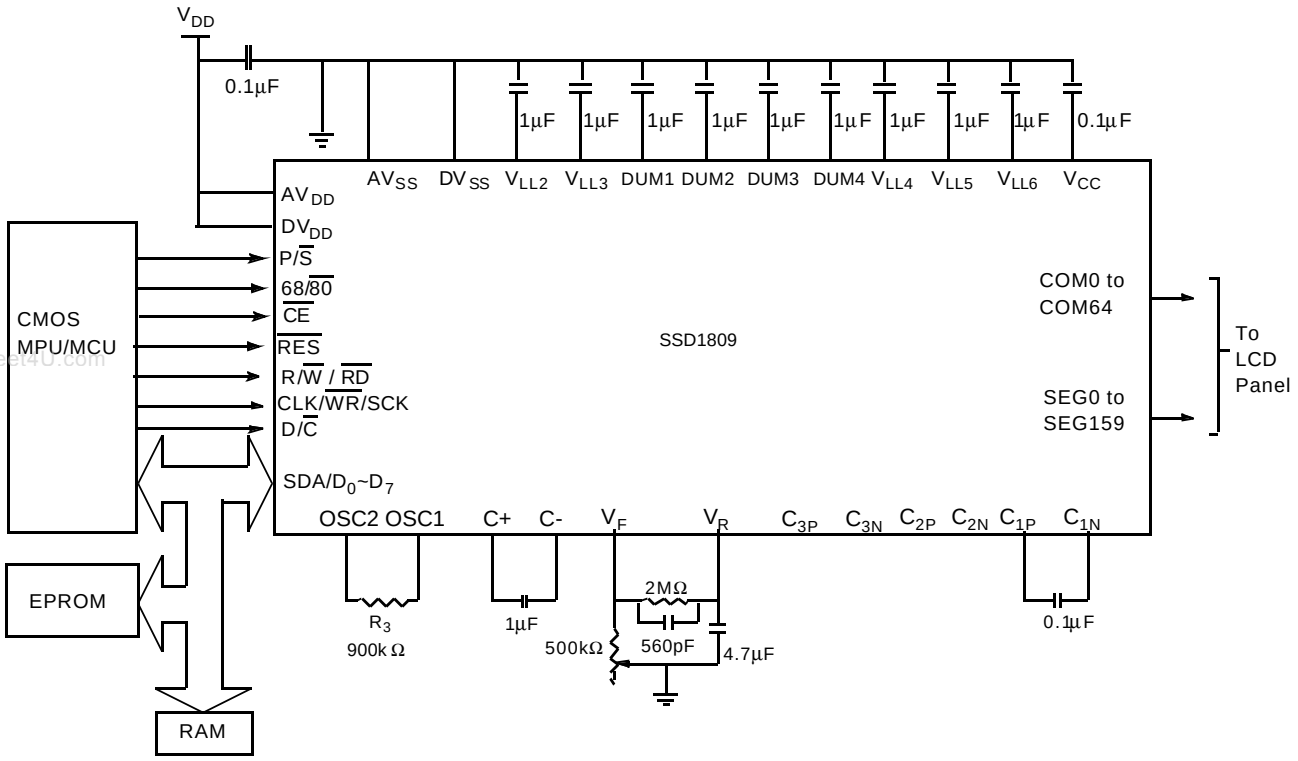
Commands Required for R/$\overline{W}$ Actions on RAM

R/$\overline{W}$ Actions on RAMs	Commands Required	
Read/Write Data from/to GDDRAM.	Set GDDRAM Page Address Set MSB of GDDRAM Column Address Set GDDRAM Column Address Read/Write Data	(000000X_1X_0)* (0010011X_0)* (1$X_6X_5X_4X_3X_2X_1X_0$)* ($X_7X_6X_5X_4X_3X_2X_1X_0$)
Save/Restore GDDRAM Column Address.	Save/Restore GDDRAM Column Address.	(0011010X_0)
Master Clear GDDRAM	Set Clear Page GDDRAM (160 x 64 bits) Dummy Write Data	(00110110) ($X_7X_6X_5X_4X_3X_2X_1X_0$)
Master Clear Icon RAM	Set GDDRAM Page Address to Page 9 Master Clear Icon RAM (160 bits) Dummy Write Data	(00001001)* (00110111) ($X_7X_6X_5X_4X_3X_2X_1X_0$)

* No need to resend the command again if it is set previously.

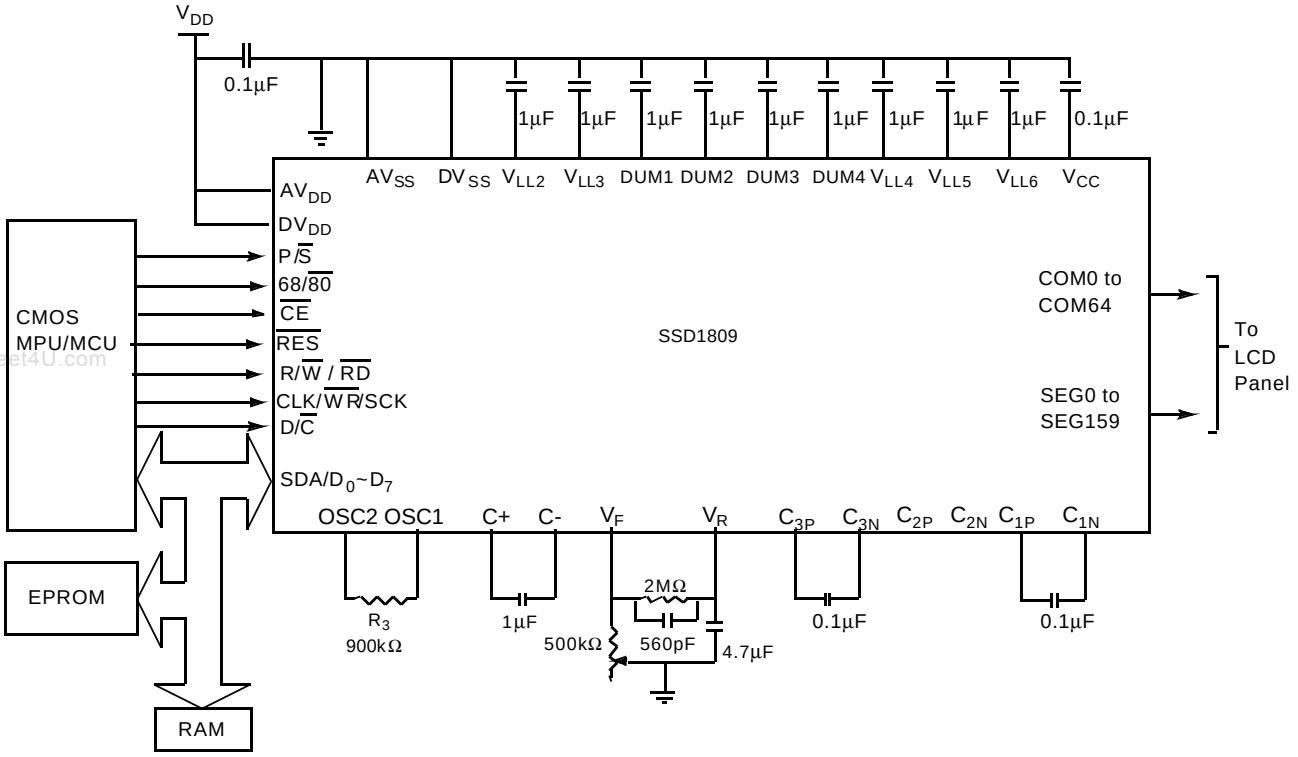
The read / write action to the Display Data RAM does not depend on the display mode. This means the user can change the RAM content whether the target RAM content is being displayed.

Application Circuit for 2X DC-DC converter: (All Internal Analog Block Enabled)



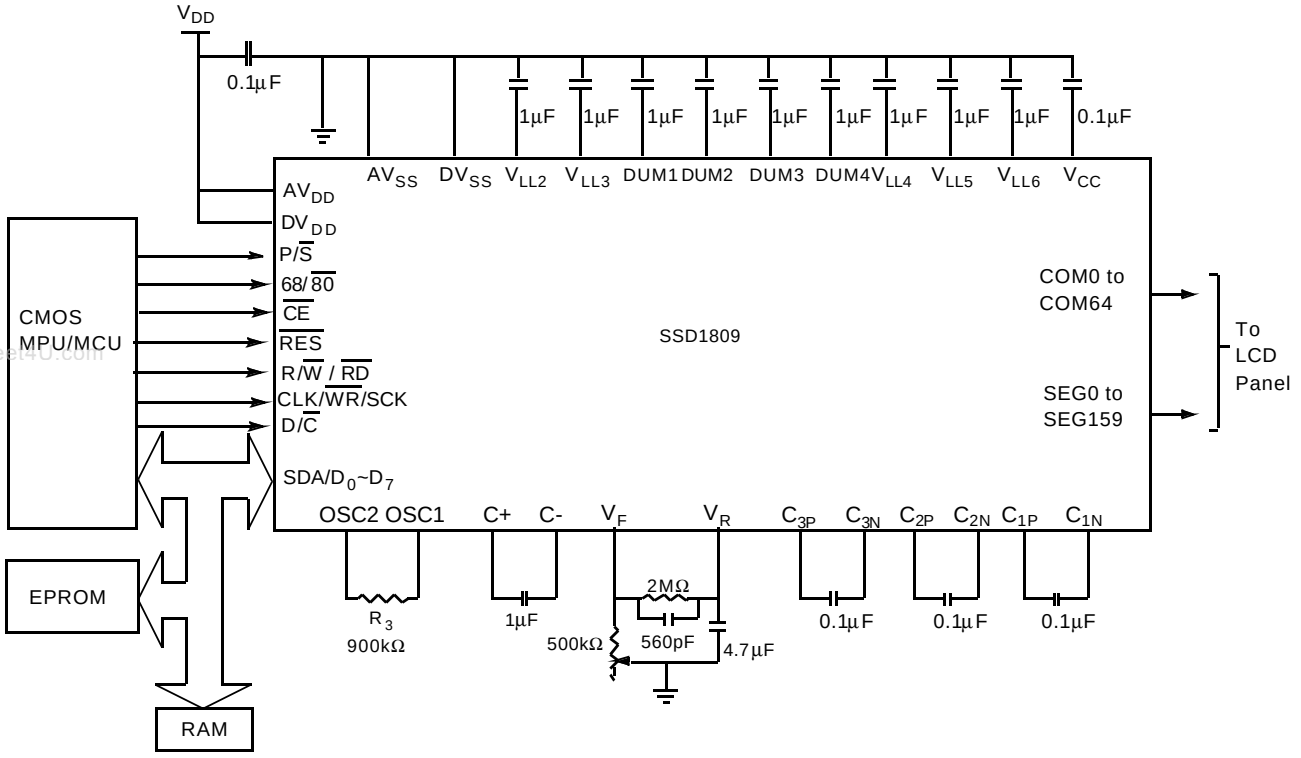
Remarks :
1. R_3 can be omitted for external oscillator.
2. V_R and V_F can be left open for Regulator disable, TC = 0% and Contrast Disable.
3. $\overline{RES}$, CLK/$\overline{WR}$/SCK, R/$\overline{W}$/$\overline{RD}$, $\overline{CE}$ and D/$\overline{C}$ should be at a known state.

Application Circuit for 3X/4X DC-DC converter: (All Internal Analog Block Enabled)



Remarks:
1. R_3 can be omitted for external oscillator.
2. V_R and V_F can be left open for Regulator disable, TC = 0% and Contrast Disable.
3. $\overline{RES}$, CLK/$\overline{WR}$/SCK, R/$\overline{W}$/$\overline{RD}$, $\overline{CE}$ and D/$\overline{C}$ should be at a known state.

Application Circuit for 5X DC-DC converter: (All Internal Analog Block Enabled)

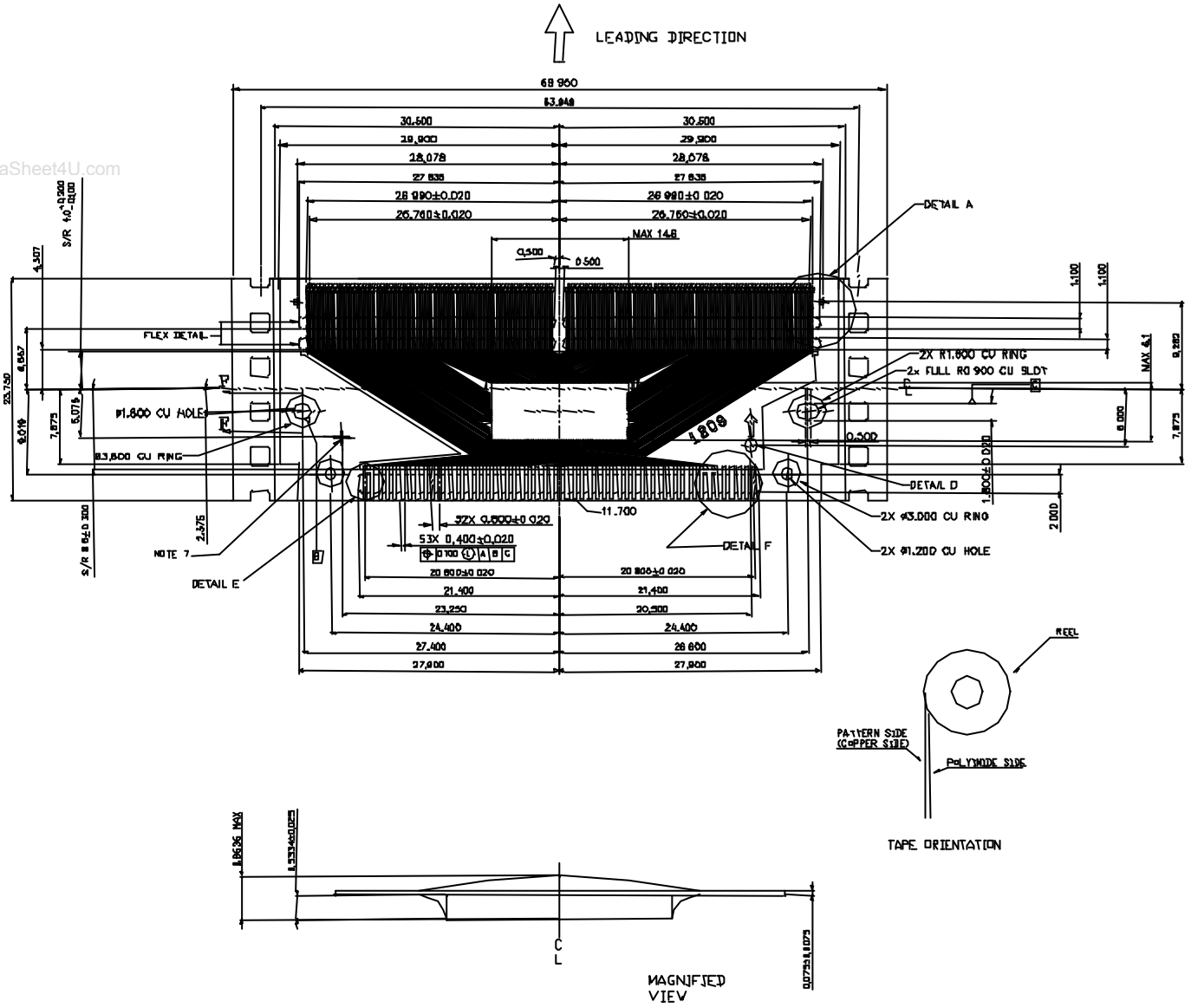


Remarks :
1. R_3 can be omitted for external oscillator.
2. V_R and V_F can be left open for Regulator disable, TC = 0% and Contrast Disable.
3. $\overline{RES}$, CLK/$\overline{WR}$/SCK, R/$\overline{W}$/$\overline{RD}$, $\overline{CE}$ and D/$\overline{C}$ should be at a known state.

PACKAGE DIMENSIONS

SSD1809T

TAB PACKAGE DIMENSION - 1



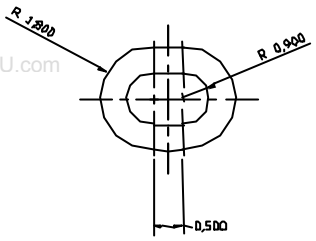
NOTES FOR ALL PAGES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
2. IF NOT SPECIFIED, SIZE IN MILLIMETER
3. UNSPECIFIED DIMENSION TOLERANCE IS ±0.05
4. BASE MATERIAL: 75 MICRON UPILEX-S
5. COPPER TYPE: 3/4 OZ COPPER (THICKNESS TYP. 25 MICROMETER, MIN 18 MICROMETER)
6. 5 SPROCKET HOLES DEVICE
7. OPTIONAL FEATURE WHICH MAY BE REPLACED BY Ø2.0 MM HOLE.

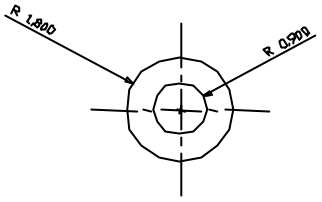
PACKAGE DIMENSIONS

SSD1809T

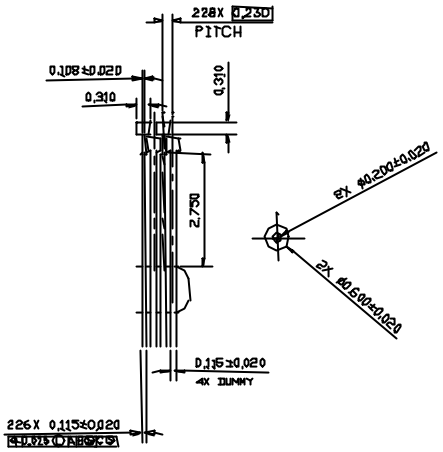
TAB PACKAGE DIMENSION - 2



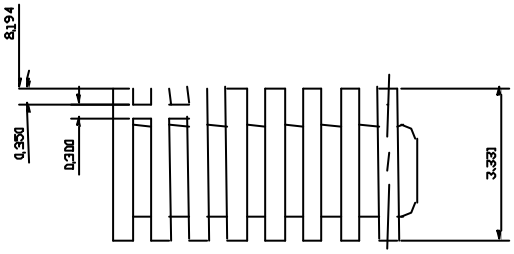
DETAIL C



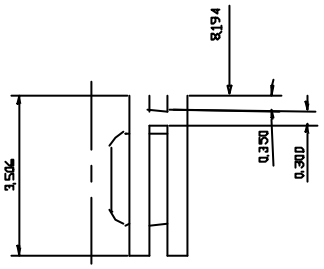
DETAIL B



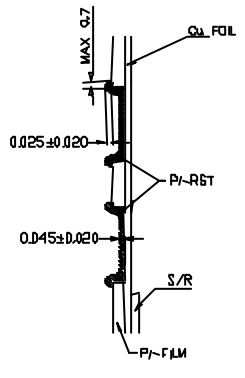
DETAIL A



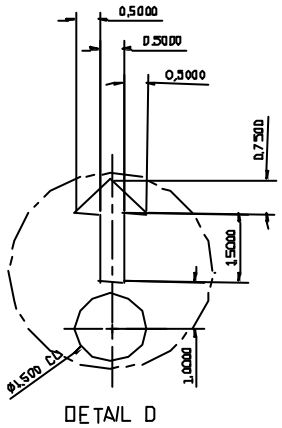
DETAIL F



DETAIL E



FLEX MATERIAL DETAIL



DETAIL D