1.8/2.5/3.3 V Low Jitter, Low Skew Clock Buffer/Level Translator

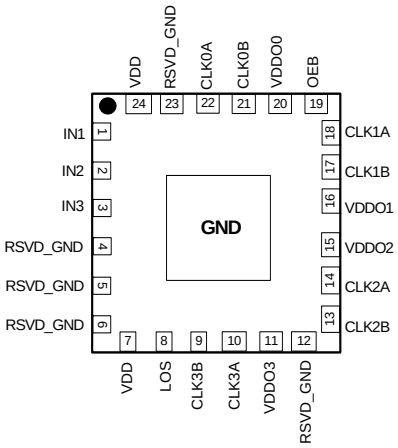
Features

- Supports single-ended or differential input clock signals
- Generates four differential (LVPECL, LVDS, HCSL) or eight single-ended (CMOS, SSTL, HSTL) outputs
- Provides signal level translation
  - Differential to single-ended
  - Single-ended to differential
  - Differential to differential
  - Single-ended to single-ended
- Wide frequency range
  - LVPECL, LVDS: 5 to 710 MHz
  - HCSL: 5 to 250 MHz
  - SSTL, HSTL: 5 to 350 MHz
  - CMOS: 5 to 200 MHz
- Additive jitter: 150 fs RMS typ
- Output-output skew: 100 ps
- Propagation delay: 2.5 ns typ
- Single core supply with excellent PSRR: 1.8, 2.5, or 3.3 V
- Output driver supply voltage independent of core supply: 1.5, 1.8, 2.5, or 3.3 V
- Loss Of Signal (LOS) indicator allows system clock monitoring
- Output Enable (OEB) pin allows glitchless control of output clocks
- Low power: 10 mA typical core current
- Industrial temperature range: –40 to +85 °C
- Small size: 24-lead, 4 x 4 mm QFN

Ordering Information:

See page 14.

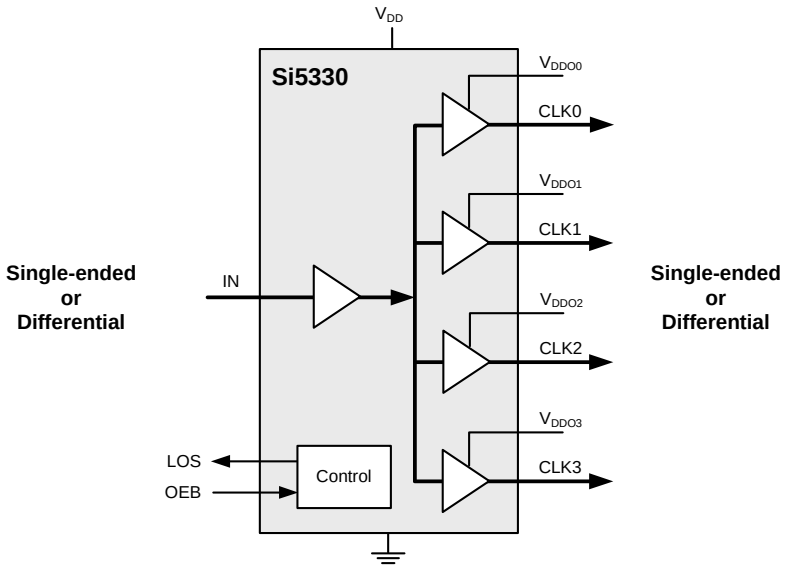
Pin Assignments



Applications

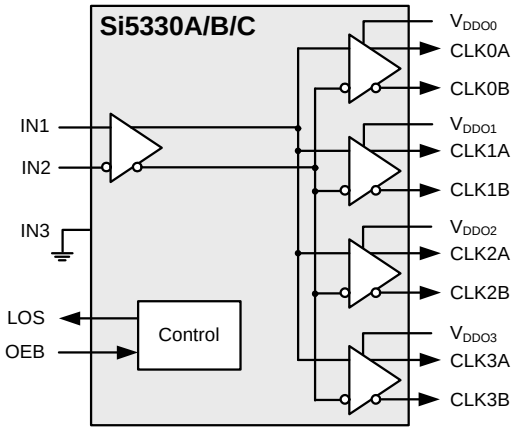
- High Speed Clock Distribution
- Ethernet Switch/Router
- SONET / SDH
- PCI Express 2.0/3.0
- Fibre Channel
- MSAN/DSLAM/PON
- Telecom Line Cards

Functional Block Diagram

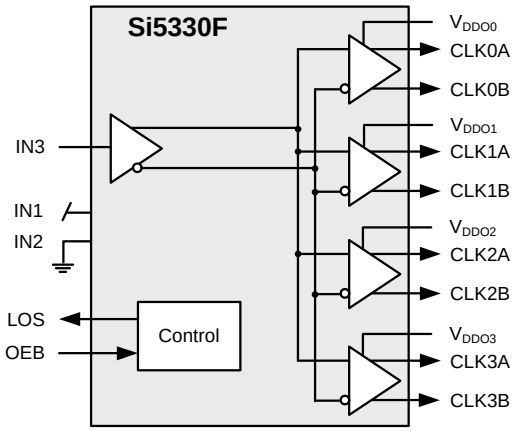


1. Functional Block Diagrams Based on Orderable Part Number*

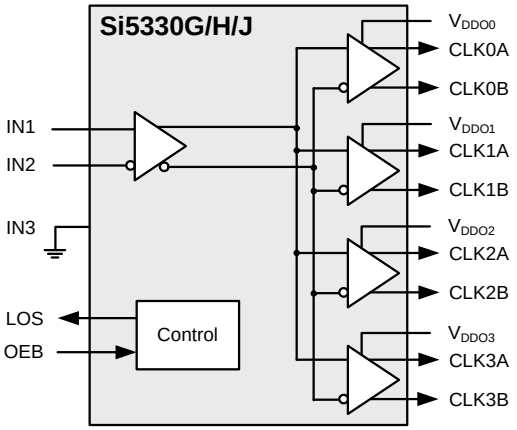
1:4 Differential to Differential Buffer



1:8 Single-Ended to Single-Ended Buffer



1:8 Differential to Single-Ended Buffer



1:4 Single-Ended to Differential Buffer

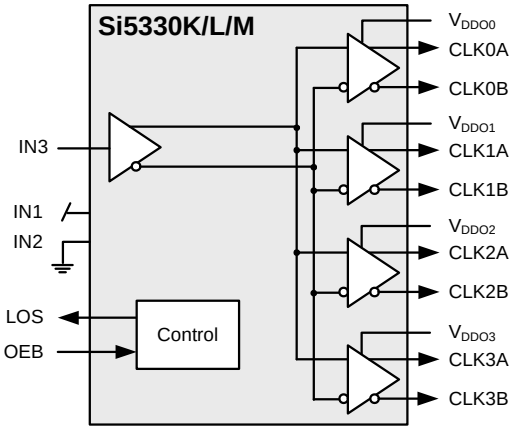


Figure 1. Si5330 Functional Block Diagrams

***Note:** See Table 10 for detailed ordering information.

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Section **Page**

2. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.98	V
Output Buffer Supply Voltage	V_{DDOn}		1.4	—	3.63	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
ESD Tolerance		HBM (100 pF, 1.5 kΩ)	2.5	kV
ESD Tolerance		CDM	550	V
ESD Tolerance		MM	175	V
Latch-up Tolerance			JESD78 Compliant	

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. DC Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	50 MHz refclk	—	10	—	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 710 MHz	—	—	30	mA
		LVDS, 710 MHz	—	—	8	mA
		HCSL, 250 MHz 2 pF load capacitance	—	—	20	mA
		SSTL, 350 MHz	—	—	19	mA
		CMOS, 50 MHz 15 pF load capacitance	—	—	28	mA
		CMOS, 200 MHz 2 pF load capacitance	—	—	28	mA
		HSTL, 350 MHz	—	—	19	mA

Table 4. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	25	°C/W

Table 5. Performance Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CLKIN Loss of Signal Assert Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal De-Assert Time	t_{LOS_B}		0.01	0.2	1	µs
Input-to-Output Propagation Delay	t_{PROP}		—	2.5	—	ns
Output-Output Skew	t_{DSKEW}	Outputs at same frequency, signal format	—	—	100	ps

Table 6. Input and Output Clock Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC Coupled Differential Input Clocks on Pin IN1/2)						
Frequency	f_{IN}		5	—	710	MHz
Differential Voltage Swing	V_{PP}	710 MHz input	0.4	—	2.4	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	1.0	ns
Duty Cycle	DC	< 1 ns tr/tf	—	50	—	%
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		—	3.5	—	pF
Input Clock (DC-Coupled Single-Ended Input Clock on Pin IN3)						
Frequency	f_{IN}	CMOS	5	—	200	MHz
Input Voltage	V_I		–0.1	—	3.63	Vpp
Input Voltage Swing (CMOS Standard)		200 MHz, Tr/Tf = 1.3 ns	0.8	—	3.73	V
Rise/Fall Time	t_R/t_F	20%–80%	—	—	4	ns
Duty Cycle	DC	< 2 ns tr/tf	—	50	—	%
Input Capacitance	C_{IN}		—	2	—	pF
Output Clocks (Differential)						
Frequency	f_{OUT}	LVPECL, LVDS	5	—	710	MHz
		HCSL	5	—	250	MHz
LVPECL Output Voltage	V_{OC}	common mode	—	V_{DDO} – 1.4 V	—	V
	V_{SEPP}	peak-to-peak single-ended swing	0.55	0.8	0.96	V_{PP}
LVDS Output Voltage (2.5/3.3 V)	V_{OC}	common mode	1.125	1.2	1.275	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
LVDS Output Voltage (1.8 V)	V_{OC}	common mode	0.8	0.875	0.95	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
HCSL Output Voltage	V_{OC}	common mode	0.35	0.375	0.400	V
	V_{SEPP}	peak-to-peak single-ended swing	0.575	0.725	0.85	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	450	ps
Duty Cycle*	DC	CKn < 350 MHz	45	—	55	%
		350 MHz < CLKn < 710 MHz	40	—	60	%
Output Clocks (Single-Ended)						
Frequency	f_{OUT}	CMOS	5	—	200	MHz
		SSTL, HSTL	5	—	350	MHz

Table 6. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CMOS 20%-80% Rise/Fall Time	t_R/t_F	2 pF load	—	0.45	0.85	ns
CMOS 20%-80% Rise/Fall Time	t_R/t_F	15 pF load	—	—	1.7	ns
CMOS Output Resistance			—	50	—	Ω
SSTL Output Resistance			—	50	—	Ω
HSTL Output Resistance			—	50	—	Ω
CMOS Output Voltage	V_{OH}	4 mA load	VDDO–0.3	—		V
	V_{OL}	4 mA load		—	0.3	V
SSTL Output Voltage	V_{OH}	SSTL-3 VDDOx = 2.97 to 3.63 V	0.45xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.45xVDDO –0.41	V
	V_{OH}	SSTL-2 VDDOx = 2.25 to 2.75 V	0.5xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.5xVDDO–0.41	V
	V_{OH}	SSTL-18 VDDOx = 1.71 to 1.98 V	0.5xVDDO+0.34	—		V
	V_{OL}		—	—	0.5xVDDO–0.34	V
HSTL Output Voltage	V_{OH}	VDDO = 1.4 to 1.6 V	0.5xVDDO +0.3	—	—	V
	V_{OL}		—	—	0.5xVDDO –0.3	V
Duty Cycle*	DC		45	—	55	%

***Note:** Input clock has a 50% duty cycle.

Table 7. OEB Input Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage Low	V_{IL}		—	—	0.3 x V_{DD}	V
Input Voltage High	V_{IH}		0.7 x V_{DD}	—	—	V
Input Resistance	R_{IN}		20	—	—	kΩ

Table 8. Jitter Specifications

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Additive Phase Jitter (12 kHz–20 MHz)	t_{RPHASE}	0.7 V pk-pk differential input clock at 622.08 MHz with 70 ps rise/fall time	—	0.150	—	ps RMS
Additive Phase Jitter (50 kHz–80 MHz)	$t_{RPHASEWB}$	0.7 V pk-pk differential input clock at 622.08 MHz with 70 ps rise/fall time	—	0.225	—	ps RMS

3. Functional Description

The Si5330 is a low-jitter, low-skew fanout buffer optimized for high-performance PCB clock distribution applications. The device produces four differential or eight single-ended, low-jitter output clocks from a single input clock. The input can accept either a single-ended or a differential clock allowing the device to function as a clock level translator.

3.1. V_{DD} and V_{DDO} Supplies

The core V_{DD} and output V_{DDO} supplies have separate and independent supply pins allowing the core supply to operate at a different voltage than the I/O voltage levels.

The V_{DD} supply powers the core functions of the device, which operates from 1.8, 2.5, or 3.3 V. Using a lower supply voltage helps minimize the device's power consumption. The V_{DDO} supply pins are used to set the output signal levels and must be set at a voltage level compatible with the output signal format.

3.2. Loss Of Signal Indicator (LOS)

The input is monitored for a valid clock signal using an LOS circuit that monitors input clock edges and declares an LOS condition when signal edges are not detected over a 5 µs observation period. The LOS pin is asserted "low" when valid clock is present. A "high" level on the LOS pin indicates a loss of signal (LOS). The LOS pin must be pulled to VDD as shown in Figure 2.

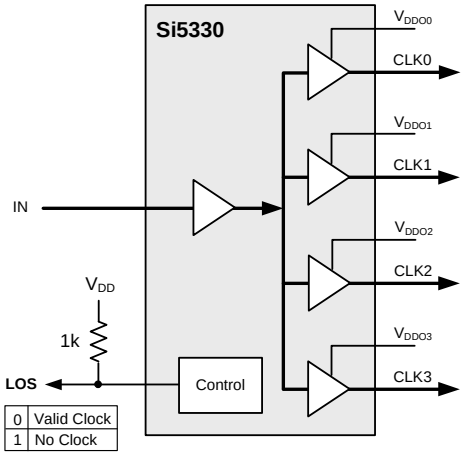


Figure 2. LOS Indicator with External Pull-Up

3.3. Output Enable (OEB)

The output enable (OEB) pin allows disabling or enabling of the outputs clocks (CLK0-CLK3). The output enable is logically controlled to ensure that no glitches or runt pulses are generated at the output as shown in Figure 3.

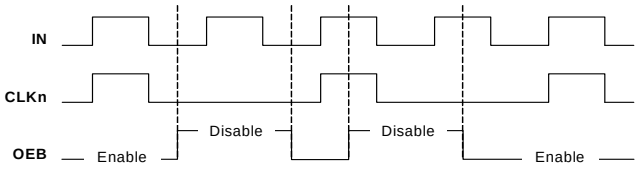


Figure 3. OEB Glitchless Operation

All outputs are enabled when the OEB pin is connected to ground or below the V_{IL} voltage for this pin. Connecting the OEB pin to VDD or above the V_{IH} level will disable the outputs. Both V_{IL} and V_{IH} are specified in Table 7. All outputs are forced to a logic "low" when disabled. The OEB pin is 3.3 V tolerant.

3.4. Input Signals

The Si5330 can accept single-ended and differential input clocks. See "AN408: Termination Options for Any-Frequency, Any-Output Clock Generators and Clock Buffers—Si5338, Si5334, Si5330" for details on connecting a wide variety of signals to the Si5330 inputs.

3.5. Output Driver Formats

The Si5330 supports single-ended output formats of CMOS, SSTL, and HSTL and differential formats of LVDS, LVPECL, and HCSL. It is normally required that the LVDS driver be dc-coupled to the 100 Ω termination at the receiver end. If your application requires an ac-coupled 100 Ω load, contact the applications team for advice. See AN408 for additional information on the terminations for these driver types.

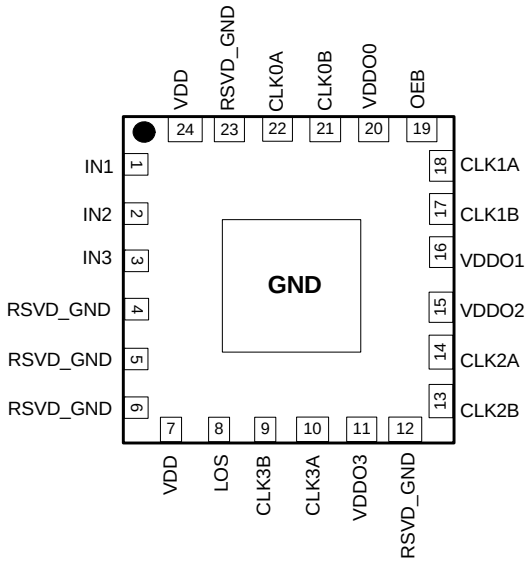
3.6. Input and Output Terminations

See AN408 for detailed information.

4. Ordering the Si5330

The Si5330 can be ordered to meet the requirements of the most commonly-used input and output signal types, such as CMOS, SSTL, HSTL, LVPECL, LVDS, and HSCL. See Figure 1, "Si5330 Functional Block Diagrams," on page 2 and Table 10, "Order Numbers and Device Functionality," on page 14 for specific ordering information.

5. Pin Descriptions—Si5330



Note: Center pad must be tied to GND for normal operation.

Table 9. Si5330 Pin Descriptions

Pin #	Pin Name	I/O	Signal Type	Description
1	IN1	I	Multi	**Si5330A/B/C/G/H/J Differential Input Devices.**
2	IN2	I	Multi	These pins are used as the differential clock input. IN1 is the positive input; IN2 is the negative input. Refer to "AN408: Termination Options for Any-Frequency, Any-Output Clock Generators and Clock Buffers—Si5338, Si5334, Si5330" for interfacing and termination details. **Si5330F/K/L/M Single-Ended Input Devices.** These pins are not used. Leave IN1 unconnected and IN2 connected to ground.
3	IN3	I	Multi	**Si5330F/K/L/M Single-Ended Devices.** This is the single-ended clock input. Refer to AN408 for interfacing and termination details. **Si5330A/B/C/G/H/J Differential Input Devices.** This pin is not used. Connect to ground.
4	RSVD_GND			**Ground.** Must be connected to system ground.
5	RSVD_GND			**Ground.** Must be connected to system ground.
6	RSVD_GND			**Ground.** Must be connected to system ground.

Table 9. Si5330 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
7	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
8	LOS	O	Open Drain	**Loss of Signal Indicator.** 0 = CLKIN present. 1 = Loss of signal (LOS). This pin requires an external $\geq$1 kΩ pull-up resistor.
9	CLK3B	O	Multi	**Si5330A/B/C/K/L/M Differential Output Devices.** This is the negative side of the differential CLK3 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Output Devices.** This is one of the single-ended CLK3 outputs. Both CLK3A and CLK3B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
10	CLK3A	O	Multi	**Si5330A/B/C/K/L/M Differential Devices.** This is the positive side of the differential CLK3 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Devices.** This is one of the single-ended CLK3 outputs. Both CLK3A and CLK3B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
11	VDDO3	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage for CLK3A/B. Use a 0.1 µF bypass cap as close as possible to this pin. If CLK3 is not used, this pin must be tied to V_{DD} (pin 7 and/or pin 24).
12	RSVD_GND			**Ground.** Must be connected to system ground.
13	CLK2B	O	Multi	**Si5330A/B/C/K/L/M Differential Output Devices.** This is the negative side of the differential CLK2 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Output Devices.** This is one of the single-ended CLK2 outputs. Both CLK2A and CLK2B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.

Table 9. Si5330 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
14	CLK2A	O	Multi	**Si5330A/B/C/K/L/M Differential Devices.** This is the positive side of the differential CLK2 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Devices.** This is one of the single-ended CLK2 outputs. Both CLK2A and CLK2B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
15	VDDO2	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage for CLK2A/B. Use a 0.1 µF bypass cap as close as possible to this pin. If CLK2 is not used, this pin must be tied to V_{DD} (pin 7 and/or pin 24).
16	VDDO1	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage for CLK1A,B. Use a 0.1 µF bypass cap as close as possible to this pin. If CLK1 is not used, this pin must be tied to V_{DD} (pin 7 and/or pin 24).
17	CLK1B	O	Multi	**Si5330A/B/C/K/L/M Differential Output Devices.** This is the negative side of the differential CLK1 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Output Devices.** This is one of the single-ended CLK1 outputs. Both CLK1A and CLK1B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
18	CLK1A	O	Multi	**Si5330A/B/C/K/L/M Differential Devices.** This is the positive side of the differential CLK1 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-Ended Devices.** This is one of the single-ended CLK1 outputs. Both CLK1A and CLK1B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
19	OEB	I	CMOS	**Output Enable.** All outputs are enabled when the OEB pin is connected to ground or below the V_{IL} voltage for this pin. Connecting the OEB pin to V_{DD} or above the V_{IH} level will disable the outputs. Both V_{IL} and V_{IH} are specified in Table 7. All outputs are forced to a logic “low” when disabled. This pin is 3.3 V tolerant.

Table 9. Si5330 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
20	VDDO0	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage for CLK0A,B. Use a 0.1 µF bypass cap as close as possible to this pin. If CLK2 is not used, this pin must be tied to V_{DD} (pin 7 and/or pin 24).
21	CLK0B	O	Multi	**Si5330A/B/C/K/L/M Differential Output Devices.** This is the negative side of the differential CLK0 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-ended Output Devices.** This is one of the single-ended CLK0 outputs. Both CLK0A and CLK0B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
22	CLK0A	O	Multi	**Si5330A/B/C/K/L/M Differential Devices.** This is the positive side of the differential CLK0 output. Refer to AN408 for interfacing and termination details. Leave unconnected when not in use. **Si5330F/G/H/J Single-ended Devices.** This is one of the single-ended CLK0 outputs. Both CLK0A and CLK0B single-ended outputs are in phase. Refer to AN408 for interfacing and termination details. Leave unconnected when not is use.
23	RSVD_GND			**Ground.** Must be connected to system ground.
24	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	Supply	**Ground Pad.** This is main ground connection for this device. It is located at the bottom center of the package. Use as many vias as possible to connect this pad to the main ground plane.

6. Orderable Part Numbers and Device Functionality

Table 10. Order Numbers and Device Functionality

Part Number	Input Signal Format	Output Signal Format	Number of Outputs	Frequency Range
LVPECL Buffers				
Si5330A-A00200-GM	Differential	3.3 V LVPECL	4	5 to 710 MHz
Si5330A-A00202-GM	Differential	2.5 V LVPECL	4	5 to 710 MHz
LVDS Buffers				
Si5330B-A00204-GM	Differential	3.3 V LVDS	4	5 to 710 MHz
Si5330B-A00205-GM	Differential	2.5 V LVDS	4	5 to 710 MHz
Si5330B-A00206-GM	Differential	1.8 V LVDS	4	5 to 710 MHz
HCSL Buffers				
Si5330C-A00207-GM	Differential	3.3 V HCSL	4	5 to 250 MHz
Si5330C-A00208-GM	Differential	2.5 V HCSL	4	5 to 250 MHz
Si5330C-A00209-GM	Differential	1.8 V HCSL	4	5 to 250 MHz
CMOS Buffers				
Si5330F-A00214-GM	Single-Ended	3.3 V CMOS	8	5 to 200 MHz
Si5330F-A00215-GM	Single-Ended	2.5 V CMOS	8	5 to 200 MHz
Si5330F-A00216-GM	Single-Ended	1.8 V CMOS	8	5 to 200 MHz
CMOS Buffers (Differential Input)				
Si5330G-A00217-GM	Differential	3.3 V CMOS	8	5 to 200 MHz
Si5330G-A00218-GM	Differential	2.5 V CMOS	8	5 to 200 MHz
Si5330G-A00219-GM	Differential	1.8 V CMOS	8	5 to 200 MHz
SSTL Buffers (Differential Input)				
Si5330H-A00220-GM	Differential	3.3 V SSTL	8	5 to 350 MHz
Si5330H-A00221-GM	Differential	2.5 V SSTL	8	5 to 350 MHz
Si5330H-A00222-GM	Differential	1.8 V SSTL	8	5 to 350 MHz
HSTL Buffers (Differential Input)				
Si5330J-A00223-GM	Differential	1.5 V HSTL	8	5 to 350 MHz
LVPECL Buffers (Single-Ended Input)				
Si5330K-A00224-GM	Single-Ended	3.3 V LVPECL	4	5 to 350 MHz
Si5330K-A00226-GM	Single-Ended	2.5 V LVPECL	4	5 to 350 MHz
Note: Custom configurations with mixed output types are also available. Please contact the factory for ordering details.				

Table 10. Order Numbers and Device Functionality (Continued)

Part Number	Input Signal Format	Output Signal Format	Number of Outputs	Frequency Range
LVDS Buffers (Single-Ended Input)				
Si5330L-A00228-GM	Single-Ended	3.3 V LVDS	4	5 to 350 MHz
Si5330L-A00229-GM	Single-Ended	2.5 V LVDS	4	5 to 350 MHz
Si5330L-A00230-GM	Single-Ended	1.8 V LVDS	4	5 to 350 MHz
HCSL Buffers (Single-Ended Input)				
Si5330M-A00231-GM	Single-Ended	3.3 V HCSL	4	5 to 250 MHz
Si5330M-A00232-GM	Single-Ended	2.5 V HCSL	4	5 to 250 MHz
Si5330M-A00233-GM	Single-Ended	1.8 V HCSL	4	5 to 250 MHz
Note: Custom configurations with mixed output types are also available. Please contact the factory for ordering details.				

7. Package Outline: 24-Lead QFN

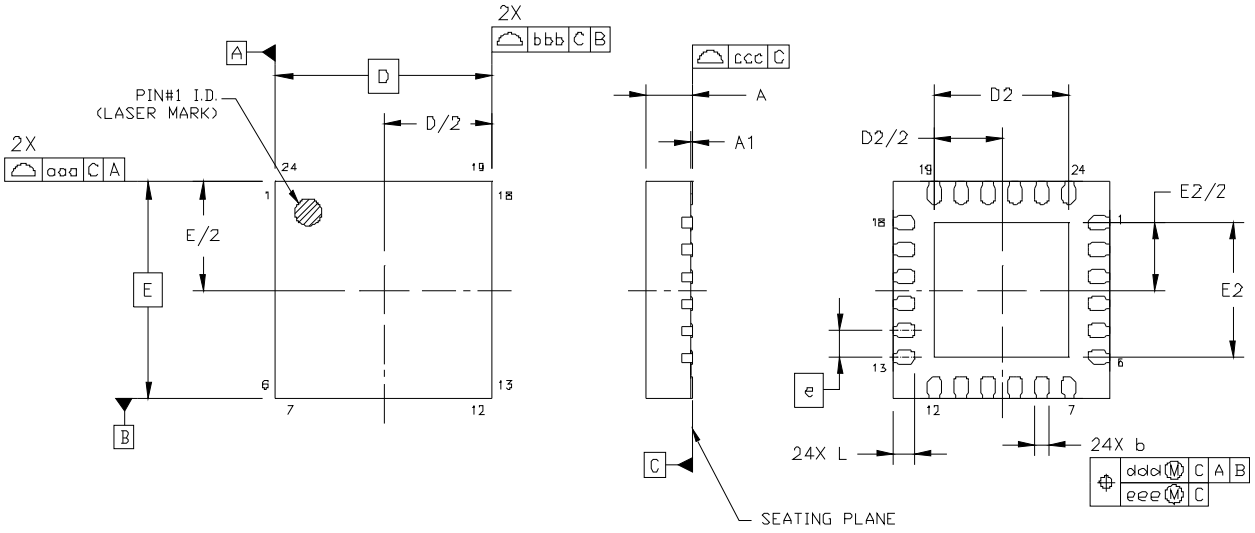


Figure 4. 24-Lead Quad Flat No-lead (QFN)

Table 11. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Recommended PCB Layout

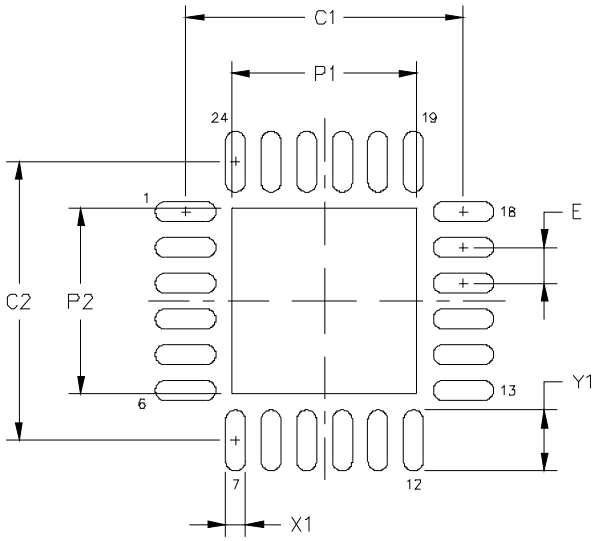


Table 12. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. Connect the center ground pad to a ground plane with no less than five vias to a ground plane that is no more than 20 mils below it. Via drill size should be no smaller than 10 mils. A longer distance to the ground plane is allowed if more vias are used to keep the inductance from increasing.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
9. A 2x2 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Clarified documentation to reflect that Pin 19 is OEB (OE Enable Low).
- Updated Table 4, “Jitter Specifications” on page 7.

Revision 0.2 to Revision 0.3

- Major editorial updates to improve clarity.
- Updated “Additive Jitter” Specification Table.
- Updated “Core Supply Current” Specification in Table 3.
- Removed the Low-Power LVPECL output options from the ordering table in section 6.
- Removed D/E ordering options.

Revision 0.3 to Revision 0.35

- Typo of 150 ps on front page changed to 150 fs.
- Updated PCB layout notes.
- Added no ac coupling for LVDS outputs.
- Changed input rise/fall time spec to 2 ns.

NOTES:

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