LSI/CSI

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RED SERIES

AC LINE FREQUENCY DIVIDERS

July 2000

RED SERIES

RED 5/6	Divide by 5 or 6
RED 50/60	Divide by 50 or 60
RED 100/120	Divide by 100 or 120
RED 300/360	Divide by 300 or 360
RED 500/600	Divide by 500 or 600
RED 3000/3600	Divide by 3000 or 3600

FEATURES:

- Clock input pulse shaper accepts 50Hz/60Hz sine wave directly
- Fully static counter operation
- +4.5V to +15V operation (V_{DD} - V_{SS})
- Low power dissipation
- High noise immunity
- Reset
- Input Enable
- 50Hz/60Hz division select input
- Output low power TTL compatible at +4.5V operation
- Square Wave Output (except for ÷ 5)
- RED x/y (DIP); RED x/y-S (SOIC) See Figure 1

APPLICATION:

Time base generator from either 50Hz or 60Hz line frequency to produce:

10 pulses per second	(RED 5/6)
1 pulse per second	(RED 50/60)
1 pulse per 2 seconds	(RED 100/120)
1 pulse per .1 minute	(RED 300/360)
1 pulse per 10 seconds	(RED 500/600)
1 pulse per minute	(RED 3000/3600)

DESCRIPTION OF OPERATION:

The counter advances by one on each negative transition of the input clock pulse as long as the Enable signal is High and the Reset signal is Low. When the Enable signal is Low the input clock pulses will be inhibited and the counter will be held at the state it was in prior to bringing the Enable Low. A High Reset signal clears the counter to zero count.

Depending on the device used, a Low on the Division Select input will cause a Divide by 6, 60, 120, 360, 600 or 3600. A High on the Division Select will cause a Divide by 5, 50, 100, 300, 500 or 3000.

All outputs are 50% duty cycle except RED 5, where output is low for two clocks and high for three clocks.

CLOCK INPUT

If input signals are less than the Vss or greater than V_{DD}, a series input resistor should be used to limit the maximum input current to 2 mA.

PIN ASSIGNMENT - TOP VIEW

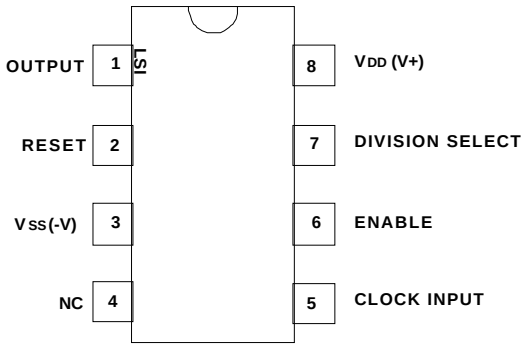

FIGURE 1

MARKING AS FOLLOWS:

PART	MARKING
RED 5/6	RED 6
RED 50/60	RED 60
RED 100/120	RED 120
RED 300/360	RED 360
RED 500/600	RED 600
RED 3000/3600	RED 3600

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNIT
Storage Temperature	T_{STG}	-65 to +150	˚C
Operating Temperature	T_A	-40 to +85	˚C
DC Supply Voltage	(V_{DD}-Vss)	+18	V
Voltage at any input	V_{IN}	Vss -.3 to V_{DD} +.3	V

ENABLE SIGNAL TIMING

If the Enable signal switches Low during a positive clock phase and then switches High during a negative clock phase, a false count will be registered. To prevent this from happening, the Enable signal should not switch Low during a positive clock phase unless the switch to High also occurs during a positive clock phase. The Enable signal should normally be switched during a negative clock phase.

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

ELECTRICAL CHARACTERISTICS: (TA = 25° unless otherwise specified)

TEST CONDITIONS: Vss = OV
Output Capacitance Load = 15 pF
Input Rise and Fall times = 20 ns,
except clock Rise and Fall times
Input Capacitance = 5pF max (any input)

	V_{DD}	Min	Max	Units
Quiescent Device Current	5V	-	10	uA
	10V	-	20	uA
Output Voltage, Low Level	5V	-	0.0	V
	10V	-	0.0	V
High Level	5V	4.99	-	V
	10V	9.99	-	V
Clock Input Voltage, Low Level	5V	-	1	V
	10V	-	2	V
High Level	5V	4	-	V
	10V	8	-	V
Input Noise Immunity (except clock)	5V	1.5	-	V
(Low and High)	10V	3.0	-	V
Output Drive Current				
Full Temp. Range - N Channel Sink Current (Vout - Vss +.4v)	4.5V	0.18	-	mA
	10V	0.45	-	mA
P Channel Sink Current (Vout - VDD -1)	4.5V	0.3	-	mA
	10V	0.75	-	mA

	V_{DD}	MIN	MAX	UNITS
Clock Rise and Fall Time:	5V	No Maximum Limit		-
	10V	No Maximum Limit		-
Clock Frequency	5V	DC	600	kHz
	10V	DC	1200	kHz
Input Clock Pulse Width	5V	800	-	ns
	10V	400	-	ns
Output Rise and Fall Time	5V	-	225	ns
	10V	-	150	ns
Propagation Delay to Output	5V	-	1500	ns
	10V	-	750	ns
Enable Set-up Time	5V	-	300	ns
	10V	-	150	ns
Reset Pulse Width	5V	800	-	ns
	10V	400	-	ns
Reset Removal Time	5V	-	1200	ns
	10V	-	600	ns
Reset Propagation Delay to Output	5V	-	1400	ns
	10V	-	700	ns

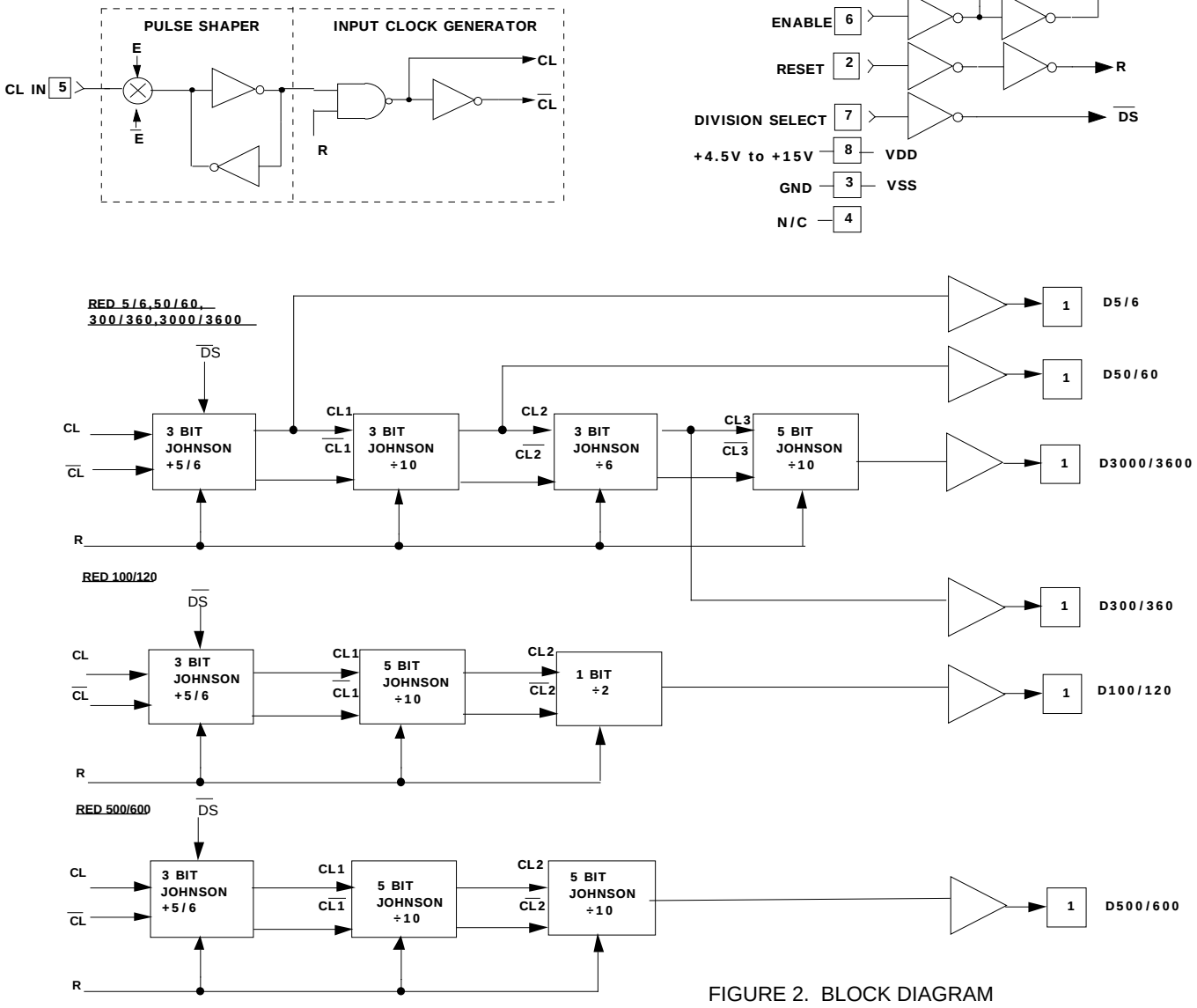

FIGURE 2. BLOCK DIAGRAM