mosaic

Mosaic Semiconductor Inc.

PUMA 2S8000

PUMA 2S8000-85/10/12

Issue 1.1 : December 1991

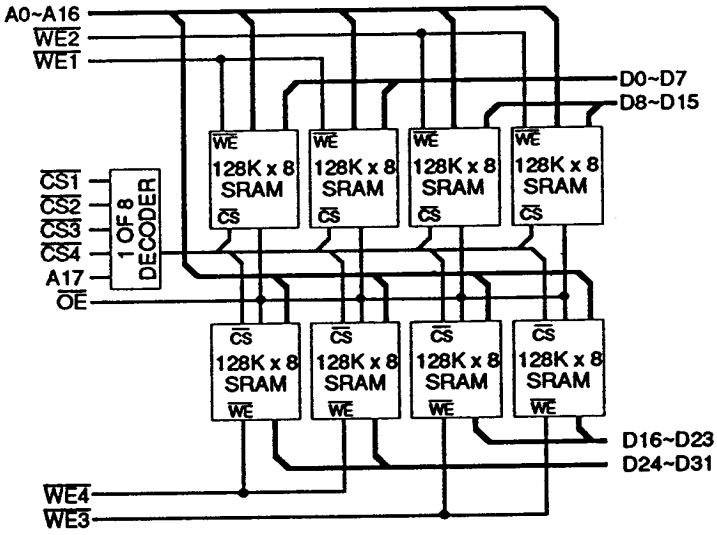
ADVANCE PRODUCT INFORMATION

8,388,608 bit CMOS High Speed Static RAM

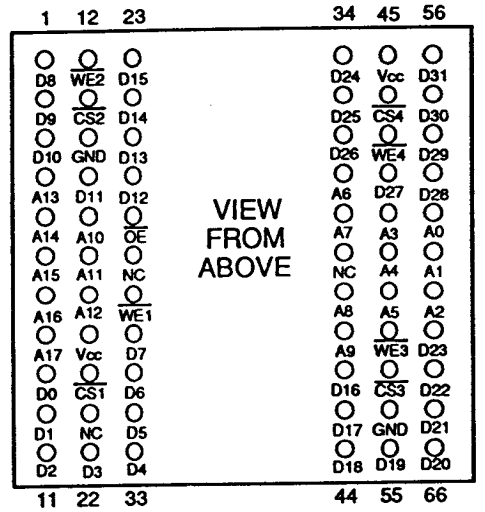
Features

Fast access times of 85/100/120 ns.
Pin grid array gives 4:1 improvement over DIL.
User Configurable as 8 / 16 / 32 bit wide output.
Operating Power 135 / 205 / 365 mW (typ)
Low Power Standby 100µW (typ) -L version.
Package Suitable for Thermal Ladder Applications.
On board decoupling capacitors.
Battery back-up capability.
May be screened in accordance with MIL-STD-883C.

Block Diagram



Pin Definition

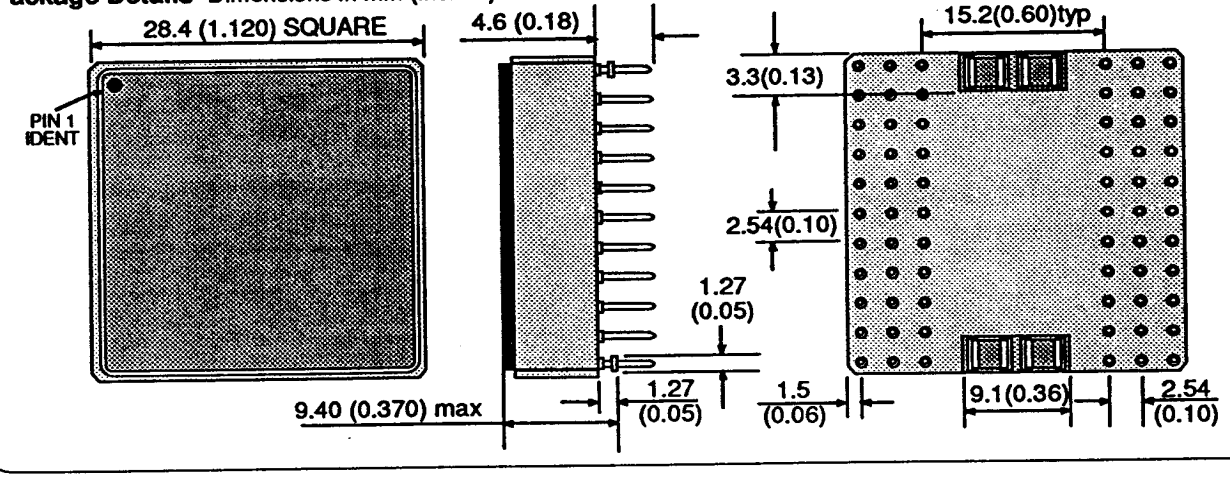


See page 5 for pinout

Pin Functions

A0 -A17	Address Inputs
D0-31	Data Inputs/Outputs
$\overline{CS1\text{-}4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE1\text{-}4}$	Write Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_T	-0.5V to +7	V
Power Dissipation	P_T	2	W
Storage Temperature	T_{STG}	-65 to +125	°C

Note: V_T can be -3.0V pulse of less than 30ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C (2S8000)
	T_{AI}	-40	-	85	°C (2S8000I)
	T_{AM}	-55	-	125	°C (2S8000M, MB)

Note: V_{IL} can be -3.0V pulse of less than 30ns.

DC Electrical Characteristics (V_{CC}=5V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*	*Notes*
I/P Leakage, $\overline{WE}$, $\overline{CS}$, A17	I_{LI1}	V_{IN}=0V to V_{CC}	-	-	4	µA	
A0-A16, $\overline{OE}$	I_{LI2}	V_{IN}=0V to V_{CC}	-	-	16	µA	
Output Leakage Current	I_{LO}	$\overline{CS}$ or $\overline{OE}$ or $\overline{WE}$=V_{IH}, $V_{I/O}$=0V to V_{CC},16 BIT	-	-	8	µA	(2)
Operating Supply Current	I_{CC}	$\overline{CS}$=V_{IL},$I_{I/O}$=0mA, I/P's static, 32 BIT MODE	-	69	157	mA	(2)
Average Supply Current		Min. cycle, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA					
	I_{CC8}	32 BIT MODE	-	190	297	mA	
	I_{CC16}	16 BIT MODE	-	100	163	mA	
	I_{CC32}	8 BIT MODE	-	57	96	mA	
	I_{CC1}	1µs cycle, duty=100%,$I_{I/O}$=0mA, 32 Bit Mode, $\overline{CS}$≤0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	69	137	mA	
Standby Current	I_{SB}	$\overline{CS}$=V_{IH}	-	11	27	mA	(2)
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, I/P's<0.2V or ≥V_{CC}-0.2V	-	0.17	17	mA	(2)
L-Part	I_{SB2}	$\overline{CS}$≥V_{CC}-0.2V, I/P's<0.2V or ≥V_{CC}-0.2V	-	20	3300	µA	(2)
Output Voltage Low	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V	
Output Voltage High	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V	

Notes: (1) Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.
(2) $\overline{CS}$ above is accessed through $\overline{CS1-4}$ These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
I/P Capacitance $\overline{WE}$, $\overline{CS}$, A17	C_{IN1}	V_{IN}=0V	-	36	pF
A0-A16, $\overline{OE}$	C_{IN2}	V_{IN}=0V	-	84	pF
I/O Capacitance: 32 BIT MODE	$C_{I/O}$	$V_{I/O}$=0V	-	30	pF

Note: This parameter is calculated and not measured.

AC Test Conditions

*Input pulse levels: 0.0V to 3.0V
*Input rise and fall times: 5ns
*Input and Output timing reference levels: 1.5V
*Output load: 1 TTL gate + 100pF
*V_{cc}=5V±10%
*Tested in 32 bit mode

Operating Modes

The Table below shows the logic inputs required to control the operating modes of each of the SRAMs in the PUMA 2S8000.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	*V_{CC} Current*	*I/O Pin*	*Reference Cycle*
Not Selected	1	X	X	I_{SB1}, I_{SB2}	High Z	-
Read	0	0	1	I_{CC}	D_{OUT}	Read Cycle
Write	0	1	0	I_{CC}	D_{IN}	Write Cycle No.1
Write	0	0	0	I_{CC}	D_{IN}	Write Cycle No.2

$1 = V_{IH}$, $0 = V_{IL}$, X = Don't Care

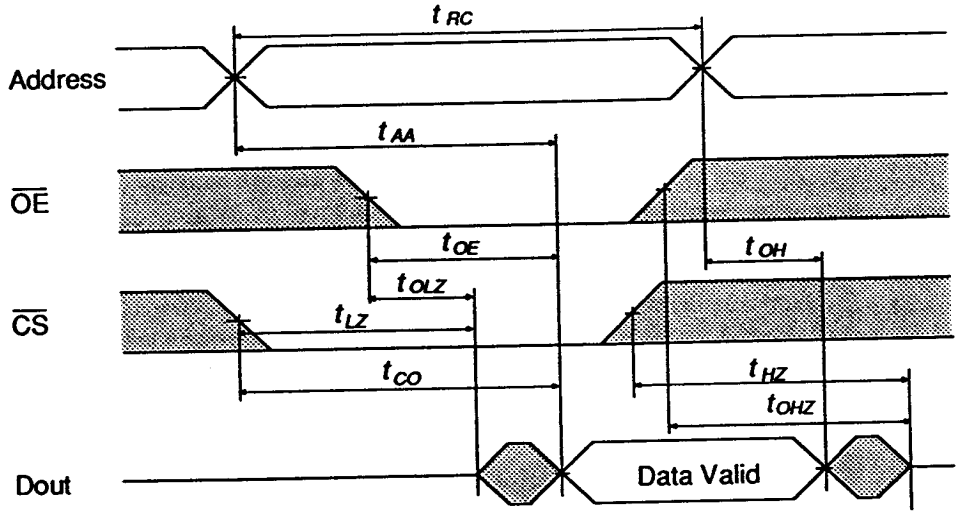
Note: $\overline{CS}$ is accessed through $\overline{CS1\text{-}4}$, and $\overline{WE}$ is accessed through $\overline{WE1\text{-}4}$. For correct operation, $\overline{CS1\text{-}4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation. $\overline{WE1\text{-}4}$ must also be operated in the same manner.

Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

		-85		-10		-12		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	85	-	100	-	120	-	ns
Address Access Time	t_{AA}	-	85	-	100	-	120	ns
Chip Select Access Time	t_{CO}	-	85	-	100	-	120	ns
Output Enable to Output Valid	t_{OE}	-	40	-	50	-	60	ns
Chip Select to O/P in low Z (2)	t_{LZ}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z (2)	t_{OLZ}	5	-	5	-	5	-	ns
Chip Deselect to O/P High Z (2)	t_{HZ}	0	30	0	35	0	45	ns
Output Hold from Address Change	t_{OH}	10	-	15	-	15	-	ns
Output Disable to Output in High Z (2)	t_{OHZ}	0	30	0	35	0	45	ns

Read Cycle Timing Waveform (1)



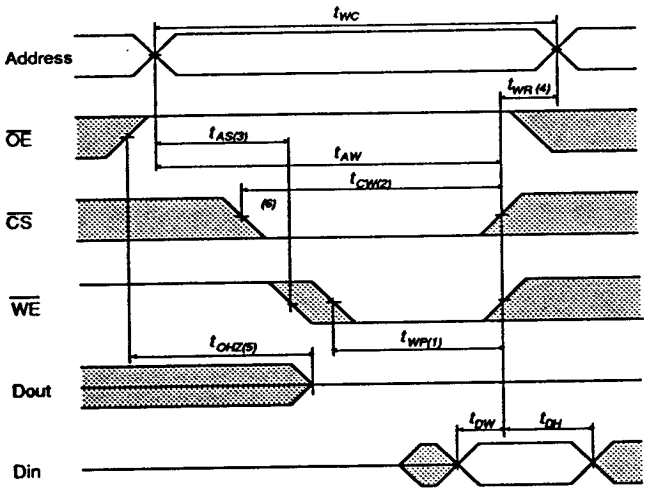
Notes: (1) $\overline{WE1\text{-}4}$ are High throughout a Read Cycle.

(2) t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device. This parameter is sampled and not 100% tested.

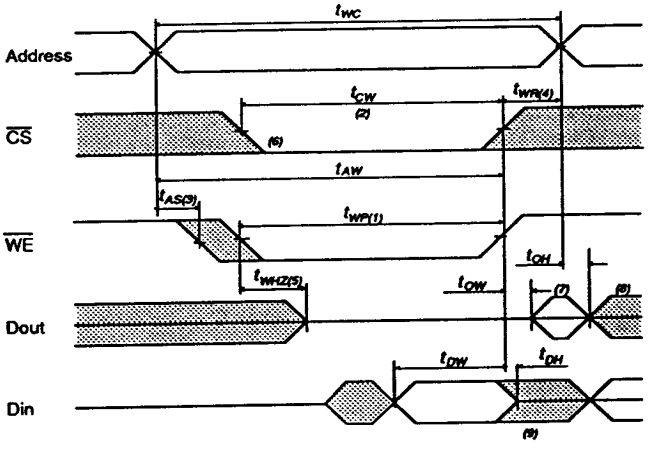
Write Cycle

Parameter	Symbol	-85 min	-85 max	-10 min	-10 max	-12 min	-12 max	Unit	Notes
Write Cycle Time	t_{WC}	85	-	100	-	120	-	ns	
Chip Selection to End of Write	t_{CW}	75	-	90	-	100	-	ns	
Address Valid to End of Write	t_{AW}	75	-	90	-	100	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	65	-	75	-	90	-	ns	
Write Recovery Time	t_{WR}	5	-	5	-	10	-	ns	
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	ns	(10)
Data to Write Time Overlap	t_{DW}	35	-	40	-	50	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	10	-	10	-	10	-	ns	(10)

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (11)



AC Characteristics Notes

Notes: (1) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high and WE going high. t_{WP} is measured from the beginning of write to the end of write.

(2) t_{CW} is measured from $\overline{CS}$ going low to the end of write.

(3) t_{AS} is measured from the address valid to the beginning of write.

(4) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(5) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(6) If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, outputs remain in high impedance state.

(7) D_{OUT} is in the same phase as written data of this write cycle.

(8) D_{OUT} is the read data of next address.

(9) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to the I/O pins.

(9) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

(11) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})

Connection Table

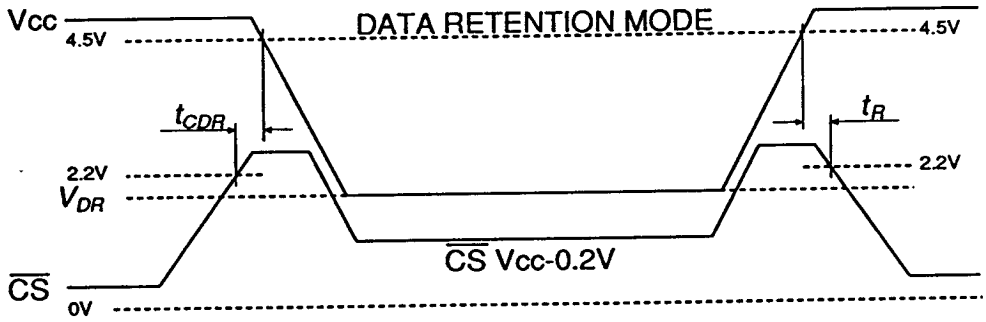
PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name
1	D8	2	D9	3	D10	4	A13	5	A14
6	A15	7	A16	8	A17	9	D0	10	D1
11	D2	12	$\overline{WE2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A11	18	A12	19	V_{cc}	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	NC	29	$\overline{WE1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A6	38	A7	39	NC	40	A8
41	A9	42	D16	43	D17	44	D18	45	V_{cc}
46	$\overline{CS4}$	47	$\overline{WE4}$	48	D27	49	A3	50	A4
51	A5	52	$\overline{WE3}$	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A0
61	A1	62	A2	63	D23	64	D22	65	D21
66	D20								

Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$ ≥V_{CC}-0.2V. V_{IN} ≥ 0V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V,V_{IN} ≥ 0V, $\overline{CS}$ ≥V_{CC}-0.2V.	-	12	2500	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Note (1) Typical figures are measured at 25°C.

Low V_{cc} Data Retention Timing Waveform



Military Screening Procedure

MultiChip Screening Flow for high reliability,non compliant product is detailed below.

MB MULTICHIP MODULE SCREENING FLOW		
SCREEN	***TEST METHOD***	***LEVEL***
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y_1 only) (10,000g)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015,Condition D,T_A=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post burn-in at T_A=+25°C	10%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 2S8000LMB-10

Speed	85	= 85 ns
	10	= 100 ns
	12	= 120 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Screened in accordance with MIL-STD-883C
Power Consumption	Blank	= Standard Power Part
	L	= Low Power Part
Memory Arrangement	2S8000	= 256Kx32 SRAM (Configurable as 512K x 16 and 1M x 8)

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

8

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