MOTOROLA

MCM5303
MCM5003
MCM5304
MCM5004

MTTL

512-BIT PROGRAMMABLE READ ONLY MEMORY

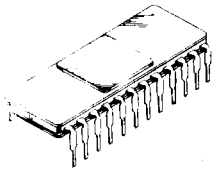
512-BIT PROGRAMMABLE READ ONLY MEMORY

The MCM5303/5003 and MCM5304/5004 are monolithic bipolar 512-bit Programmable Read Only Memories (PROMs) organized as 64 eight-bit words. These memories are field programmable, i.e., the user can custom program these memories himself. Metal interconnections establish each bit initially in the logic "0" state. By "blowing" appropriate nichrome resistors and thus breaking metalization links these bits can be changed to the logic "1" state to meet specific program requirements. Detailed programming instructions are contained in this data sheet.

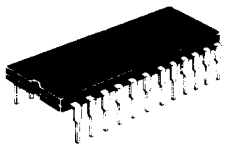
The MCM5303/5003 and MCM5304/5004 have six address inputs to select the proper word and two chip enable inputs, as well as outputs for each of the eight bits.

The MCM5303 and MCM5304 are specified over an operating temperature range of -55°C to +125°C. The MCM5003 and MCM5004 are specified over an operating temperature range of 0°C to +70°C.

The MCM5303 and MCM5003 have positive enables with open collector outputs. The MCM5304 and MCM5004 have positive enables with 2.0 kilohm pullup resistors on the collector outputs.



AL SUFFIX
CASE 684
CERAMIC PACKAGE



L SUFFIX
CERAMIC PACKAGE
CASE 623

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_{in}	-1.0 to +5.5	Vdc
Output Voltage (Open collectors)	V_{OH}	-0.5 to +7.0	Vdc
Thermal Resistance	θ_{JA}	100	°C/W
Operating Temperature Range MCM5303, MCM5304 MCM5003, MCM5004	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +165	°C

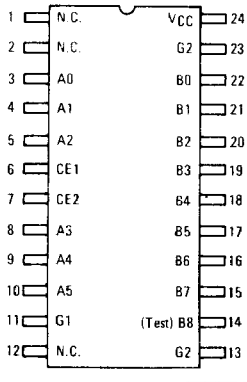
FEATURES:

- Positive Logic for Both Inputs and Outputs
  Logic "0" — Output Device ON (V_{OL})
  Logic "1" — Output Device OFF (V_{OH})
- Logic Levels Compatible with MDTL and All MTTL Families
- Ninth Bit Available for Circuit Test
- Access Time < 75 ns
- Outputs Sink 12 mA Open Collector, 10 mA with Pullup Resistors
- Field Programmable by Blowing Nichrome Links
- Hermetic Package

APPLICATIONS:

- Look Up Tables
- Micro Programs
- Decode Functions
- Code Conversion
- Number Conversion
- Random Logic
- Character Generation

PIN ASSIGNMENT



DC ELECTRICAL CHARACTERISTICS (T_A = -55°C to +125°C for MCM5303 and MCM5304, 0°C to +70°C for MCM5003 and MCM5004 unless otherwise noted)

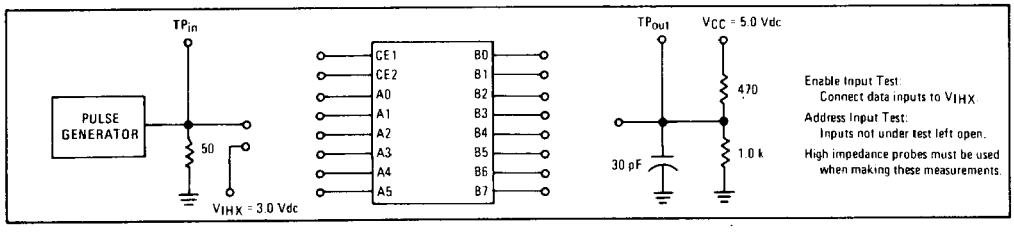
Characteristic		Symbol	Min	Max	Unit
Input Forward Current (V_{IL} = 0.4 Vdc, V_{CC} = 5.25 Vdc)		I_{IL}	–	1.6	mAdc
Input Leakage Current (V_{IH} = V_{CC} = 5.25 Vdc)		I_{IH}	–	100	μAdc
Logic "0" Output Voltage*		V_{OL}			Vdc
(T_A = 0°C to +125°C for MCM5303 and MCM5304, 0°C to +70°C for MCM5003 and MCM5004)					
(I_{OL} = 12 mAdc, V_{CC} = 4.75 Vdc)	Open Collectors		–	0.45	
(I_{OL} = 10 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors		–	0.45	
(T_A = -55°C for MCM5303 and MCM5304)					
(I_{OL} = 12 mAdc, V_{CC} = 4.75 Vdc)	Open Collectors		–	0.50	
(I_{OL} = 10 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors		–	0.50	
Logic "1" Output Voltage (I_{OH} = -0.5 mAdc, V_{CC} = 4.75 Vdc)	Pullup Resistors	V_{OH}	2.5	–	Vdc
Output Leakage Current (V_{CC} = V_{CEX} = 5.25 Vdc)	Open Collectors	I_{CEX}	–	200	μAdc
Power Supply Drain Current		I_{CC}			mAdc
(Enable and all other inputs grounded, V_{CC} = 5.0 Vdc)	Open Collectors		–	95	
	Pullup Resistors		–	120	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C)

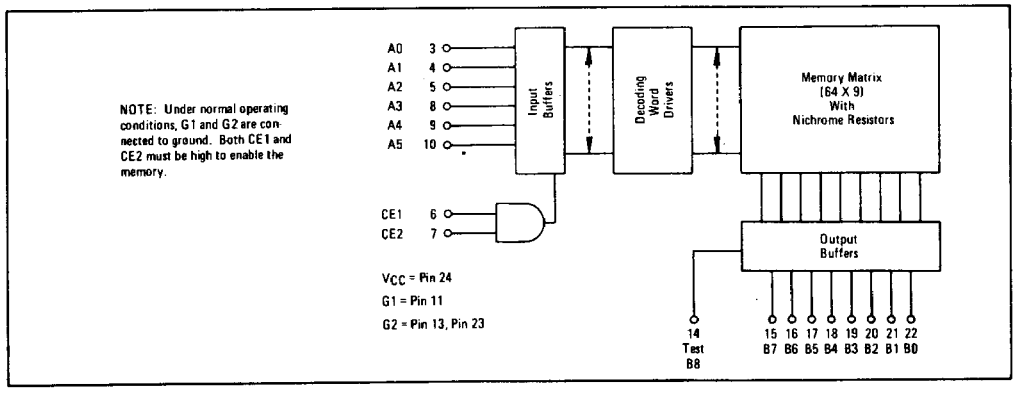
Access Times* (30pF Load)				ns
Address to Output	t_{AO}	25	120	
Enable to Output	t_{EO}	25	120	

*Pin 13 is schematically connected to G2. For optimum propagation delay and V_{OL} characteristics, externally tie Pin 13 to Pin 23 (G2).

SWITCHING TIME TEST CIRCUIT



BLOCK DIAGRAM



PROGRAMMING THE MCM5303/5003 AND MCM5304/5004

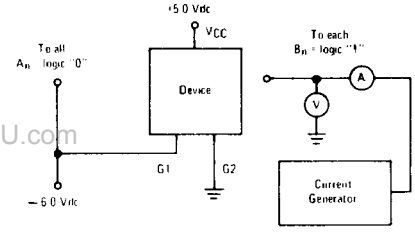
The table and diagram below give instructions for field programming the MCM5303/5003 and MCM5304/5004. All data given is for ambient temperatures of 25°C. If necessary, further programming aid can be obtained from Motorola engineering and product marketing personnel by contacting your nearest Motorola sales office.

Programming Voltage Limits

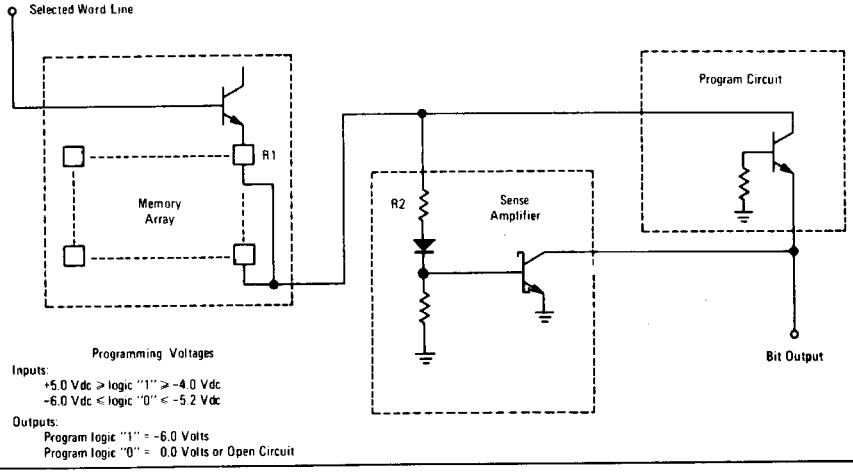
	Symbol	Value	Unit
Address and Chip Enable Voltages	V_{IH} V_{IL}	−4.0 to +5.0 −6.0 to −5.2	Vdc
Power Supply Voltage	V_{CC}	+5.0 ±5%	Vdc
G1 Voltage	V_{G1}	-6.0 ±5%	Vdc
G2 Voltage	V_{G2}	0.0	Vdc
Program Voltage at Desired Bit Output	V_{BP}	-6.0 ±5%	Vdc

Programming Procedure

1. Select the address code desired. Connect low (logic "0") inputs to −6.0 Vdc nominal. Leave high (logic "1") inputs unconnected.
2. With the output voltage of a 120-mA current generator clamped to −6.0 Vdc, apply a negative-going current pulse of 800 ms duration to any output to be programmed as a logic "1".
3. Repeat step 2 for each output to be programmed as a logic "1", one bit at a time.
4. Select next address code desired and repeat steps 2 and 3.



Link Programming Diagram



TRUTH TABLE FORMAT

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WORD 0								
WORD 1								
WORD 2								
WORD 3								
WORD 4								
WORD 5								
WORD 6								
WORD 7								
WORD 8								
WORD 9								
WORD 10								
WORD 11								
WORD 12								
WORD 13								
WORD 14								
WORD 15								
WORD 16								
WORD 17								
WORD 18								
WORD 19								
WORD 20								
WORD 21								
WORD 22								
WORD 23								
WORD 24								
WORD 25								
WORD 26								
WORD 27								
WORD 28								
WORD 29								
WORD 30								
WORD 31								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WORD 32								
WORD 33								
WORD 34								
WORD 35								
WORD 36								
WORD 37								
WORD 38								
WORD 39								
WORD 40								
WORD 41								
WORD 42								
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WORD 58								
WORD 59								
WORD 60								
WORD 61								
WORD 62								
WORD 63								

WHY THE NINTH BIT?

The ninth bit was designed into the MCM5303/MCM5003 and the MCM5304/MCM5004 because field-programmable ROMs present testing problems not encountered with conventional mask-programmable ROMs.

Three areas of testing are affected: Program Element Testing, Functional Testing, and AC Testing. The ninth bit helps to solve the problem of Program Element Testing by assuring that links can be blown without destroying any of the normal 64x8 bit array.

Functional and ac performance are assured by verifying that changes do occur at the outputs as the addresses change. This is important in that all of the outputs are in a logic "0" state regardless of the address selected, and no way is available to determine whether the functions are correctly operating without the ninth testing bit.

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