19-0659; Rev 0; 10/06

EVALUATION KIT AVAILABLE

4V to 72V Input LDOs with Boost Preregulator

General Description

The MAX5092A/MAX5092B/MAX5093A/MAX5093B low-quiescent-current, low-dropout (LDO) regulators contain simple boost preregulators operating at a high frequency. The devices seamlessly provide a preset 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B) LDO output voltage from an automotive cold-crank through load-dump (3.5V to 80V) input voltage conditions. The MAX5092_/MAX5093_ deliver up to 250mA with excellent load and line regulation. During normal operation, when the battery is healthy, the boost preregulator is completely turned off, reducing quiescent current to 65µA (typ). This makes the devices suitable for always-on power supplies.

The buck-boost operation achieved by this combination of LDO and boost preregulator offers the advantage of using a single off-the-shelf inductor in place of the multiple-winding custom magnetics needed in typical single-ended primary inductor converter (SEPIC) and transformer-based flyback topologies. The high operating frequency of the boost regulator significantly reduces component size. The MAX5092_ integrates a blocking diode to further reduce the external component count. The boost preregulator output voltage is preset to 7V. Both LDO and boost output voltages are programmable using external resistors. The boost preregulator output voltage is adjustable up to 11V (MAX5092_), or up to 12V (MAX5093_). The LDO output voltage is adjustable from 1.5V to 9V (MAX5092_) or from 1.5V to 10V (MAX5093_).

The devices feature a shutdown mode with 5µA (typ) shutdown current, a $\overline{HOLD}$ input to implement a self-holding circuit, and a power-on-reset output ($\overline{RESET}$) with an externally programmable timeout period. Additional features include output overload, short-circuit, and thermal protection.

The MAX5092_/MAX5093_ are available in a thermally enhanced, 16-pin 5mm x 5mm thin QFN package and can dissipate up to 2.7W at +70°C on a multilayer PC board.

Applications

Automotive—Body Electronics

Automotive—ECU

Industrial

Typical Operating Circuit and Selector Guide appear at end of data sheet.

Features

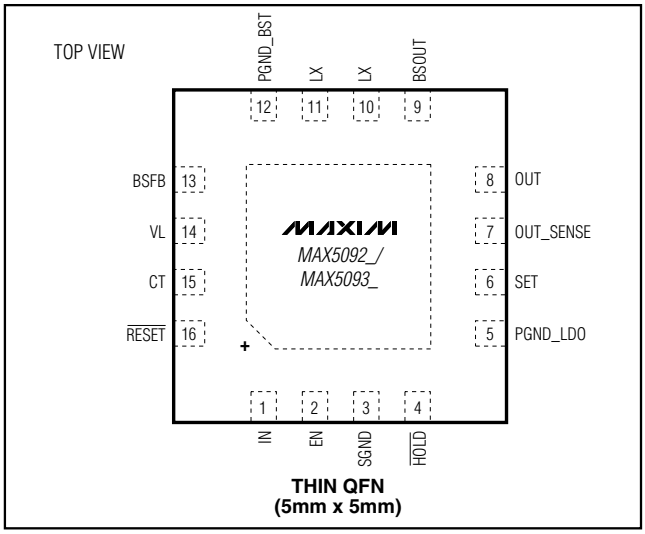
- **Wide Operating Input Voltage Range: 3.5V to 72V with a 4V Startup Voltage**
- **LDO Output Regulates to 5V Seamlessly from an Input Voltage of 3.5V to 72V**
- **Up to 250mA Output Current**
- **Preset 3.3V, 5V, or Externally Programmable LDO Output Voltage from 1.5V to 9V (MAX5092_) or from 1.5V to 10V (MAX5093_)**
- **Preset 7V or Externally Programmable Boost Output Voltage Up to 11V (MAX5092_) or Up to 12V (MAX5093_)**
- **65µA Quiescent Current in LDO Mode (V_{IN} ≥8V)**
- **5µA Shutdown Current**
- **Power-On Reset ($\overline{RESET}$) with Programmable Timeout Period**
- **Output Short-Circuit and Thermal Protection**
- **TQFN Package Capable of Dissipating Up to 2.7W at +70°C**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5092AATE+*	-40°C to +125°C	16 TQFN-EP**	T1655-3
MAX5092BATE+	-40°C to +125°C	16 TQFN-EP**	T1655-3
MAX5093AATE+*	-40°C to +125°C	16 TQFN-EP**	T1655-3
MAX5093BATE+	-40°C to +125°C	16 TQFN-EP**	T1655-3

+Denotes lead-free package.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Pin Configuration



THIN QFN (5mm x 5mm)

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

4V to 72V Input LDOs with Boost Preregulator

ABSOLUTE MAXIMUM RATINGS

IN, EN, LX, BSOUT to SGND .....-0.3V to +80V
PGND_BST, PGND_LDO to SGND .....-0.3V to +0.3V
VL, $\overline{RESET}$, OUT, OUT_SENSE to SGND .....-0.3V to +12V
BSOUT to LX (MAX5092_).....-0.3V to +12V
SET, BSFB, CT to SGND .....-0.3V to +6V
$\overline{HOLD}$ to SGND.....-0.3V to (V_{OUT} + 0.3V)
OUT Current (I_{OUT}) Short Circuit to PGND_LDO,
(V_{IN} ≤ 28V) .....Continuous
$\overline{RESET}$ Sinking Current 5mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin Thin QFN (derate 33.3mW/°C
above +70°C).....2666mW (Note 1)
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: As per JEDEC Standard 51 (Multilayer Board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = 14V, I_{OUT} = 1mA, C_{IN} = 47µF, C_{BSOUT} = 22µF, C_{OUT} = 10µF, C_{VL} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. See Figures 4–7 as applicable. Typical specifications are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Input Voltage Range	V_{IN}	(Note 3)		4		72	V
Internal Input Undervoltage Lockout	V_{UVLOF}	V_{IN} falling		3.0	3.2	3.4	V
	V_{UVLOR}	V_{IN} rising		3.4	3.6	3.8	
Supply Current (Boost Converter Off)	I_Q	LDO mode, I_{OUT} = 100µA	T_J = -40°C to +125°C (Note 4)		65	85	µA
		LDO mode, I_{OUT} = 250mA			70	100	
Supply Current (Boost Converter On)	I_S	V_{IN} = 5V			0.4	1.0	mA
Shutdown Supply Current	I_{SHDN}	V_{EN} ≤ +0.4V	T_J = -40°C to +125°C (Note 4)		6	10	µA
BOOST CONVERTER							
Minimum BSOUT Output Current	I_{BSOUT}	V_{IN} = 4V			250		mA
Boost Converter Disable Threshold	V_{BST_DIS}	V_{IN} rising		7.5	8.0	8.5	V
Boost Converter Disable Threshold Hysteresis					0.5		V
BSOUT Output Voltage	V_{BSOUT}	V_{IN} = 4V, BSFB = SGND		6.65	7.00	7.35	V
Maximum BSOUT Output Voltage	$V_{BSOUT(MAX)}$	MAX5092_			11		V
		MAX5093_			12		
BSFB Regulation Voltage	V_{BSFB}			1.18	1.24	1.30	V
BSFB Input Bias Current	I_{BSFB}					100	nA
Boost Internal Switch On-Resistance	$R_{DS(ON)}$				0.5	1.2	Ω
Boost Internal Switch Minimum Off-Time	t_{OFF}			0.80	1	1.25	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = 14V, I_{OUT} = 1mA, C_{IN} = 47µF, C_{BSOUT} = 22µF, C_{OUT} = 10µF, C_{VL} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. See Figures 4–7 as applicable. Typical specifications are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Internal Switch Maximum On-Time	t_{ON-MAX}			1.80	2.25	2.70	µs
Internal Switch Current Limit	I_{LIM}	Measured in steady-state condition		1.5		3.0	A
Boost Turn-On Response Time		Time from V_{BSOUT} falling below regulation to switch on-time			2	5	µs
Internal Diode Forward Voltage Drop	V_F	MAX5092_ only, I_F = 1A			0.95		V
LDO							
Guaranteed Output Current	I_{OUT}	V_{BSOUT} - V_{OUT} = 2V (Note 5)		250			mA
Output Voltage	V_{OUT}	SET = SGND, MAX5092A/ MAX5093A	I_{OUT} = 1mA	3.25	3.3	3.35	V
			100µA ≤ I_{OUT} ≤ 250mA	3.2	3.3	3.4	
		SET = SGND, MAX5092B/ MAX5093B	I_{OUT} = 1mA	4.900	5	5.075	
			100µA ≤ I_{OUT} ≤ 250mA	4.85	5	5.10	
Minimum Adjustable Output Voltage	V_{ADJMIN}	Boost operation, V_{IN} = 4V, V_{BSOUT} = 7V			1.5		V
Maximum Adjustable Output Voltage	V_{ADJMAX}	Boost operation, V_{IN} = 4V	MAX5092_, V_{BSOUT} = 11V		9		V
			MAX5093_, V_{BSOUT} = 12V		10		
Adjustable Output Voltage	V_{ADJ}	LDO operation, V_{IN} ≥ V_{BST_DIS} (boost converter off) (Note 6)		1.5		10.0	V
Dropout Voltage	ΔV_{DO}	I_{OUT} = 250mA (Note 7)			0.9	1.6	V
LDO Startup Response Time		Rising edge of V_{BSOUT} to the rising edge of V_{OUT}, R_L = 500Ω, SET = SGND			200		µs
Line Regulation	ΔV_{OUT} / ΔV_{IN}	7V ≤ V_{IN} ≤ 72V, I_{LOAD} = 10mA	MAX5092A/MAX5093A			0.4	mV/V
			MAX5092B/MAX5093B			0.5	
		7V ≤ V_{IN} ≤ 28V, I_{LOAD} = 250mA			1.6		
SET Reference Voltage	V_{SET}			1.205	1.235	1.265	V
SET Input Bias Current	I_{SET}				0.5	100	nA
Load Regulation	ΔV_{OUT} / ΔI_{OUT}	I_{OUT} = 1mA to 250mA			0.2	0.6	mV/mA
Power-Supply Rejection Ratio	PSRR	f = 100Hz	I_{OUT} = 10mA, $V_{BSOUT(AC)}$ = 500mV_{P-P}, V_{OUT} = 5V		80		dB
		f = 1MHz	I_{OUT} = 10mA, $V_{BSOUT(AC)}$ = 500mV_{P-P}, V_{OUT} = 5V		60		
Short-Circuit Current	I_{SC}			255	490		mA

4V to 72V Input LDOs with Boost Preregulator

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = 14V, I_{OUT} = 1mA, C_{IN} = 47µF, C_{BSOUT} = 22µF, C_{OUT} = 10µF, C_{VL} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. See Figures 4–7 as applicable. Typical specifications are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE, $\overline{HOLD}$ and $\overline{RESET}$						
EN High Input Threshold	EN_H		2.4			V
EN Low Input Threshold	EN_L				0.4	V
EN Input Bias Current	I_{EN}			0.25	2	µA
$\overline{HOLD}$ Low Input Threshold	V_{IL}	Regulator on, EN transition from high to low			0.4	V
$\overline{HOLD}$ Release Voltage	V_{IH}	EN = low	V_{OUT} - 0.4			V
$\overline{HOLD}$ Pullup Current	I_{HOLD}	Internally connected to OUT		4		µA
$\overline{RESET}$ Voltage Threshold	V_{RESET}	% of V_{OUT}, V_{OUT} falling	87	90	92	%
$\overline{RESET}$ Threshold Hysteresis	V_{RHYST}	% of V_{OUT}		2		%
$\overline{RESET}$ Output Low Voltage	V_{RL}	I_{SINK} = 1mA			0.4	V
$\overline{RESET}$ Output High Leakage Current	I_{RH}	$V_{\overline{RESET}}$ = 5V			1	µA
$\overline{RESET}$ Output Minimum Timeout Period		C_{CT} not connected		25		µs
EN to $\overline{RESET}$ Minimum Timeout Delay		C_{CT} not connected		260		µs
Delay Comparator Threshold (Rising)	V_{CTTH}		1.205	1.24	1.265	V
Delay Comparator Threshold Hysteresis	$V_{CTTH-HYS}$			100		mV
CT Charge Current	I_{CT-CHG}		1.5	2	2.5	µA
CT Discharge Current	I_{CT-DIS}			5		mA

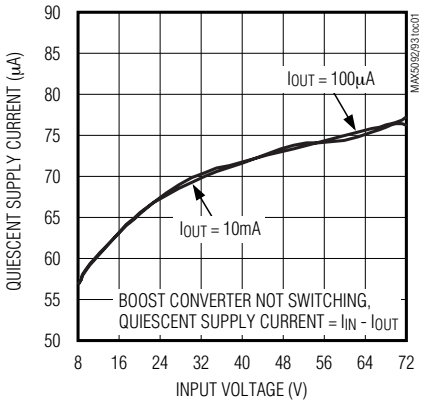
Note 2: Limits at -40°C are guaranteed by design and characterization; not production tested.
Note 3: Guaranteed minimum operating voltage is 3.5V on V_{IN} falling only.
Note 4: Guaranteed by design and not production tested.
Note 5: The continuous maximum output current from the LDO is guaranteed according to the maximum power dissipation imposed by the package thermal constraints.
Note 6: Maximum output adjustable value is conditioned by the maximum adjustable BSOUT Output Voltage Range minus the maximum dropout across the pass transistor.
Note 7: Dropout voltage is defined as (V_{BSOUT} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT} for V_{BSOUT} = V_{OUT} + 2V.

4V to 72V Input LDOs with Boost Preregulator

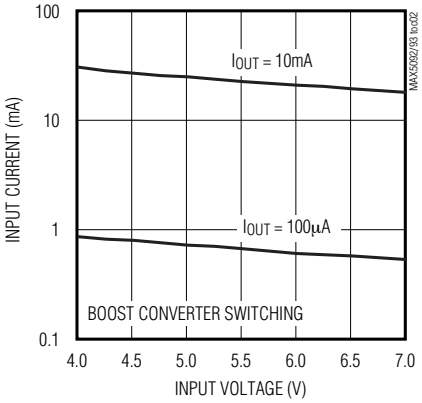
Typical Operating Characteristics

(V_{IN} = V_{EN} = 14V, C_{IN} = 47µF, C_{BSOUT} = 22µF, C_{OUT} = 10µF, C_{VL} = 1µF, T_A = +25°C, unless otherwise noted.) (See Figures 4–7 as applicable.)

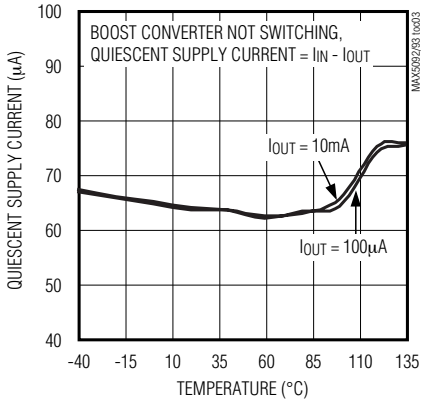
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5092B)



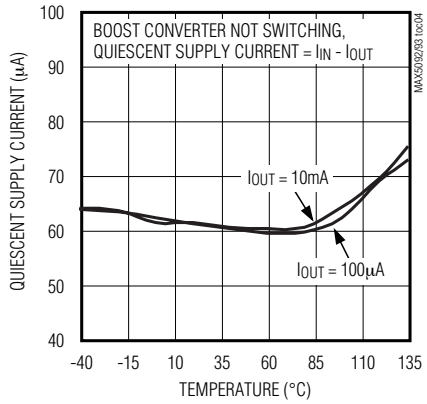
INPUT CURRENT (I_{IN}) vs. INPUT VOLTAGE (MAX5092B)



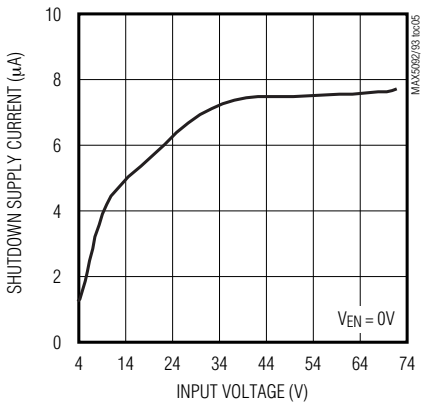
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE (MAX5092B)



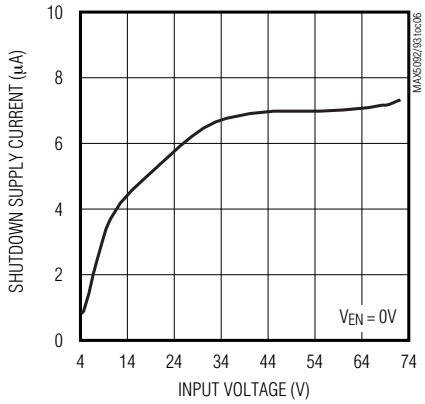
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE (MAX5093B)



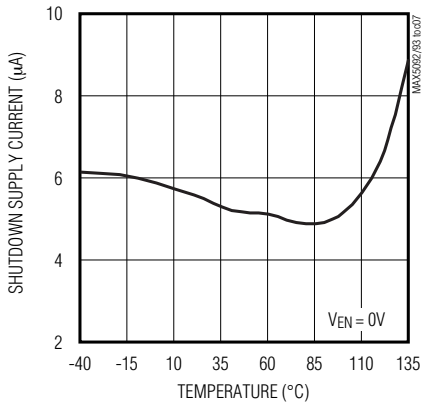
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5092B)



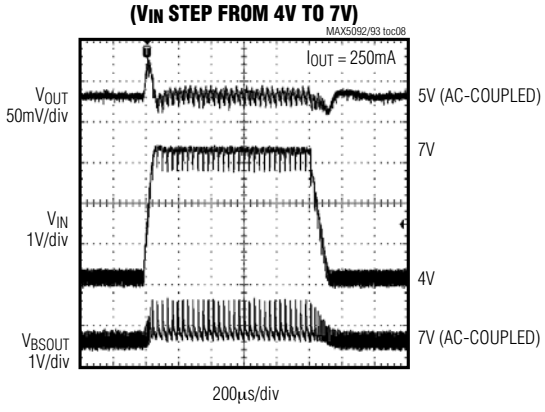
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE (MAX5093B)



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5092B)



LINE-TRANSIENT RESPONSE (V_{IN} STEP FROM 4V TO 7V)

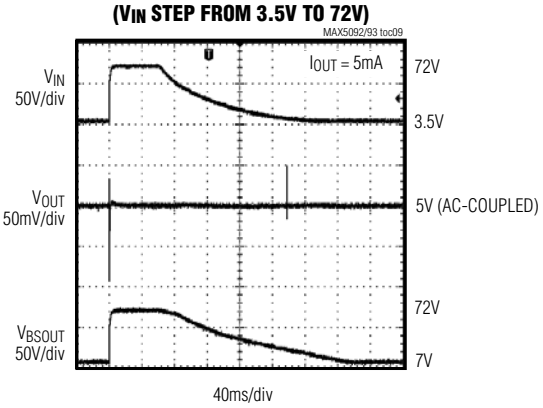


4V to 72V Input LDOs with Boost Preregulator

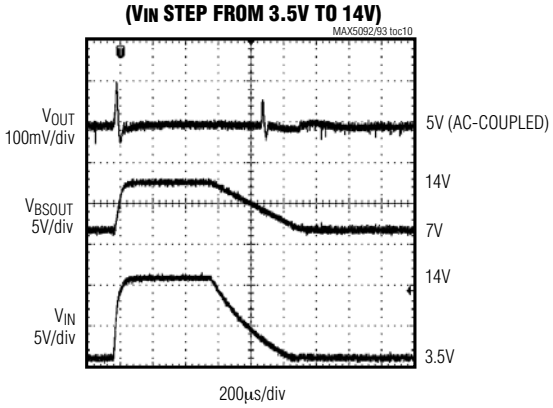
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 14V, C_{IN} = 47µF, C_{BSOUT} = 22µF, C_{OUT} = 10µF, C_{VL} = 1µF, T_A = +25°C, unless otherwise noted.) (See Figures 4–7 as applicable.)

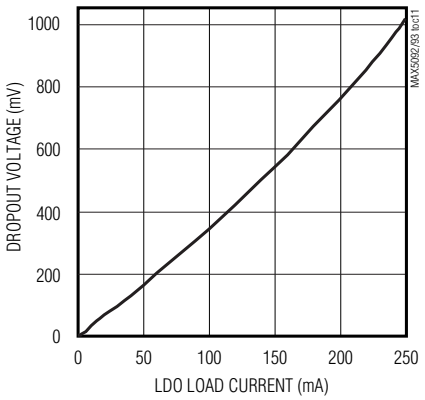
LINE-TRANSIENT RESPONSE (V_{IN} STEP FROM 3.5V TO 72V)



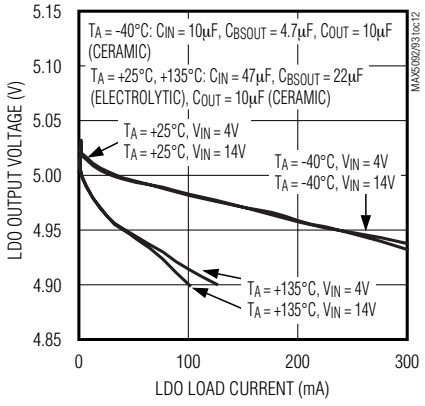
LINE-TRANSIENT RESPONSE (V_{IN} STEP FROM 3.5V TO 14V)



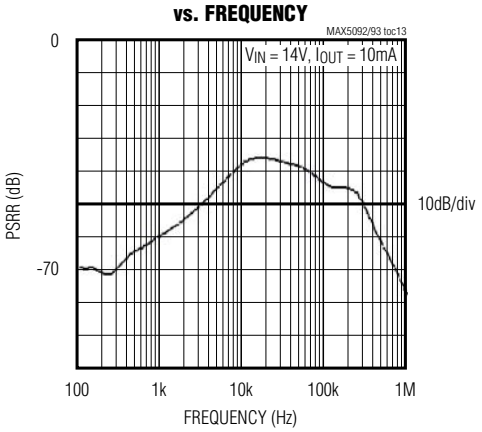
DROPOUT VOLTAGE (V_{BSOUT} - V_{OUT}) vs. LDO LOAD CURRENT



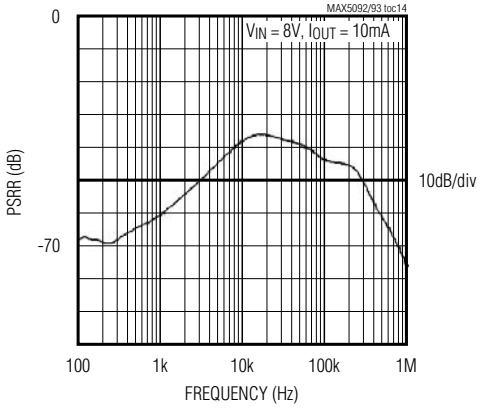
LDO OUTPUT VOLTAGE vs. LDO LOAD CURRENT (MAX5092B)



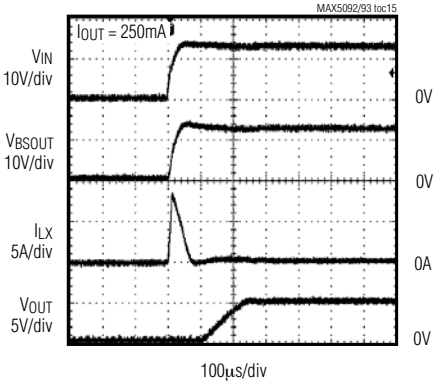
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



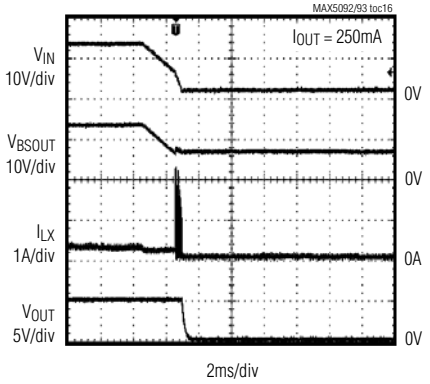
STARTUP THROUGH INPUT VOLTAGE



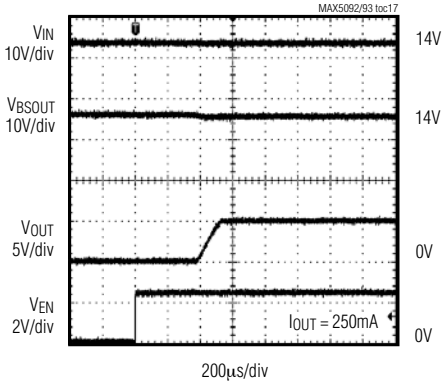
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 14V, C_{IN} = 47µF, C_{BSOUT} = 22µF, C_{OUT} = 10µF, C_{VL} = 1µF, T_A = +25°C, unless otherwise noted.) (See Figures 4–7 as applicable.)

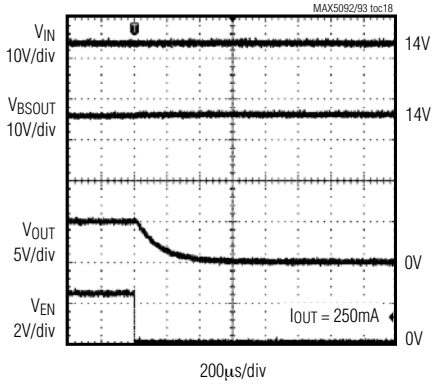
SHUTDOWN THROUGH V_{IN}



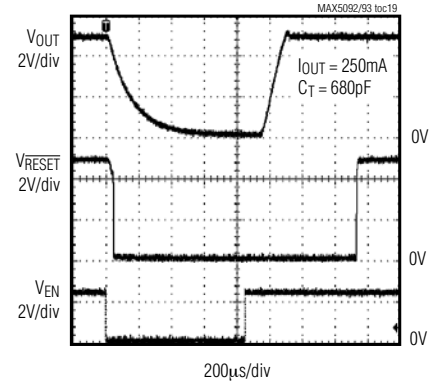
STARTUP THROUGH ENABLE



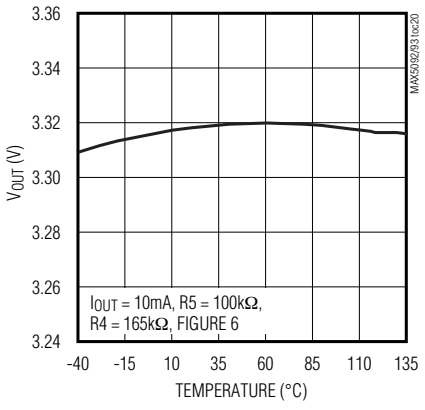
SHUTDOWN THROUGH ENABLE



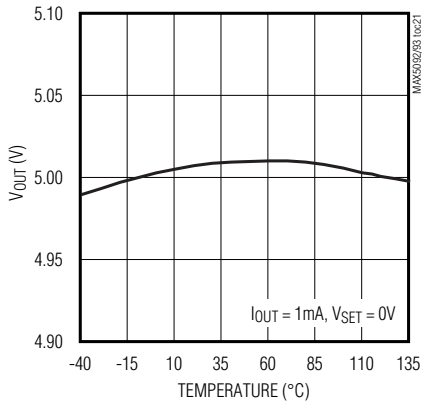
$\overline{RESET}$ TIMING RESPONSE



V_{OUT} vs. TEMPERATURE



V_{OUT} vs. TEMPERATURE (MAX5092B)

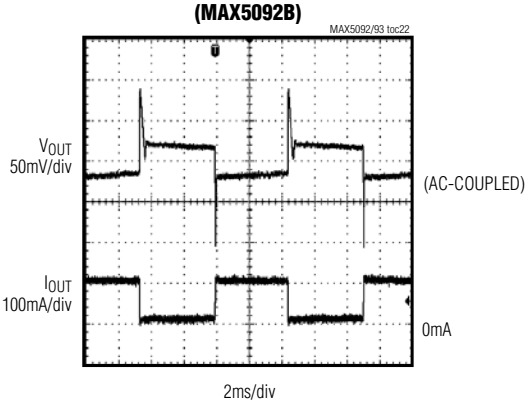


4V to 72V Input LDOs with Boost Preregulator

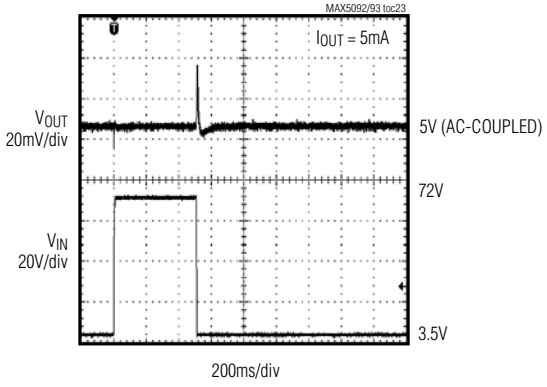
Typical Operating Characteristics (continued)

(V_{IN} = V_{EN} = 14V, C_{IN} = 47µF, C_{BSOUT} = 22µF, C_{OUT} = 10µF, C_{VL} = 1µF, T_A = +25°C, unless otherwise noted.) (See Figures 4–7 as applicable.)

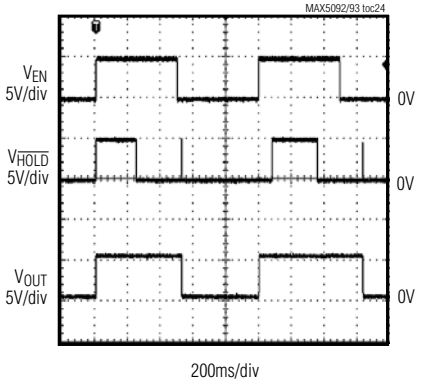
LDO LOAD-TRANSIENT RESPONSE (MAX5092B)



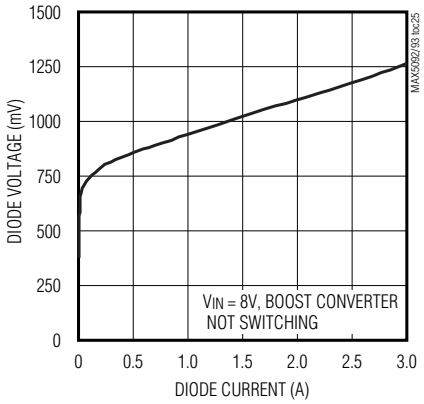
INPUT-VOLTAGE STEP RESPONSE



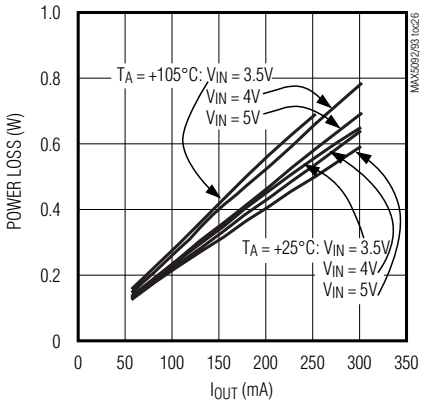
ENABLE AND HOLD TIMING



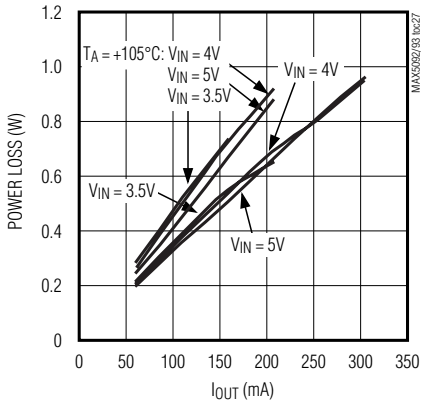
INTERNAL BOOST DIODE FORWARD DROP (MAX5092)



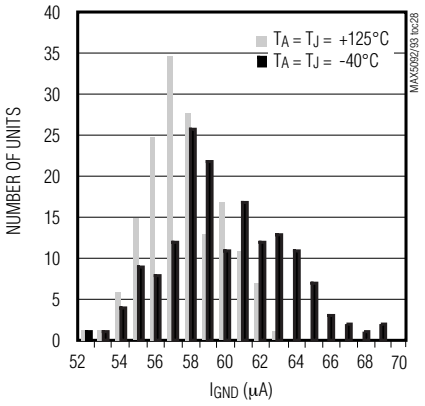
BOOST CONVERTER POWER LOSS (V_{BSOUT} = 7V)



BOOST CONVERTER POWER LOSS (V_{BSOUT} = 11V)



GROUND CURRENT DISTRIBUTION (162 UNITS TESTED)



Pin Description

PIN	NAME	FUNCTION
1	IN	Input Supply Voltage. Bypass IN to the power ground plane with a 47µF (low-ESR) aluminum electrolytic capacitor in parallel with a 1µF ceramic capacitor placed as close to the IC as possible.
2	EN	Enable Input. Drive EN high to turn on the IC. Drive EN low to disable the IC. Connect EN directly to IN for always-on operation.
3	SGND	Signal Ground. Connect SGND to the signal ground plane and the exposed paddle. Connect the power ground and signal ground plane together at the negative terminal of the input capacitor(s).
4	$\overline{HOLD}$	Output Hold. When $\overline{HOLD}$ is forced low, the regulator stores the on-state of the output, allowing the regulator to remain enabled even if EN is pulled low. To shut down the regulator, release $\overline{HOLD}$ after EN is pulled low. If $\overline{HOLD}$ is unused, either connect $\overline{HOLD}$ to OUT or leave unconnected. $\overline{HOLD}$ is internally connected to OUT through a 4µA pullup current.
5	PGND_LDO	LDO Power Ground. Connect PGND_LDO to the power ground plane. Connect the PGND_LDO ground and signal ground plane together.
6	SET	Feedback Input for the LDO. Connect SET directly to SGND to set the output voltage of the LDO to the preset voltage of 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B). Connect SET to the center tap of a resistor-divider connected between the LDO output and SGND to set the output voltage. V_{SET} regulates to 1.24V when using an adjustable output.
7	OUT_SENSE	LDO Regulator Output Sense. Connect OUT_SENSE to OUT at the output capacitor near the load.
8	OUT	LDO Regulator Output. Bypass OUT to the power ground plane with a 10µF ceramic capacitor. V_{OUT} regulates to a preset voltage of 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B), or is adjustable from 1.5V to 9V (MAX5902_) or 1.5V to 10V (MAX5093_).
9	BSOUT	Boost Regulator Output Voltage. Bypass BSOUT to the PGND_BST ground plane with a 22µF (low-ESR) aluminum electrolytic capacitor in parallel with a 1µF ceramic capacitor placed as close to the IC as possible. Connect BSFB directly to SGND to regulate the BOOST output to a fixed voltage of 7V for $V_{IN} \le 7V$. V_{BSOUT} follows V_{IN} for $V_{IN} > 7V$. V_{BSOUT} is programmable up to 11V (MAX5092_) or 12V (MAX5093_) by connecting BSFB to the center tap of an external resistor-divider connected between the BOOST output and PGND_BST.
10, 11	LX	Inductor Connection to the Drain of the Internal Power MOSFET. Connect LX to the switched side of the inductor. Connect pins 10 and 11 together as close to the device as possible. For the MAX5093, also connect LX to the anode of the external Schottky diode.
12	PGND_BST	Boost Regulator Power Ground. Connect PGND_BST to the power ground plane. Connect the PGND_BST ground plane and the signal ground plane together at the negative terminal of the input capacitor(s).
13	BSFB	Feedback Input for the Boost Regulator. Connect BSFB directly to SGND to set the boost regulator output voltage to 7V. Connect BSFB to the center tap of an external resistor-divider connected between BSOUT and SGND to set the output voltage. V_{BSFB} regulates to 1.24V when using an adjustable output.
14	VL	Internal Regulator Output for IC Supply. Bypass VL to SGND with a 1µF/6.3V ceramic capacitor placed as close to the IC as possible. V_{VL} regulates to 5.5V with $V_{BSOUT} \ge 5.5V$.
15	CT	$\overline{RESET}$ Timeout Programming Input. Connect a capacitor from CT to SGND to set the $\overline{RESET}$ timeout period. See the *CT Capacitor Selection* section.
16	$\overline{RESET}$	$\overline{RESET}$ Output. $\overline{RESET}$ is an open-drain output that goes high impedance when V_{OUT} exceeds 92% of the output voltage threshold after a programmed time delay. $\overline{RESET}$ pulls low immediately once V_{OUT} drops below 90% of the regulated LDO output voltage.
—	EP	Exposed Paddle. Connect to the signal ground plane (SGND). Connect to a large-signal ground plane for increased thermal performance.

4V to 72V Input LDOs with Boost Preregulator

Functional Diagrams

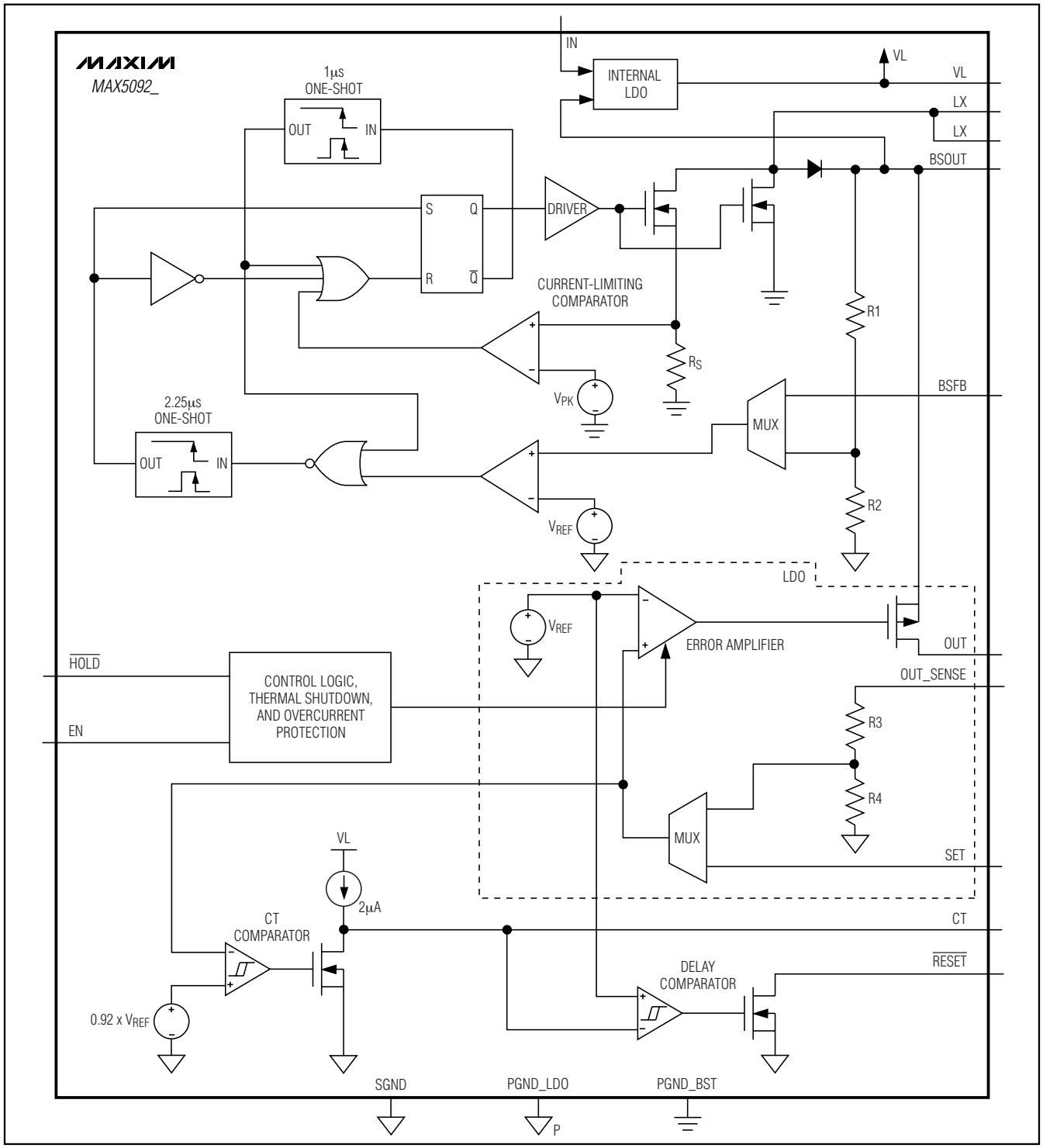


Figure 1. MAX5092_ Functional Diagram

Functional Diagrams (continued)

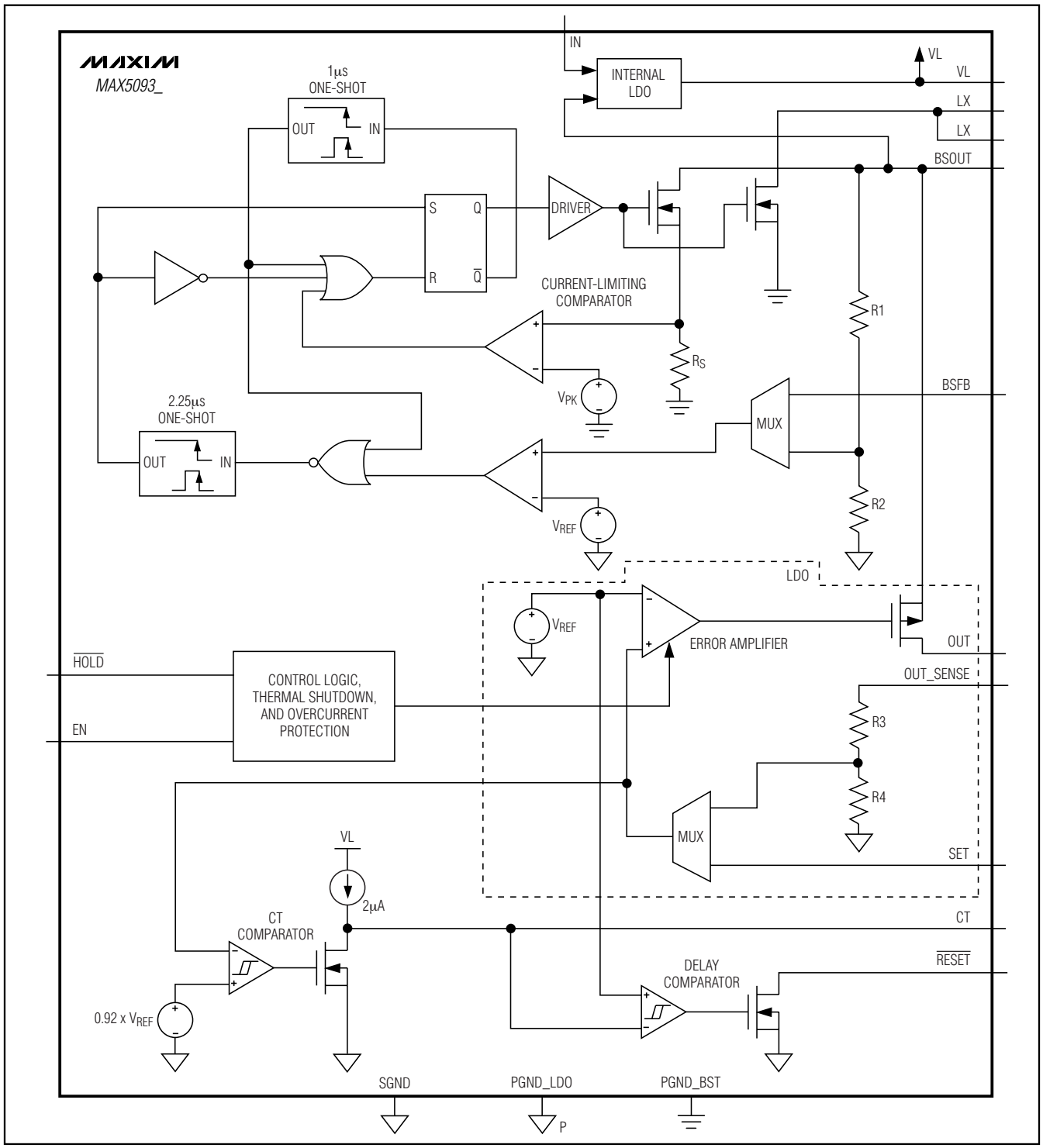


Figure 2. MAX5093_ Functional Diagram

4V to 72V Input LDOs with Boost Preregulator

Detailed Description

The MAX5092A/MAX5092B/MAX5093A/MAX5093B include a step-up, switch-mode DC-DC converter and a linear regulator to provide step-up/-down voltage conversion over a wide range of input voltages. This combination of an LDO and a boost converter offers the advantage of using a single off-the-shelf inductor in place of the multiple-winding custom magnetics needed in typical SEPIC or transformer-based flyback topologies. The boost preregulator is completely turned off during normal automotive operation (V_{IN} = 14V), reduces quiescent current to 65µA (typ), and makes the devices suitable for always-on power supplies.

The devices have an internal UVLO threshold of 3.8V (max, V_{IN} rising) that must be exceeded before the device is enabled. When V_{IN} is above V_{UVLO}, the internal boost converter starts switching and regulates V_{BSOUT} to the programmed boost output voltage. The low quiescent-current LDO steps down V_{BSOUT} to the programmed LDO output voltage. The boost output is preset to 7V, and the LDO output is preset to 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B). Both output voltages can be adjusted by using external resistor-dividers.

If V_{IN} rises above 8V (typ), the boost converter is disabled, forcing V_{BSOUT} to follow V_{IN}. If V_{IN} falls below 7.5V (typ), the boost converter starts switching and regulates V_{BSOUT} to 7V if BSFB is directly connected to SGND. The boost converter regulates V_{BSOUT} for V_{IN} down to 3.5V, providing uninterrupted operation during low cold-crank voltages even if the programmed LDO output voltage is greater than V_{IN} (but less than 9V). The boost converter turn-on response time is less than 10µs, making cold-crank input glitches transparent to the system even at full load.

The boost-converter output is followed by a high PSRR, low-quiescent-current LDO. The LDO rejects the switching noise present at BSOUT and provides a clean, regulated output voltage. The linear regulator uses an internal p-channel MOSFET pass element. Additional features include a power-on-reset function with an externally adjustable timeout, an enable (EN) input, and a hold ($\overline{HOLD}$) regulator control input.

Boost Converter

The switch-mode converter uses a minimum off-time, maximum on-time pulse frequency modulation (PFM) control scheme. The internal MOSFET turns on whenever V_{BSOUT} falls below the regulation point determined by V_{BSFB} (see the *Setting the Boost Output Voltage (V_{BSOUT})* section). The MOSFET turns off when the inductor current reaches the peak current limit (2.5A typ) or after 2.25µs maximum on-time, whichever occurs first. The MOSFET is held off for at least 1µs after the turn-on phase. A new switching cycle initiates once V_{BSOUT} falls below the threshold. In this control scheme, switching frequency and output ripple are functions of load current and input voltage. No frequency compensation is needed in the PFM control scheme.

The output of the boost converter is preset to 7V and is adjustable by using external resistors. See the *Setting the Boost Output Voltage V_{BSOUT}* section. Due to the integrated blocking diode in the MAX5092_, V_{BSOUT} is limited to 11V. Use the MAX5093_ for higher boost output voltages (or to reduce the power dissipation in to the package). The MAX5093_ requires an external diode for the boost converter. Select the external diode according to the *Schottky Diode Selection (MAX5093_)* section.

Linear Regulator

The MAX5092_/MAX5093_ contain an internal p-channel MOSFET used as the pass transistor for the LDO. The output of the boost regulator is connected to the source of the p-MOSFET. The LDO starts up 200µs after the boost regulator starts up. The LDO supplies up to 250mA with a typical dropout voltage of 0.9V. The maximum LDO output current is determined by the package power-dissipation limit as well as the internal current limit. The LDO is designed to be a low-quiescent-current type. During normal operation when the battery voltage is > 9V, the MAX5092_/MAX5093_ consume only 75µA (max) at +85°C and 100µA load.

The output voltage of the LDO is set using the SET input. Connect SET to SGND to use the factory-preset output voltage. Connect SET to the center of an external resistor-divider connected from OUT to SGND to program a different output voltage. See the *Setting the LDO Output Voltage (V_{OUT})* section.

Internal Regulator (VL)

An internal regulator (VL) is used to supply all internal low-voltage blocks. Bypass VL to SGND with a 1µF ceramic capacitor placed as close to the IC as possible. V_{VL} regulates to 5.5V when V_{BSOUT} is above 5.5V. V_{VL} tracks the voltage at BSOUT when V_{BSOUT} is below 5.5V.

Power-On-Reset Output ($\overline{RESET}$)

The MAX5092_/MAX5093_ contain an open-drain output ($\overline{RESET}$) that indicates when the LDO output (V_{OUT}) is out of regulation. If the output of the LDO falls below 90% of the nominal output voltage, $\overline{RESET}$ pulls low after a short delay. Once the output rises above 92% of the nominal output voltage, $\overline{RESET}$ goes high impedance after the programmed reset timeout period. Connect a 100kΩ pullup resistor from OUT to $\overline{RESET}$. See the *CT Capacitor Selection* section for details on setting the $\overline{RESET}$ timeout period.

Enable and Hold Inputs

The MAX5092_/MAX5093_ utilize two logic inputs, EN (active-high) and $\overline{HOLD}$ (active low), to implement a self-holding circuit with no additional components. For example, an automotive ignition switch drives EN high and the regulator turns on. If $\overline{HOLD}$ is then driven low, the regulator remains on even if EN goes low. As long as $\overline{HOLD}$ is forced low and remains low after initial regulator power-up, the regulator remains on. From this state, release $\overline{HOLD}$ (an internal current source connects $\overline{HOLD}$ to OUT), or connect $\overline{HOLD}$ to OUT to turn the regulator off. Drive EN low and $\overline{HOLD}$ high to place the IC into shutdown mode. Shutdown mode reduces supply current to 5µA. Figure 3 shows the timing diagram for the enable and hold functions. Table 1 shows the state of the regulator output with respect to the voltage level at EN and $\overline{HOLD}$ with reference to Figure 3. Connect $\overline{HOLD}$ to OUT or leave unconnected to disable the hold feature and use EN as a standard on/off control input.

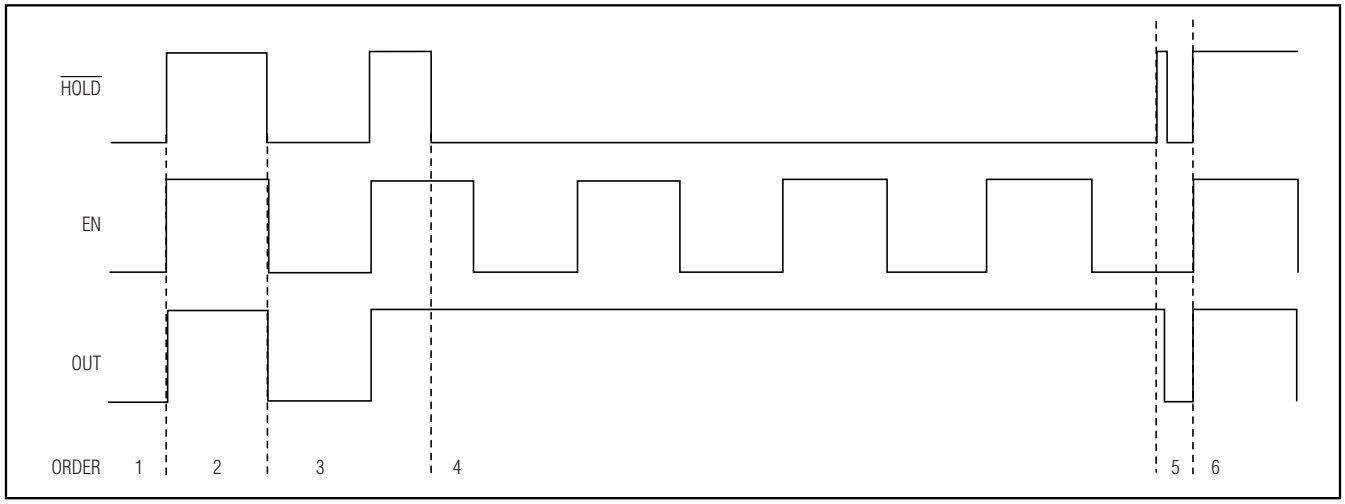


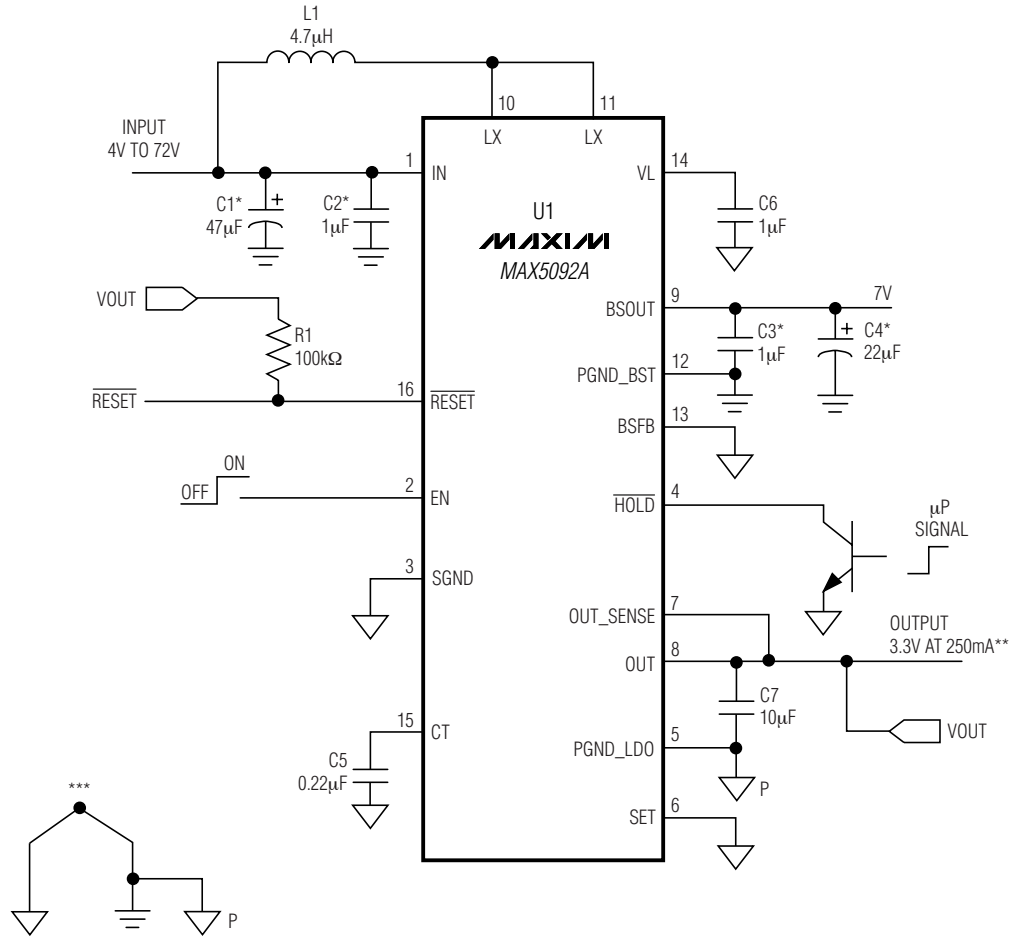
Figure 3. Enable and Hold Timing Diagram

Table 1. Truth Table for Enable and Hold Timing Diagram

ORDER	EN	$\overline{HOLD}$	OUT	COMMENTS
1	Low	X	Off	Initial State. EN has a 500nA pulldown to GND. $\overline{HOLD}$ has an internal current source to OUT. $\overline{HOLD}$ follows OUT.
2	High	Released	On	Regulator output is active when EN is pulled high. $\overline{HOLD}$ is in release state, and it follows OUT.
3	Low	Released	Off	$\overline{HOLD}$ is in release state. OUT follows EN.
4	High	Low	On	$\overline{HOLD}$ is pulled low externally after OUT turns on. The regulator output is forced on regardless of the state of EN. A self-holding state.
5	Low	Released	Off	$\overline{HOLD}$ is released after EN is pulled low. Output turns off.
5	High	X	On	Regulator enabled. Normal turn-on behavior. Regulator follows EN and $\overline{HOLD}$ follows OUT.

4V to 72V Input LDOs with Boost Preregulator

Applications Information



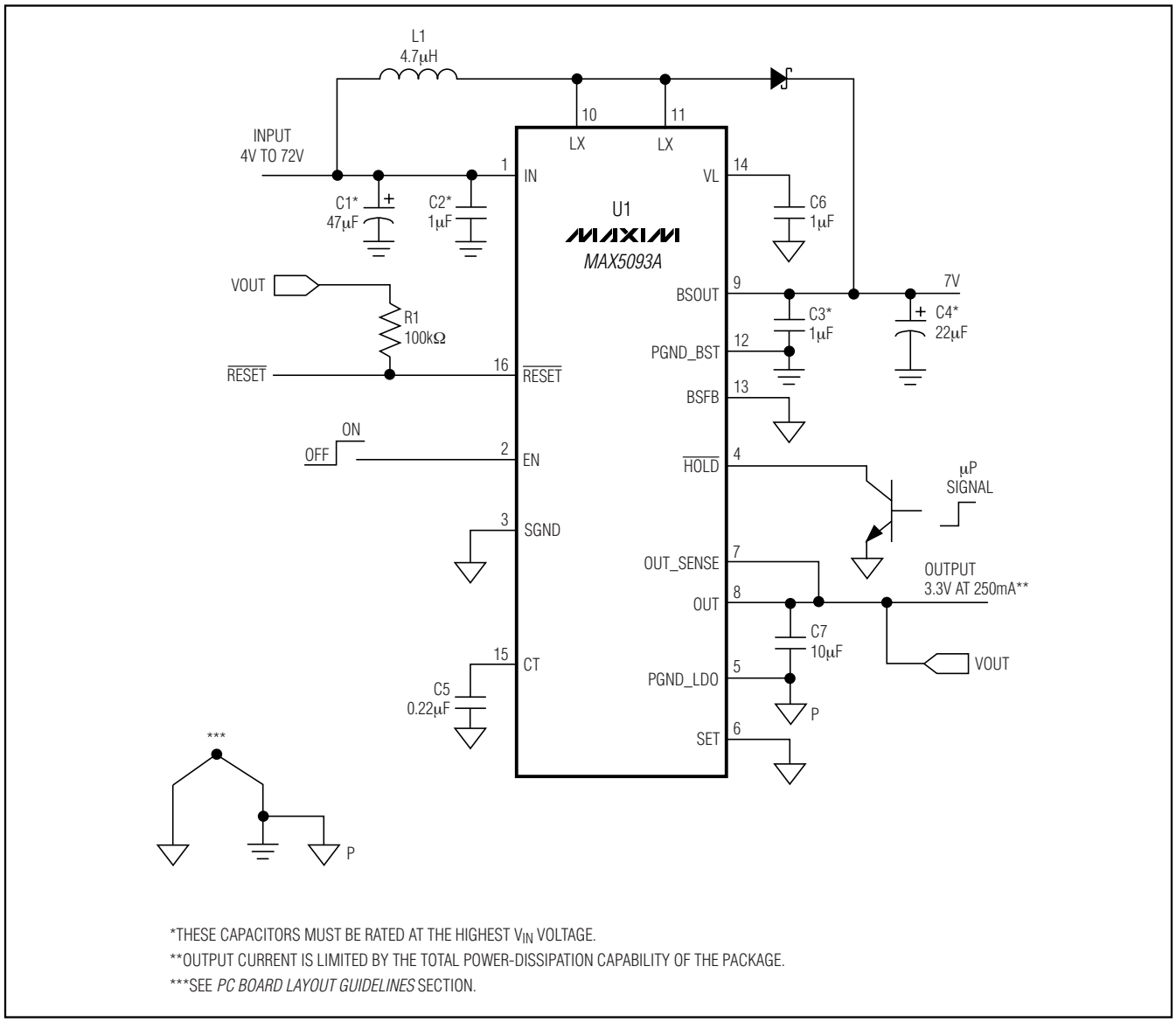
*THESE CAPACITORS MUST BE RATED AT THE HIGHEST V_{IN} VOLTAGE.

**OUTPUT CURRENT IS LIMITED BY THE TOTAL POWER-DISSIPATION CAPABILITY OF THE PACKAGE.

***SEE *PC BOARD LAYOUT GUIDELINES* SECTION.

Figure 4. MAX5092A Typical Application Circuit with Factory Preprogrammed LDO and Boost Output Voltages

Applications Information (continued)



*THESE CAPACITORS MUST BE RATED AT THE HIGHEST V_{IN} VOLTAGE.

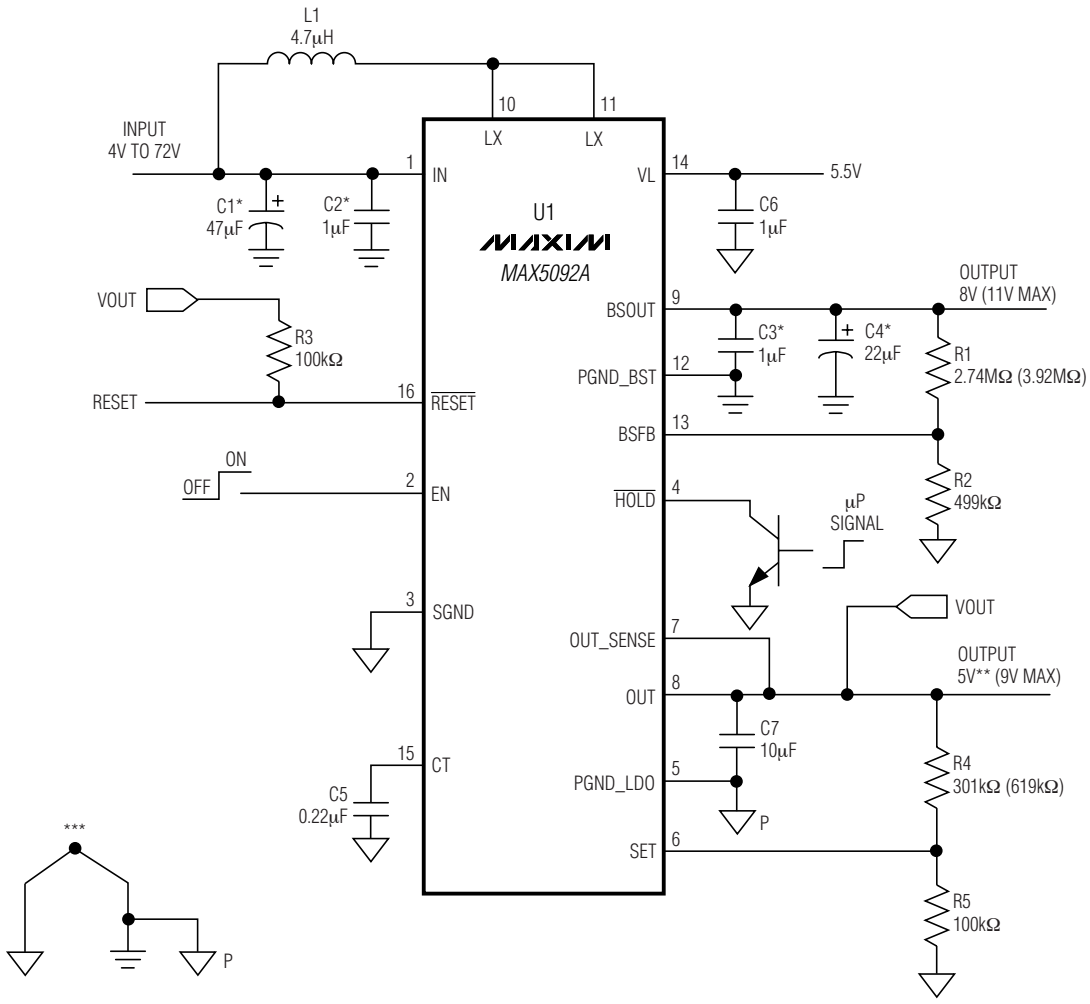
**OUTPUT CURRENT IS LIMITED BY THE TOTAL POWER-DISSIPATION CAPABILITY OF THE PACKAGE.

***SEE *PC BOARD LAYOUT GUIDELINES* SECTION.

Figure 5. MAX5093A Typical Application Circuit with Factory Preprogrammed Boost and LDO Output Voltages

4V to 72V Input LDOs with Boost Preregulator

Applications Information (continued)



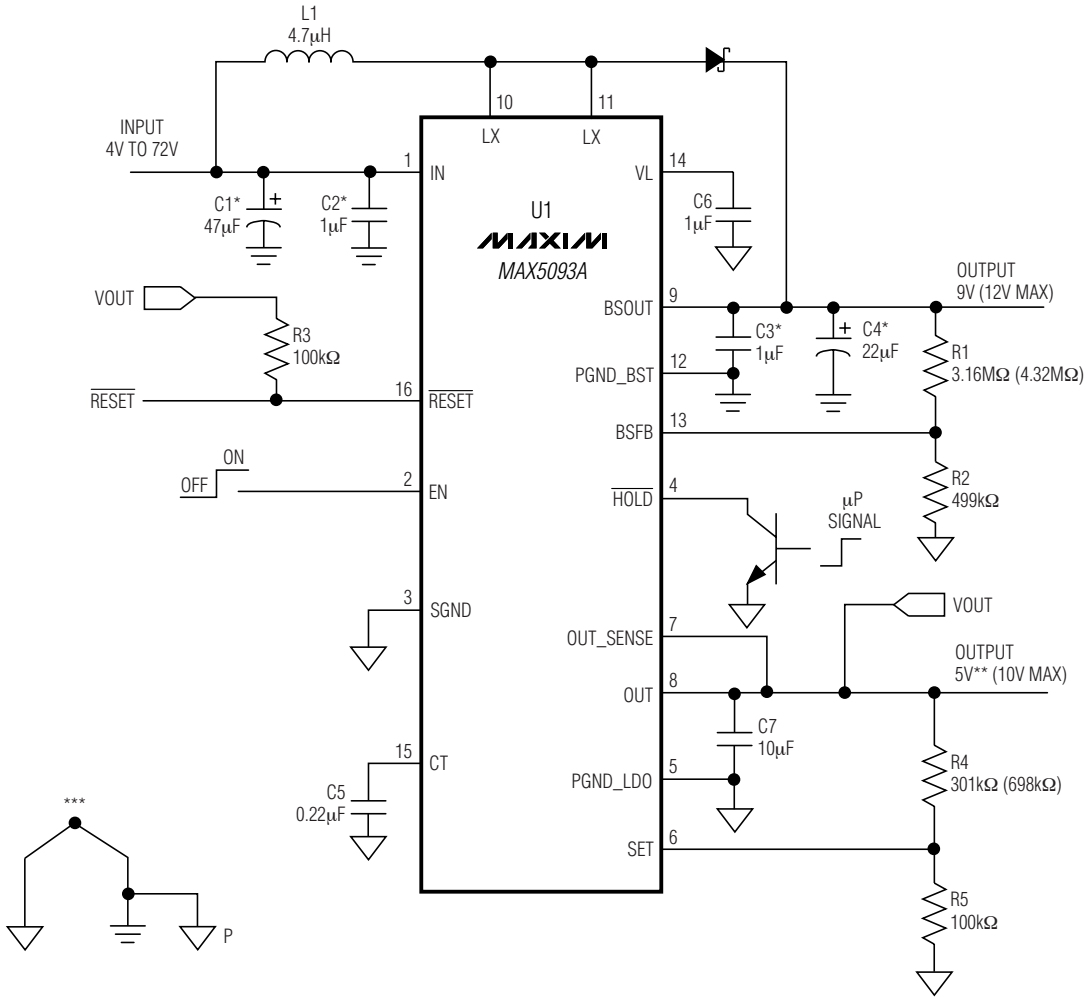
*THESE CAPACITORS MUST BE RATED AT THE HIGHEST V_{IN} VOLTAGE.

**OUTPUT CURRENT IS LIMITED BY THE TOTAL OUTPUT POWER AND THE DISSIPATION CAPABILITY OF THE PACKAGE.

***SEE *PC BOARD LAYOUT GUIDELINES* SECTION.

Figure 6. MAX5092A Typical Application Circuit with User-Programmed LDO and Boost Output Voltages

Applications Information (continued)



*THESE CAPACITORS MUST BE RATED AT THE HIGHEST V_{IN} VOLTAGE.

**OUTPUT CURRENT IS LIMITED BY THE TOTAL OUTPUT POWER AND THE DISSIPATION CAPABILITY OF THE PACKAGE.

***SEE *PC BOARD LAYOUT GUIDELINES* SECTION.

Figure 7. MAX5093A Typical Application Circuit with User-Programmable Boost Output Voltage and LDO Output Voltage

4V to 72V Input LDOs with Boost Preregulator

Design Guidelines

Input Capacitor (C_{IN}) and Boost Capacitor (C_{BSOUT}) Selection

The input current waveform of the boost converter is continuous, and usually does not demand high capacitance at its input. However, the MAX5092_/MAX5093_ boost converter is designed to fully turn on as soon as the input drops below a certain voltage in order to ride out cold-crank droops. This operation demands low input source impedance for proper operation. If the source (battery) is located far from the IC, high-capacity, low-ESR capacitors are recommended for C_{IN}. The worst-case peak capacitor current could be as high as 3A. Use a 47µF, 100mΩ low-ESR capacitor placed as close as possible to the input of the device. Note that the aluminum electrolytic capacitor ESR increases significantly at cold temperatures. In the cold temperature case, choose an electrolyte capacitor with ESR lower than 40mΩ or connect a low-ESR ceramic capacitor (10µF) in parallel with the electrolytic capacitor.

The boost converter output (BSOUT) is fed to the input of the internal 250mA LDO. The boost-converter output current waveform is discontinuous and requires high-capacity, low-ESR capacitors at BSOUT to ensure low V_{BSOUT} ripple. During the on-time of the internal MOSFET, the BSOUT capacitor supplies 250mA current to the LDO input. During the off-time, the inductor dumps current into the output capacitor while supplying the output load current. The internal 250mA LDO is designed with high PSRR; however, high-frequency spikes may not be rejected by the LDO. Thus, high-value, low-ESR electrolytic capacitors are recommended for C_{BSOUT}. Peak-to-peak V_{BSOUT} ripple depends on the ESR of the electrolyte capacitor. Use the following equation to calculate the required ESR (ESR_{BSOUT}) of the BSOUT capacitor:

$$ESR_{BSOUT} = \frac{\Delta V_{ESRBS}}{I_{LIM} - I_{OUT}}$$

where ΔV_{ESRBS} is 75% of total peak-to-peak ripple at BSOUT, I_{LIM} is the internal switch current limit (3A max), and I_{OUT} is the LDO output current. Use a 100mΩ or lower ESR electrolytic capacitor. Make sure the ESR at cold temperatures does not cause excessive ripple voltage. Alternately, use a 10µF ceramic capacitor in parallel with the electrolyte capacitor.

During the switch on-time, the BSOUT capacitor discharges while supplying I_{OUT}. The ripple caused by the capacitor discharge (ΔV_{CBS}) is estimated by using the following equation:

$$\Delta V_{CBS} = \frac{I_{OUT} \times 2.7 \times 10^{-6}}{C_{BSOUT}}$$

where I_{OUT} is the LDO output current and C_{BSOUT} is the BSOUT capacitance.

Inductor Selection

The control scheme of the MAX5092/MAX5093 permits flexibility in choosing an inductor value. Smaller inductance values typically offer smaller physical size for a given series resistance, allowing the smallest overall circuit dimensions. Circuits using larger inductance may provide higher efficiency and exhibit less ripple, but also may reduce the maximum output current. This occurs when the inductance is sufficiently large to prevent the LX current limit (I_{LIM}) from being reached before the maximum on-time (t_{ON-MAX}) expires.

For maximum output current, choose the inductor value so that the controller reaches the current limit before the maximum on-time is reached:

$$L \le \frac{V_{IN} \times t_{ON-MAX}}{I_{LIM}}$$

where t_{ON-MAX} is typically 2.25µs, and the current limit (I_{LIM}) is a maximum of 3A (see the *Electrical Characteristics*). Choose an inductor with the maximum saturation current (I_{SAT}) greater than 3A.

Setting the Boost Output Voltage (V_{BSOUT})

The MAX5092_/MAX5093_ feature Dual Mode™ operation for the internal boost converter output voltage. These devices operate in a preset output-voltage mode or an adjustable output-voltage mode. In preset mode, internal trimmed feedback resistors set V_{BSOUT} to a fixed 7V. Select the preset mode by directly connecting BSFB to SGND (Figures 4 and 5). Ensure a low-impedance path between BSFB and SGND to limit the transient at BSFB to below 100mV. In adjustable mode, connect BSFB to the center tap of an external resistor-divider connected between BSOUT and SGND to program V_{BSOUT} (Figures 6 and 7). Note that the current drawn by the resistor-divider at BSOUT adds to the quiescent current and the shutdown current of the IC. Use the resistor-divider only if V_{BSOUT} is required to be significantly different than 7V. Select 499kΩ or lower resistance value for the bottom resistor (R2) of the divider connected to SGND. The top resistor (R1) value is calculated as:

$$R1 = R2 \times \left(\frac{V_{BSOUT}}{V_{BSFB}} - 1 \right)$$

where V_{BSFB} is the regulation voltage at BSFB (1.24V typ) and V_{BSOUT} is the desired output voltage for BSOUT.

Setting the LDO Output Voltage (V_{OUT})

The LDO output voltage is also Dual Mode (preset and adjustable). Preset mode is selected by connecting SET to SGND (Figures 4 and 5). In preset mode, V_{OUT} regulates to 3.3V (MAX5092A/MAX5093A) or 5V (MAX5092B/MAX5093B) by internal trimmed feedback resistors. Adjustable mode is selected by connecting SET to the center tap of an external resistor-divider connected between OUT and SGND (Figures 6 and 7). Note that the current drawn by the resistor-divider at OUT adds to the quiescent current of the LDO. Use the resistor-divider only if V_{OUT} is required to be significantly different than the preset voltage. Select 100kΩ or lower value for the bottom resistor (R5) of the divider connected to SGND. The top resistor (R4) value is calculated as:

$$R4 = R5 \times \left(\frac{V_{OUT}}{V_{SET}} - 1 \right)$$

where V_{SET} is the regulation voltage at SET (1.24V typ) and V_{OUT} is the desired output voltage for the LDO output.

Schottky Diode Selection (MAX5093_)

The MAX5093_ requires an external diode connected between LX and BSOUT (Figures 5 and 7). Proper selection of an external diode can offer a lower forward-voltage drop and a higher reverse-voltage handling capability. Since the high switching frequency of the IC demands a high-speed rectifier, Schottky diodes are recommended for most applications because of their fast recovery time and low forward-voltage drop. Ensure that the diode's peak current rating is greater than or equal to the peak current limit of internal boost converter MOSFET. A diode average forward current rating of at least 1A is recommended. Additionally, the diode reverse breakdown voltage must be greater than the worst-case load-dump-condition voltage.

CT Capacitor Selection

The MAX5092_/MAX5093_ contain an open-drain power-on-reset output ($\overline{RESET}$) that indicates when the LDO output voltage (V_{OUT}) is out of regulation. When V_{OUT} rises above 92% of the nominal output voltage, $\overline{RESET}$ goes high impedance after a user-programmable time delay. This time duration is programmable by a capacitor (C_{CT}) from CT to SGND (Figures 4–7). For a chosen $\overline{RESET}$ active timeout period (t_{DELAY}), calculate the required capacitor value as:

$$C_{CT} = \frac{2 \times 10^{-6} \times t_{DELAY}}{1.24}$$

When V_{OUT} drops below 90% of the LDO output regulation voltage, a 5mA pulldown current from CT to SGND discharges C_{CT}. The time required to discharge CT determines the delay necessary to pull $\overline{RESET}$ low. This delay provides glitch immunity to the $\overline{RESET}$ function. The glitch immunity delay is directly proportional to the CT capacitor and is approximately 70µs for a 0.1µF capacitor at CT.

Dual Mode is a trademark of Maxim Integrated Products, Inc.

4V to 72V Input LDOs with Boost Preregulator

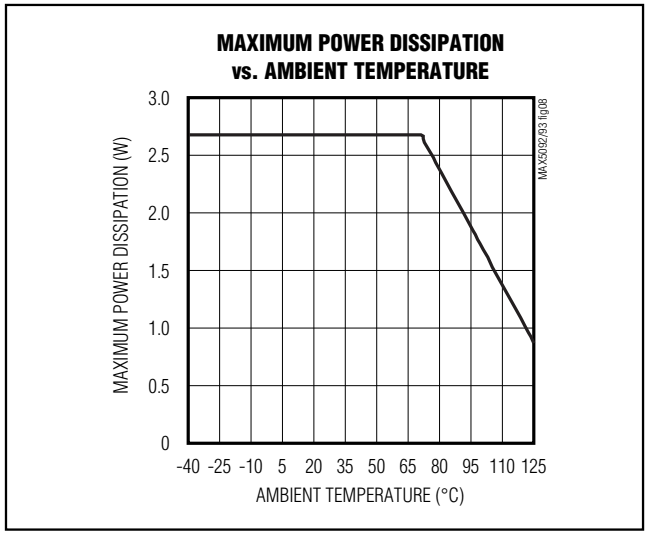


Figure 8. MAX5092/MAX5093 Package Power Dissipation

Maximum Output Current (I_{OUT_MAX})

The MAX5092_/MAX5093_ high input voltage (+72V max) provides up to 250mA of current from OUT. Package power-dissipation limits the amount of output current available for a given input/output voltage and ambient temperature. Figure 8 depicts the maximum power-dissipation curve for the devices. The graph assumes that the exposed metal pad of the IC package is soldered to the PC board copper according to the JEDEC 51 standard (multilayer board). Use Figure 8 to determine the allowable package dissipation for a given ambient temperature. Alternately, use the following formula to calculate the allowable package dissipation (P_{DISS}) in watts:

For $T_A \le +70°C$:

$$P_{DISS} = 2.67$$

For $+70°C < T_A \le +125°C$:

$$P_{DISS} = 2.67 - (0.0333 \times (T_A - 70))$$

where $+70°C < T_A \le +125°C$ and 0.0333W/°C is the package thermal derating. After determining the allowable package dissipation, calculate the maximum output current (I_{OUT_MAX}) using the following formula:

$$I_{OUT\_MAX} = \frac{P_{DISS} - P_{LOSS(BST)}}{V_{IN} - V_{OUT}}$$

where P_{DISS} is the allowable package power dissipation and $P_{LOSS(BST)}$ is the boost converter power loss. P_{DISS} includes the losses in the boost converter operation and the LDO itself. The boost converter loss $P_{LOSS(BST)}$, depends on V_{IN}, V_{BSOUT}, and I_{OUT}. See the Boost Converter Power Loss graphs in the *Typical Operating Characteristics* to estimate the losses at a given V_{IN} and V_{BSOUT} at room temperature. At a higher ambient temperature of +105°C, $P_{LOSS(BST)}$ increases by up to 20% due to higher R_{DS-ON} and switching losses of the internal boost converter MOSFET. (Note: I_{OUT_MAX} must be less than 250mA).

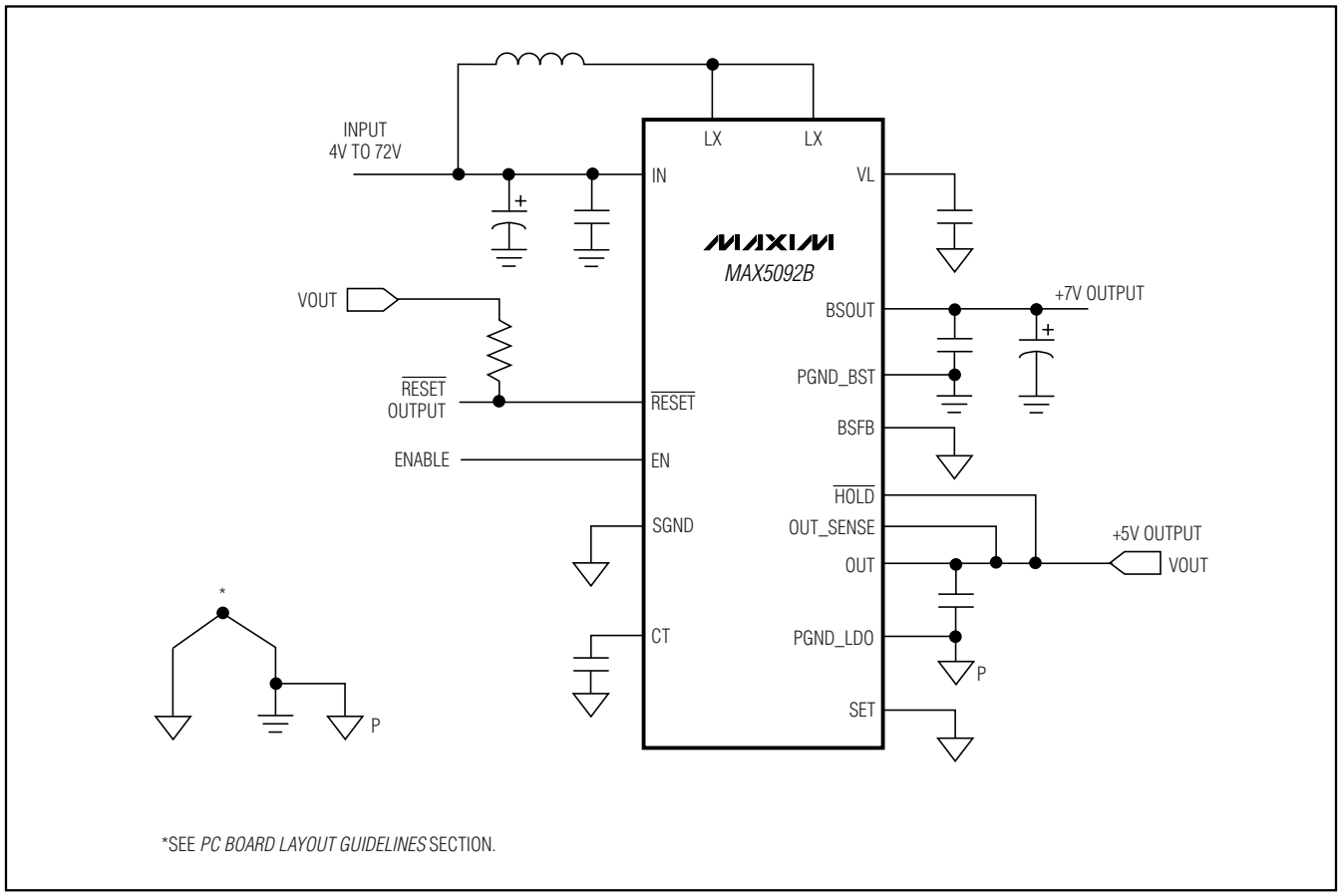
PC Board Layout Guidelines

Good PC board (PCB) layout and routing are required in high-frequency switching power supplies to achieve proper regulation and stability. It is strongly recommended that the evaluation kit PCB layouts be followed as closely as possible. Refer to the MAX5092 EV kit for an example layout. Follow these guidelines for good PCB layout:

1) For SGND, use a large copper plane under the IC and solder it to the exposed paddle. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose this copper area on the top and bottom side of the PCB. Do not make a direct connection from the EP copper plane to pin 3 (SGND) underneath the IC so as to minimize ground bounce.
2) Isolate the power components and high-current path from the sensitive analog circuit.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
4) Connect the return terminals of input capacitors and boost output capacitors to the PGND_BST power ground plane. Connect the power ground (PGND_BST) and signal ground (SGND) planes together at the negative terminal of the input capacitors. Do not connect them anywhere else. Connect PGND_LDO ground plane to SGND ground plane at a single point.
5) Ensure that the feedback connections are short and direct. Ensure a low-impedance path between BSFB and SGND to limit the transient at BSFB to 100mV.
6) Route high-speed switching nodes away from the sensitive analog areas. Use the internal PCB layer for SGND as an EMI shield to keep radiated noise away from the IC, feedback dividers, and bypass capacitors.

4V to 72V Input LDOs with Boost Preregulator

Typical Operating Circuit



*SEE *PC BOARD LAYOUT GUIDELINES* SECTION.

Selector Guide

PART	PRESET LDO OUTPUT (V)	ADJUSTABLE LDO OUTPUT	PRESET BSOUT OUTPUT (V)	ADJUSTABLE BSOUT OUTPUT	BOOST DIODE
MAX5092AATE+	3.3	Yes	7	Yes	Internal
MAX5092BATE+	5	Yes	7	Yes	Internal
MAX5093AATE+	3.3	Yes	7	Yes	External
MAX5093BATE+	5	Yes	7	Yes	External

Chip Information

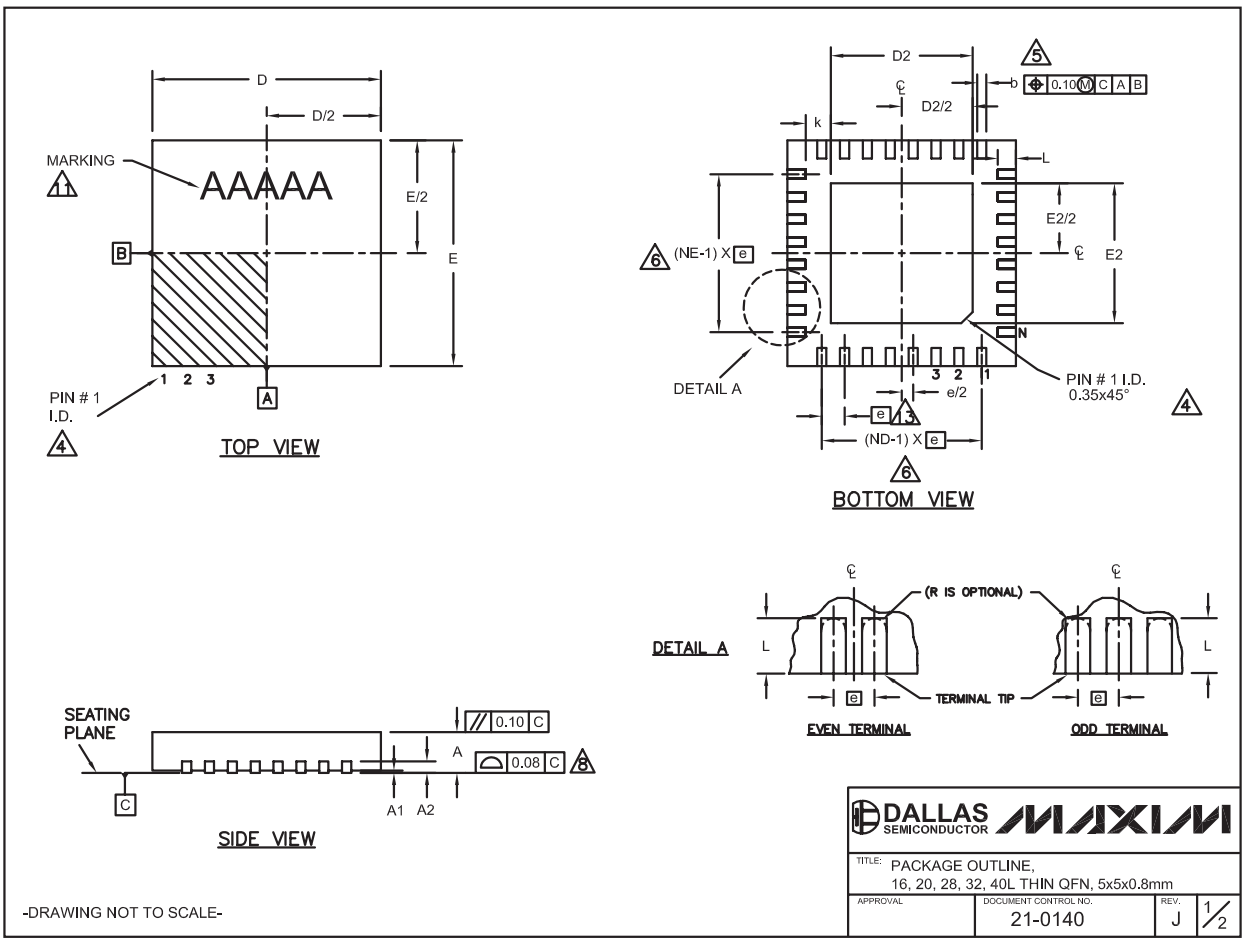
PROCESS: BiCMOS

4V to 72V Input LDOs with Boost Preregulator

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



4V to 72V Input LDOs with Boost Preregulator

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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