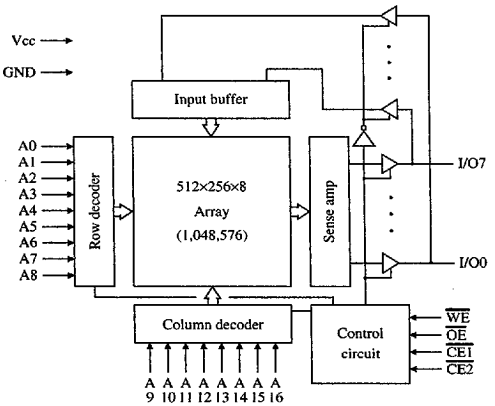
Low power 128K×8 CMOS SRAM (Common I/O)

Advance information

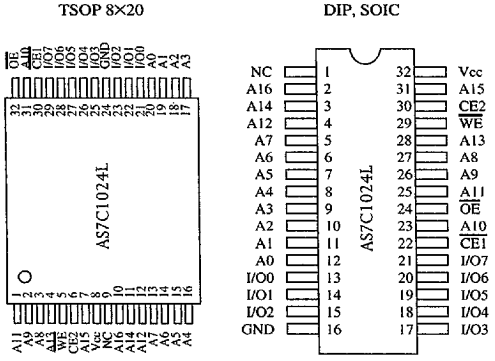
Features

- Organization: 131,072 words × 8 bits
- Single 5V power supply
- High speed
  - 55/70 ns address access time
  - 30/35 ns output enable access time
- Very low power consumption
- Active:385 mW max, (55 ns cycle)
  - Standby: 550 µW max, CMOS I/O, L version
    138 µW max, CMOS I/O, LL version
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- Ideal for modem, portable computing, handheld instruments
  - 75% power reduction during CPU idle mode
- 32-pin JEDEC standard packages
  - 600 mil PDIP
  - 445 mil SOIC
  - 8 × 20 TSOP
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement



Selection guide

		7C1024L-55	7C1024L-70	Unit
Maximum address access time		55	70	ns
Maximum output enable access time		30	35	ns
Maximum operating current		70	70	mA
Maximum CMOS standby current	L	100	100	µA
	LL	25	25	µA

Functional description

The AS7C1024L is a low power CMOS 1,048,576-bit Static Random Access Memory (SRAM) organized as 131,072 words × 8 bits.

The device enters standby mode when $\overline{CE1}$ is HIGH or CE2 is LOW. CMOS standby mode consumes a maximum of ≤18. mW (≤3.6mW for the L version). Normal operation offers 75% power reduction after initial access, resulting in significant power savings during CPU idle, suspend, and stretch mode. Both versions of the AS7C1024L offer 2.0V data retention.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 55/70 ns with output enable access times (t_{OE}) of 30/35 ns are ideal for high performance applications. The active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and 5V tolerant. Operation is from a single 5.0±0.5V supply. The AS7C1024L is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{CC}	−0.5	+7.0	V
Input voltage relative to GND	V_{IN}	−0.5	V_{CC}+0.5	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	−55	+150	°C
Temperature under bias	T_{bias}	−10	+85	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB}, I_{SB1})
X	L	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	H	High Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

T_a = 0°C to +70°C

Parameter	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
	V_{IL}	−0.3†	–	0.8	V

†V_{IL} min = −2.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics [1]

V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0°C to +70°C

Parameter	Symbol	Test conditions		L version Min	L version Max	LL version Min	LL version Max	Unit
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = GND to V_{CC}		–	1	–	1	µA
Output leakage current	$\|I_{LO}\|$	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{CC} = Max, V_{out} = GND to V_{CC}		–	1	–	1	µA
Operating power supply current	I_{CC}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, f = f_{max}, I_{out} = 0 mA		–	70	–	70	mA
Standby power supply current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, f = f_{max}		–	3	–	2	mA
	I_{SB1}	$\overline{CE1}$ ≥ V_{CC}−0.2V or CE2 ≤ 0.2V, V_{in} ≤ 0.2V or V_{in} ≥ V_{CC}−0.2V, f = 0	LL	–	100	–	100	µA
Output voltage	V_{OL}	I_{OL} = 2.1 mA, V_{CC} = Min		–	0.4	–	0.4	V
	V_{OH}	I_{OH} = −1.0 mA, V_{CC} = Min		2.4	–	2.4	–	V

Capacitance [2]

f = 1 MHz, T_a = Room temperature, V_{CC} = 3.3V

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	6	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	8	pF

SRAM

Key to switching waveforms

Rising input | Falling input | Undefined output/don't care

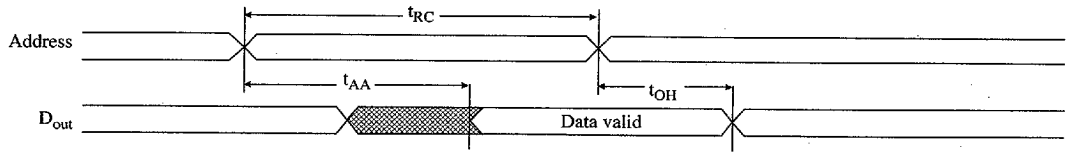
Read cycle [3,9,12]

(V_{CC} = 5.0±0.5V, GND = 0V, T_a = 0°C to +70°C)

		-55		-70			
Parameter	*Symbol*	*Min*	*Max*	*Min*	*Max*	*Unit*	*Notes*
Read cycle time	t_{RC}	55	–	70	–	ns	
Address access time	t_{AA}	–	55	–	70	ns	3
Chip enable ($\overline{CE1}$) access time	t_{ACE1}	–	55	–	70	ns	3, 12
Chip enable (CE2) access time	t_{ACE2}	–	55	–	70	ns	3, 12
Output enable ($\overline{OE}$) access time	t_{OE}	–	30	–	35	ns	
Output Hold from address change	t_{OH}	5	–	5	–	ns	5
$\overline{CE1}$ LOW to output in Low Z	t_{CLZ1}	10	–	10	–	ns	4, 5, 12
CE2 HIGH to output in Low Z	t_{CLZ2}	10	–	10	–	ns	4, 5, 12
$\overline{CE1}$ HIGH to output in High Z	t_{CHZ1}	–	20	–	25	ns	4, 5, 12
CE2 LOW to output in High Z	t_{CHZ2}	–	20	–	25	ns	4, 5, 12
$\overline{OE}$ LOW to output in Low Z	t_{OLZ}	5	–	5	–	ns	4, 5
$\overline{OE}$ HIGH to output in High Z	t_{OHZ}	–	20	–	25	ns	4, 5

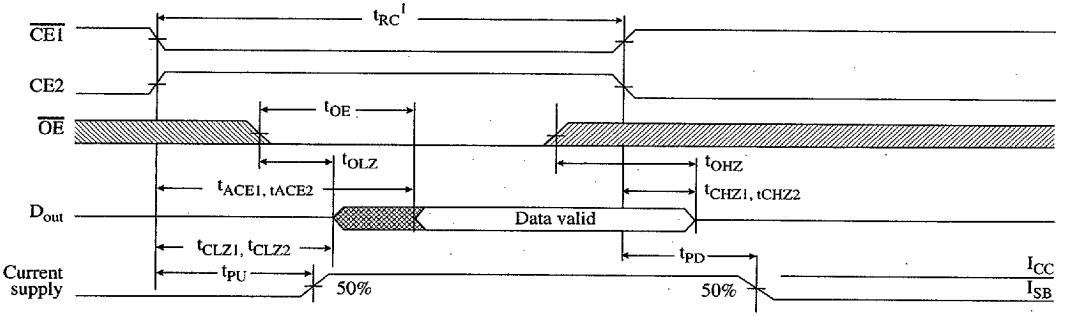
Read waveform 1 [3,6,7,9,12]

Address controlled



Read waveform 2 [3,6,8,9,12]

$\overline{CE1}$ and CE2 controlled



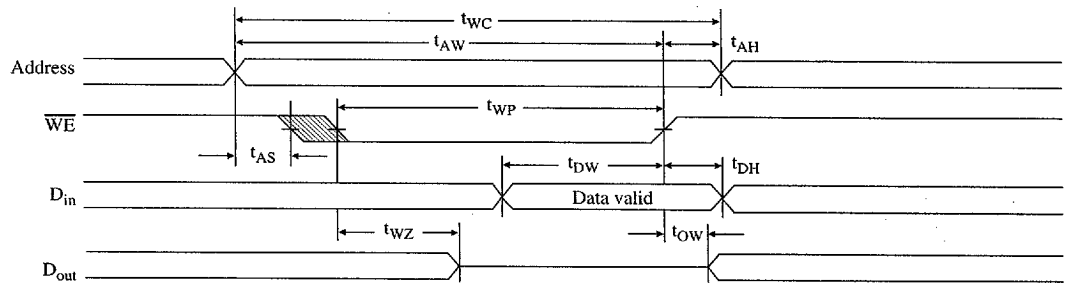
Write cycle [11,12]

V_{CC} = 5.0±0.5V, GND = 0V, Ta = 0°C to +70°C

		-55		-70			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	55	–	70	–	ns	
Chip enable ($\overline{CE1}$) to write end	t_{CW1}	50	–	60	–	ns	12
Chip enable (CE2) to write end	t_{CW2}	50	–	60	–	ns	12
Address setup to write end	t_{AW}	50	–	60	–	ns	
Address setup time	t_{AS}	0	–	0	–	ns	12
Write pulse width	t_{WP}	40	–	50	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	ns	
Data valid to write end	t_{DW}	25	–	30	–	ns	
Data hold time	t_{DH}	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}	–	25	–	30	ns	4, 5
Output active from write end	t_{OW}	5	–	5	–	ns	4, 5

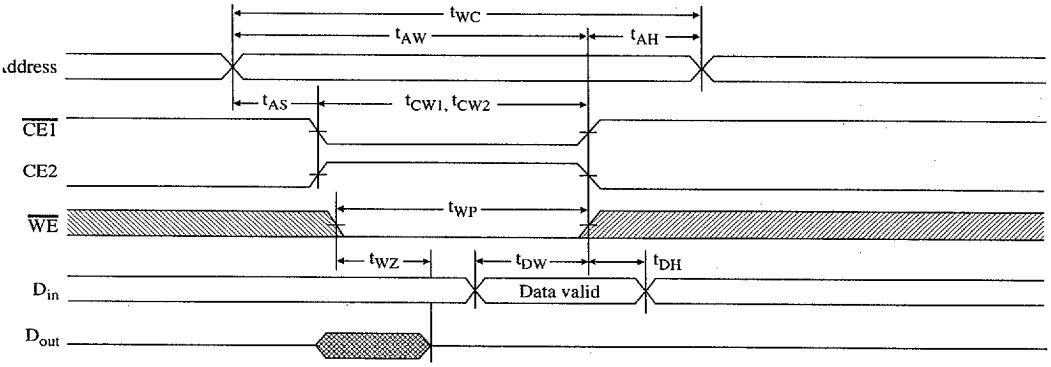
Write waveform 1 [10,11,12]

$\overline{WE}$ controlled



Write waveform 2 [10,11,12]

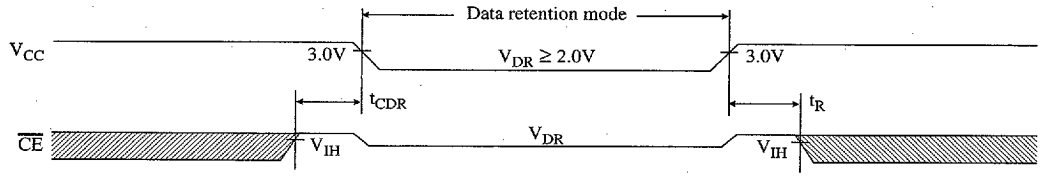
$\overline{CE1}$ and CE2 controlled



Data retention characteristics

Parameter		Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention		V_{DR}	V_{CC} = 2.0V	2.0	–	V
Data retention current	L	I_{CCDR}	$\overline{CE1} \geq V_{CC}-0.2V$ or CE2 ≤ 0.2V	–	50	µA
	LL			–	10	µA
Chip enable to data retention time		t_{CDR}	$V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	0	–	ns
Operation recovery time		t_R		5	–	ns
Input leakage current		$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

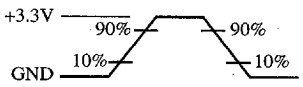


Figure A: Input waveform

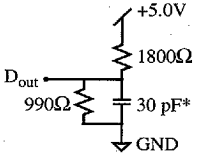


Figure B: Output load

Thevenin equivalent:

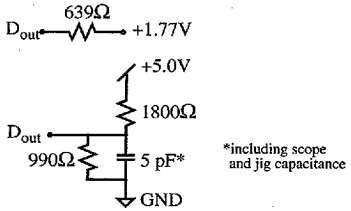


Figure C: Output load for t_{CLZ}, t_{CHZ}

Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE1}$ or $\overline{WE}$ must be HIGH or CE2 LOW during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 $\overline{CE1}$ and CE2 have identical timing.

AS7C1024L ordering information

Package \ Access Time	55 ns	70 ns
Plastic DIP, 600 mil	AS7C1024L-55PC AS7C1024LL-55PC	AS7C1024L-70PC AS7C1024LL-70PC
Plastic SOIC, 445 mil	AS7C1024L-55JC AS7C1024LL-55JC	AS7C1024L-70JC AS7C1024LL-70JC
TSOP 8x20	AS7C1024L-55TC AS7C1024LL-55TC	AS7C1024L-70TC AS7C1024LL-70TC

AS7C1024L part numbering system

AS7C	1024	XX	–XX	X	C
SRAM prefix	Device number	L = Low power LL= Very low power	Access time	Package: P = PDIP 600 mil S = SOIC 445mil T = TSOP 8x20	Commercial tmperature range, 0°C to 70 °C