A2624/A2625

Turbo 3D USB+PS/2 optical mouse controller

1. General Description

A2624/A2625 is a 3D 5key crystal-free optical mouse controller designed for USB and PS/2 applications. It minimizes external components to ensure competitive low cost BOM. A2624/A2625 supports the USB Standard v1.1 as well as HID Class Definition v1.1. It is compatible with Microsoft 3D Intellimouse and IBM PS/2 mouse. It also supports mechanical scroll, opto-mechanical scroll.

2. Features

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- Crystal-free design with internal oscillator directly feeding clock to sensor implements totally crystal-free system design
- Spread spectrum function to reduce EMI
- SPI interface to control the sensor IC with minimal wire line connection
- Microsoft 3D Intellimouse and IBM PS/2 mouse compatible
- Complete USB v1.1 1.5Mbps compatibility
- Complete USB HID v1.1 compatibility
- USB Plug and Play functions
- Compatible with PS/2 protocol
- Supports Windows2000 and XP ,ME, 98/DOS (with USB driver)
- USB-IF certification passed
- WHQL certification passed
- Variable resolution selection for multi-resolution sensor
- Built-in de-bounce circuits
- Built-in 3.3V regulator
- Built-in power-on reset
- Suspend function and wake-up feature to reduce power consumption
- Minimal external components
- 18-pin DIP package. ROHS compliant
- Supports mechanical and opto-mechanical axis Z scroll
- Supports dynamic acceleration up to X2.5
- Supports sensor rolling clockwise 90 degree
- Supports double-click and continuous-click
- USB only mode supported

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3. Block Diagram

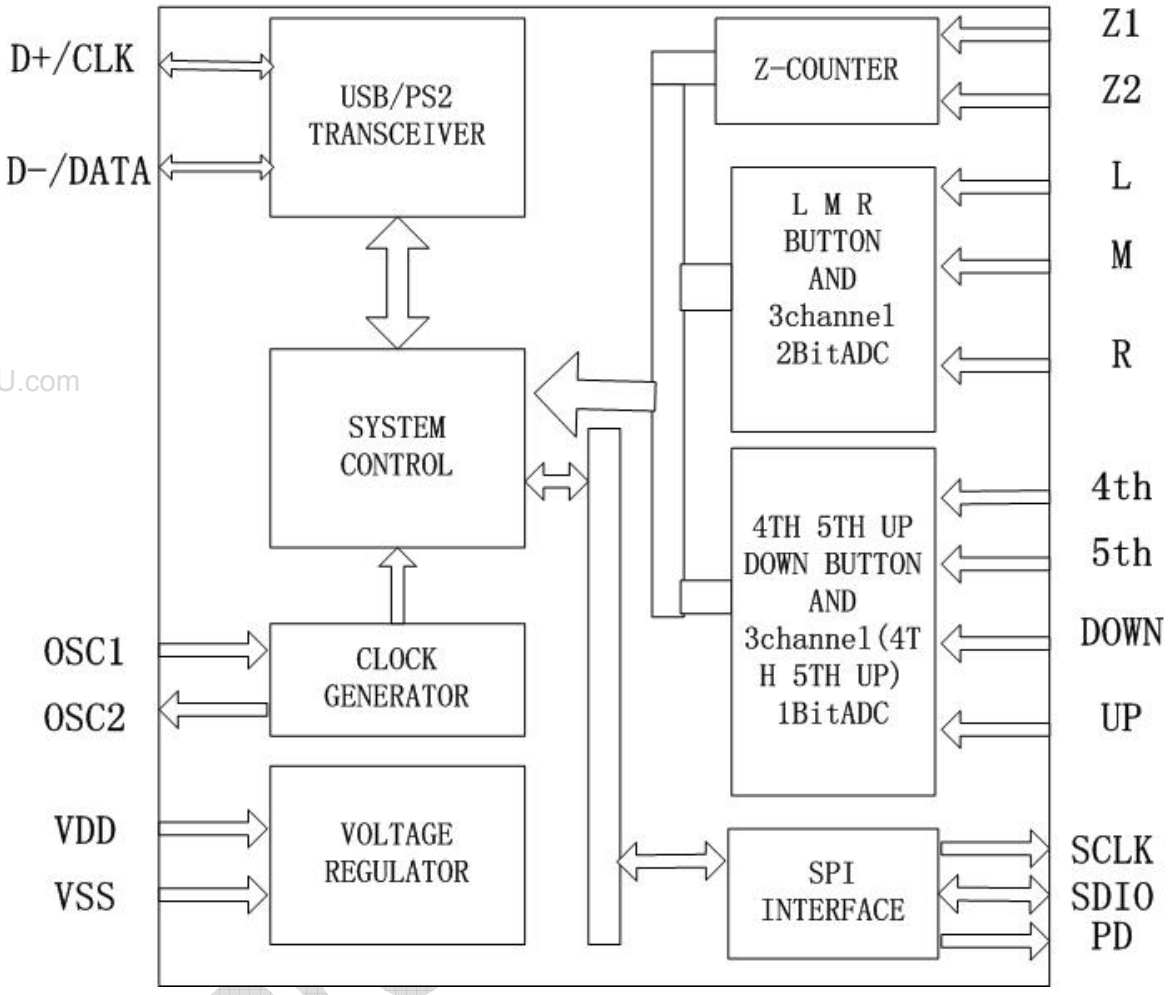

Figure 1: Block Diagram

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4. Pin Assignment

A2624 is 5-button 18-pin with UP/DOWN dynamic acceleration for 400 DPI sensor only.

A 2625 is 5-button 18-pin with UP/DOWN dynamic acceleration for all sensors.

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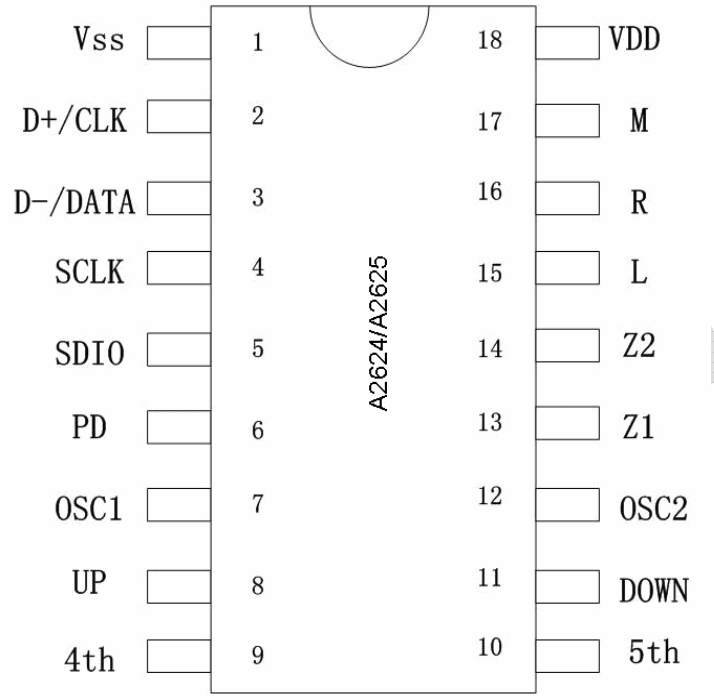

Figure 2: Pin Assignment (Top View)

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5. Pin description

Table 1 Pin description

Pin No.	Pin Name	I/O	Description
1	VSS	--	Ground
2	D+/CLK	I/O	USB data plus or PS2 Clock,
3	D–/DATA	I/O	USB data minus or PS2 Data,
4	SCLK	O	SPI Clock.
5	SDIO	I/O	SPI Data
6	PD	O	Power Down control for sensor
7	OSC1	I	External resistor for frequency fine tune(see table 9)
8	UP	I	Acceleration key Input and optional function select(see table 7)
9	4th Key	I	Forward Acceleration Button and optional function select (see table 5)
10	5th Key	I	Backward deceleration Button and optional function select (see table 6)
11	DOWN	I	deceleration key Input and optional function select(see table 8)
12	OSC2	O	Clock output for test
13	Z1	I	Z-Axis Input
14	Z2	I	Z-Axis Input
15	L	I	Left Button and optional function select (see table 2)
16	R	I	Right Button and optional function select (see table 3)
17	M	I	Middle Button and optional function select (see table 4)
18	VDD	--	5V power supply

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5.1 Strap pin setting on L, R, M

Table 2 L key setting

Pin	Setting	Voltage(V)	Function	
L	500KΩ pull-up	VDD	Z/2	rotate 0°
	2.1MΩ pull-down	5/8 VDD	Z/4	rotate 0°
	910kΩ pull-down	3/8 VDD	Z/2	rotate 90°
	280kΩ pull-down	1/8 VDD	Z/4	rotate 90°

Note: Z/2 means counter for wheel is divided by 2. Z/4 means counter for wheel is divided by 4. Rotate 0° means normal sensor bonding. Rotate 90°means sensor bonding with 90°clockwise rotation.

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Table 3 R key setting

Pin	Setting	Voltage(V)	Function	
R	500KΩ pull-up	VDD	U+P	No SS
	2.1MΩ pull-down	5/8 VDD	U+P	SS
	910kΩ pull-down	3/8 VDD	USB only	No SS
	280kΩ pull-down	1/8 VDD	USB only	SS

Note: U+P means USB and PS/2 mode can be supported. SS is spread-spectrum function for EMI reduction.

Table 4 M key setting

Pin	Setting	Voltage(V)	Dynamic-resolution
M	500KΩ pull-up	VDD	1:1
	2.1MΩ pull-down	5/8 VDD	1.5:1
	910kΩ pull-down	3/8 VDD	2:1
	280kΩ pull-down	1/8 VDD	2.5:1

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5.2 Strap pin setting on 4th Key, 5th Key

Table 5 4th key setting

Pin	Setting	Function
4th Key	OPEN	3-key mode
	50KΩ pull-down	5-key mode

Table 6 5th key setting

Pin	mode	Function
5th Key	3-key mode	double click
	5-key mode	Forward acceleration

5.3 Strap pin setting on UP, DOWN

Table 7 UP key setting

Pin	Setting	Function
UP	OPEN	Resistance control acceleration
	50KΩ pull-down	KEY control acceleration

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Table 8 DOWN key setting

Pin Name	Setting	Functions
DOWN	OPEN	Reserved
	50KΩ pull-down	Reserved

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5.4 5-Key function

The 5 -key function is implemented in the A2624/A2625.

A. when 5-key function is enabled, the 4th and 5th keys perform as normal keys.

B. when 5-key function is disabled

1. Option 1 ---- when the 5th key is pulled down by resistor

- A click on 4th key indicates double-clicking of left key.
- Hold Pressing down the 5th key indicates continuing-clicking of left key. Releasing the 5th key stops the clicking.

2. Option 2 ---- When the 5th key is floating

- A click on 4th key indicates double-clicking of left key
- A click on 5th key indicates continuing-clicking the left key. The second click indicates stopping continuing-clicking of left key.

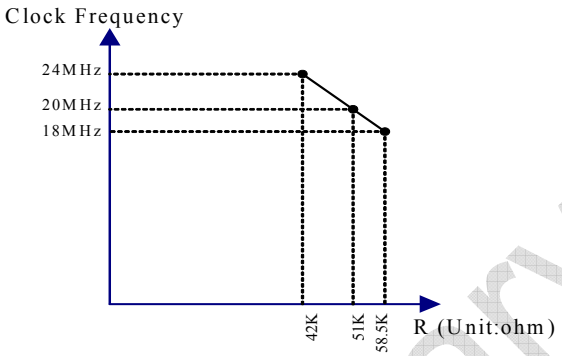
5.5 UP/DOWN function

UP key is used to increase the DPI resolution one level by one click. DOWN key is used to decrease DPI resolution one level by one click there are 4 level resolution modes (e.g x2.5, x2.0, x1.5 and x1.0). The default mode of UP/Down key is x1.0

5.6 Setting OSC frequency output

Table 9

Resistor R value	OSC2 frequency output
42KΩ	24MHz±1MHz
58.5KΩ	18MHz±0.7MHz



Typically R value VS. frequency

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5.7 SPI interface definition

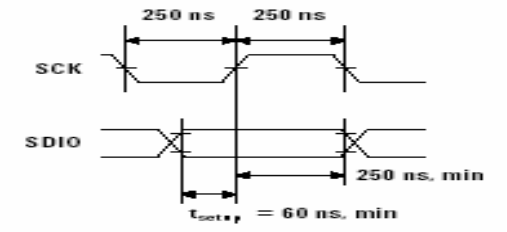
5.7.1 Signals definition

a. SCLK: The serial port clock. It is always generated by A2624/A2625.

b. SDIO: The data line. It is bi-directional signal.

c. PD: Power Down. It's usually used to place the sensor in a low power mode to meet USB suspend specification. It can also be used to force re-synchronization between A2624/A2625 and the sensor in case of an error. It also provides the sink current for the infrared diode for the axis Z.

5.7.2 SCLK timing definition



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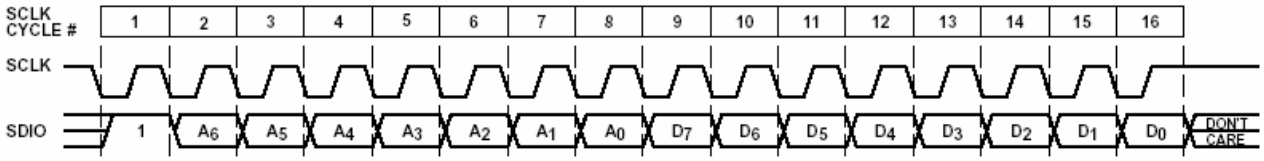
5.7.3 SPI Write operation

A2624/A2625 drives the SCLK to sensor. The address and data will be driven on SDIO at each negative edge of SCLK. The bit sequence is shown below.



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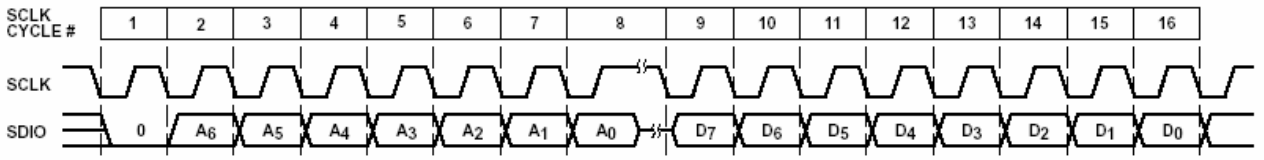
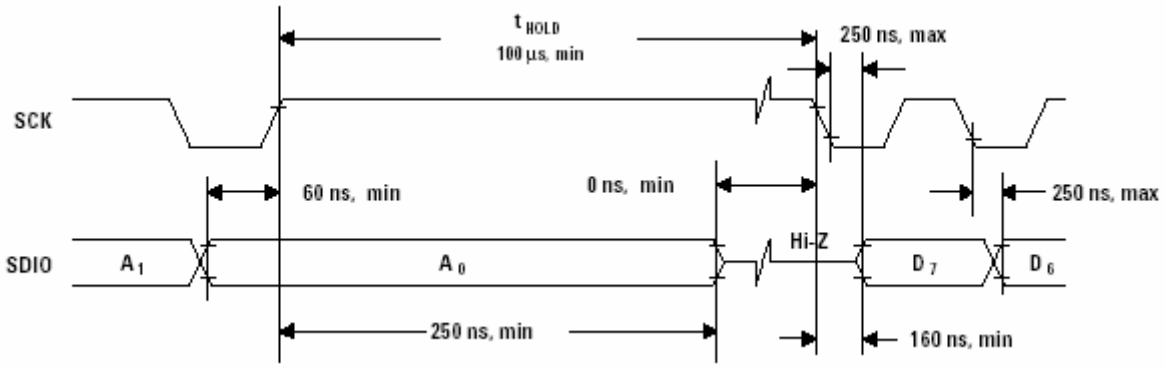
5.7.4 SPI Read operation

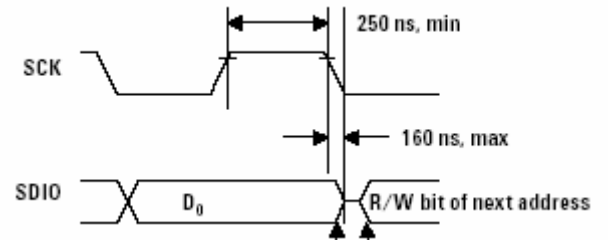
A2624/A2625 always drives the SCLK to sensor. The address will be driven out on SDIO at each negative edge of SCLK. After address transaction, the SDIO will be left hiZ until sensor drives the data on it at each negative edge of SCLK. A2624/A2625 captures the data at each negative edge of SCLK. The bit sequence is shown below.



There is data waiting time requirement for reading of A2624/A2625 between the last address bit and the first data bit the sensor drives. The timing diagram for sensor to prepare the data to be sent is shown below.



There is turning around time requirement between the last data bit the sensor sent and the command bit A2624/A2625 drives. A2624/A2625 will leave the SDIO hiZ at the falling edge of SCLK at least 160ns to avoid bus conflict.



5.7.5 SPI PD re-syncs

After power on or ESD event, the SPI bus will be in unknown state. The PD pulse can be used to re-sync the SPI bus.

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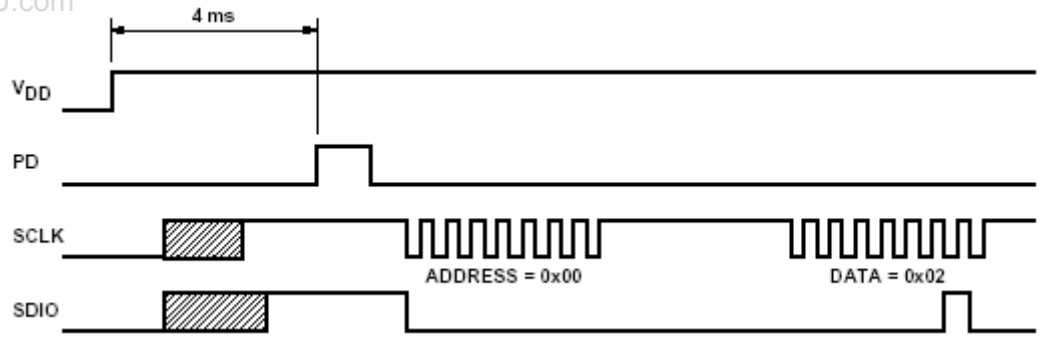
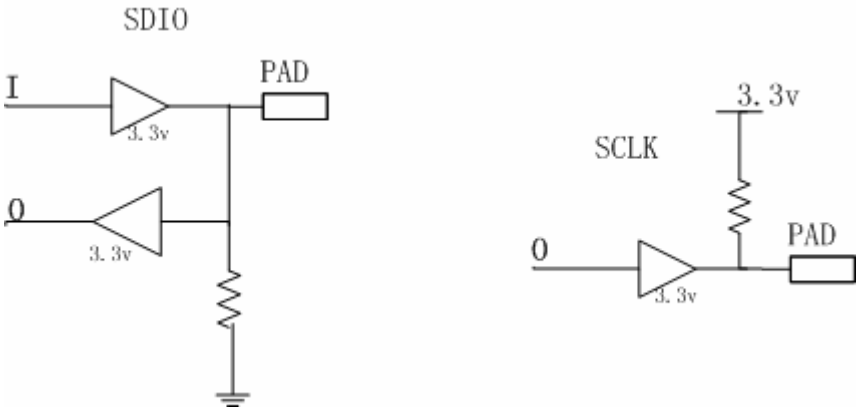


5.7.6 SPI I/O configuration



6. Absolute Maximum Ratings (Ta=25℃)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	VSS-0.5 ~ VDD+0.5 V	V
Operating Temperature	T_{OPR}	-15 ~ +55	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: These are stress ratings only. Stresses exceeding the range specified under Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

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7. Electrical Characteristics (Ta=25℃)

Symbol	Parameter	Test Conditions			Min	Type	Max	Unit
		VDD	Conditions					
VDD	Operating Voltage	--	--		4.5	--	5.5	V
IDD	Operating Current	5V	No load	USB mode	–	8.5	12	mA
				PS/2 mode	–	6.5	10	mA
I_{STB}	Standby Current	5V	No load, system suspend		75	90	95	uA
V_{IL1}	Input Low Voltage for I/O Ports	5V	–		0	–	1.0	V
V_{IH1}	Input High Voltage for I/O Ports	5V	–		3.5	–	5	V
V_{IH2}	Input High Voltage for USB I/O Ports	3.3V	--		2.8	--	3.6	V
V_{OH3}	Input High Voltage for SDIO SCLK out Ports	5V			3.0		3.6	V
V_{OL2}	Input Low Voltage for SDIO SCLK out Ports	5V			0		0.3	V
V_{IH3}	Input High Voltage for SDIO SCLK in Ports	5V			2.1		5	V
V_{IL2}	Input Low Voltage for SDIO SCLK in Ports	5V			0		0.9	V
V_{POR}	Power on Reset VDD Detection Voltage	5V	--		3.5	--	3.9	V
I_{OL1}	Output Port Sink Current (LED)	5V	V_{OL}=0.5V		--	20	--	mA

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8. Typical Application circuits

8.1 Application circuit 1

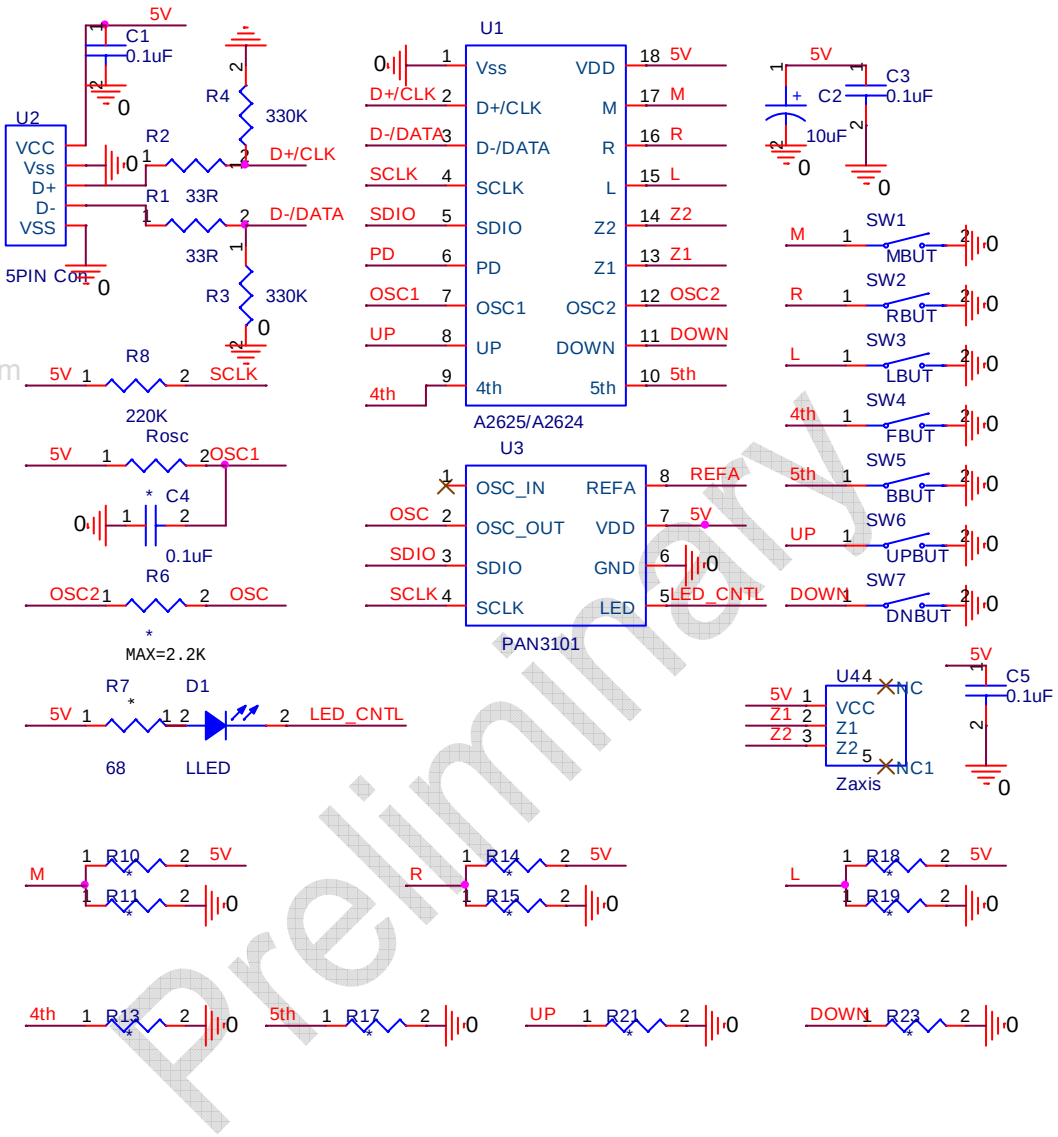

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Figure 3: Typical Application Circuit 1

8.2 Application circuit 2

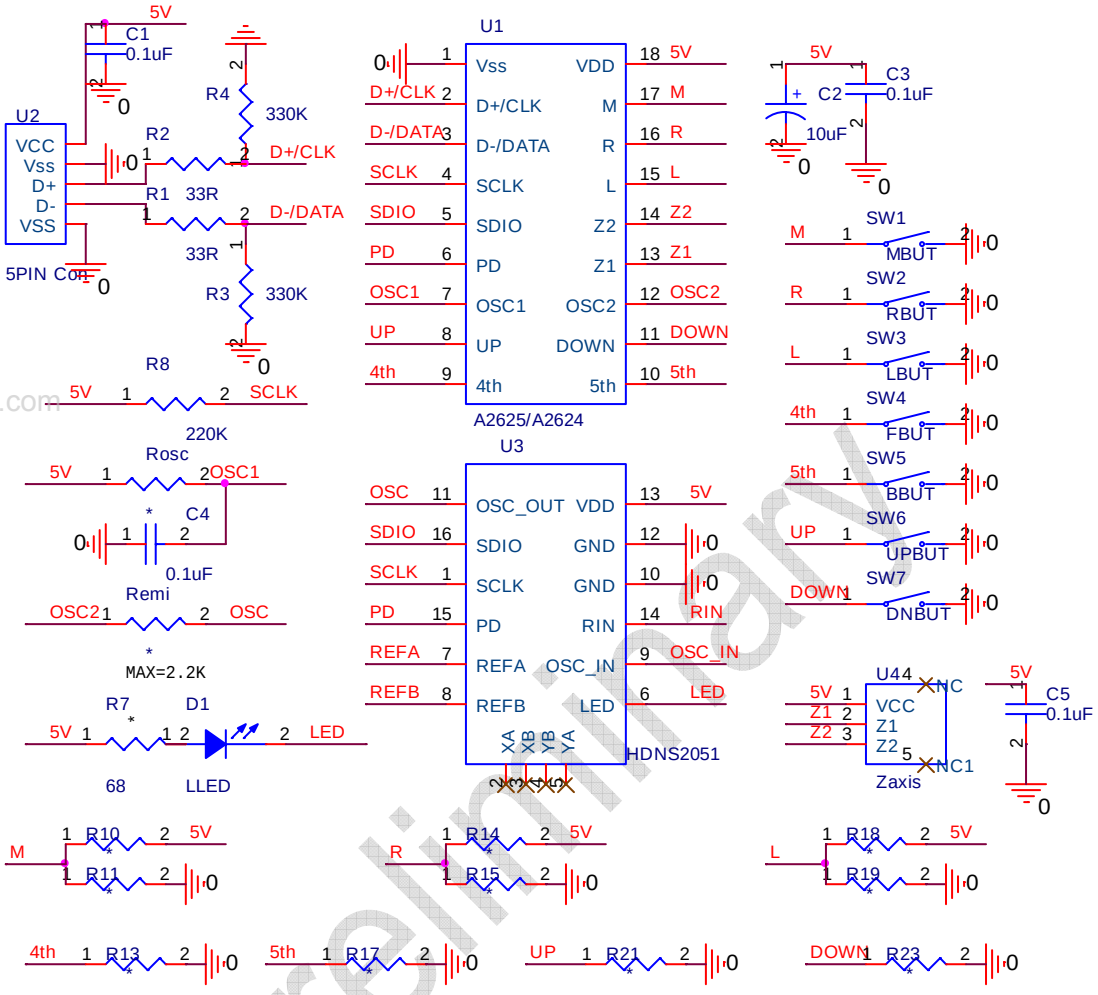

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Figure 4: Typical Application Circuit 2

8.3 Application circuit 3

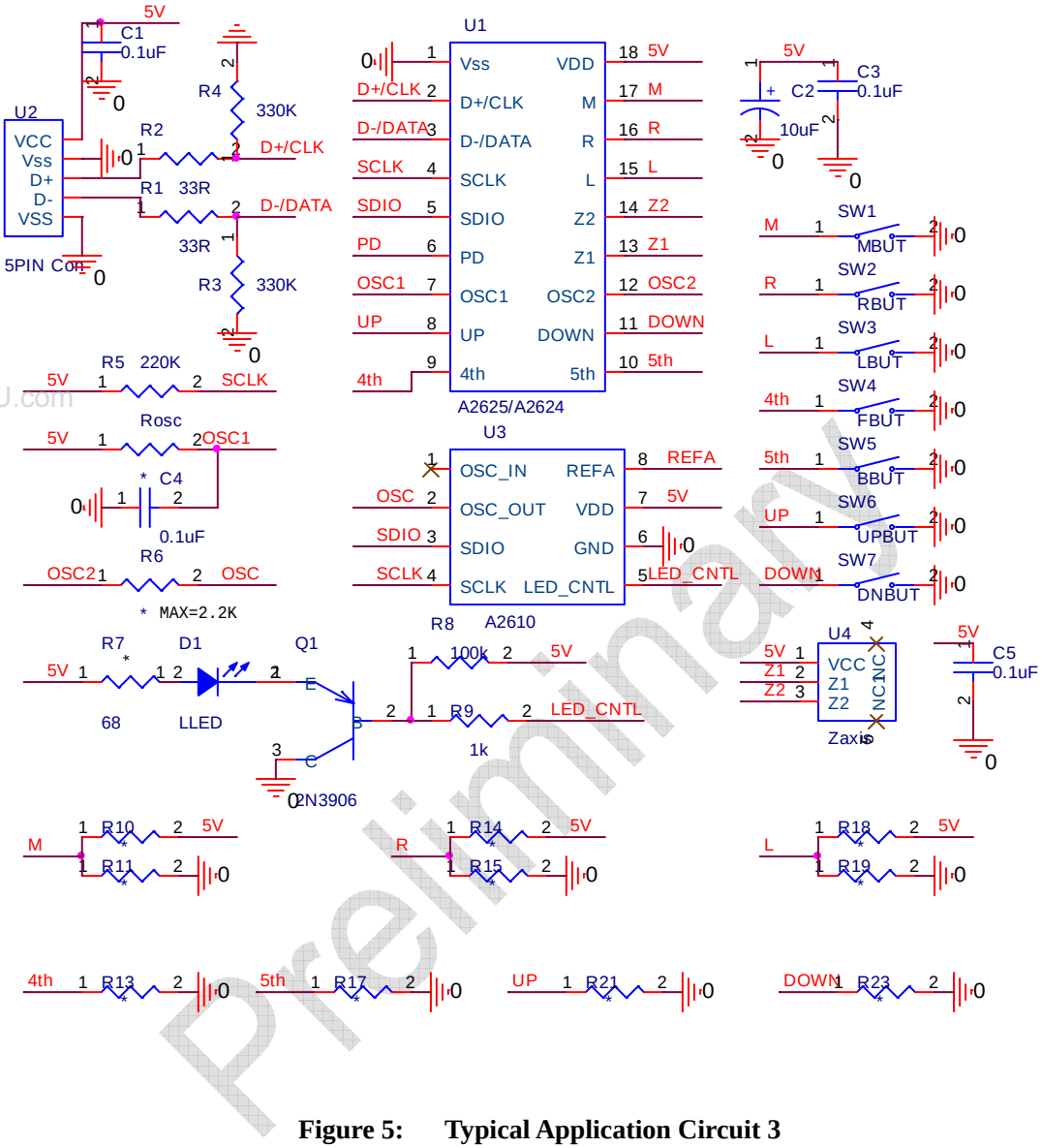

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Figure 5: Typical Application Circuit 3

9. Version History

Version name	Details
A2624/A2625_datasheet_V0.2	Preliminary version
A2624/A2625_datasheet_V0.3	Modifiable error in SCH page, page 12,13,14

10. Package Information

• DIP18

(Units : mm)

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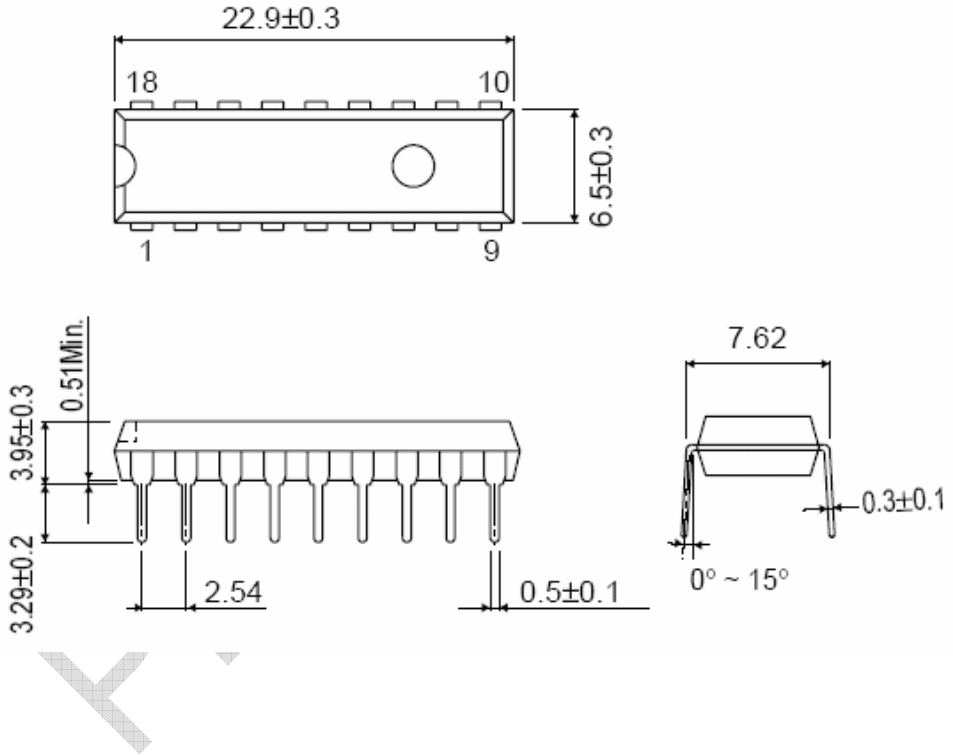

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