SD1010D

Digital-Interface XGA TFT LCD Display Controller

February 2000

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SD1010D DATA SHEET

DAT-SD1010-0200-C

February 2000

Document	Revisions	Date
DAT-SD1010-1099-A	SD1010 Data Sheet - A	October 1999
DAT-SD1010-1199-B	SD1010 Data Sheet - B	November 1999
DAT-SD1010-0200-C	SD1010 Data Sheet - C	February 2000

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igital-interface
gnals from a
onal CRT
monitor. This feature makes digital-interface LCD monitor a true replacement of a conventional CRT monitor.

The digital input RGB signals are first received by TMDS receiver, and the 24-bit RGB data are then fed into the SD1010D. The SD1010D is capable of performing automatic detection of the display resolution and timing of input signals generated from various PC graphic cards. No special driver is required for the timing detection, nor any manual adjustment. The SD1010D then automatically scales the input image to fill the full screen of the LCD monitor. The SD1010D can interface with TFT LCD panels from various manufacturers by generating either 24-bit or 48-bit RGB signal to the LCD panel based upon the timing parameters saved in the EEPROM.

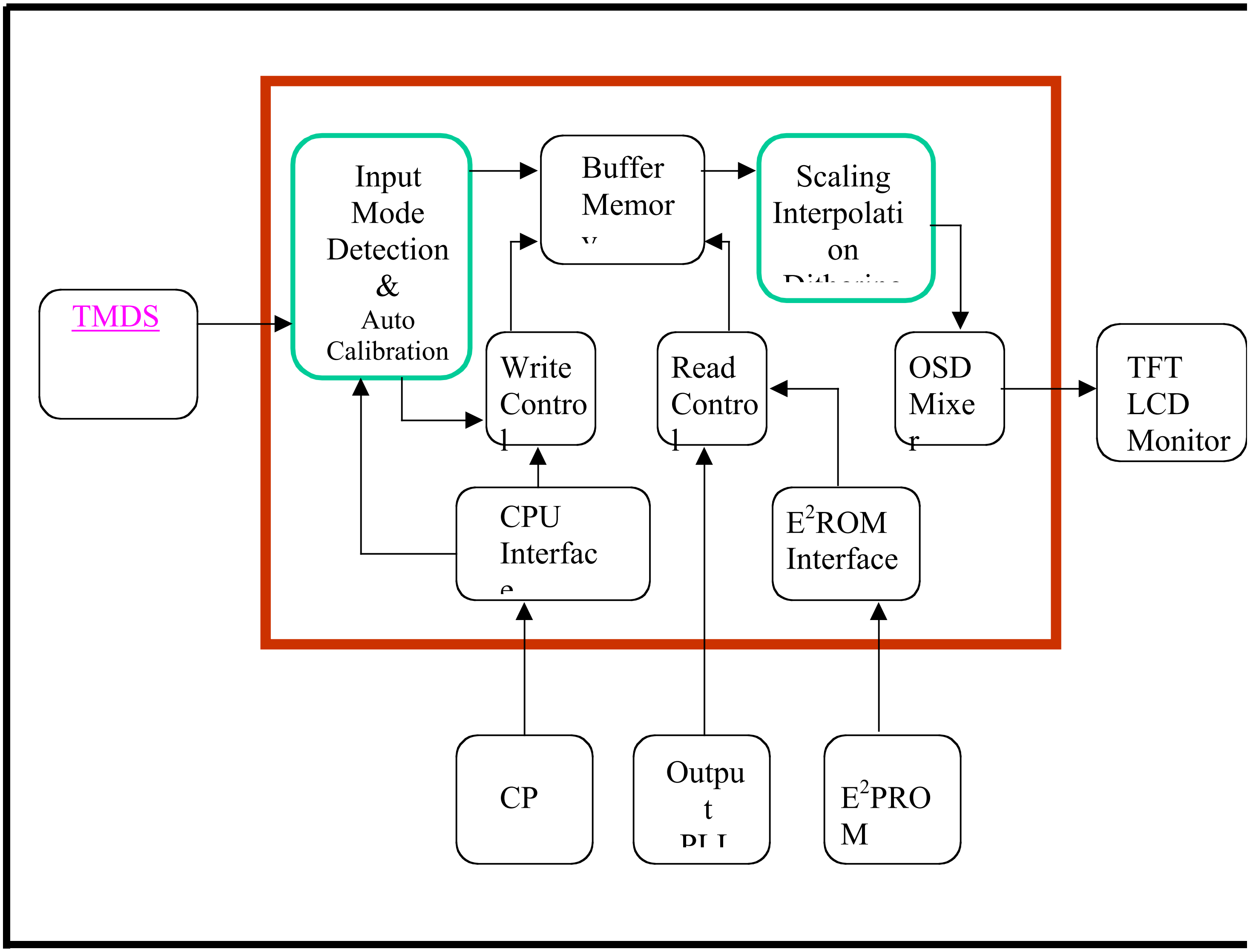
The SD1010D implements four advanced display technologies:
1. Advanced mode detection without any external CPU assist
2. Advanced programmable interpolation algorithm
3. Stand-alone mode support, and
4. Advanced true color support with both dithering and frame modulation.

The SD1010D also provides distinguished system features to the TFT LCD monitor solution. The first one is "plug-and-play", and the second one is "cost-effective system solution". To be truly plug-and-display, the SD1010D performs automatic input mode detection. Furthermore, the SD1010D can generate output video even when the input signal is beyond the specifications or no input signal is fed.

For "cost-effective system solution", the SD1010D implements many system support features such as OSD mixer, error status indicators, 2-wire serial interface for both EEPROM and host CPU interface, and low-cost IC package. Another important contributing factor is that the SD1010D does not require external frame buffer memory for the automatic image scaling and synchronization.

Figure 1 shows the block diagram of the SD1010D as well as the connections of important system components around the SD1010D.

Figure 1: SD1010D Functional Block Diagram



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PIN DESCRIPTION

Figure 2: SD1010D package diagram

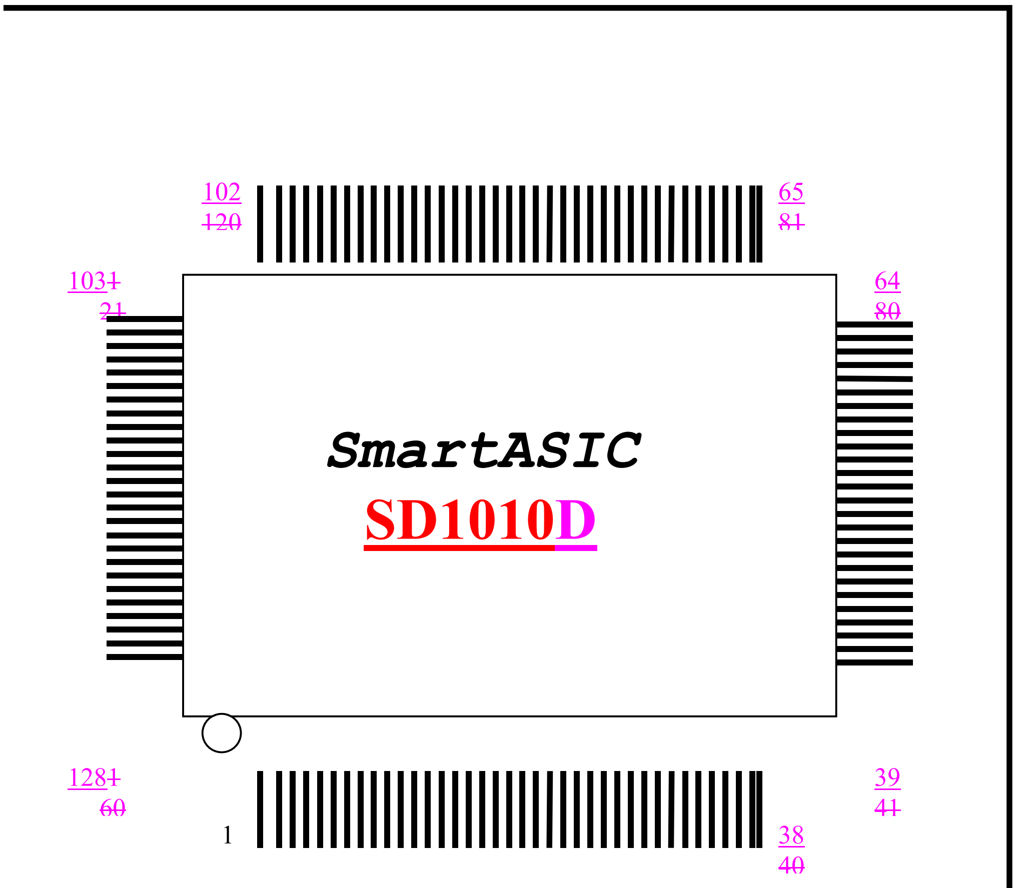

Table 1: SD1010 pin description (sorted by pin number)

Symbol	PIN Number	I/O	Description
ROM_SCL	1	O	SCL in I^2C for EEPROM interface
ROM_SDA	2	I/O	SDA in I^2C for EEPROM interface
GND	3		Ground
CPU_SCL	4	I	SCL in I^2C for CPU interface
CPU_SDA	5	I/O	SDA in I^2C for CPU interface
PWM_CTL	6	O	PWM control signal (not used)
CLK_1M	7	I	Free Running Clock (default: 1MHz)
VDD	8		Power Supply
CLK_1M_O	9	O	Feedback of free Running Clock
RESET_B	10	I	System Reset (active LOW)
R_OSD	11	I	OSD Color Red
G_OSD	12	I	OSD Color Green
B_OSD	13	I	OSD Color Blue
EN_OSD	14	I	OSD Mixer Enable =0, No OSD output =1,R_OUT[7:0]= {R_OSD repeat 8 times} G_OUT[7:0]= {G_OSD repeat 8 times } B_OUT[7:0]= {B_OSD repeat 8 times }
SCAN_EN	15	I	Manufacturing test pin (NC)
TEST_EN	16	I	Manufacturing test pin (NC)
FCLK0	17	O	Input PLL Feedback Clock (not used)
VCLK0	18	I	Input Clock 0 (not used)
FCLK1	19	O	Output PLL Feedback Clock
VCLK1	20	I	Output PLL Output Clock
HSYNC_O	21	O	Output HSYNC (the polarity is programmable through CPU, default is active low)
VSYNC_O	22	O	Output VSYNC (the polarity is programmable through CPU, default is active low)
DCLK_OUT	23	O	Output Clock to Control Panel (the polarity is programmable through CPU)
DE_OUT	24	O	Output Display Enable for Panel (the polarity is programmable through CPU, default is active HIGH)
GND	25		Ground
VDD	26		Power Supply
R_OUT0_E	27	O	Output Color Red Even Pixel (left pixel)
R_OUT1_E	28	O	Output Color Red Even Pixel (left pixel)
R_OUT2_E	29	O	Output Color Red Even Pixel (left pixel)
R_OUT3_E	30	O	Output Color Red Even Pixel (left pixel)
HSYNC_X	31	O	Default HSYNC generated by ASIC (active LOW)
R_OUT4_E	32	O	Output Color Red Even Pixel (left pixel)
R_OUT5_E	33	O	Output Color Red Even Pixel (left pixel)
R_OUT6_E	34	O	Output Color Red Even Pixel (left pixel)
R_OUT7_E	35	O	Output Color Red Even Pixel (left pixel)
GND	36		Ground
R_OUT0_O	37	O	Output Color Red Odd Pixel (right pixel)
R_OUT1_O	38	O	Output Color Red Odd Pixel (right pixel)
R_OUT2_O	39	O	Output Color Red Odd Pixel (right pixel)
R_OUT3_O	40	O	Output Color Red Odd Pixel (right pixel)
VDD	41		Power Supply
R_OUT4_O	42	O	Output Color Red Odd Pixel (right pixel)
R_OUT5_O	43	O	Output Color Red Odd Pixel (right pixel)
R_OUT6_O	44	O	Output Color Red Odd Pixel (right pixel)

R_OUT7_O	45	O	Output Color Red Odd Pixel (right pixel)
GND	46		Ground
G_OUT0_E	47	O	Output Color Green Even Pixel (left pixel)
G_OUT1_E	48	O	Output Color Green Even Pixel (left pixel)
G_OUT2_E	49	O	Output Color Green Even Pixel (left pixel)
G_OUT3_E	50	O	Output Color Green Even Pixel (left pixel)
G_OUT4_E	51	O	Output Color Green Even Pixel (left pixel)
VDD	52		Power Supply
G_OUT5_E	53	O	Output Color Green Even Pixel (left pixel)
G_OUT6_E	54	O	Output Color Green Even Pixel (left pixel)
G_OUT7_E	55	O	Output Color Green Even Pixel (left pixel)
GND	56		Ground
GND	57		Ground
G_OUT0_O	58	O	Output Color Green Odd Pixel (right pixel)
G_OUT1_O	59	O	Output Color Green Odd Pixel (right pixel)
G_OUT2_O	60	O	Output Color Green Odd Pixel (right pixel)
G_OUT3_O	61	O	Output Color Green Odd Pixel (right pixel)
VDD	62		Power Supply
G_OUT4_O	63	O	Output Color Green Odd Pixel (right pixel)
G_OUT5_O	64	O	Output Color Green Odd Pixel (right pixel)
G_OUT6_O	65	O	Output Color Green Odd Pixel (right pixel)
G_OUT7_O	66	O	Output Color Green Odd Pixel (right pixel)
GND	67		Ground
GND	68		Ground
B_OUT0_E	69	O	Output Color Blue Even Pixel (left pixel)
B_OUT1_E	70	O	Output Color Blue Even Pixel (left pixel)
B_OUT2_E	71	O	Output Color Blue Even Pixel (left pixel)
B_OUT3_E	72	O	Output Color Blue Even Pixel (left pixel)
B_OUT4_E	73	O	Output Color Blue Even Pixel (left pixel)
B_OUT5_E	74	O	Output Color Blue Even Pixel (left pixel)
B_OUT6_E	75	O	Output Color Blue Even Pixel (left pixel)
VDD	76		Power Supply
VDD	77		Power Supply
B_OUT7_E	78	O	Output Color Blue Even Pixel (left pixel)
GND	79		Ground
B_OUT0_O	80	O	Output Color Blue Odd Pixel (right pixel)
B_OUT1_O	81	O	Output Color Blue Odd Pixel (right pixel)
B_OUT2_O	82	O	Output Color Blue Odd Pixel (right pixel)
B_OUT3_O	83	O	Output Color Blue Odd Pixel (right pixel)
VDD	84		Power Supply
B_OUT4_O	85	O	Output Color Blue Odd Pixel (right pixel)
B_OUT5_O	86	O	Output Color Blue Odd Pixel (right pixel)
B_OUT6_O	87	O	Output Color Blue Odd Pixel (right pixel)
B_OUT7_O	88	O	Output Color Blue Odd Pixel (right pixel)
GND	89		Ground
R_IN00	90	I	Channel A Data Input Color Red (LSB)
R_IN01	91	I	Channel A Data Input Color Red
R_IN02	92	I	Channel A Data Input Color Red
R_IN03	93	I	Channel A Data Input Color Red
VDD	94		Power Supply
R_IN04	95	I	Channel A Data Input Color Red
R_IN05	96	I	Channel A Data Input Color Red
R_IN06	97	I	Channel A Data Input Color Red

R_IN07	98	I	Channel A Data Input Color Red (MSB)
GND	99		Ground
VDD	100		Power Supply
GND	101		Ground
G_IN00	102	I	Channel A Data Input Color Green (LSB)
G_IN01	103	I	Channel A Data Input Color Green
G_IN02	104	I	Channel A Data Input Color Green
G_IN03	105	I	Channel A Data Input Color Green
VDD	106		Power Supply
G_IN04	107	I	Channel A Data Input Color Green
G_IN05	108	I	Channel A Data Input Color Green
ADC_CLK0	109	O	Sample Clock for ADC 0 (not used)
G_IN06	110	I	Channel A Data Input Color Green
G_IN07	111	I	Channel A Data Input Color Green (MSB)
GND	112		Ground
VDD	113		Power Supply
GND	114		Ground
B_IN00	115	I	Channel A Data Input Color Blue (LSB)
B_IN01	116	I	Channel A Data Input Color Blue
B_IN02	117	I	Channel A Data Input Color Blue
VDD	118		Power Supply
B_IN03	119	I	Channel A Data Input Color Blue
B_IN04	120	I	Channel A Data Input Color Blue
B_IN05	121	I	Channel A Data Input Color Blue
B_IN06	122	I	Channel A Data Input Color Blue
B_IN07	123	I	Channel A Data Input Color Blue (MSB)
GND	124		Ground
HSYNC_I	125	I	Input HSYNC (any polarity)
VSYNC_I	126	I	Input VSYNC (any polarity)
DE_IN	127	I	DE input for digital interface
VDD	128		Power Supply

Table 2: SD1010 pin description (sorted by function)

Symbol	PIN Number	I/O	Description
R_IN00	90	I	Channel A Data Input Color Red (LSB)
R_IN01	91	I	Channel A Data Input Color Red
R_IN02	92	I	Channel A Data Input Color Red
R_IN03	93	I	Channel A Data Input Color Red
R_IN04	95	I	Channel A Data Input Color Red
R_IN05	96	I	Channel A Data Input Color Red
R_IN06	97	I	Channel A Data Input Color Red
R_IN07	98	I	Channel A Data Input Color Red (MSB)
G_IN00	102	I	Channel A Data Input Color Green (LSB)
G_IN01	103	I	Channel A Data Input Color Green
G_IN02	104	I	Channel A Data Input Color Green
G_IN03	105	I	Channel A Data Input Color Green
G_IN04	107	I	Channel A Data Input Color Green
G_IN05	108	I	Channel A Data Input Color Green
G_IN06	110	I	Channel A Data Input Color Green
G_IN07	111	I	Channel A Data Input Color Green (MSB)
B_IN00	115	I	Channel A Data Input Color Blue (LSB)
B_IN01	116	I	Channel A Data Input Color Blue
B_IN02	117	I	Channel A Data Input Color Blue
B_IN03	119	I	Channel A Data Input Color Blue
B_IN04	120	I	Channel A Data Input Color Blue
B_IN05	121	I	Channel A Data Input Color Blue
B_IN06	122	I	Channel A Data Input Color Blue
B_IN07	123	I	Channel A Data Input Color Blue (MSB)
HSYNC_I	125	I	Input HSYNC (any polarity)
VSYNC_I	126	I	Input VSYNC (any polarity)
DE_IN	127	I	DE input for digital interface
ADC_CLK0	109	O	Sample Clock for ADC 0 (not used)
R_OUT0_E	27	O	Output Color Red Even Pixel (left pixel)
R_OUT1_E	28	O	Output Color Red Even Pixel (left pixel)
R_OUT2_E	29	O	Output Color Red Even Pixel (left pixel)
R_OUT3_E	30	O	Output Color Red Even Pixel (left pixel)
R_OUT4_E	32	O	Output Color Red Even Pixel (left pixel)
R_OUT5_E	33	O	Output Color Red Even Pixel (left pixel)
R_OUT6_E	34	O	Output Color Red Even Pixel (left pixel)
R_OUT7_E	35	O	Output Color Red Even Pixel (left pixel)
R_OUT0_O	37	O	Output Color Red Odd Pixel (right pixel)
R_OUT1_O	38	O	Output Color Red Odd Pixel (right pixel)
R_OUT2_O	39	O	Output Color Red Odd Pixel (right pixel)
R_OUT3_O	40	O	Output Color Red Odd Pixel (right pixel)
R_OUT4_O	42	O	Output Color Red Odd Pixel (right pixel)
R_OUT5_O	43	O	Output Color Red Odd Pixel (right pixel)
R_OUT6_O	44	O	Output Color Red Odd Pixel (right pixel)
R_OUT7_O	45	O	Output Color Red Odd Pixel (right pixel)
G_OUT0_E	47	O	Output Color Green Even Pixel (left pixel)
G_OUT1_E	48	O	Output Color Green Even Pixel (left pixel)
G_OUT2_E	49	O	Output Color Green Even Pixel (left pixel)
G_OUT3_E	50	O	Output Color Green Even Pixel (left pixel)

G_OUT4_E	51	O	Output Color Green Even Pixel (left pixel)
G_OUT5_E	53	O	Output Color Green Even Pixel (left pixel)
G_OUT6_E	54	O	Output Color Green Even Pixel (left pixel)
G_OUT7_E	55	O	Output Color Green Even Pixel (left pixel)
G_OUT0_O	58	O	Output Color Green Odd Pixel (right pixel)
G_OUT1_O	59	O	Output Color Green Odd Pixel (right pixel)
G_OUT2_O	60	O	Output Color Green Odd Pixel (right pixel)
G_OUT3_O	61	O	Output Color Green Odd Pixel (right pixel)
G_OUT4_O	63	O	Output Color Green Odd Pixel (right pixel)
G_OUT5_O	64	O	Output Color Green Odd Pixel (right pixel)
G_OUT6_O	65	O	Output Color Green Odd Pixel (right pixel)
G_OUT7_O	66	O	Output Color Green Odd Pixel (right pixel)
B_OUT0_E	69	O	Output Color Blue Even Pixel (left pixel)
B_OUT1_E	70	O	Output Color Blue Even Pixel (left pixel)
B_OUT2_E	71	O	Output Color Blue Even Pixel (left pixel)
B_OUT3_E	72	O	Output Color Blue Even Pixel (left pixel)
B_OUT4_E	73	O	Output Color Blue Even Pixel (left pixel)
B_OUT5_E	74	O	Output Color Blue Even Pixel (left pixel)
B_OUT6_E	75	O	Output Color Blue Even Pixel (left pixel)
B_OUT7_E	78	O	Output Color Blue Even Pixel (left pixel)
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B_OUT1_O	81	O	Output Color Blue Odd Pixel (right pixel)
B_OUT2_O	82	O	Output Color Blue Odd Pixel (right pixel)
B_OUT3_O	83	O	Output Color Blue Odd Pixel (right pixel)
B_OUT4_O	85	O	Output Color Blue Odd Pixel (right pixel)
B_OUT5_O	86	O	Output Color Blue Odd Pixel (right pixel)
B_OUT6_O	87	O	Output Color Blue Odd Pixel (right pixel)
B_OUT7_O	88	O	Output Color Blue Odd Pixel (right pixel)
HSYNC_O	21	O	Output HSYNC (the polarity is programmable through CPU, default is active low)
VSYNC_O	22	O	Output VSYNC (the polarity is programmable through CPU, default is active low)
DCLK_OUT	23	O	Output Clock to Control Panel (the polarity is programmable through CPU)
DE_OUT	24	O	Output Display Enable for Panel (the polarity is programmable through CPU, default is active HIGH)
FCLK0	17	O	Input PLL Feedback Clock (not used)
VCLK0	18	I	Input Clock 0 (not used)
FCLK1	19	O	Output PLL Feedback Clock
VCLK1	20	I	Output PLL Output Clock
ROM_SCL	1	O	SCL in I^2C for EEPROM interface
ROM_SDA	2	I/O	SDA in I^2C for EEPROM interface
CPU_SCL	4	I	SCL in I^2C for CPU interface
CPU_SDA	5	I/O	SDA in I^2C for CPU interface
PWM_CTL	6	O	PWM control signal (not used)
CLK_1M	7	I	Free Running Clock (default: 1MHz)
CLK_1M_O	9	O	Feedback of free Running Clock

RESET_B	10	I	System Reset (active LOW)
HSYNC_X	31	O	Default HSYNC generated by ASIC (active LOW)
R_OSD	11	I	OSD Color Red
G_OSD	12	I	OSD Color Green
B_OSD	13	I	OSD Color Blue
EN_OSD	14	I	OSD Mixer Enable =0, No OSD output =1,R_OUT[7:0]= {R_OSD repeat 8 times} G_OUT[7:0]= {G_OSD repeat 8 times } B_OUT[7:0]= {B_OSD repeat 8 times }
SCAN_EN	15	I	Manufacturing test pin (NC)
TEST_EN	16	I	Manufacturing test pin (NC)
VDD	8		Power Supply
VDD	26		Power Supply
VDD	41		Power Supply
VDD	52		Power Supply
VDD	62		Power Supply
VDD	76		Power Supply
VDD	77		Power Supply
VDD	84		Power Supply
VDD	94		Power Supply
VDD	100		Power Supply
VDD	106		Power Supply
VDD	113		Power Supply
VDD	118		Power Supply
VDD	128		Power Supply
GND	3		Ground
GND	25		Ground
GND	36		Ground
GND	46		Ground
GND	56		Ground
GND	57		Ground
GND	67		Ground
GND	68		Ground
GND	79		Ground
GND	89		Ground
GND	99		Ground
GND	101		Ground
GND	112		Ground
GND	114		Ground
GND	124		Ground

FUNCTIONAL DESCRIPTION

The SD1010D has the following major function blocks:
1. Input mode detection
2. Buffer memory and read/write control block
3. Image scaling, interpolation and dithering block
4. OSD mixer and LCD interface block
5. EEPROM interface block
6. CPU interface block

The following sections will describe the functionality of these blocks.

Input mode detection

i) Supported input modes

SD1010D can handle up to 14 different input modes. For SD1010D, an input mode is defined by its horizontal resolution with its vertical resolution. The input modes with the same horizontal and vertical resolution but with different frame rates are still considered as one single input mode. In the default EEPROM setup, SD1010D accepts the following seven input video modes:

1. 640 x 350
2. 640 x 400
3. 720 x 400
4. 640 x 480 (VGA)
5. 800 x 600 (SVGA)
6. 832 x 624 (MAC)
7. 1024 x 768 (XGA)

Users can easily change the definitions of the acceptable input modes by adjusting the values in the appropriate EEPROM entries. There is no frame rate restriction on the input modes. However, since the output signal is synchronized with the input signal at the same refresh rate, the input refresh rate has to be within the acceptable range of the LCD panel.

The user-defined video modes can be defined by storing appropriate timing information in the EEPROM. Detail definitions of the EEPROM entries are described in Section 3.5.2.

ii) Input mode detection

The SD1010D can automatically detect the mode of the input signal without any user adjustment or driver running on the PC host or external CPU. This block automatically detects polarity of input synchronization and the sizes of back porch, valid data window and the synchronization pulse width in both vertical and horizontal directions. The size information is then used not only to decide the input resolution, to lock the PLL output clock with HSYNC, but also to automatically scale the image to full screen and to synchronize the output signal with the input signal.

The detection logic is always active to automatically detect any changes to the input mode. Users can manually change the input mode information at run time through the CPU interface. Detailed operation of the CPU interface is described in Section 3.6. "CPU Interface".

Mode detection can be independently turned ON or OFF by the external CPU. This feature allows system customers to have better control of the mode-detection process. When the detection is turned OFF, the external CPU can change the input mode.

iii) Free Running Clock

As described in previous section, a free-running clock is needed for the SD1010D. This clock is used for many of the SD1010D's internal operations. Eeprom operation is one of them. System manufacturers can select the frequency of the free-running clock, and the default clock frequency is 1MHz. System manufacturers can use an oscillator to generate the free-running clock, and feed that clock directly to the pin "CLK_1M", or use a crystal connecting to "CLK_1M" and "CLK_1M_O".

Buffer memory and read/write control block

The SD1010D uses internal buffer memory to store a portion of the input image for image scaling and output synchronization. No external memory buffer is needed for the SD1010D. The write control logic ensures the input data are stored into the right area of the buffer memory, and the read control logic is responsible to fetch the data from the buffer memory from the correct area and at the correct timing sequence. With the precise timing control of the write and read logic, the output image is appropriately scaled to the full screen, and the output signal is perfectly synchronized with the input signals.

Image scaling, interpolation and dithering block

The SD1010D supports both automatic image scaling and interpolation.

iv) Image scaling

The SD1010D supports several different input modes, and the input image may have different sizes. It is essential to support automatic image scaling so that the input image is always

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displayed to the full screen regardless the input mode. The SD1010D scales the images in both horizontal and vertical directions. It calculates the correct scaling ratio for both directions based upon the LCD panel resolution and the input mode and timing information produced by the "Input mode detection" block. The scaling ratio is re-adjusted whenever a different input mode is detected. The ratio is then fed to the buffer memory read control logic to fetch the image data with the right sequence and timing. Some of the image data may be read more than once to achieve the scaling effect.

v) Image interpolation

The SD1010D supports image interpolation to achieve better image quality. A basic image scaling algorithm replicates the input images to achieve the scaling effect. The replication scheme usually results in a poor image quality. The SD1010D implements a proprietary interpolation algorithm to improve the image quality. The programmable interpolation is implemented with a 256-entry mapping table in the EEPROM to allow system users to adjust the bi-linear interpolation parameters to control the sharpness and smoothness quality of the image. In the default setting, the mapping table contains a straight line of slope equal to 1, i.e. the data in entry N equal to the value N. If the mapping table contains a line of slope equal to 2, then the output image will be a bit sharper than the image generated by a table with the default setting. Through an external microcontroller, users can chose among different interpolation algorithm.

vi) Dithering

The SD1010D supports 16.7 million true colors for a 6-bit panel. Two dithering algorithms are implemented and users can chose between them through the external microcontroller. The first one is area-based dithering, and the second one is a frame-based frame modulation, which also is called frame rate control. Through the external microcontroller, users can choose among different dithering algorithms.

vii) Text Enhancement

In order to generate a good picture, the SD1010D incorporate a proprietary scheme to detect text and non-text picture. Then applying the appropriate process to improve the text image based on the detection of incoming source. By using the text enhancement function correctly, the text image will look more pleasant and near perfect after scaled up or down. Users can achieve a preferred image by changing the settings in "text control" register.

viii) Sharpness Enhancement

No matter how many times the original image got enlarged or shrunk by the internal interpolator. With the embedded powerful DSP arrays, SD1010D always can enhance the overall image sharpness (edge) to different degree for the various requirements. The sharpness can be adjusted bi-directionally which means either going sharper or softer to certain point set by the user. It's easy to activate the sharpness enhancement by program "sharpness control" register.

OSD mixer and LCD interface

At the output stage, the SD1010D performs the OSD mixer function, and then generates the 24-bit / 48-bit RGB signal to the LCD panel with the correct timing.

ix) OSD mixer

In the OSD mixer block, the SD1010D mixes the normal output RGB signal with the OSD signal. The OSD output data is generated based on the "R_OSD", "G_OSD" and "B_OSD" pins as well as the "OSD Intensity" data in EEPROM entry. When the "EN_OSD" is active high, the OSD is active, and the SD1010D will send the OSD data to the LCD panel. The OSD has 16 different color schemes based on the combinations of the three OSD color pins and the "OSD Intensity" data. When R_OSD=1, and OSD_Intensity=0, the SD1010D will output 128 to the output red channel, R_OUT. When R_OSD=1 and OSD_Intensity=1, the SD1010D will output 255. The same scheme is used for G_OSD to G_OUT and for B_OSD to B_OUT.

As part of the mixer control function, the SD1010D implements three mixing control registers, "OSD R Weight" (38H), "OSD G Weight"(39H), and "OSD B Weight" (3AH). The mixing equation is shown below:

$$R\_OUT = (R\_OSD) * (OSD\ R\ Weight/255) + R * (1 - OSD\ R\ Weight/255)$$
$$G\_OUT = (G\_OSD) * (OSD\ G\ Weight/255) + G * (1 - OSD\ G\ Weight/255)$$
$$B\_OUT = (B\_OSD) * (OSD\ B\ Weight/255) + B * (1 - OSD\ B\ Weight/255)$$

When the weight is 255, the OSD output will overlay on top of the normal output. When the weight is 0, the OSD output is disabled.

x) LCD interface

The SD1010D support both 24- and 48-bit RGB interfaces with XGA LCD panels from various panel manufacturers. The LCD panel resolution and timing information is stored in the external EEPROM. The information in the EEPROM includes timing related to the output back porch, synchronization pulse width and valid data window. The timing information is used to generate the frequency divider for the output PLL, to lock the PLL output clock with HSYNC for the LCD data clock, and to synchronize the output VSYNC and input VSYNC.

EEPROM interface

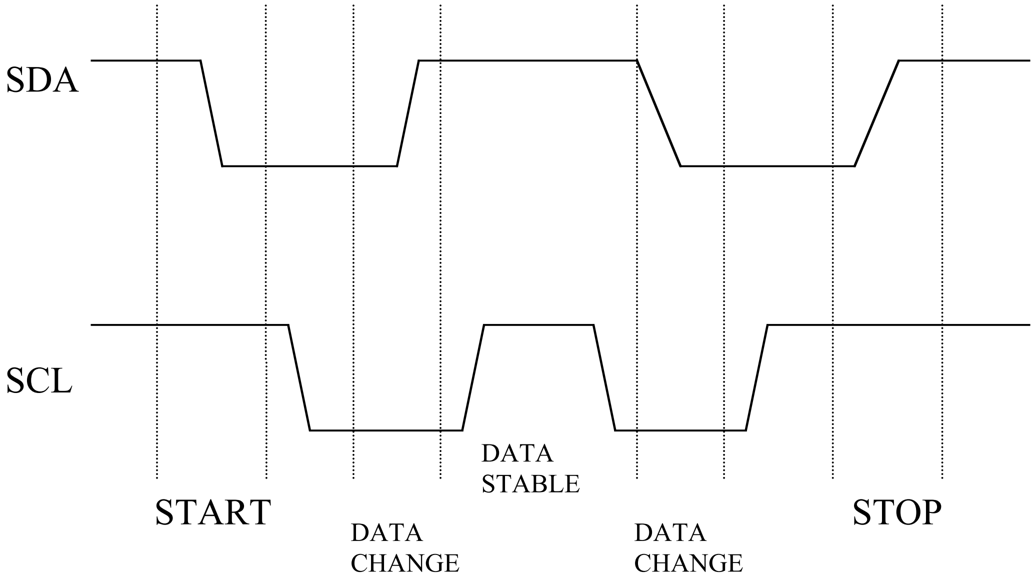
As mentioned in previous sections, the external EEPROM stores crucial information for the SD1010D internal operations. The SD1010D interfaces with the EEPROM through a 2-wire serial interface. The suggested EEPROM device is an industry standard serial-interface EEPROM (24x08). The 2-wire serial interface scheme is briefly described here and a detailed description can be found in public literature.

xi) 2-wire serial interface

The 2-wire serial interface uses 2 wires, SCL and SDA. The SCL is driven by the SD1010D and used mainly as the sampling clock. The SDA is a bi-directional signal and used mainly as a data signal. Figure 4 shows the basic bit definitions of the 2-wire serial interface.

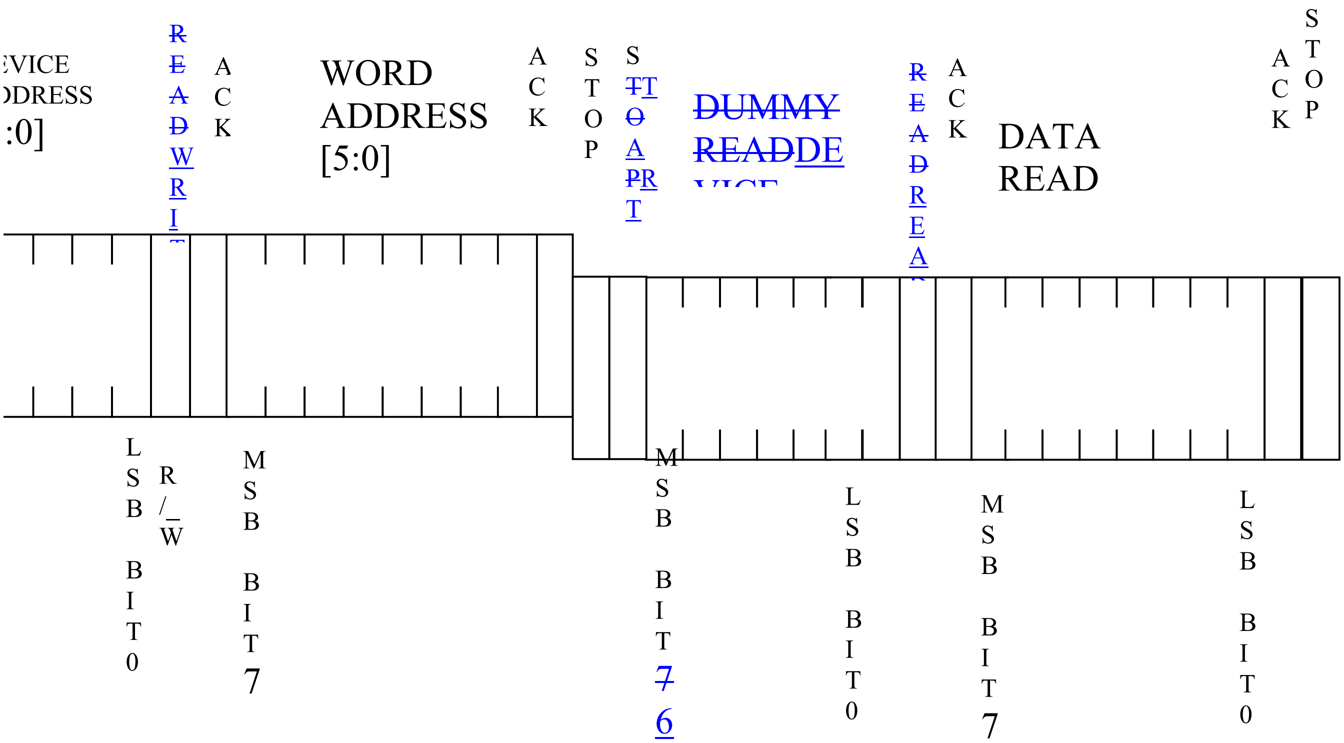
The 2-wire serial interface supports random and sequential read operations. Figures 5 and 6 show the data sequences for random read and sequential read operations.

Figure 4: START, STOP AND DATA Definitions in 2-wire serial interface



525 Race Street, Suite 250, San Jose, CA 95126, USA.
Main: (408) 283-5098 Fax: (408) 283-5099

Figure 5: Data sequence for read access (both single and multiple bytes)



525 Race Street, Suite 250, San Jose, CA 95126, USA.
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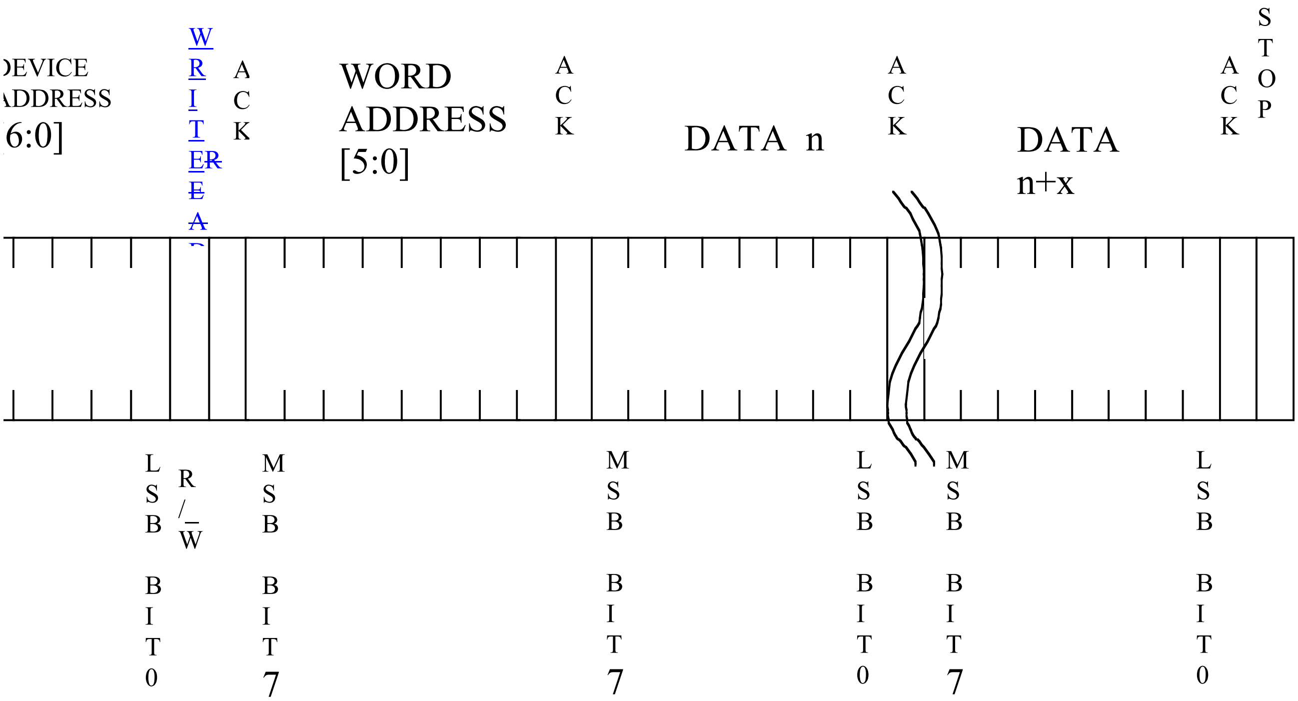
Figure 6: Data sequence for write access (both single and multiple bytes)



xii) EEPROM Contents

The contents of EEPROM are primarily dependent on the specifications of the LCD panel. SmartASIC provides suggested EEPROM contents for LCD panels from various panel manufacturers. The section presents all the entries in the EEPROM, and briefly describes their definitions. This allows the system manufacturers to have their own EEPROM contents to distinguish their monitors.

The EEPROM contents can be partitioned into 16 parts. The first 14 parts are input mode dependent. When the SD1010D detects the input mode, it will then load the information related to the detected mode from the EEPROM. The information in the 15th part is mainly for input mode detection as well as some threshold values for error status indicators. The 16th part is the look up table for the gamma correction function.
The 15th and 16th part are loaded in the SD1010D during the reset time.

In the default setting, the SD1010D is set to recognize the following seven modes: 640x350, 640x400, 720x400, 640x480, 800x600, 832x624, and 1024x768 modes. Then the EEPROM will be partitioned as follows:

- Part 1: mode 1: 640x350 mode (in default setting)
- Part 2: mode 2: 640x400 mode (in default setting)
- Part 3: mode 3: 720x400 mode (in default setting)
- Part 4: mode 4: 640x480 mode (in default setting)
- Part 5: mode 5: 800x600 mode (in default setting)
- Part 6: mode 6: 832x624 mode (in default setting)
- Part 7: mode 7: 1024x768 mode (in default setting)
- Part 8: mode 8
- Part 9: mode 9
- Part 10: mode 10
- Part 11: mode 11
- Part 12: mode 12
- Part 13: mode 13
- Part 14: mode 14
- Part 15: input mode detection and scaling related parameters
- Part 16: look up table for gamma correction

Part 1-14: Input Mode Dependent Data

Symbol	Width (bits)	Address For 640x350	Description
VPW	11	00H 01H	LCD VSYNC pulse width
VBP	11	02H 03H	LCD VSYNC back porch (including VPW)
VBP Source	11	04H 05H	LCD VSYNC back porch (source equivalent) = VBP * Line Expansion and round up
Target Skip Pixel	11	06H 07H	If VBP can not be converted into source evenly, the leftover is converted into number of pixels
VSIZE	11	08H 09H	LCD number of lines
HPW	11	0AH 0BH	LCD HSYNC pulse width
HBP	11	0CH 0DH	LCD HSYNC back porch (including HPW)
HSIZE	11	0EH 0FH	LCD number of columns
HTOTAL	11	10H 11H	LCD total number of pixels per line including all porches
HTOTAL Source	12	12H 13H	LCD total number of clocks per line (source equivalent) = HTOTAL/Line Expansion
Line Expansion	4	14H [6:3]	Vertical source-to-destination scaling factor 0: one-to-one expansion (no expansion) 1-15: expansion ratio other than one-to-one (expansion)
Pixel Expansion	3	14H [2:0]	Horizontal source-to-destination scaling factor 0: one-to-one expansion (no expansion) 1-7: expansion ratio other than one-to-one (expansion)
H. Fog Factor	8	15H[7:0]	Horizontal fogging factor high byte
H. Fog Factor	8	16H[7:0]	Horizontal fogging factor low byte
V. Fog Factor	8	17H[7:0]	Vertical fogging factor high byte
V. Fog Factor	8	18H[7:0]	Vertical fogging factor low byte
Minimum Input lines [10:8]	3	19H[6:4]	Upper 3 bits of minimum input lines
Maximum Input pixels [10:8]	3	19H[2:0]	Upper 3 bits of maximum input pixels
Minimum input lines [7:0]	8	1AH	Minimum input lines = (VSIZE + VBP)* Line Expansion When the input has fewer lines than this value, it is considered as an ERROR, and INPUT_X status bit will be HIGH.
Maximum input pixels [7:0]	8	1BH	Maximum input pixels per line. Auto clock recovery will not set input PLL divisor larger than this value.
Source HSIZE[10:8]	3	1CH [6:4]	Source horizontal size upper 3 bits
Source VSIZE[10:8]	3	1CH [2:0]	Source vertical size upper 3 bits
Source HSIZE[7:0]	8	1DH	Source horizontal size lower 8 bits

Source VSIZE[7:0]	8	1EH	Source vertical size lower 8 bits
Check sum	8	1FH	Sum of above 31 bytes (keep lower 8 bits only)

Mode	**Address Range**
640x400	20H 3FH
720x400	40H 5FH
640x480	60H 7FH
800x600	80H 9FH
832x624	A0H BFH
1024x768	C0H DFH
User define Mode 1	E0H FFH
User define Mode 2	100H 11FH
User define Mode 3	120H 13FH
User define Mode 4	140H 15FH
User define Mode 5	160H 17FH
User define Mode 6	180H 19FH
User define Mode 7	1A0H 1BFH

Part 15: Input Mode Detection Data

Symbol	Width (bits)	Address	Description
Control byte 0	8	200H	Bit 6 – bit 0 : device ID for external CPU access Bit 7: 0: load only 1 table for RGB gamma correction 1: load three separate tables for RGB gamma correction
Control byte 1	8	201H	Bit0: 0: disable automatic input gain control 1: enable automatic input gain control Bit1: 0: enable input H/V SYNC polarity control (make input SYNC positive polarity)

			1: bypass input H/V SYNC polarity control Bit2: 0: single pixel input 1: dual pixel input (set at 0) Bit3: 0: disable digital input 1: enable digital input (set at 1) Bit4: 0: YUV input format is unsigned (128 offset) 1: YUV input format is signed Bit5: 0: RGB input for video mode 1: YUV input for video mode Bit6: 0: disable video input 1: enable video input Bit7: 0: disable decimation support 1: enable decimation
Control byte 2	8	202H	Bit 0: 0: don't invert input odd/even field indicator 1: invert input odd/even field indicator Bit 1: 0: disable half clock mode for dual pixel input 1: enable half clock mode for dual pixel input (set at 0) Bit 2: 0: disable BY2 for auto calibration 1: enable BY 2 for auto calibration Bit 3: 0: disable BY4 for auto calibration 1: enable BY 4 for auto calibration Bit 4: 0: disable BY8 for auto calibration 1: enable BY 8 for auto calibration Bit7-5: output clock phase adjustment, larger number gives larger phase delay.
Reserved Entries	8	203H-220H	Set to all 0 or all 1 (not used)
Maximum VBP	8	221H	The maximum vertical back porch for input video
Mode0 vertical size	11	222H-223H	Mode0 vertical size for digital input
Mode1 vertical size	11	224H-225H	Mode1 vertical size for digital input
Mode2 vertical size	11	226H-227H	Mode2 vertical size for digital input
Mode3 vertical size	11	228H-229H	Mode3 vertical size for digital input
Mode4 vertical size	11	22AH-22BH	Mode4 vertical size for digital input
Mode5 vertical size	11	22CH-22DH	Mode5 vertical size for digital input
Mode6 vertical size	11	22EH-22FH	Mode6 vertical size for digital input
Mode7 vertical size	11	230H-231H	Mode7 vertical size for digital input
Mode8 vertical size	11	232H-233H	Mode8 vertical size for digital input
Mode9 vertical size	11	234H-235H	Mode9 vertical size for digital input
Mode10 vertical size	11	236H-237H	Mode10 vertical size for digital input
Mode11 vertical size	11	238H-239H	Mode11 vertical size for digital input
Mode12 vertical size	11	23AH-23BH	Mode12 vertical size for digital input
Mode0 horizontal size	11	23CH-23DH	Mode0 horizontal size upper bound for digital input
Mode1 horizontal size	11	23EH-23FH	Mode1 horizontal size upper bound for digital input
Mode2 horizontal size	11	240H-241H	Mode2 horizontal size upper bound for digital input
Mode3 horizontal size	11	242H-243H	Mode3 horizontal size upper bound for digital input
Mode4 horizontal size	11	244H-245H	Mode4 horizontal size upper bound for digital input
Mode5 horizontal size	11	246H-247H	Mode5 horizontal size upper bound for digital input
Mode6 horizontal size	11	248H-249H	Mode6 horizontal size upper bound for digital input
Mode7 horizontal size	11	24AH-24BH	Mode7 horizontal size upper bound for digital input
Mode8 horizontal size	11	24CH-24DH	Mode8 horizontal size upper bound for digital input
Mode9 horizontal size	11	24EH-24FH	Mode9 horizontal size upper bound for digital input
Mode10 horizontal size	11	250H-251H	Mode10 horizontal size upper bound for digital input
Mode11 horizontal size	11	252H-253H	Mode11 horizontal size upper bound for digital input
Mode12 horizontal size	11	254H-255H	Mode12 horizontal size upper bound for digital input
Reserved	8	256H	
Reserved	8	257H	

Reserved	8	258H	
Calibration mode	2	259H [1:0]	Selects different operation modes of internal phase calibration. The selection criterion is as follows: (This entry is not used) 0: when input video signal has large overshot, it results in longest calibration time 1: when input video signal has median overshot, it results in long calibration time 2: when input video signal has normal overshot, it results in normal calibration time (recommended) 3: when input video signal has no overshot, it results in shortest calibration time
PWM unit delay	16	25AH-25BH	The unit delay used in the external PWM delay circuitry. If the free-running clock is 1MHz, and the intended unit delay is 0.2 ns (= 5,000MHz), then a value of 5,000MHz/1MHz = 5,000 is used here. (This entry is not used)
Maximum link off time	22	25CH-25EH	Maximum time when input HSYNC is off before the LINK_DWN pin turns ON (unit: clock period of the free running clock). If the free-running clock is 1MHz, and the intended maximum time is 1 second, then a value of 1,000,000 µs/ 1 µs = 1,000,000 is used here.
Maximum refresh rate	16	25FH-260H	Maximum refresh rate supported by the LCD panel. If the intended maximum refresh rate is 75Hz, and the free-running clock is 1MHz, then a value of 1000000/75=133,333 is used here
Maximum input frequency	8	261H	Maximum source clock rate supported by the SD1010 (unit: frequency of free-running clock). If the intended maximum clock rate is 60MHz, and the free-running clock is 1MHz, then a value of 60 is used here. If the input signal has a higher frequency than this value, the VCLK0_X status bit will turn ON.
Minimum pixels per line for LCD	11	262H-263H	Minimum number of pixels per line for LCD panel
Switching options	1	264H[4]	Enable for switching to standalone hsync and vsync during no input conditions: Default is 1 1: cpu controls the switching 0: SD1010D controls the switching.
LCD polarity	4	264H[3:0]	Controls the polarity of output VSYNC, HSYNC, clock and display enable:Bit0: 0: clock active high, 1: clock active low Bit1: 0: HSYNC active low, 1: HSYNC active high Bit2: 0: VSYNC active low, 1: VSYNC active high Bit4: 0: de active high, 1: de active low
Output enable for output pin 51-54, 56-59, 61-64, 66-69, 71-74, 76-79, 81-84, 86-89, 91-97, 99, 101-104, 106-109	1	265H[3]	Enable for programmable output pad: 1: output is enabled 0: output is tri-state
Driving capability control for output pin 51-54, 56-59, 61-64, 66-69, 71-74, 76-79, 81-84, 86-89, 91-97, 99, 101-104, 106-109	3	265H[2:0]	0: 2mA 1: 6mA 2: 6mA 3: 10mA 4: 4mA 5: 8mA

			6: 8mA 7: 12mA
utput enable for output in 49 (DE)	1	266H[7]	Enable for programmable output pad: 1: output is enabled 0: output is tri-state
riving capability ontrol for output pin 49 DE)	3	266H[6:4]	0: 2mA 1: 6mA 2: 6mA 3: 10mA 4: 4mA 5: 8mA 6: 8mA 7: 12mA
utput enable for output in 46 (HSYNC_O)	1	266H[3]	Enable for programmable output pad: 1: output is enabled 0: output is tri-state
riving capability ontrol for output pin 46 HSYNC_O)	3	266H[2:0]	0: 2mA 1: 6mA 2: 6mA 3: 10mA 4: 4mA 5: 8mA 6: 8mA 7: 12mA
utput enable for output in 49 (VSYNC_O)	1	267H[7]	Enable for programmable output pad: 1: output is enabled 0: output is tri-state
riving capability ontrol for output pin 49 VSYNC_O)	3	267H[6:4]	0: 2mA 1: 6mA 2: 6mA 3: 10mA 4: 4mA 5: 8mA 6: 8mA 7: 12mA
utput enable for output in 46 (DCLK_OUT)	1	267H[3]	Enable for programmable output pad: 1: output is enabled 0: output is tri-state
riving capability ontrol for output pin 46 DCLK_OUT)	3	267H[2:0]	0: 2mA 1: 6mA 2: 6mA 3: 10mA 4: 4mA 5: 8mA 6: 8mA 7: 12mA
Extension right	4	268H[7:4]	Numbers of pixels extended right for support of non-full screen expansion for secondary resolution to avoid exceeding panel specification
Extension left	4	268H[3:0]	Numbers of pixels extended left for support of non-full screen expansion for secondary resolution to avoid exceeding panel specification
Extension down	2	269H[1:0]	Numbers of lines extended down for support of non-full screen expansion for secondary resolution to avoid exceeding panel specification
Check sum	8	26AH	Sum of all above bytes (keep only lower 8 bit)

Part 16: Gamma Correction Lookup Table

Symbol	Width (bits)	Address	Description
Mapped value	8	2C0H-3BFH	This is the lookup table for the gamma correction function If 200H[7] = 0, the mapped value is used for all RGB If 200H[7] = 1, the mapped value is used only for R
Check sum	8	3C0H	Sum of above 256 bytes (keep only lower 8 bit)
Mapped value	8	420H-51FH	This is the lookup table for the gamma correction function for green. This is needed only if 200H[7]=1
Check sum	8	520H	Sum of above 256 bytes (keep only lower 8 bits)
Mapped value	8	5A0H-69FH	This is the lookup table for the gamma correction function for blue. This is needed only if 200H[7] = 1
Check sum	8	6A0H	Sum of above 256 bytes (keep only lower 8 bits)

CPU interface

The SD1010D supports a 2-wire serial interface to an external CPU. The interface allows the external CPU to access and modify control registers inside the SD1010D. The 2-wire serial interface is similar to the EEPROM interface, and the CPU is the host that drives the SCL all the time as the clock and for “start” and “stop” bits. The SCL frequency can be as high as 5MHz. The SDA is a bi-directional data wire. This interface supports random and sequential write operations for the CPU to modify one or multiple control registers, and random and sequential read operations for the CPU to read all or part of the control registers.

The default device ID for the SD1010D is fixed “1111111”. The device ID can be programmed through EEPROM entry 200H bit 0 through bit 6. This avoids any conflict with other 2-wire serial devices on the same bus.

The following table briefly describes the SD1010D control registers. The external CPU can read these registers to know the state of the SD1010D as well as the result of input mode detection and phase calibration. The external CPU can modify these control registers to disable several SD1010D features and force the SD1010D into a particular state. When the CPU modifies the control registers, the new data will be first stored in a set of shadow registers, and then copied into the actual control registers when the “CPU Control Enable” bit is set. When the “CPU Control Enable” bit is set, the external CPU will retain control and the SD1010D will not perform the auto mode detection and auto calibration.

The external CPU is able to adjust the size of the output image and move the output image up and down by simply changing the porch size and pixel and line numbers of the input signal. These adjustments can be tied to the external user control button on the monitor.

A set of four control registers are used to generate output signal when there is no input signal available to the SD1010D or the input signal is beyond the acceptable ranges. This operation mode is called standalone mode, which is very important for the end users when they accidentally select an input mode beyond the acceptable range of the SD1010D or when the input cable connection becomes loose for any reason. System manufacturers can display appropriate OSD warning messages on the LCD panel to notify the users about the problem.

Table 3: SD1010 Control Registers

Symbol	Width	Mode	Address	Description
VBP Source	11	RW	0H-1H	Input VSYNC back porch (not include pulse width)
VSIZE Source	11	RW	2H-3H	Input image lines per frame
VTOTAL Source	11	RW	4H-5H	Input total number of lines including porches
HBP Source	11	RW	6H-7H	Input HSYNC back porch (not include pulse width)
HSIZE Source	11	RW	8H-9H	Input image pixels per line
HTOTAL Source	11	RW	AH-BH	Input total number of pixels per line including porches
Mode Source	4	RW	CH[3:0]	Input video format 0: 640x350 1: 640x400 2: 720x400 3: 640x480 4: 800x600 5: 832x624 6: 1024x768 7: user defined mode 1 8: user defined mode 2 9: user defined mode 3 10: user defined mode 4 11: user defined mode 5 12: user defined mode 6 13: user defined mode 7 14-15: error
Clock Phase Source	10	RW	DH-EH	Input sampling clock phase
VPW standalone	11	RW	FH-10H	For standalone mode, the pulse width of VSYNC
VTOTAL standalone	11	RW	11H-12H	For standalone mode, total number of line per frame
HPW standalone	11	RW	13H-14H	For standalone mode, HSYNC active time in µs
HTOTAL standalone	11	RW	15H-16H	For standalone mode, HSYNC cycle time in µs
Reserved Entries	8	RW	17H-26H	Can be set to all 0 or all 1 (not used)
Bypass Sync Polarity	1	RW	27H[7]	Bypass Input SYNC polarity detection (default 0): 1: bypass input SYNC polarity detection 0: detect input SYNC polarity and make them negative polarity
Dithering Enable	1	RW	28H[7]	Enable dithering for 6-bit panel (default 0): 1: enable dithering 0: disable dithering *also check register Control_C[6]
Frame Modulation Enable	1	RW	28H[6]	Enable frame modulation for 6-bit panel (default 0): 1: enable frame modulation 0: disable frame modulation *also check register Control_B[5] and Control_B[7]
Horizontal Interpolation Enable	1	RW	28H[5]	Enable horizontal interpolation (default 0): 1: enable horizontal interpolation 0: disable horizontal interpolation
Vertical Interpolation Enable	1	RW	28H[4]	Enable vertical interpolation (default 0): 1: enable vertical interpolation 0: disable vertical interpolation
Horizontal Rounding Enable	1	RW	28H[3]	Enable horizontal rounding (default 0): 1: enable horizontal rounding 0: disable horizontal rounding
Vertical Rounding Enable	1	RW	28H[2]	Enable vertical rounding (default 0): 1: enable vertical rounding 0: disable vertical rounding
Horizontal Table	1	RW	28H[1]	Enable horizontal Table Lookup (default 0):

Lookup Enable				1: enable horizontal Table Lookup 0: disable horizontal Table Lookup
Vertical Table Lookup Enable	1	RW	28H[0]	Enable vertical Table Lookup (default 0): 1: enable vertical Table Lookup 0: disable vertical Table Lookup
HSYNC Threshold Enable	1	RW	29H[4]	Enable detection of short lines (IBM panel only, default 0): 1: Enable such detection 0: disable such detection
OSD Intensity	1	RW	29H[3]	OSD intensity selection: 0: half intensity 1: full intensity
Load ALL EEPROM	1	RW	29H[2]	Should be kept low most of the time. A high pulse will force SD1010 to reload all EEPROM entries
Load Mode Dependent EEPROM	1	RW	29H[1]	Should be kept low most of the time. A high pulse will force SD1010 to reload mode dependent EEPROM entries
CPU control enable	1	RW	29H[0]	External CPU control enable: 0: disable external CPU control. SD1010 can write control registers, but CPU only read control registers. 1: enable external CPU control. CPU can read/write control registers. SD1010 cannot write control registers
Status 0	8	R	2AH	Read only internal status registers: 1: indicate error status 0: indicate normal status Bit 0: EEPROM gamma correction table loading Bit 1: EERPOM gamma correction table loading Bit 2: EEPROM mode dependent entries loading Bit 3: EEPROM calibration entries loading Bit 4: input has too few lines Bit 5: no input video Bit 6: input data clock is too fast Bit 7: refresh rate exceed LCD panel specification
Status 1	4	R	2BH[3:0]	Internal auto calibration state 0: Idle State 1-4: Loading EEPROM data 5-9: Frequency Calibration State (Auto Frequency Calibration will be done after state 9) 10: Phase Calibration State (Auto Phase Calibration will be done after state 10) 11: Adjust Horizontal Back Porch state 12: Phase Tracking state
Control_A	8	RW	2CH[7:0]	Control Register A: 0 – disable 1 – enable default is 00H Bit 0: Horizontal Interpolation Offset Enable Bit 1: Vertical Interpolation Offset Enable Bit 2: Horizontal Interpolation Fraction Reset Enable Bit 3: Vertical Interpolation Fraction Reset Enable Bit 4: Horizontal Interpolation Integer Increment Enable Bit 5: Vertical Interpolation Integer Increment Enable Bit 6: Single Pixel Output Mode Enable Bit 7: Disable “DE_OUT”, for blanking screen purpose
Control_B	8	RW	2DH[7:0]	Control Register B

				Bit [2:0]: Pixel Comparison Mode: 0: compare r even(default) 1: compare g even 2: compare b even 3: invalid 4: compare r odd 5: compare g odd 6: compare b odd 7: invalid *Using pixel comparison should program register "Pixel Comparison Value" and check register "Status 2[1:0]" Bit [4:3]: Brightness Control: 0: disable brightness control(default) 1: reduce brightness 2: increase brightness 3: invalid *Using brightness control should specify register "Brightness Adjustment" and check register "Status 2[2]" Bit [5]: Frame Modulation Mode: 0: 2-bit mode(default) 1: 1-bit mode Bit [6]: 6-bit Panel Rounding Enable: 0: disable(default) 1: enable Bit [7]: Frame Modulation Scheme Selection: 0: Scheme A(default) 1: Scheme B
Control_C	8	RW	2EH[7:0]	Control Register C Bit [1:0]: Horizontal Interpolation Special Processing Mode: 0: disable 1: linear 2: replication(default) 3: invalid Bit [3:2]: Vertical Interpolation Special Processing Mode: 0: disable 1: linear 2: replication(default) 3: invalid Bit [4]: OSD Transparency Enable: 0: disable(default) 1: enable *also need to program registers "OSD R Weight", "OSD G Weight" and "OSD B Weight" Bit [5]: Advanced Post Processing Enable: 0: disable(default) 1: enable

				*also need to specify registers "Advanced Processing R Weight", "Advanced Processing G Weight", "Advanced Processing B Weight" , "Advanced Processing R Value", "Advanced Processing G Value" and "Advanced Processing B Value" for properly functioning Bit [6]: Dithering Scheme Selection 0: Scheme A(default) 1: Scheme B Bit [7]: Reserved
Control_D	8	RW	2FH[7:0]	Control Register D Bit [3:0]: Advanced Processing Shift Amount. From 0 – 8. 8 is the default value. Bit [4]: Advance Mixing Shift Enable 0: disable(default) 1: enable *This is a option for Advanced Post Processing Bit [5]: OSD mode 0: Dual osd pixel mode 1: Single osd pixel mode Bit[6]: OSD pixel swaping enable 0: disable 1: enable (only valid in single osd pixel mode) Bit [7]: Reserved
Interpolation H. Offset	8	RW	30H[7:0]	High Byte For Interpolation Horizontal Offset Default is 00H
Interpolation H. Offset	8	RW	31H[7:0]	Low Byte For Interpolation Horizontal Offset Default is 00H
Interpolation V. Offset	8	RW	32H{7:0]	High Byte For Interpolation Vertical Offset Default is 00H
Interpolation V. Offset	8	RW	33H[7:0]	Low Byte For Interpolation Vertical Offset Default is 00H
H. Interpolation Rest Count	8	RW	34H[7:0]	Bit [2:0]: High Bits For Horizontal Interpolation Reset Count. Default is 0H. Bit [7:3]: Reserved
H. Interpolation Reset Count	8	RW	35H[7:0]	Low Byte For Horizontal Interpolation Reset Count. Default is 00H.
V. Interpolation Reset Count	8	RW	36H[7:0]	Bit [1:0]: High Bits For Vertical Interpolation Reset Count. Default is 0H.
V. Interpolation Reset Count	8	RW	37H[7:0]	Low Byte For Interpolation Vertical Reset Count. Default is 00H.
OSD R Weight	8	RW	38H[7:0]	Mixing Weight For OSD R. Default is 00H.
OSD G Weight	8	RW	39H[7:0]	Mixing Weight For OSD G. Default is 00H.
OSD B Weight	8	RW	3AH[7:0]	Mixing Weight For OSD B. Default is 00H.
Advanced Processing R Weight	8	RW	3BH[7:0]	Weight For Advanced Post Processing R default is 00H
Advanced Processing G Weight	8	RW	3CH[7:0]	Weight For Advanced Post Processing G Default is 00H
Advanced Processing B Weight	8	RW	3DH[7:0]	Weight For Advanced Post Processing B Default is 00H
Advanced Processing	8	RW	3EH[7:0]	Value For Advanced Post Processing R

R Value				Default is 00H
Advanced Processing G Value	8	RW	3FH[7:0]	Value For Advanced Post Processing G Default is 00H
Advanced Processing B Value	8	RW	40H[7:0]	Value For Advanced Post Processing B Default is 00H
Brightness Adjustment	8	RW	41H[7:0]	The Adjust Amount For Reducing/Increasing Brightness. Default is 00H.
Pixel Comparison Value	8	RW	42H[7:0]	The Value To Compare The Incoming Pixel Data. Default is 00H.
Status 2	8	R	43H[7:0]	The Status Register 2 Bit [1:0]: Result for comparing the selected incoming pixel with "Pixel Comparison Value": 0: invalid 1: incoming pixel > "Pixel Comparison Value" 2: incoming pixel = "Pixel Comparison Value" 3: incoming pixel < "Pixel Comparison Value" Bit [2]: Status for brightness control 0: Normal, no underflow/overflow 1: brightness reduced too much causes underflow/increased too much causes overflow Bit [7:3]: Reserved
Recovery Control	8	RW	44H	Clock Recovery Control Register: Default value is 71H Bit 0: clock frequency is divisible by 2 Bit 1: clock frequency is divisible by 4 Bit 2: clock frequency is divisible by 8 Bit 3: enable phase tracking feature Bit 4: enable auto phase calibration Bit 5: enable auto frequency calibration Bit 6: enable auto mode detection Bit 7: enable operation at half clock speed (not used)
Phase Range	4	RW	45H	Offset value added to the calibrated phase when phase tracking occurs
Phase Track Waiting Time	24	RW	46H 48H	Number of frames waited before phase tracking occurs
Quick Phase Enable	1	RW	49H[0]	0: Normal phase calibration (default) 1: Final phase = phase total – phase offset
PWM Enable	1	RW	49H[1]	0: Disable auto phase total calculation 1: Enable auto phase total calculation (default)
Standalone Enable	1	RW	49H[2]	0: Uses the external incoming SYNC signals (default) 1: Allow the use of the default SYNC signals instead of the incoming SYNC signals
Digital Enable	1	RW	49H[3]	0: Analog interface 1: Digital interface (no auto calibration) should be set at 1
Phase Offset	10	RW	4AH 4BH	Offset value subtracted from phase total when doing quick phase calculation
Phase Total	10	RW	4CH 4DH	User defined value for a particular frequency
Man_hsize_valid	1	R	4EH[4]	Indicates when hsize value is ready for cpu to read in man_freq_state. Read only
Man_iq_valid	1	R	4EH[3]	Indicates when image quality is ready for cpu to read in man_phase_state. Read only

Auto_iq_valid	1	R	4EH[2]	Indicates when image quality is ready for cpu to read in auto calibrate mode. Read only
Divisor_valid	1	R	4EH[1]	Indicates when auto clock frequency calibration is done and frequency value is ready for cpu to read. Read only
Non_full_screen	1	R	4EH[0]	Indicates when input data is non full screen. Read only
Href_reg	8	R	4FH	This reg reports the period of hsync by counting the number of free clock cycle in one single hsync period.
Vref_reg	16	R	50H-51H	This reg reports the period of vsync by counting the number of free clock cycle in one single vsync period.
Text Control	8	RW	52H[7:0]	Text-Enhancement Control Bit[0]: text enhancement enable 0: disable 1: enable Bit[1]: Reserved Bit[6:2]: text-enhanced level Level 0 – 14. Level "0" is the same as original source, and "14" is the highest enhancement level. Bit[7]: Reserved Default is 00H
Sharpness Control	8	RW	53H[7:0]	Sharpness-Enhancement Control Bit[0]: sharpness enhancement enable 0: disable 1: enable Bit[1]: Reserved Bit[6:2]: sharpness-enhanced level Level 1 – 19. Level "5" is the same as the original source. From "4" to "1" intend to soften the picture, and "1" is the softest level. From level "6" to "19" will sharpen the picture gradually. Level "19" is the sharpest output. Bit[7]: Reserved Default is 14H
Control_E	8	RW	54H[7:0]	Control Register E Bit[3:0]: text enhancement threshold. Bit[4]: reserved Bit[6:5]: Frame Modulation Mode 0: compatible with SD1010 1-3: new schemes Bit[7]: reserved Default is 05H
Pixel_h	11	RW	55H[10:8] 56H[7:0]	The x location for reading "Pixel_out" register
Pixel_v	11	RW	57H[10:8]	The y location for reading "Pixel_out" register

			58H[7:0]	
Pixle_out	24	R	59H, 5AH, 5BH	Read out pixel located by “Pixel_h” and “Pixel_v”
Vbp_asic_update_en	1	RW	5CH[6]	Enables SD1010D to update its internal vbp value. Default is high
Sel_ext_sync	1	RW	5CH[5]	Select external hsync and vsync.
Fc3_start	1	RW	5CH[4]	Forces auto calibration to recalculate h back porch Set at 0 (not used)
Channel_select	1	RW	5CH[3]	Only for single pixel input 0: takes input data from channel 1 1: takes input data from channel 0 For 128 pin package set this bit at 0
Dual_pixel	1	RW	5CH[2]	0: takes input data from one single channel 1: takes input data from both channels For 128 pin package set this bit at 0
Soft_start	1	RW	5CH[1]	Software reset SD1010D
Man_phase_state	1	RW	5CH[0]	Forces auto calibration to calculate the image quality for a particular clock phase (not used for sd1010d)
Hsize_by842_en	1	RW	5DH[7]	Turn on internal hsize matching by8, 4, 2 when clock frequency calibration is done by8, 4, 2. Used mainly for special non-full screen inputs. (not used)
Video_mode	1	RW	5DH[6]	0: disable input video mode 1: input is video
Input_yuv	1	RW	5DH[5]	0: input video format is RGB 1: input video format is YUV 4:2:2
Yuv_signed	1	RW	5DH[4]	0: input video YUV format is unsigned 1: input video YUV format is signed
decimation	1	RW	5DH[3]	Used when input resolution is higher than output 1: enable special decimation control 0: disable special decimation
Detect_en	2	RW	5DH[2:1]	Input data range detection. The results are put in register 64H and 65H 0: disable detection 1: detect MAX/MIN using R color 2: detect MAX/MIN using G color 3: detect MAX/MIN using B color
Agc_en	1	RW	5DH[0]	Automatic gain control enable
Agc_gain_red	8	RW	5EH	Gain amount for R color
Agc_gain_green	8	RW	5FH	Gain amount for G color
Agc_gain_blue	8	RW	60H	Gain amount for B color
Agc_offset_red	8	RW	61H	Offset amount for R color
Agc_offset_green	8	RW	62H	Offset amount for G color
Agc_offset_blue	8	RW	63H	Offset amount for B color
Input_max	8	R	64H	Detected maximum input data (please see 5DH)
Input_min	8	R	65H	Detected minimum input data (please see 5DH)
Man_freq_state	1	RW	66H[5]	Forces auto calibration to calculate the hsize value for a particular clock frequency (not used for sd1010d)
Clear_man_hsize_ valid	1	RW	66H[4]	Reset Man_hsize_valid register. (not used)
Clear_man_iq_valid	1	RW	66H[3]	Reset Man_iq_valid register. (not used)
Clear_iq_valid	1	RW	66H[2]	Reset IQ_valid register. (not used)
Clear_divisor_valid	1	RW	66H[1]	Reset Divisor_valid register (not used)
Clear_nonfullscreen	1	RW	66H[0]	Reset Non_full_screen register.
Divisor_value	11	R	67H[2:0], 68H	Read only register containing value of clock frequency when divisor_valid is asserted
IQ_value	30	R	69H[5:0],	Read only register containing value of image quality

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			6AH,6BH, 6CH	when either man_iq_valid or iq_valid is asserted
Panel_on	1	RW	6DH[0]	1: turn on all the outputs to the panel 0: disable outputs to the panel (need to disable EEPROM 265H[3], 266H[7], 266H[3], 267H[7], 267H[3] to get complete output disable).
Man_hsize_value	11	R	6EH[2:0], 6FH	Read only register containing value of hsize when man_hsize_valid is asserted. (not used in sd1010d)
Shift_hbp_digital	1	RW	70H[7]	Move picture in left-right direction in digital mode
Forward	1	RW	70H[6]	1: move picture to left 0: move picture to right Used mainly to compensate in the unlikely event when data and de are unalign coming into the SD1010D
Rom_clk_sel	6	RW	70H[5:0]	Divisor value use to divide fast pwm_free_clk to slower free_clk
Control_F	8	RW	71H	Control Register F Bit[2:0]: Dithering Mode 0: compatible with SD1000 1-5: new schemes Bit[6:3]: reserved Bit[7]: gamma enable Default is 00H
Data high threshold	8	RW	72H	High water mark for valid data. If the data is larger than this threshold, it is considered High internally
Data low threshold	8	RW	73H	Low water mark for valid data. If the data is smaller than this threshold, it is considered LOW internally
Edge threshold	8	RW	74H	Minimum difference between the data value of two adjacent pixels to be considered as an edge.

Control Flow

When SD1010D is powered up, the reference system and SD1010D will perform the following functions in sequence:

1. System will generate a Power-On Reset to SD1010D.

2. Once the SD1010D receives the Reset, SD1010D will load the contents of EEPROM and start the auto-detection process.

3. In the meantime, the external CPU can change the contents of the control registers of the SD1010D. If necessary, the external CPU can send an additional Reset to restart the whole process.

ELECTRICAL SPECIFICATIONS

This section presents the electrical specifications of the SD1010D.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VCC	Power Supply	-0.3 to 3.6	V
Vin	Input Voltage	-0.3 to VCC + 0.3	V
Vout	Output Voltage	-0.3 to VCC +0.3	V
VCC5	Power Supply for 5V	-0.3 to 6.0	V
Vin5	Input Voltage for 5V	-0.3 to VCC5 + 0.3	V
Vout5	Output Voltage for 5V	-0.3 to VCC5 +0.3	V
TSTG	Storage Temperature	-55 to 150	°C

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VCC	Power Supply	3.0	3.3	3.6	V
Vin	Input Voltage	0		VCC	V
VCC5	Commercial Power Supply for 5V	4.75	5.0	5.25	V
VIN5	Input Voltage for 5V	0	-	VCC5	V
TJ	Commercial Junction Operating Temperature	0	25	115	°C

General DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
IIL	Input Leakage Current	no pull – up or pull - down	-1		1	µA
IOZ	TRI-state Leakage Current		-1		1	µA
CIN3	3.3V Input Capacitance			2.8		ρF
COUT3	3.3V Output Capacitance		2.7		4.9	ρF
CBID3	3.3V Bi-directional Buffer Capacitance		2.7		4.9	ρF
CIN5	5V Input Capacitance			2.8		ρF
COUT5	5V Output Capacitance		2.7		5.6	ρF
CBID5	5V Bi-directional Buffer Capacitance		2.7		5.6	ρF

Note: *The capacitance above does not include PAD capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance, which is about 0.5 ρF, and the package capacitance*

DC Electrical Characteristics for 3.3 V Operation

(Under Recommended Operation Conditions and V_{CC} = 3.0 ~ 3.6V, T_J = 0°C to +115°C)

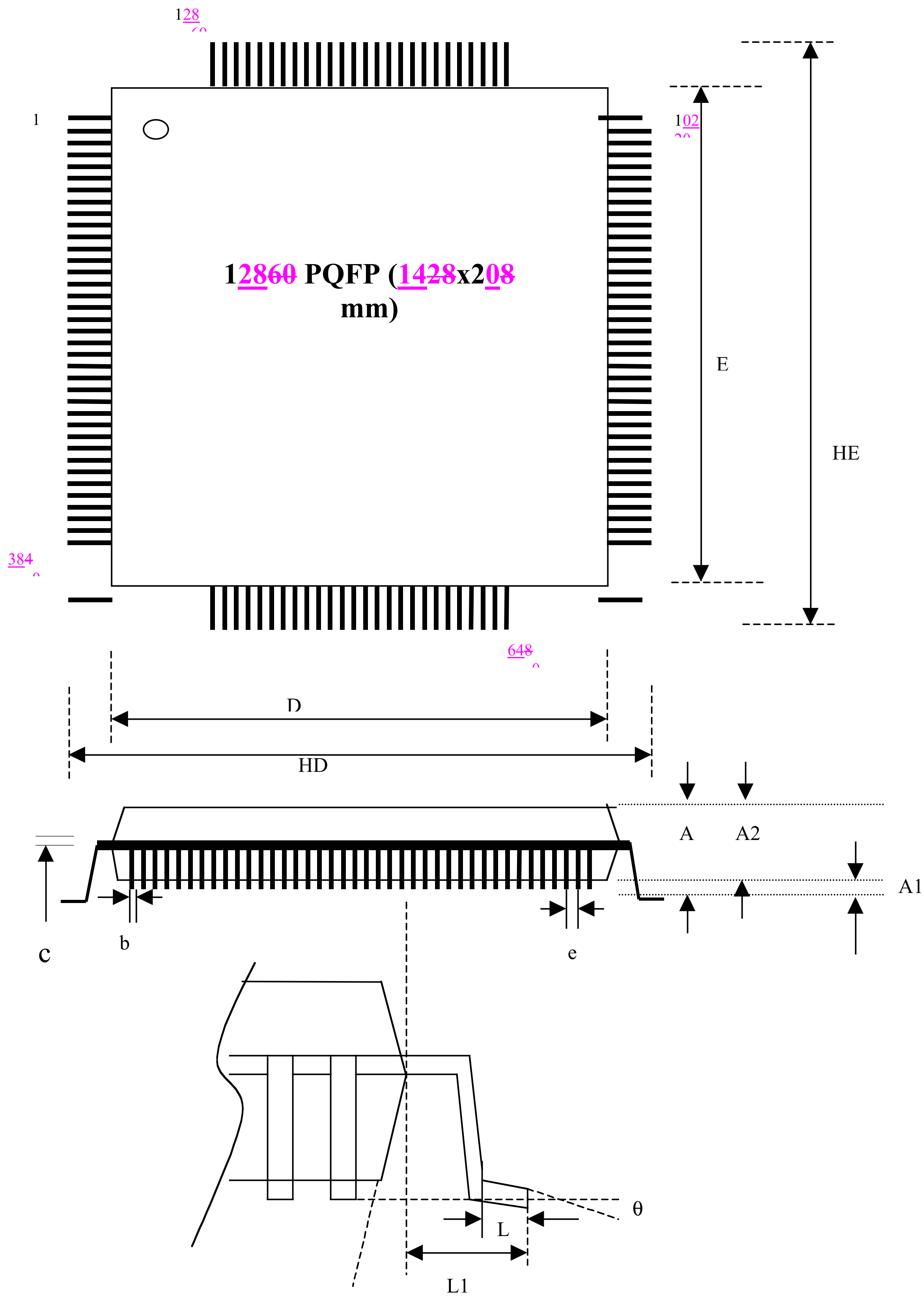
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIL	Input low voltage	CMOS			0.3*VCC	V
VIH	Input high voltage	CMOS	0.7*VCC			V
VT-	Schmitt trigger negative going threshold voltage	COMS		1.20		V
VT+	Schmitt trigger positive going threshold voltage	COMS		2.10		V
VOL	Output low voltage	IOH=2,4,8,12, 16,24 mA			0.4	V
VOH	Output high voltage	IOH=2,4,8,12, 16,24 mA	2.4			V
RI	Input pull-up /down resistance	VIL=0V or VIH=VCC		75		KΩ

DC Electrical Characteristics for 5V Operation

(Under Recommended Operation Conditions and V_{CC}=4.75~5.25,T_J=0°C to +115°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIL	Input low voltage	COMS			0.3*VCC	V
VIH	Input high voltage	COMS	0.7*VCC			V
VIL	Input low voltage	TTL			0.8	V
VIH	Input high voltage	TTL	2.0			V
VT-	Schmitt trigger negative going threshold voltage	CMOS		1.78		V
VT+	Schmitt trigger positive going threshold voltage	COMS		3.00		V
VT-	Schmitt trigger negative going threshold voltage	TTL		1.10		V
VT+	Schmitt trigger positive going threshold voltage	TTL		1.90		V
VOL	Output low voltage	IOL=2,4,8,16,24mA			0.4	V
VOH	Output high voltage	IOH=2,4,8,16,24 mA	3.5			V
RI	Input pull-up / down resistance	VIL=0V or VIH=VCC		50		KΩ

PACKAGE DIMENSIONS



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Symbol\Unit	Inch (Base)	MM (Base)
A	0.134(Max)	3.40 (Max)
A1	0.010 (Min)	0.25 (Min)
A2	0.112 +/-0.003	2.85 +/- 0.08
b	0.007 (Min) – 0.011(Max)	0.17(Min) – 0.27(Max)
c	.004 (Min) – 0.008 (Max)	0.09(Min) – 0.20(Max)
D	0.551+/-0.002	14.000+/-0.10
E	0.787+/-0.002	20.000+/-0.10
e	0.020 (Ref)	0.5(Ref)
HD	0.677 +/- 0.01	17.20 +/- 0.25
HE	0.913 +/- 0.01	23.20 +/- 0.25
L	0.035+/-0.006	0.88+/-0.15
L1	0.063(Ref)	1.60(Ref)
θ	0 - 7.0°	0 - 7.0°

ORDER INFORMATION

Order Code	Temperature	Package	Speed
SD1010	Commercial 0°C ~ 70°C	128-pin PQFP 14 x 20 (mm)	100MHz

SmartASIC, Inc.

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to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.