

1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- Performance range:

	trAC	tcAC	trC	tHPC
KM416V1004A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416V1004A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416V1004A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- Extended Data Out Mode
(Fast Page Mode with Extended Data Out)
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +3.3V ± 0.3V power supply
- Refresh Cycle
 - 4096 cycle/64ms (Normal)
 - 4096 cycle/128ms (L-version)
 - 4096 cycle/128ms (F-version)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

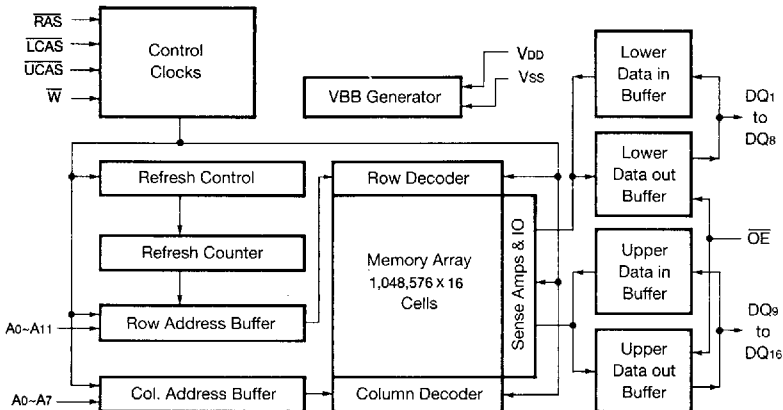
GENERAL DESCRIPTION

The Samsung KM416V1004A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416V1004A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

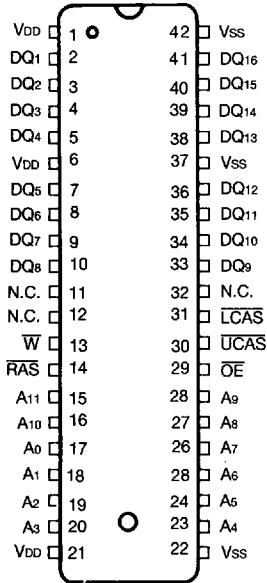
The KM416V1004A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



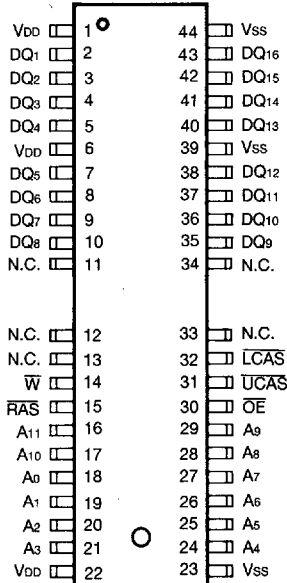
PIN CONFIGURATION (Top Views)

• KM416V1004AJ



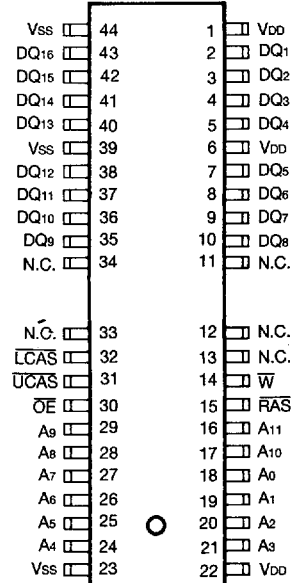
(SOJ)

• KM416V1004AT



(TSOP(II)-Forward)

• KM416V1004AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A ₀ -A ₁₁	Address Inputs
DQ ₁ -16	Data In/Out
V _{SS}	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
V _{DD}	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5 to 4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (\overline{RAS} , \overline{UCAS} or \overline{LCAS} , Address Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I _{CC1}	-	90 80 70	mA mA mA
Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$)	KM416V1004A KM416V1004AL KM416V1004ALL	I _{CC2}	-	2 1 1	mA mA mA
\overline{RAS} -Only Refresh Current* ($\overline{UCAS}=\overline{LCAS}=V_{IH}$, \overline{RAS} , Address Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I _{CC3}	-	90 80 70	mA mA mA
EDO Mode Current* ($\overline{RAS}=V_{IL}$, \overline{UCAS} or \overline{LCAS} , Address Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I _{CC4}	-	110 100 90	mA mA mA
Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{DD}-0.2V$)	KM416V1004A KM416V1004AL KM416V1004ALL	I _{CC5}	-	1 300 200	mA μ A μ A
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} , \overline{UCAS} or \overline{LCAS} Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I _{CC6}	-	90 80 70	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V, Input Low Voltage(V _{IL})=0.2V \overline{UCAS} , \overline{LCAS} =0.2V DIN=Don't Care, trc=31.25 μ s (L-Version) tr _{AS} =tr _{AS} min~300ns	KM416V1004A-L	I _{CC7}	-	450	μ A

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DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A11=VDD-0.2V or 0.2V DQ1-DQ16=VDD-0.2V or 0.2V or Open	Iccs	-	250	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ VDD+0.3V, all other pins not under test=0 V)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ VDD)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=2mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while RAS=VIL. In Icc4, Address can be changed maximum once while one Hyper page mode cycle time tHPC.

CAPACITANCE (TA=25°C, VDD=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~11)	CIN1	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	CIN2	-	7	pF
Output Capacitance (DQ1~DQ16)	COO	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VDD=3.3V ± 0.3V, See notes 1,2)

(Test condition : VIH/VIL=2.1V/0.8V, VOH/VOL=2.0V/0.8V, Output Loading CL=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from RAS	tRAC		60		70		80	ns	3,4,11
Access time from CAS	tCAC		17		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	3		3		3		ns	3
OE to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from CAS	tOEZ	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
RAS precharge time	tRP	40		50		60		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	tRSH	17		20		20		ns	
CAS hold time	tCSH	50		60		70		ns	
CAS pulse width	tCAS	10	10,000	15	10,000	20	10,000	ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	4



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to RAS	tAR	45		55		60		ns	6
Column address to RAS lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to RAS	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		15		20		ns	
Write command to CAS lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to RAS	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
CAS to W delay time	tCWD	40		50		50		ns	8,17
RAS to W delay time	tRWD	85		95		105		ns	8
Column address to W delay time	tAWD	55		60		65		ns	8
CAS precharge to W delay time	tCPWD	60		65		70		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		ns	20
RAS precharge to CAS hold time	tRPC	5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		25		30		ns	
RAS hold time referenced to OE	tROH	15		20		20		ns	
OE access time	tOEA		15		20		20	ns	
OE to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from OE	tOEZ	3	15	3	20	3	20	ns	7
OE command hold time	tOEH	15		20		20		ns	
Access time from CAS precharge	tCPA		35		40		45	ns	3

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
CAS precharge time (Hyper page mode)	tCP	10		10		10		ns	16
RAS pulse width (Hyper Page mode)	tRASP	60		70		80		ns	
RAS hold time from CAS precharge	tRHCP	35		40		45		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from RAS	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from W	tWEZ	3	15	3	20	3	20	ns	7
OE to CAS hold time	tOCH	5		5		5		ns	
CAS hold time to OE	tCHO	5		5		5		ns	
OE precharge time	tOEP	5		5		5		ns	
W pulse width	tWPE	5		5		5		ns	
W to data delay	tWED	15		20		20		ns	
RAS pulse width (F-ver)	tRASS	100		100		100		μs	13
RAS precharge time (F-ver)	tRPS	110		130		150		ns	13
CAS hold time (F-ver)	tCHS	-50		-50		-50		ns	13

KM416V1004A/A-L/A-F Truth Table

RAS	LCAS	UCAS	W	OE	DQ1-DQ8	DQ9-DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

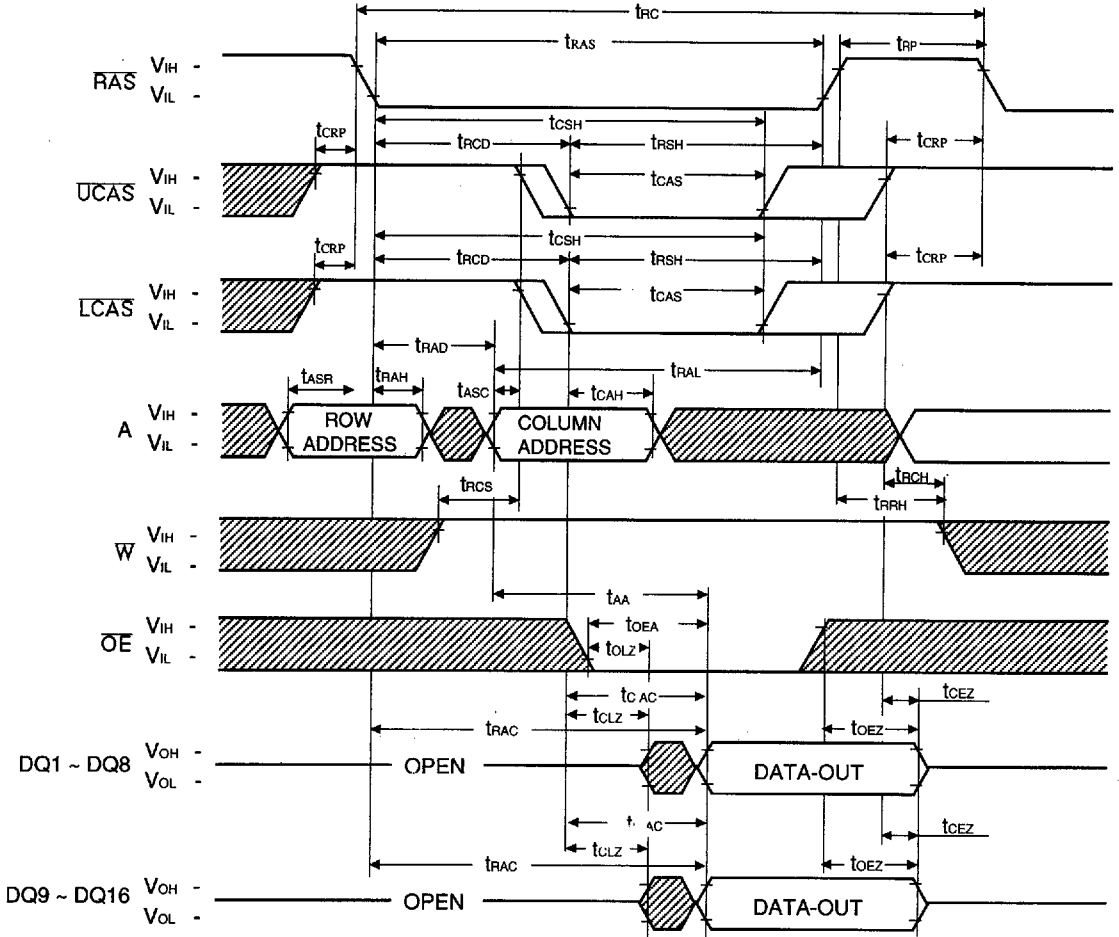
NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(min)$ and $V_{IL}(max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL Loads and 100pF.
4. Operation within the $t_{RCO}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCO}(max)$ is specified as a reference point only. If t_{RCO} is greater than the specified $t_{RCO}(max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCO} \geq t_{RCO}(max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(min)$, $t_{RWD} \geq t_{RWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled by t_{AA} .
12. $t_{ASC} \geq t_{CP} min$, Assume $t_T=2.0ns$.
13. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
15. t_{ASC} , t_{CAH} are referenced to the earlier \overline{CAS} falling edge.
16. t_{CP} is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
17. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.
19. t_{CSR} is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
20. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low.
21. t_{DS} , t_{DH} is independently specified for lower byte $D_{in(1-8)}$, upper byte $D_{in(9-16)}$



TIMING DIAGRAM
WORD READ CYCLE

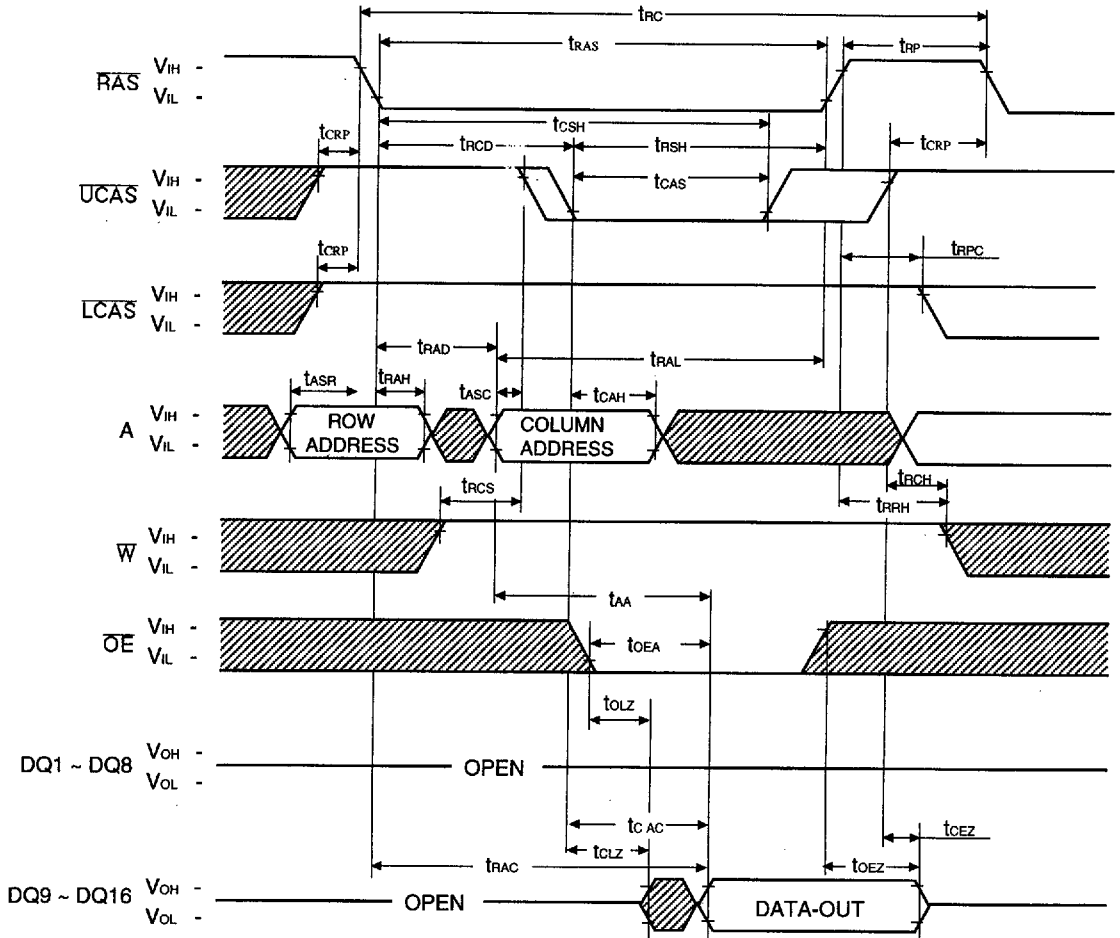
NOTE : D_{IN} = OPEN



 Don't Care

TIMING DIAGRAM
UPPER BYTE READ CYCLE

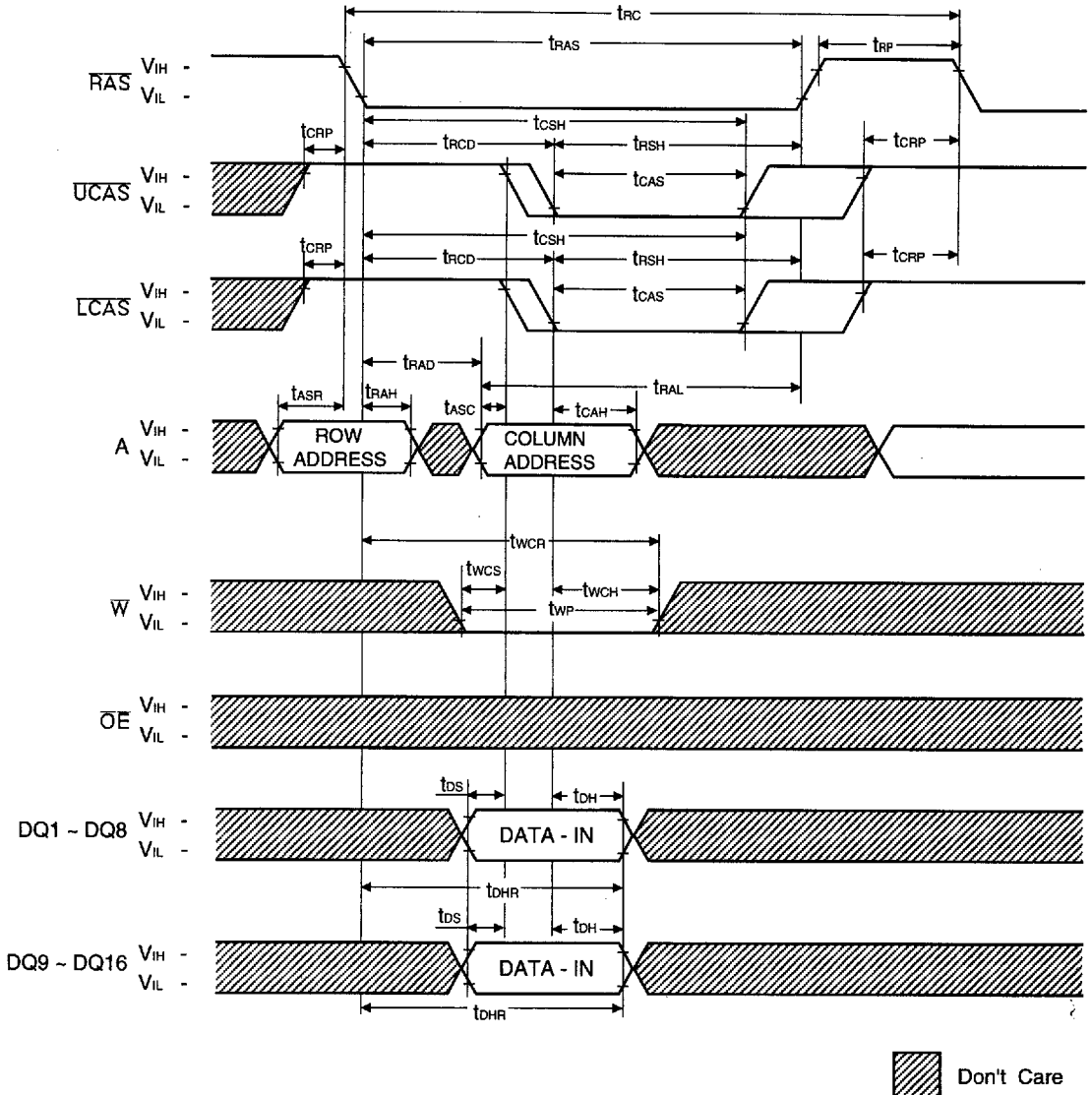
NOTE : $D_{IN} = OPEN$



 Don't Care

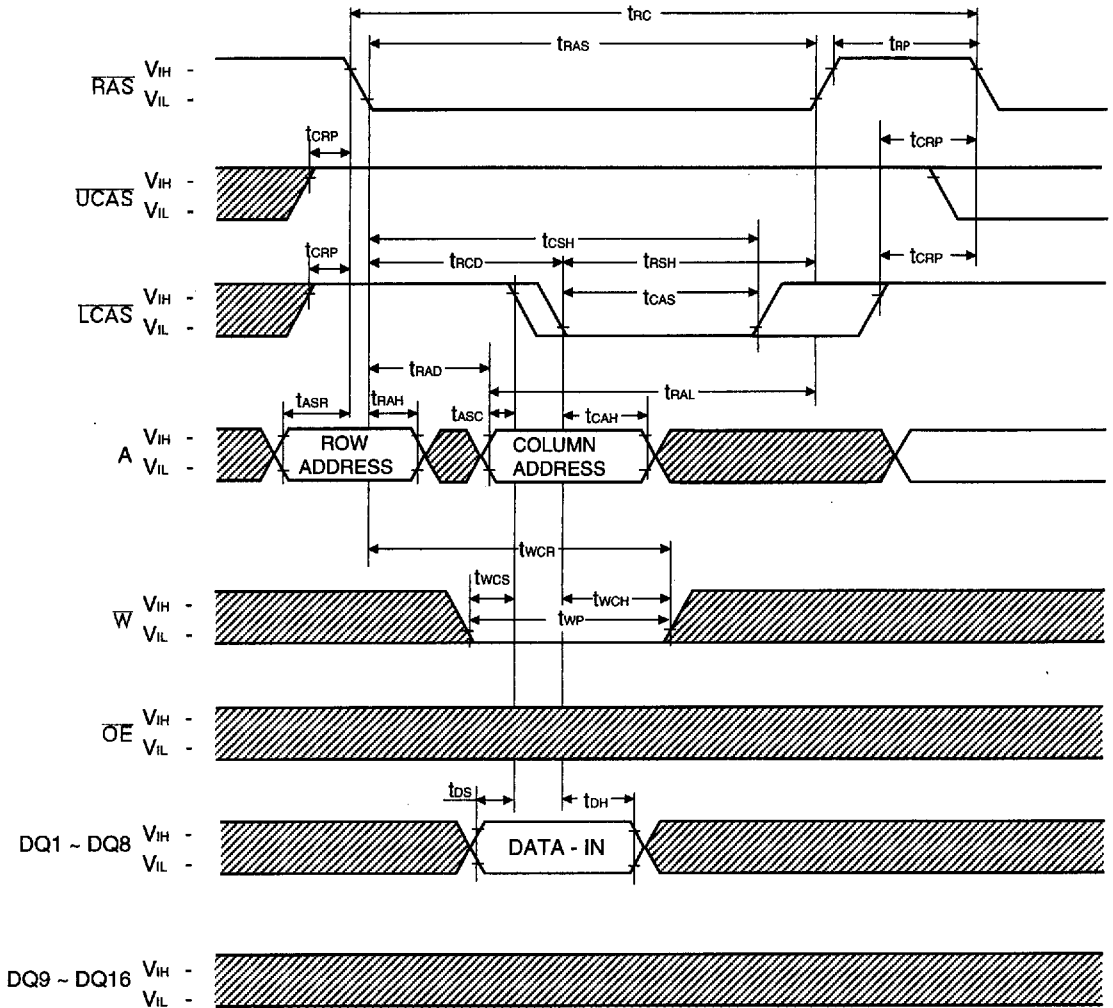
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



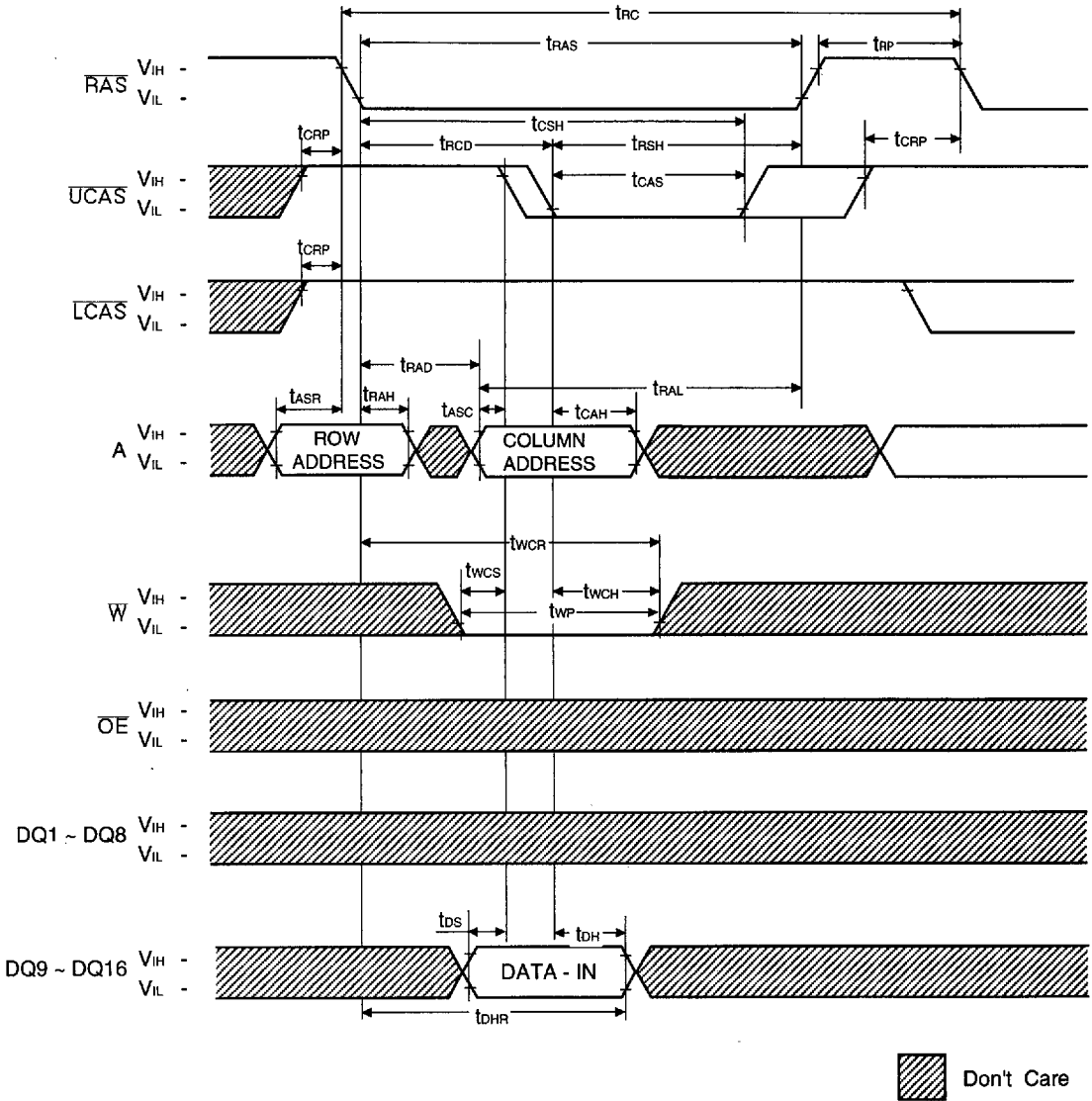
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



UPPER BYTE WRITE CYCLE (EARLY WRITE)

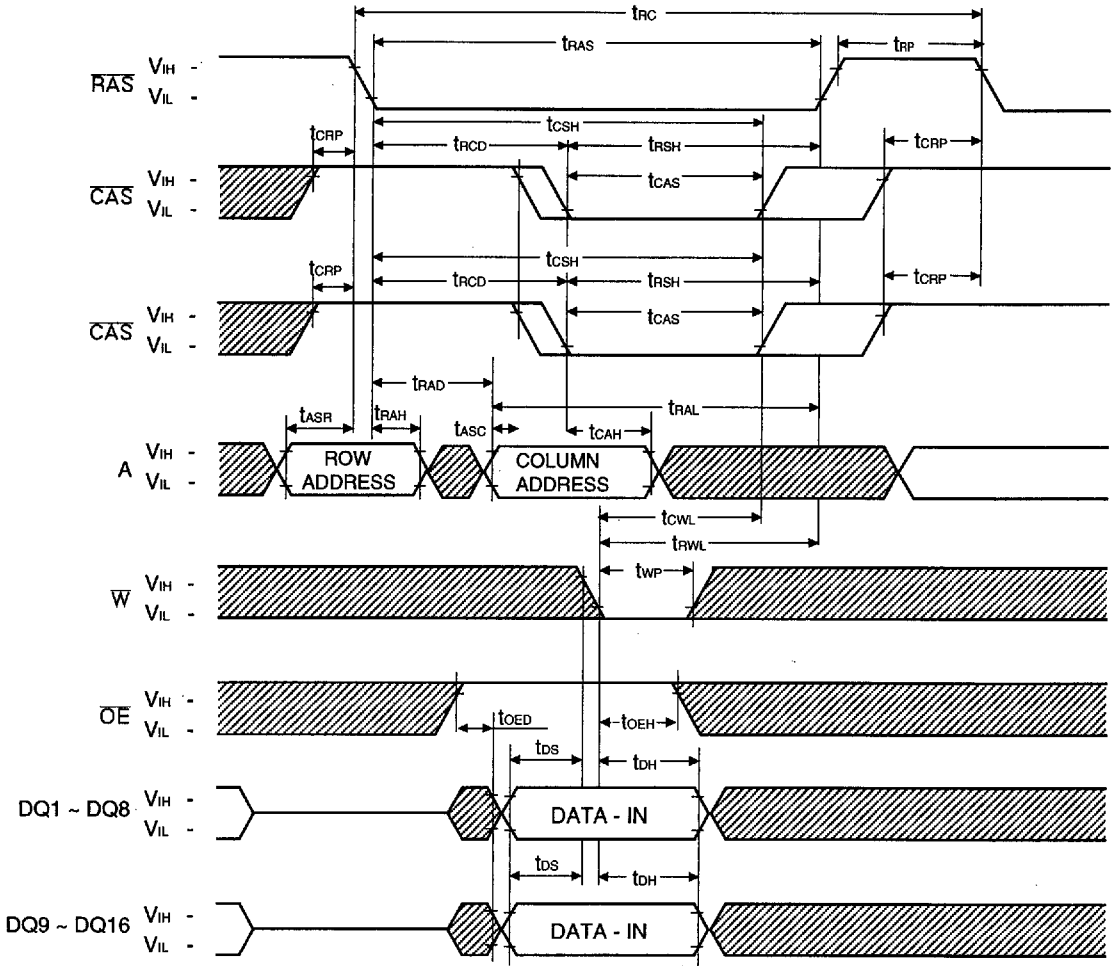
NOTE : D_{OUT} = OPEN



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WORD WRITE CYCLE (OE CONTROLLED WRITE)

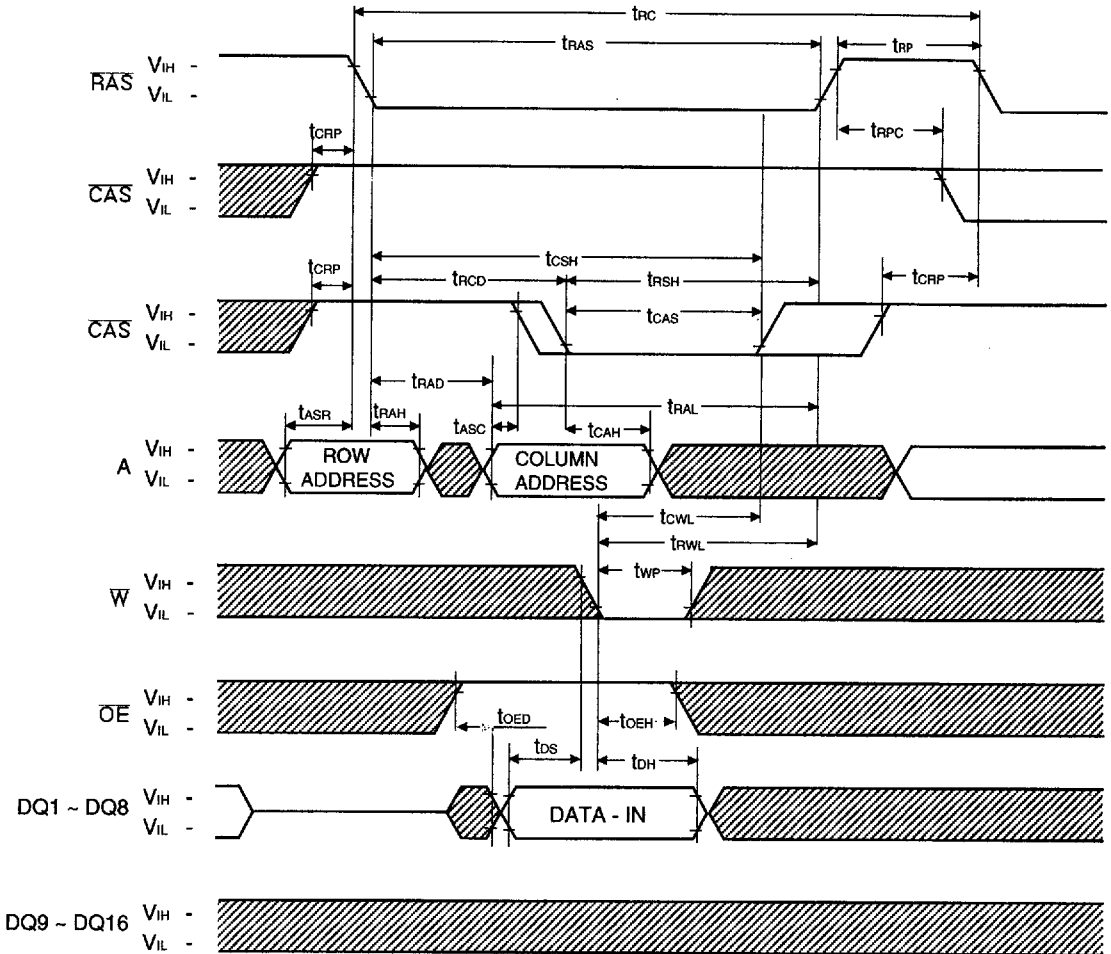
NOTE : D_{OUT} = OPEN



 Don't Care

LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : Dout = OPEN

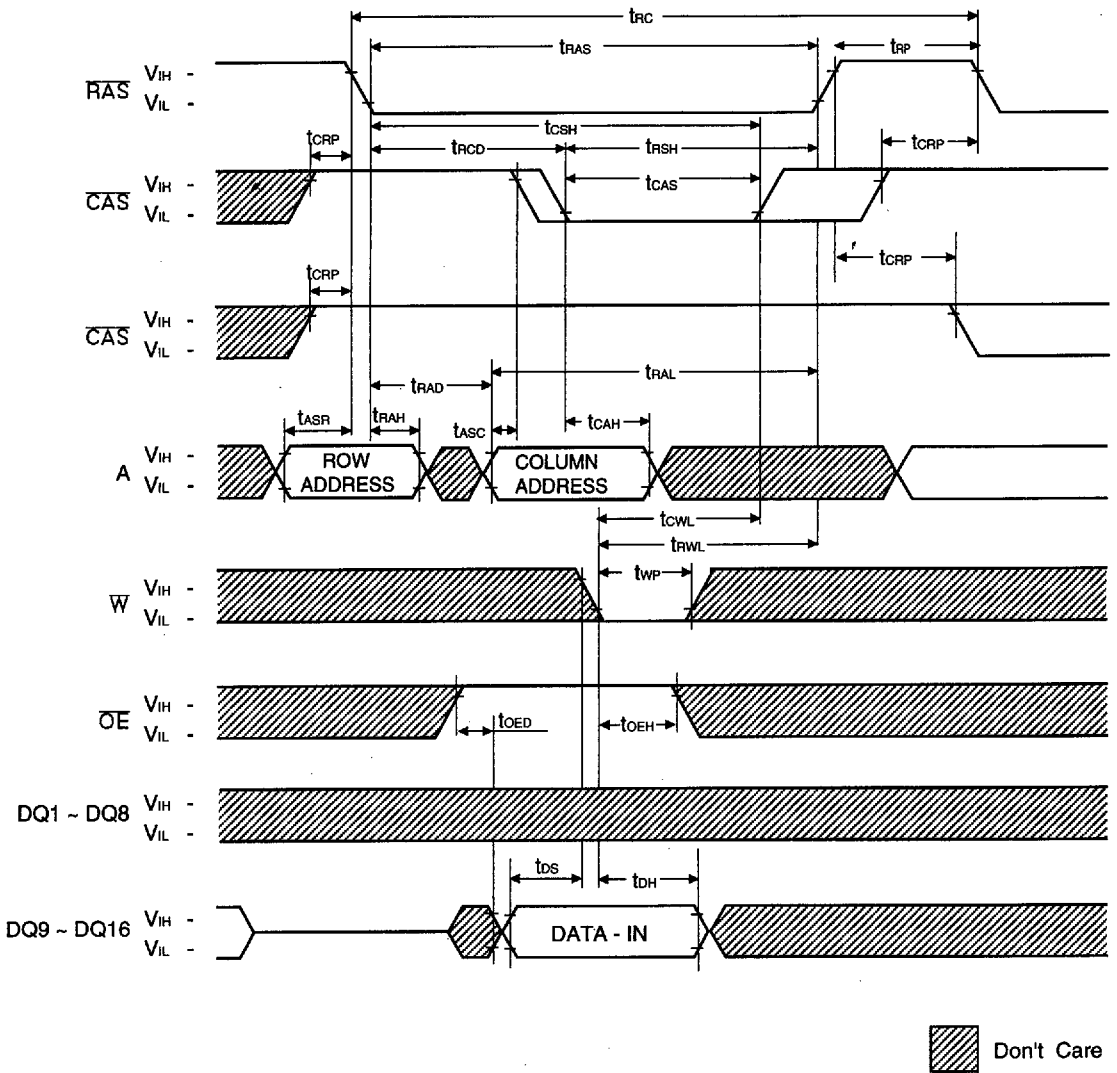


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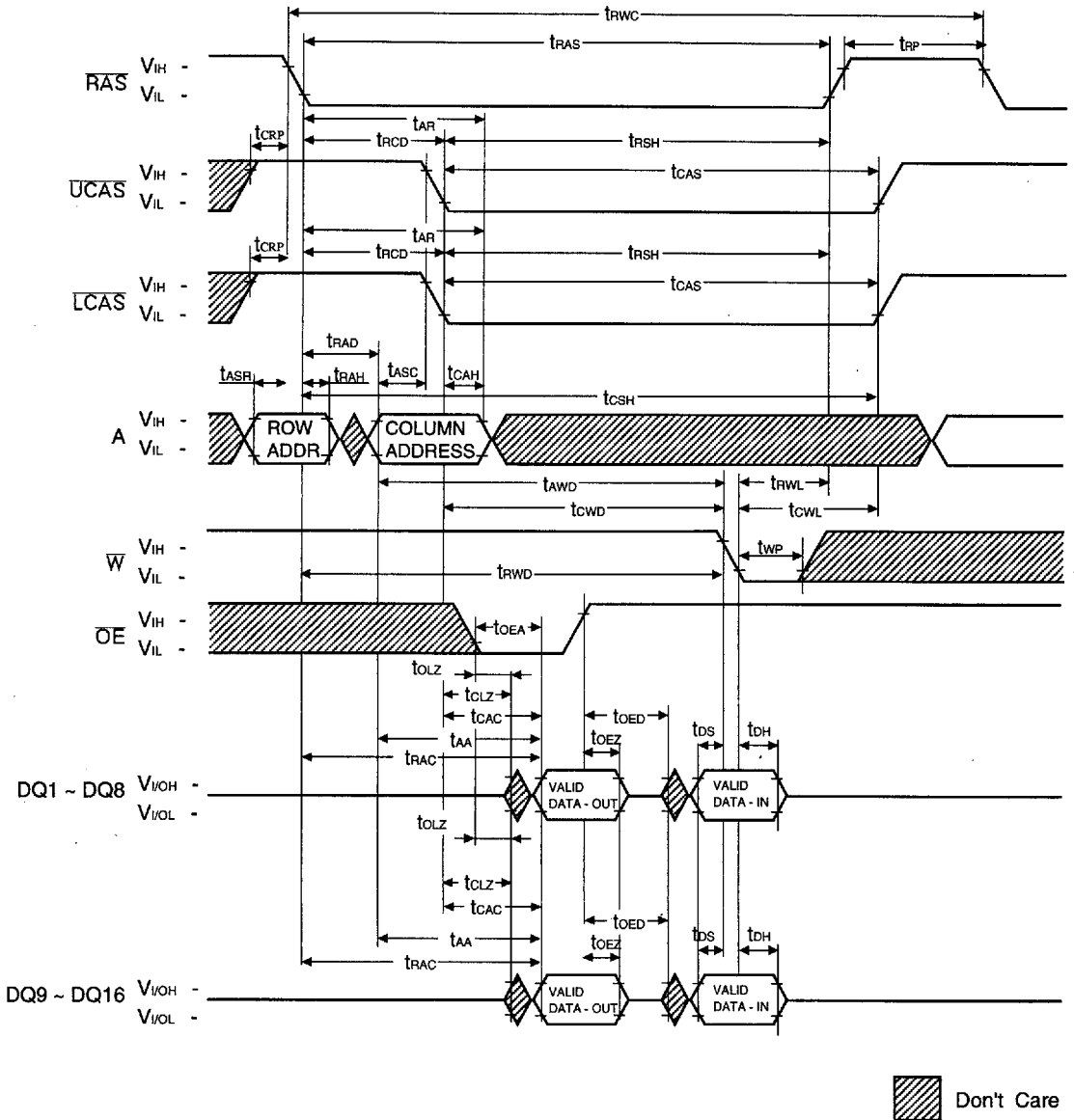
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UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

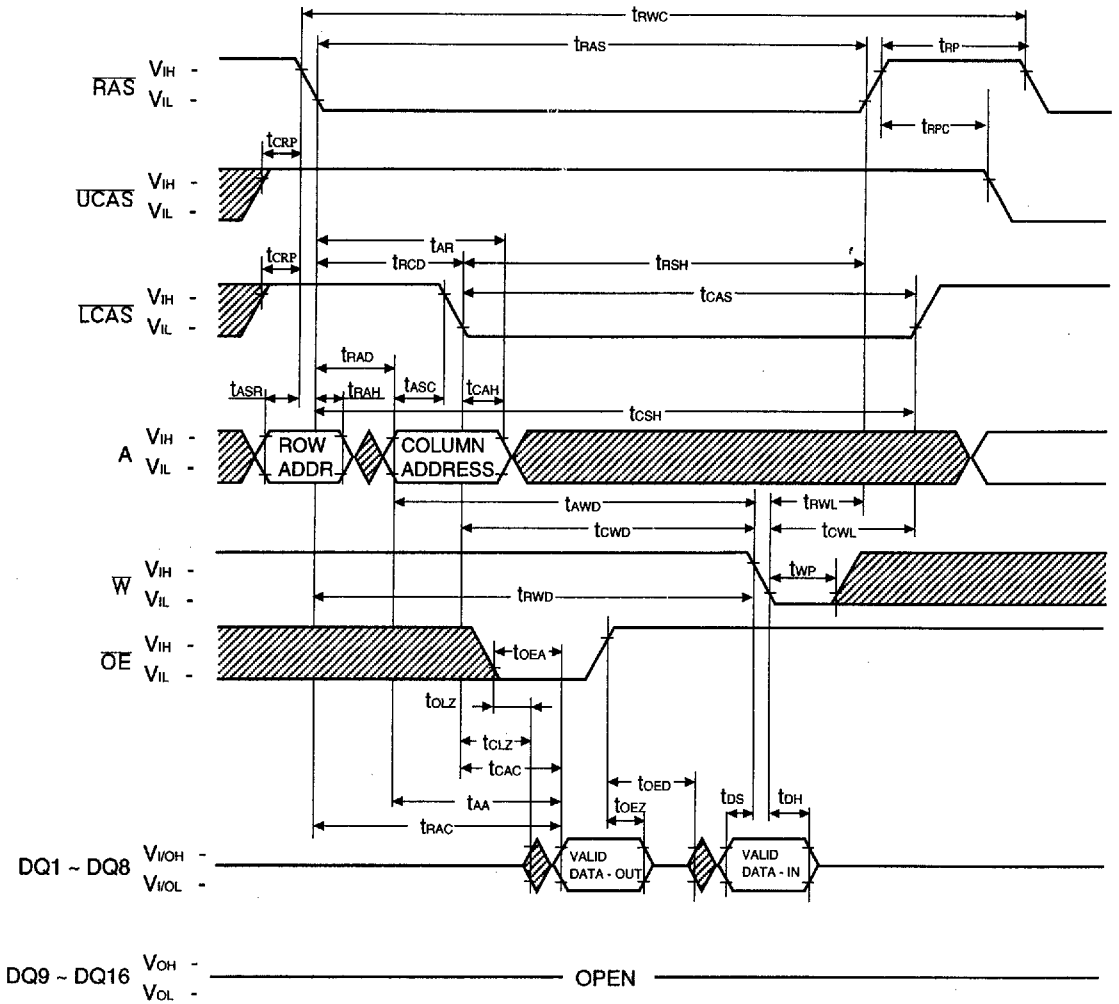



WORD READ - MODIFY - WRITE CYCLE



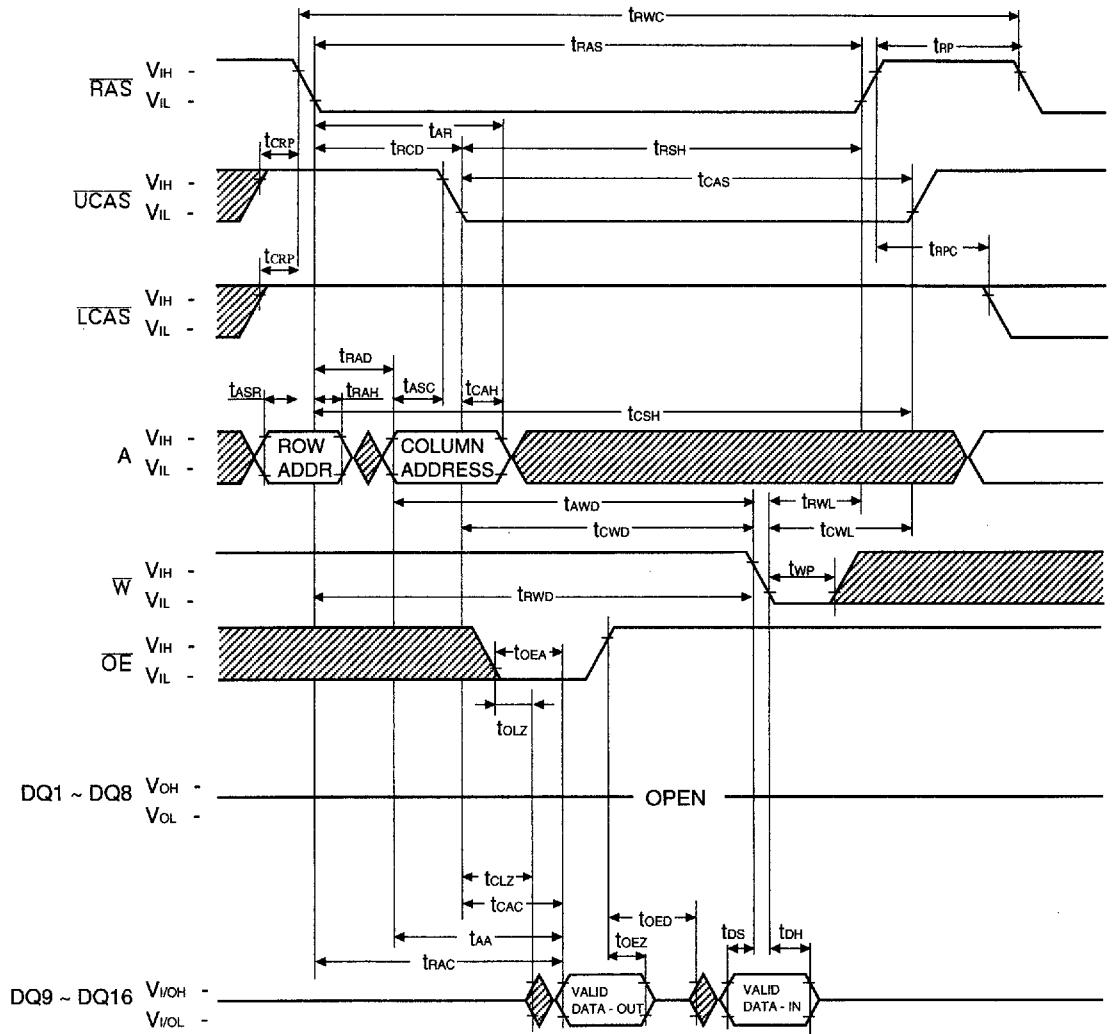
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LOWER-BYTE READ - MODIFY - WRITE CYCLE



 Don't Care

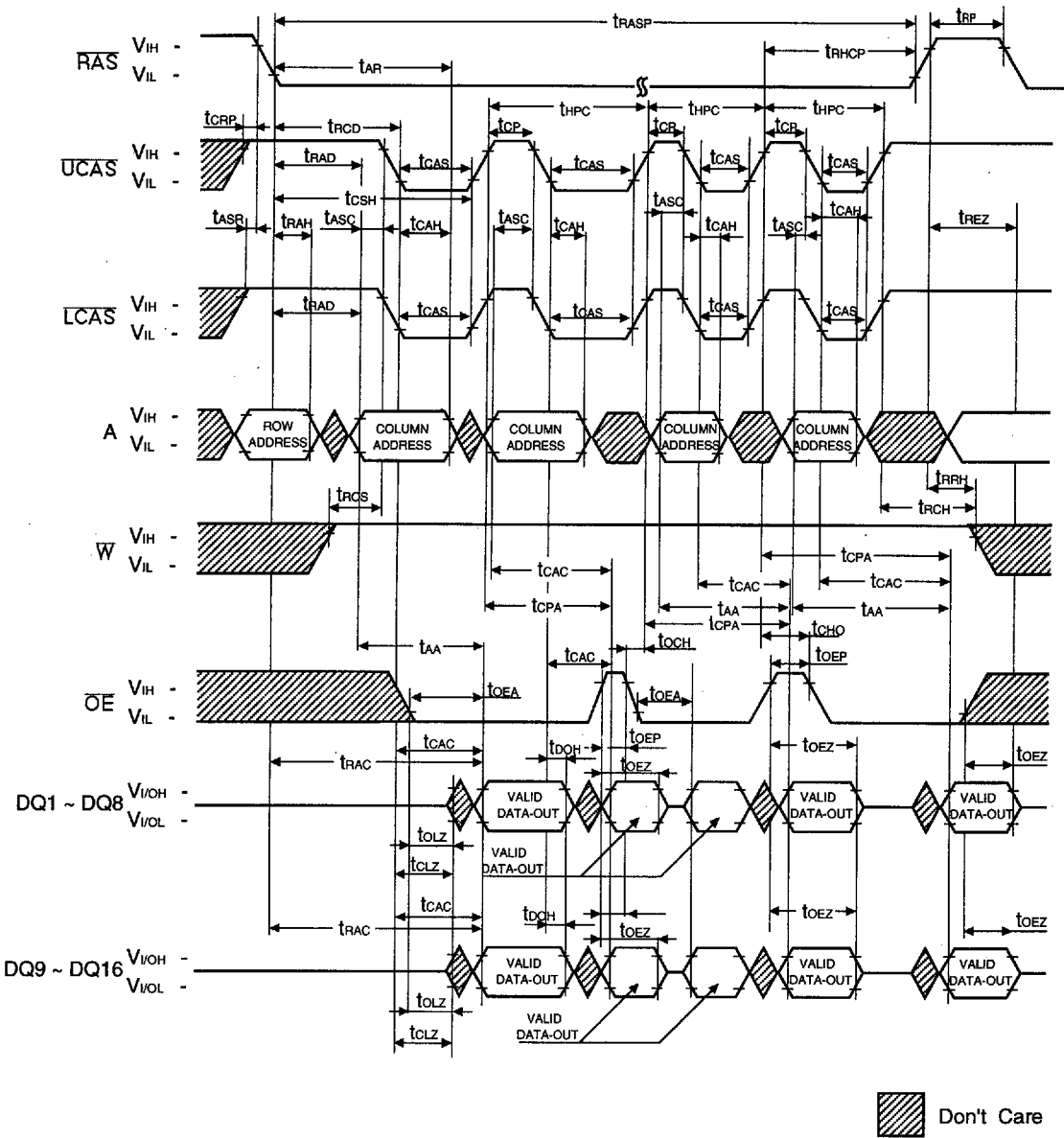
UPPER-BYTE READ - MODIFY - WRITE CYCLE



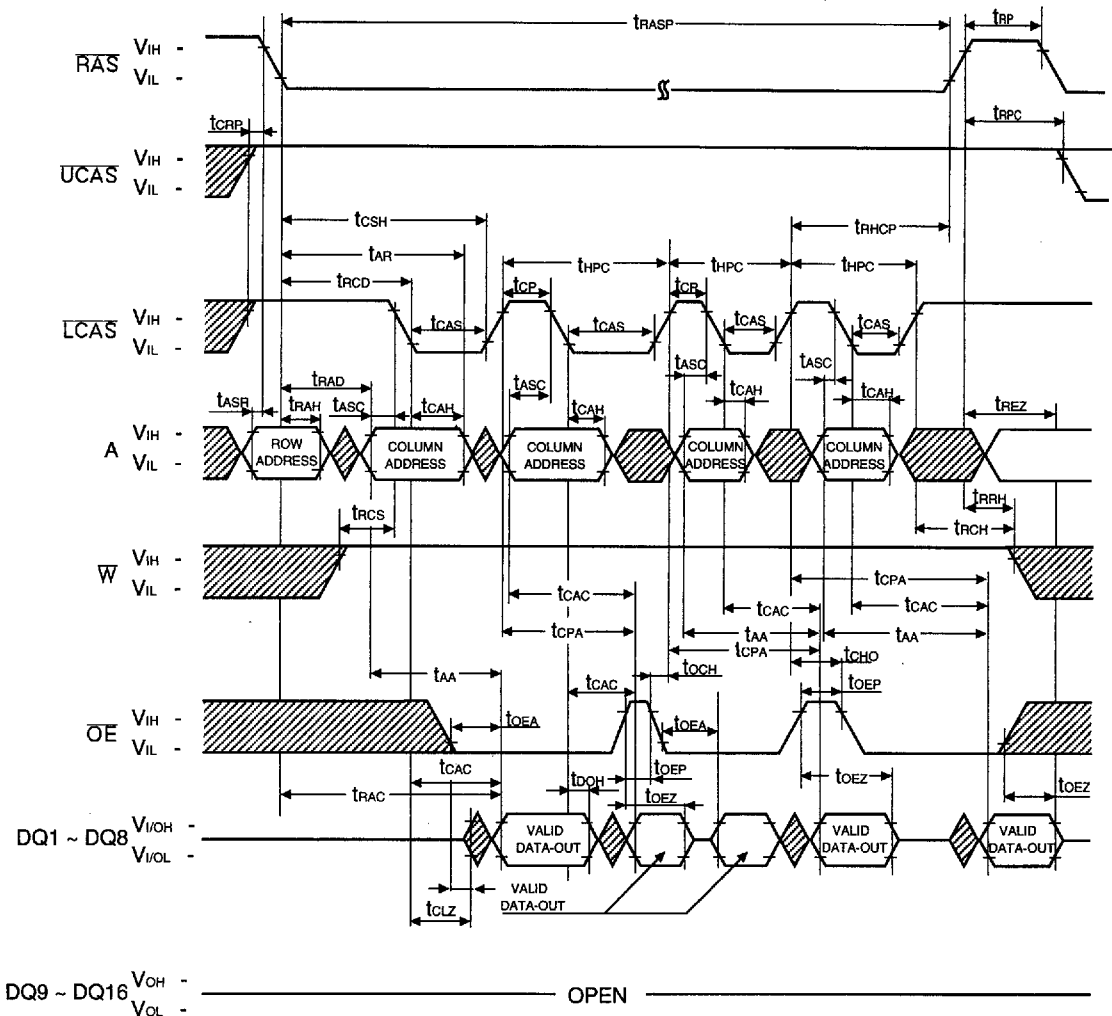
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HYPER PAGE MODE WORD READ CYCLE



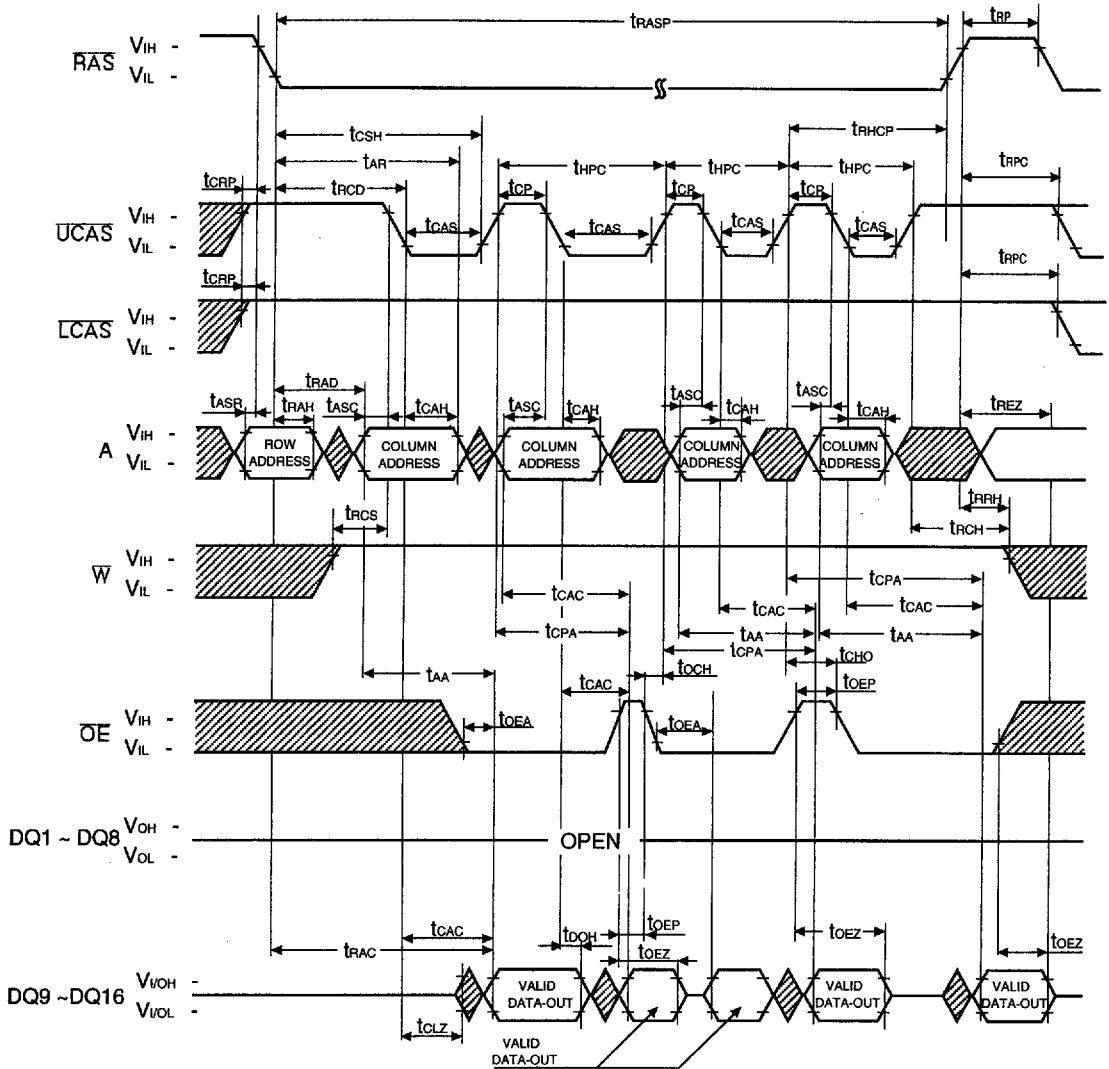
HYPER PAGE MODE LOWER BYTE READ CYCLE



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Don't Care

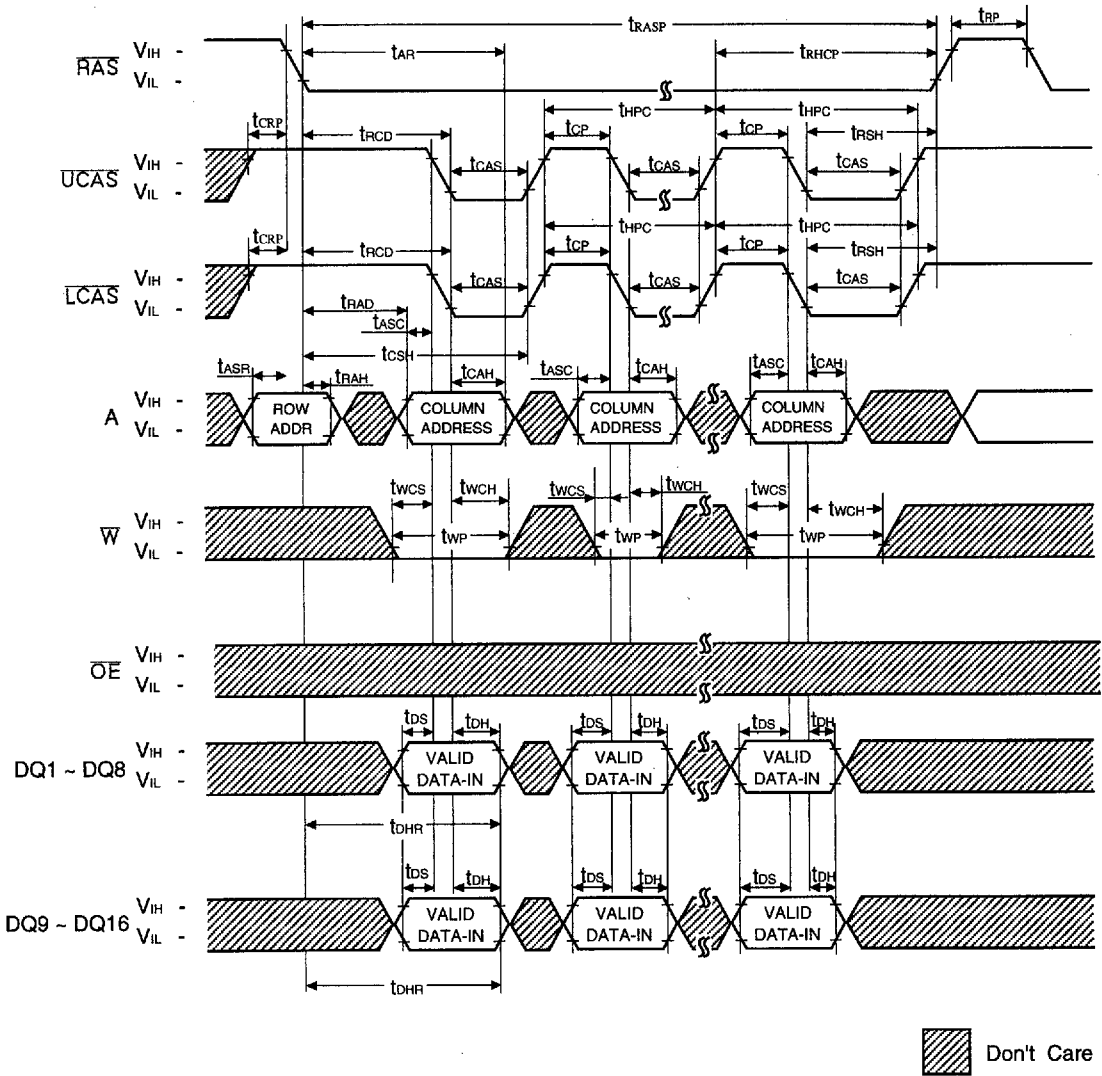
HYPER PAGE MODE UPPER BYTE READ CYCLE



 Don't Care

HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

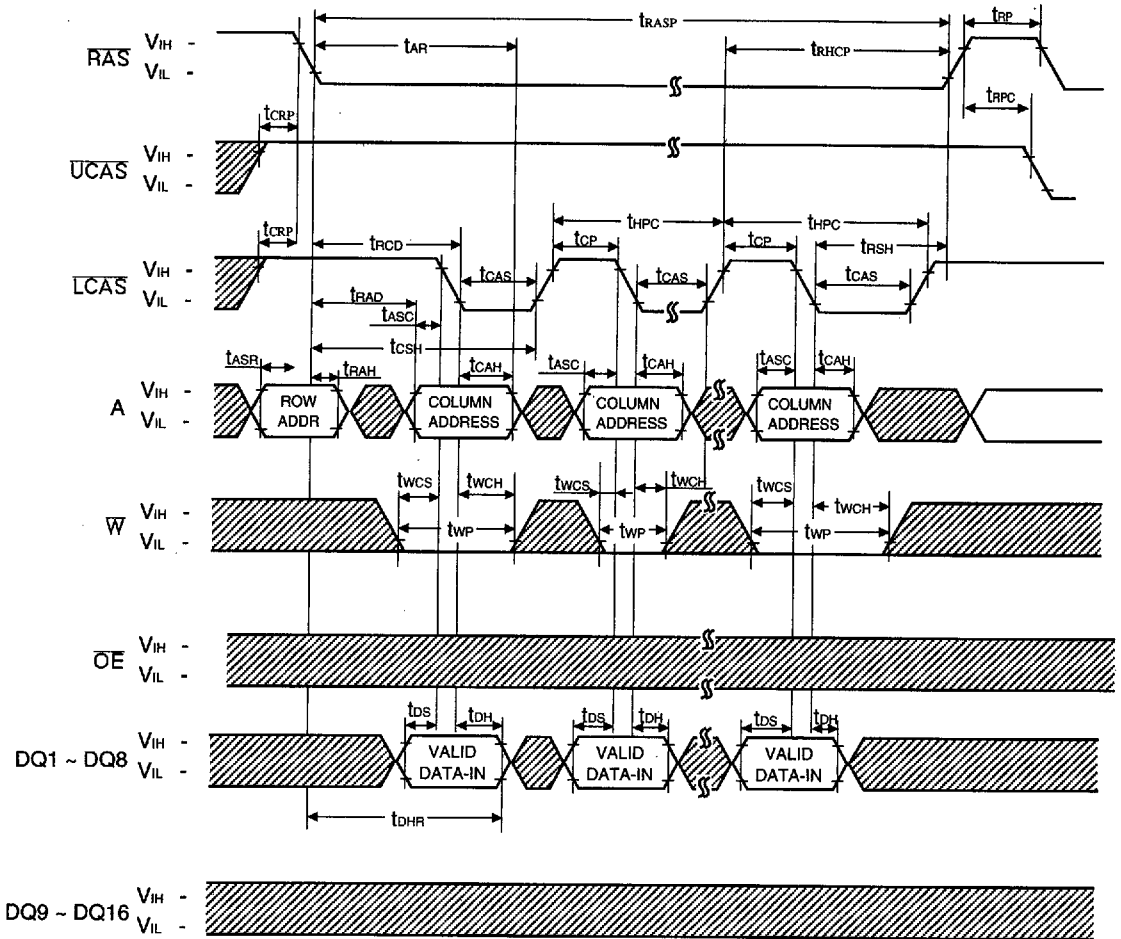
NOTE : D_{OUT} = Open



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HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

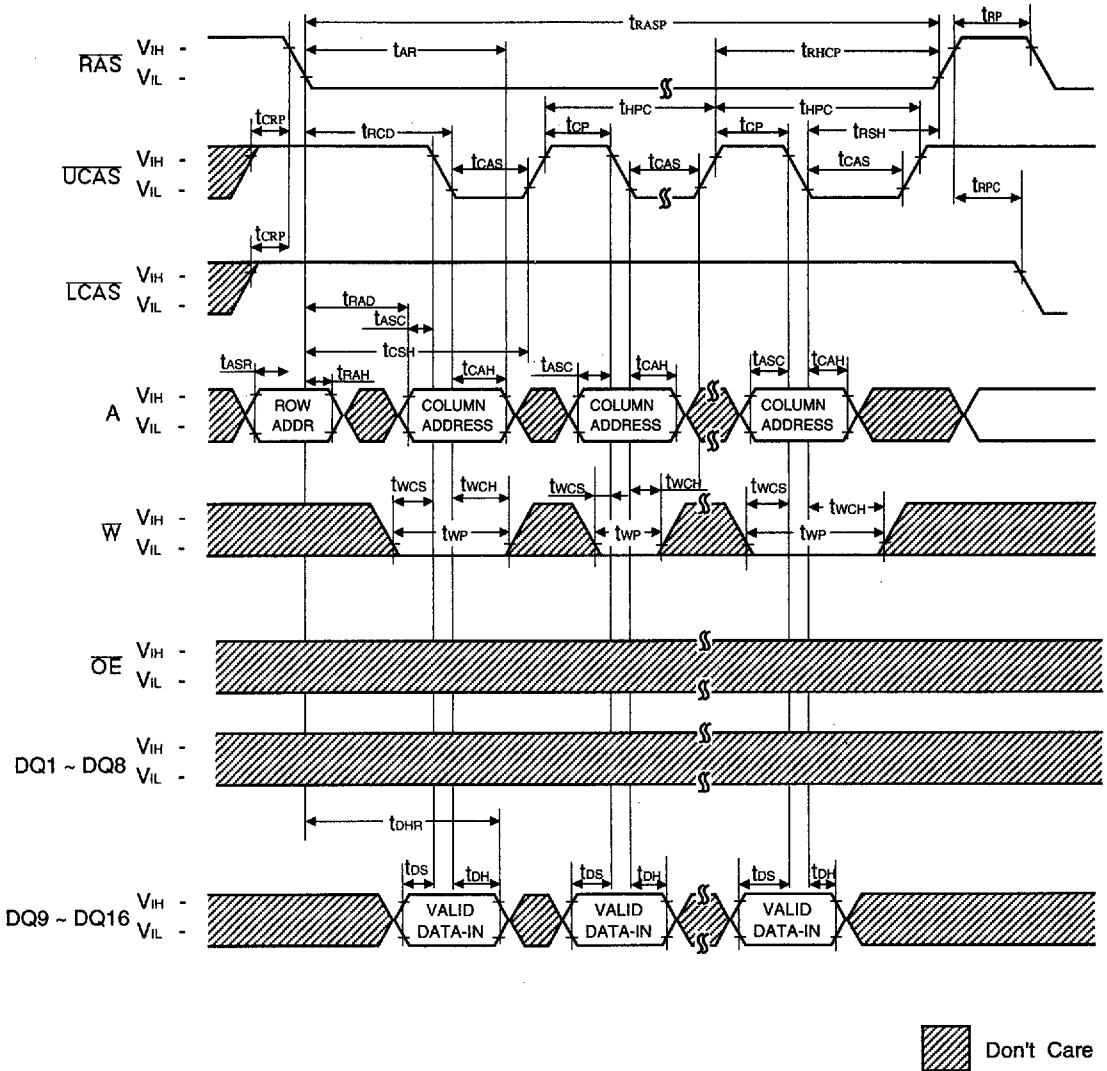
NOTE : Dout = Open



 Don't Care

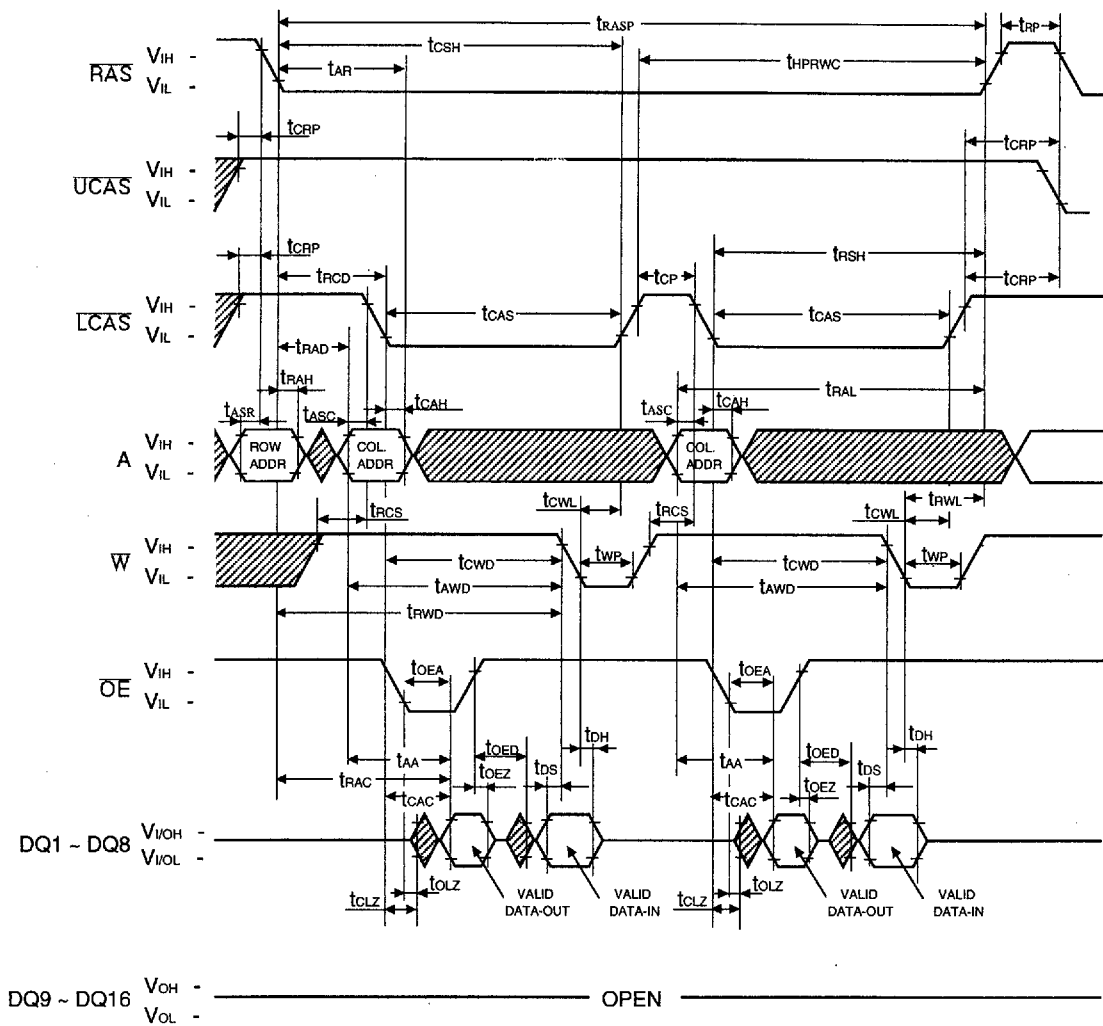
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)


NOTE : D_{out} = Open



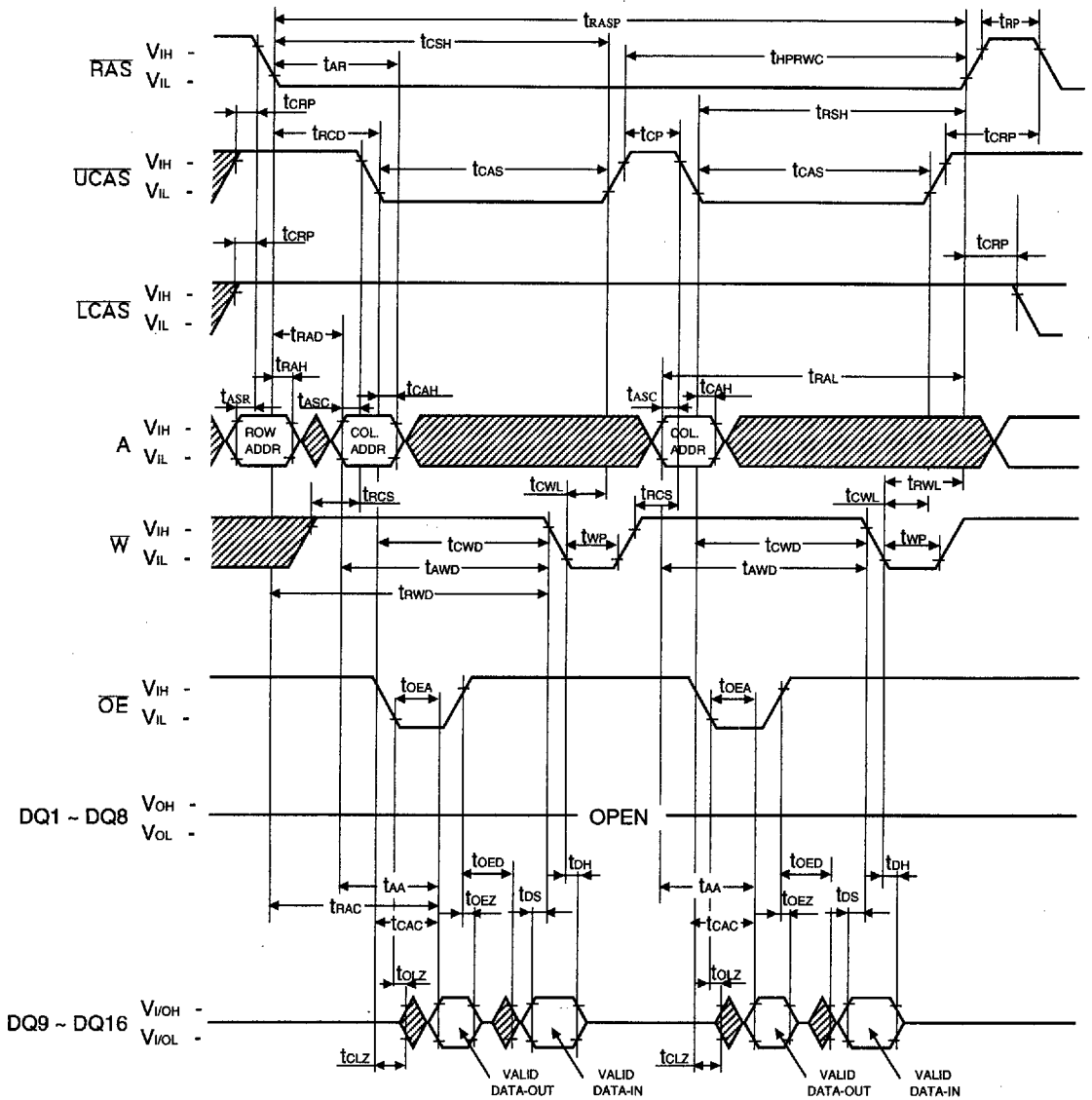
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HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



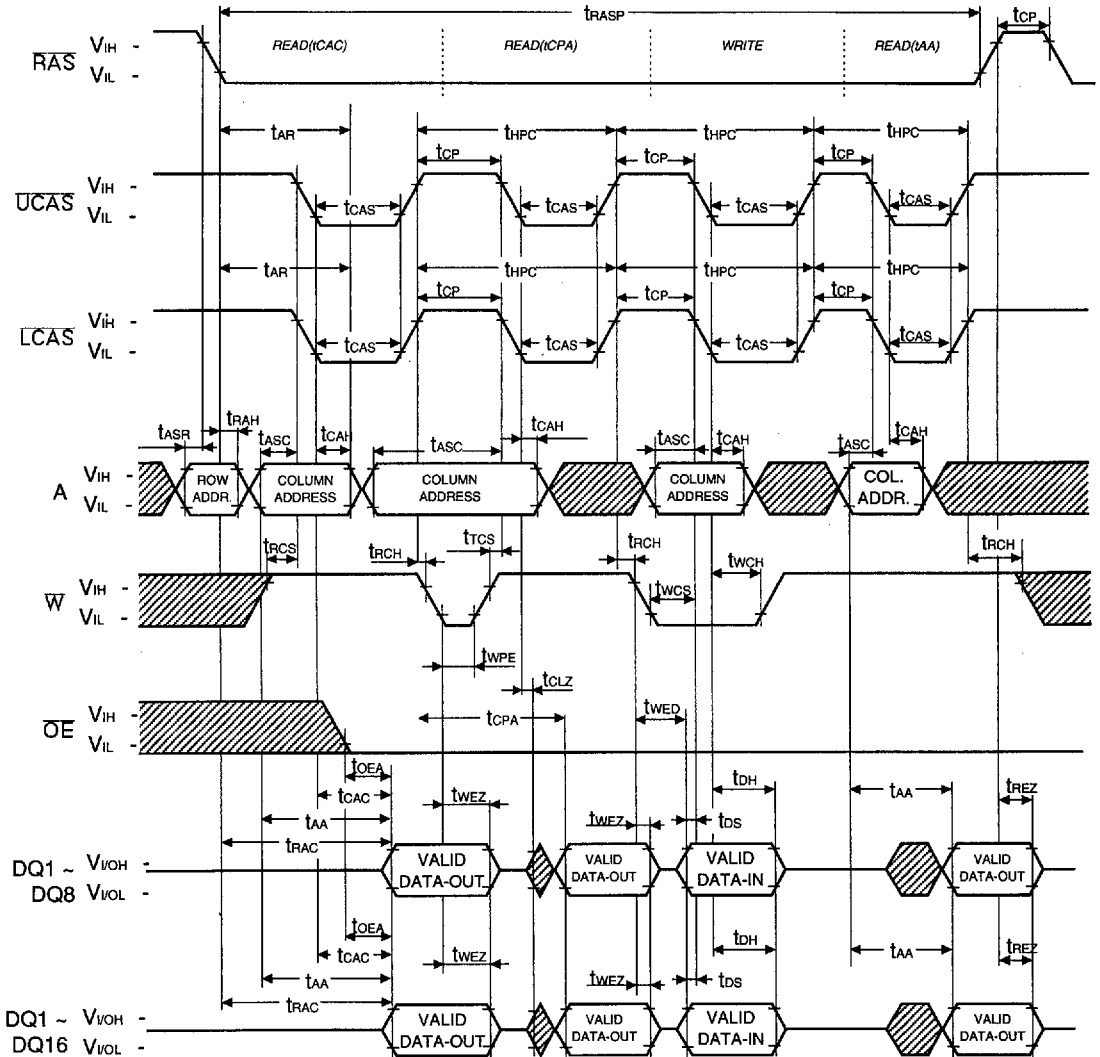
 Don't Care

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



Don't Care

HYPER PAGE READ AND WRITE MIXED CYCLE

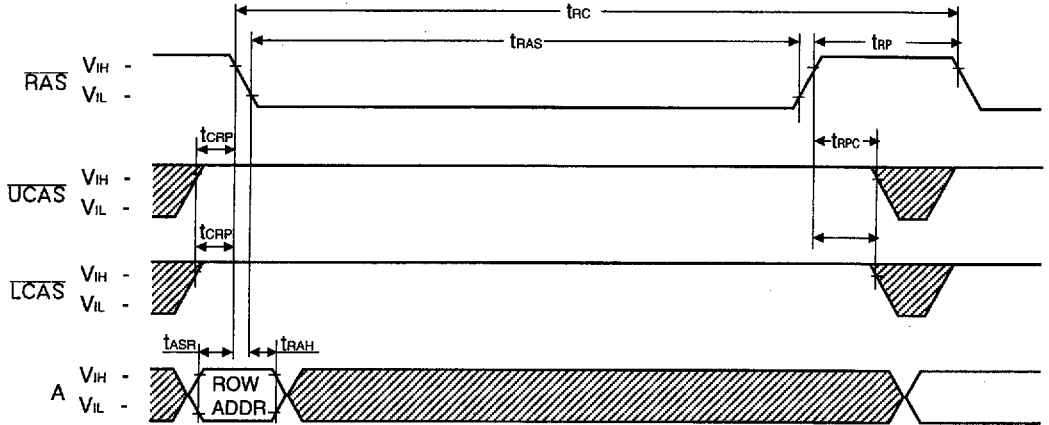


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Don't Care

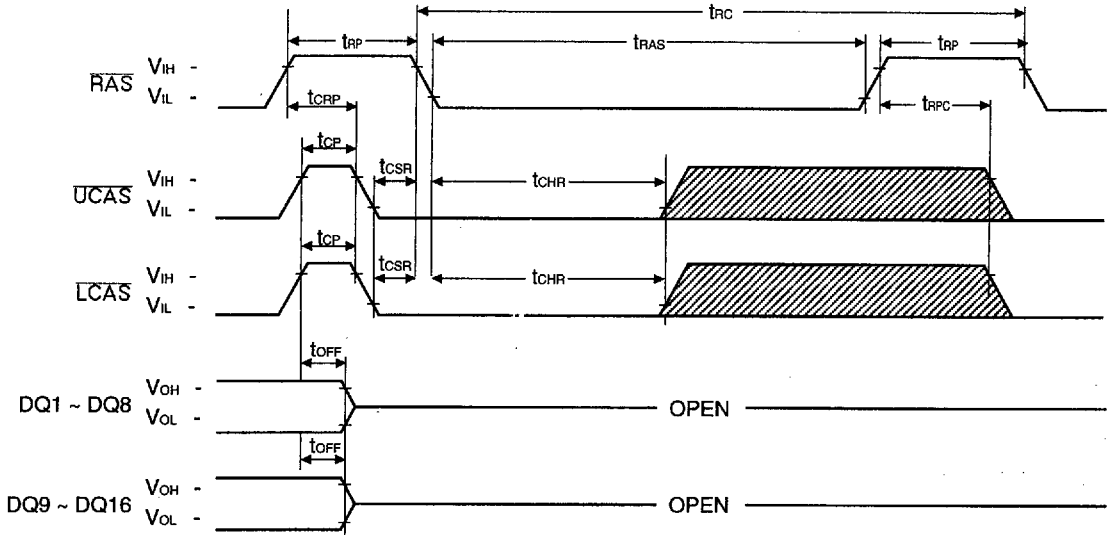
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{IN} = Don't care
 D_{OUT} = Open



CAS-BEFORE-RAS REFRESH CYCLE

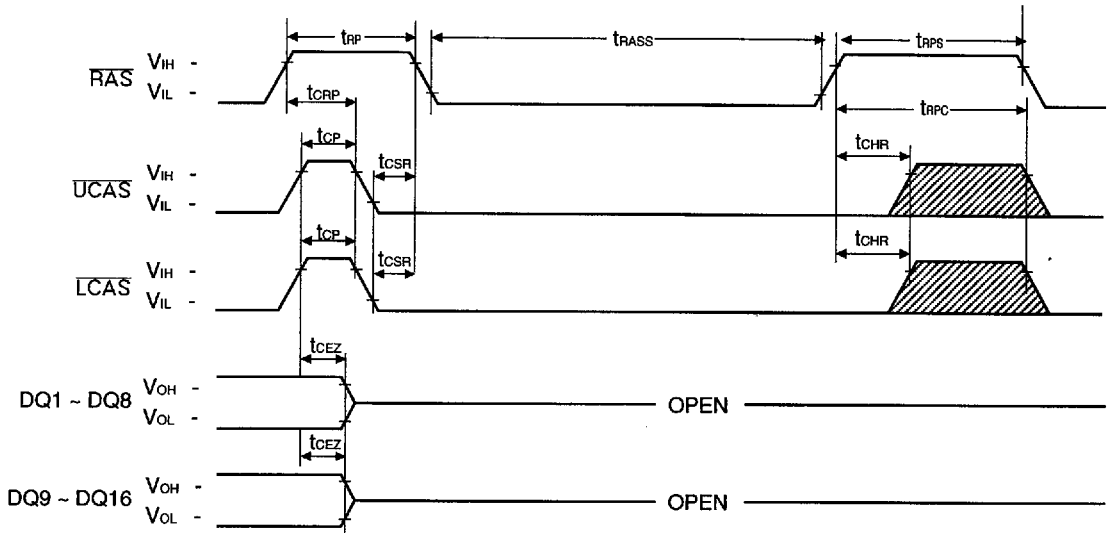
NOTE : \bar{W} , \bar{OE} , A = Don't Care



Don't Care

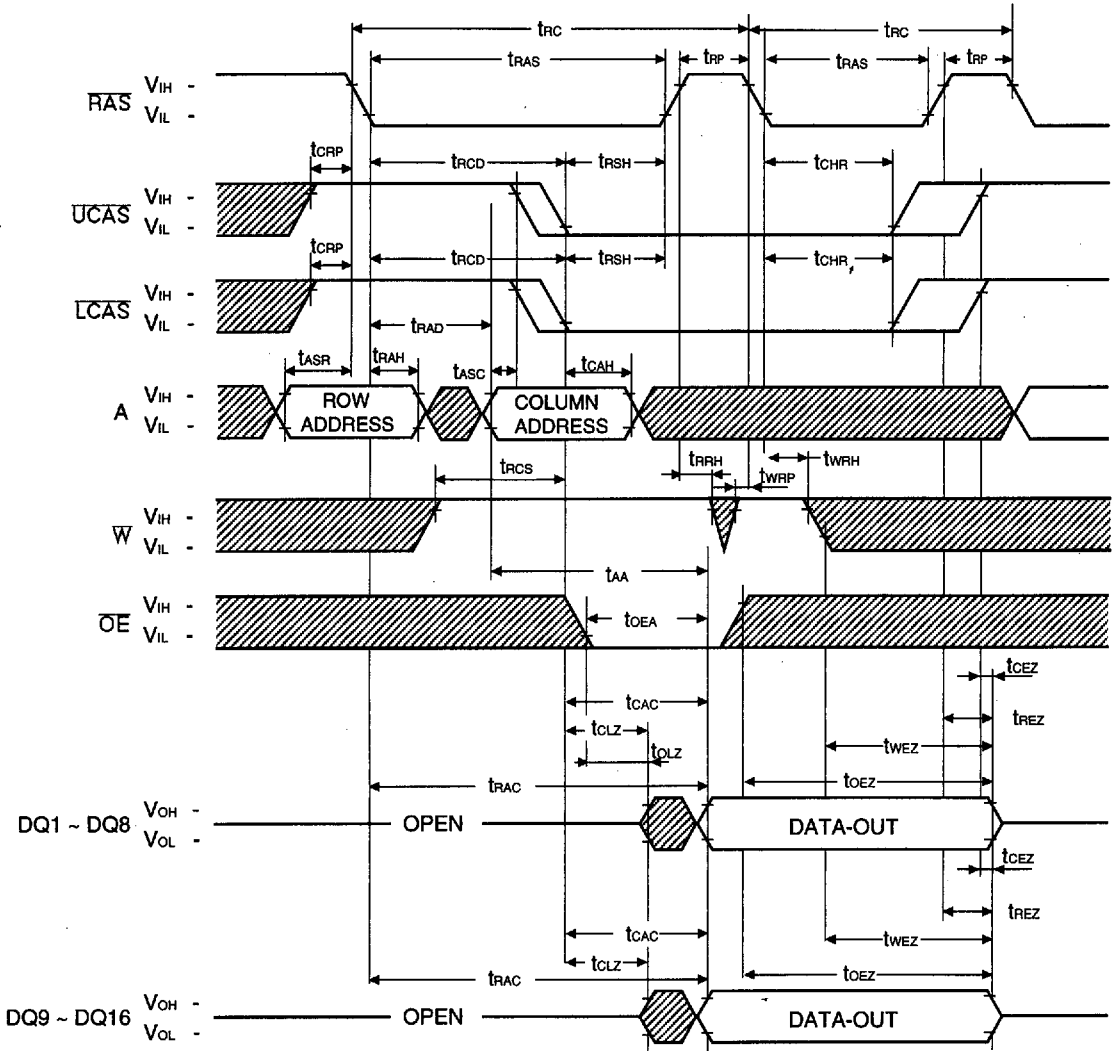
$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ SELF REFRESH CYCLE(LL-version)

NOTE : W, $\overline{\text{OE}}$, A = Don't Care



 Don't Care

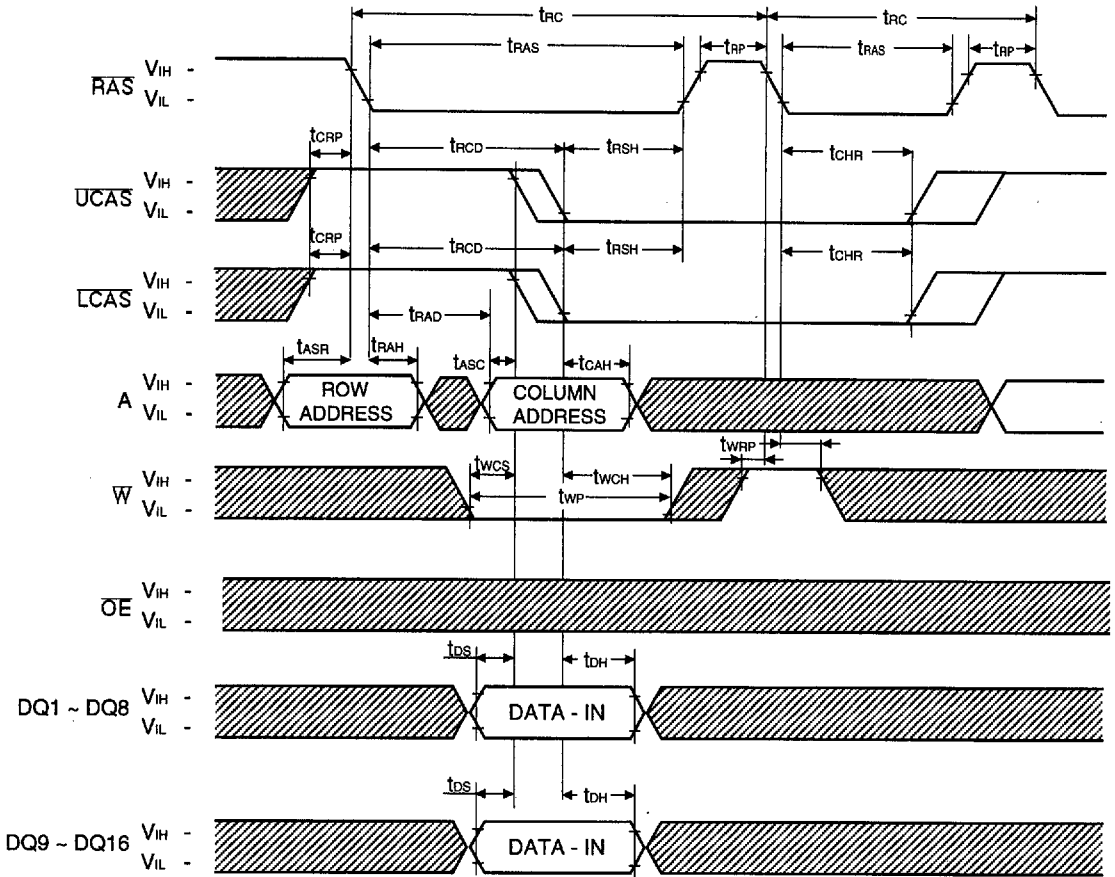
HIDDEN REFRESH CYCLE (READ)



 Don't Care

HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



6

 Don't Care

