Bulletin I25202 rev. A 01/00

International
IOR Rectifier

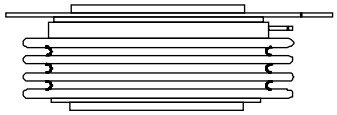
ST1000C..K SERIES

PHASE CONTROL THYRISTORS **Hockey Puk Version**

1473A

Features

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case A-24 (K-PUK)
- High profile hockey-puk



case style A-24 (K-PUK)

Typical Applications

- DC motor controls
- Controlled DC power supplies
- AC controllers

Major Ratings and Characteristics

Parameters		ST1000C..K	Units
$I_{T(AV)}$		1473	A
	@ T_{hs}	55	°C
$I_{T(RMS)}$		2913	A
	@ T_{hs}	25	°C
I_{TSM}	@ 50Hz	20.0	KA
	@ 60Hz	21.2	KA
I^2t	@ 50Hz	2000	KA^2s
	@ 60Hz	1865	KA^2s
$I^2\sqrt{t}$		20000	$KA^2\sqrt{s}$
V_{DRM}/V_{RRM}	range	1200 to 2600	V
t_q	typical	300	µs
T_J	range	-40 to 125	°C

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{RRM}, maximum repetitive peak reverse voltage V	V_{RSM}, maximum non-repetitive peak rev. voltage V	I_{RRM} max. @ T_J = 125°C mA
ST1000C..K	12	1200	1300	100
	16	1600	1700	
	20	2000	2100	
	22	2200	2300	
	24	2400	2500	
	26	2600	2700	

On-state Conduction

	Parameter	ST1000C..K	Units	Conditions		
$I_{T(AV)}$	Maximum average on-state current	1473 (630)	A	180° conduction, half sine wave		
	@ Heatsink temperature	55 (85)	°C	Double side (single side) cooled		
$I_{T(RMS)}$	Maximum RMS on-state current	6540	A	DC @ 25°C heatsink temp. double side cooled		
I_{TSM}	Maximum peak, one-cycle, non-repetitive surge current	20.0	KA	t = 10ms	No voltage reapplied	Sinusoidal half wave, Initial $T_J = T_J$ max.
		21.2		t = 8.3ms		
		17.0		t = 10ms	100% V_{RRM} reapplied	
		18.1		t = 8.3ms		
I^2t	Maximum I^2t for fusing	2000	KA^2s	t = 10ms	No voltage reapplied	
		1865		t = 8.3ms		
		1445		t = 10ms	100% V_{RRM} reapplied	
		1360		t = 8.3ms		
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	20000	$KA^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reapplied		
$V_{T(TO)1}$	Low level value of threshold voltage	0.950	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ max.		
$V_{T(TO)2}$	High level value of threshold voltage	1.024		$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ max.		
r_{t1}	Low level value of on-state slope resistance	0.283	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ max.		
r_{t2}	High level value of on-state slope resistance	0.265		$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ max.		
V_{TM}	Maximum on-state voltage drop	1.80	V	I_{pk} = 3000A, T_J = 125°C, t_p = 10ms sine pulse		
I_H	Maximum holding current	600	mA	T_J = 25°C, anode supply 12V resistive load		
I_L	Typical latching current	1000				

Switching

	Parameter	ST1000C..K	Units	Conditions
di/dt	Maximum non repetitive rate of rise of turned-on current	1000	A/µs	Gate drive 20V, 20Ω, $t_r \leq$ 1µs $T_J = T_J$ max., anode voltage ≤ 80% V_{DRM}
t_d	Typical delay time	1.9	µs	Gate current 1A, di_g/dt = 1A/µs V_d = 0.67% V_{DRM}, T_J = 25°C
t_q	Typical turn-off time	300	A/µs	I_{TM} = 550A, $T_J = T_J$ max, di/dt = 40A/µs, V_R = 50V dv/dt = 20V/µs, Gate 0V 100Ω, $t_p \leq$ 500µs

Blocking

	Parameter	ST1000C..K	Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	500	V/µs	$T_J = T_J$ max., linear to 80% rated V_{DRM}
I_{RRM} I_{DRM}	Maximum peak reverse and off-state leakage current	100	µs	$T_J = T_J$ max., rated V_{DRM}/V_{RRM} applied

Triggering

	Parameter	ST1000C..K		Units	Conditions	
P_{GM}	Maximum peak gate power	16		W	$T_J = T_J$ max., $t_p \leq$ 5ms	
$P_{G(AV)}$	Maximum peak average gate power	3		W	$T_J = T_J$ max., f = 50Hz, d% = 50	
I_{GM}	Maximum peak positive gate current	3.0		A	$T_J = T_J$ max., $t_p \leq$ 5ms	
$+V_{GM}$	Maximum peak positive gate voltage	20		V		
$-V_{GM}$	Maximum peak negative gate voltage	5.0		V		
I_{GT}	DC gate current required to trigger	TYP.	MAX.			
		200	-		T_J = -40°C	
		100	200	mA	T_J = 25°C	Max. required gate trigger / current / voltage are the lowest value which will trigger all units 12V anode-to-cathode applied
		50	-		T_J = 125°C	
V_{GT}	DC gate voltage required to trigger	1.4	-		T_J = -40°C	
		1.1	3.0	V	T_J = 25°C	
		0.9	-		T_J = 125°C	
I_{GD}	DC gate current not to trigger	10		mA	$T_J = T_J$ max.	Max. gate current / voltage not to trigger is the max. value which will not trigger any units with rated V_{DRM} anode-to-cathode applied
V_{GD}	DC gate voltage not to trigger	0.25		V		

Thermal and Mechanical Specifications

	Parameter	ST1000C..K	Units	Conditions
T_J	Max. junction operating temperature range	-40 to 125	°C	
T_{stg}	Max. storage temperature range	-40 to 150		
R_{thJ-hs}	Max. thermal resistance, junction to heatsink	0.042	K/W	DC operation single side cooled
		0.021		DC operation double side cooled
R_{thC-hs}	Max. thermal resistance, case to heatsink	0.006	K/W	DC operation single side cooled
		0.003		DC operation double side cooled
F	Mounting force, ± 10%	24500 (2500)	N (Kg)	
wt	Approximate weight	425	g	
	Case style	A-24 (K-PUK)		See outline table

ΔR_{thJC} Conduction

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction		Rectangular conduction		Units	Conditions
	Single Side	Double Side	Single Side	Double Side		
180°	0.003	0.003	0.002	0.002	K/W	$T_J = T_J$ max.
120°	0.004	0.004	0.004	0.004		
90°	0.005	0.005	0.005	0.005		
60°	0.007	0.007	0.007	0.007		
30°	0.012	0.012	0.012	0.012		

Ordering Information Table

Device Code

ST	100	0	C	26	K	1	
①	②	③	④	⑤	⑥	⑦	⑧

1 - Thyristor

2 - Essential part number

3 - 0 = Converter grade

4 - C = Ceramic Puk

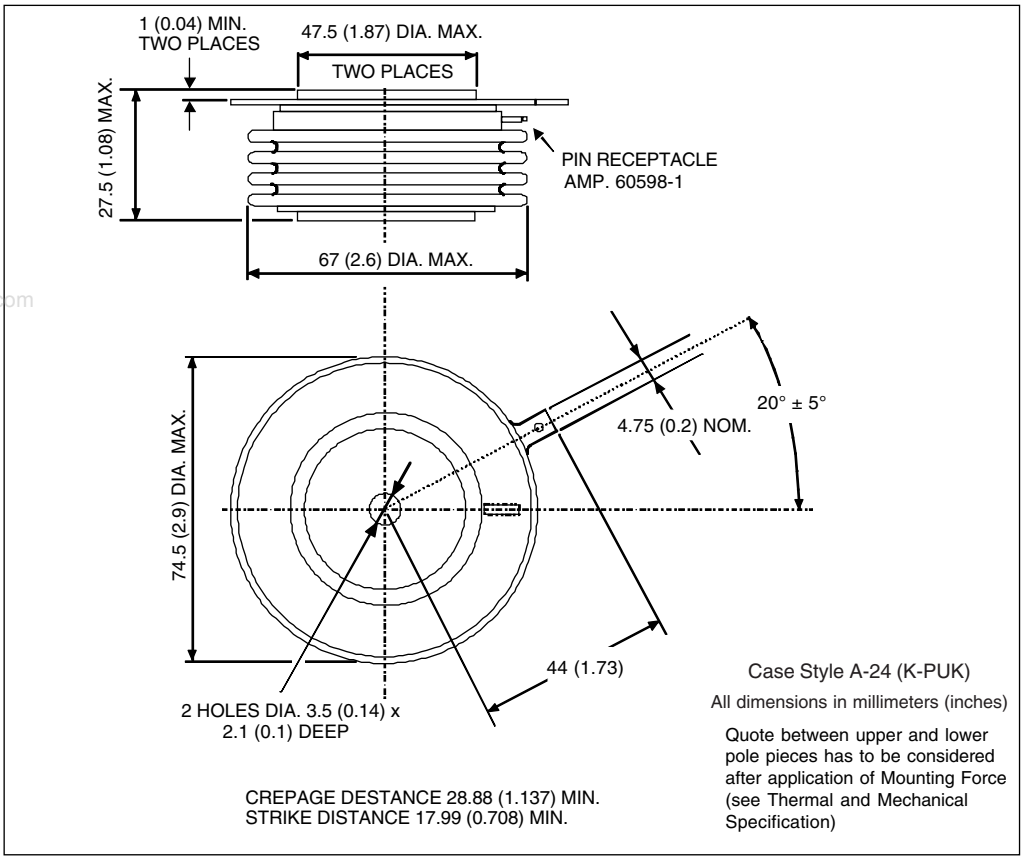
5 - Voltage code: Code x 100 = V_{RRM} (See Voltage Ratings Table)

6 - K = Puk Case A-24 (K-PUK)

7 - 0 = Eyelet terminals (Gate and Auxiliary Cathode Unsoldered Leads)
1 = Fast-on terminals (Gate and Auxiliary Cathode Unsoldered Leads)
2 = Eyelet terminals (Gate and Auxiliary Cathode Soldered Leads)
3 = Fast-on terminals (Gate and Auxiliary Cathode Soldered Leads)

8 - Critical dv/dt: None = 500V/µsec (Standard selection)
L = 1000V/µsec (Special selection)

Outline Table



Case Style A-24 (K-PUK)

All dimensions in millimeters (inches)

Quote between upper and lower pole pieces has to be considered after application of Mounting Force (see Thermal and Mechanical Specification)

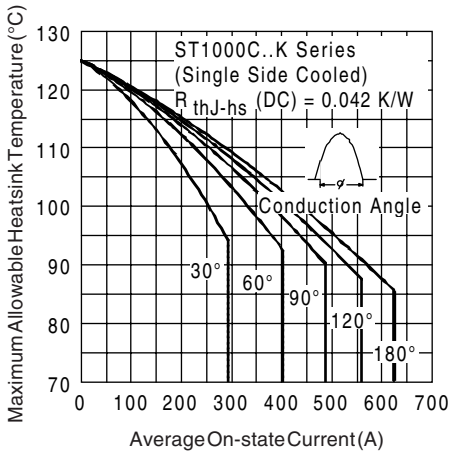


Fig. 1 - Current Ratings Characteristics

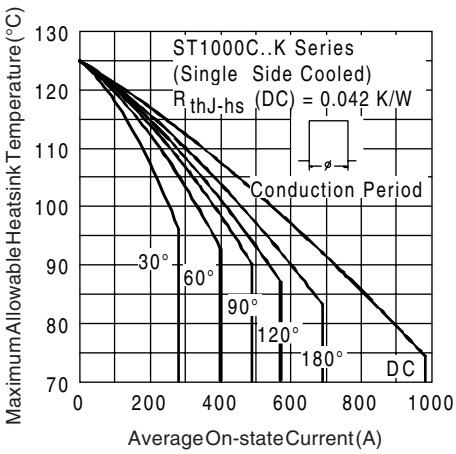


Fig. 2 - Current Ratings Characteristics

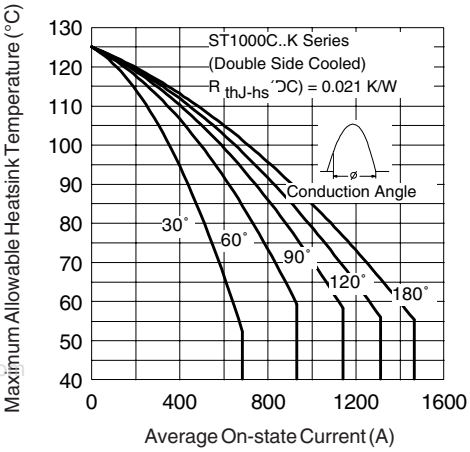


Fig. 3 - Current Ratings Characteristics

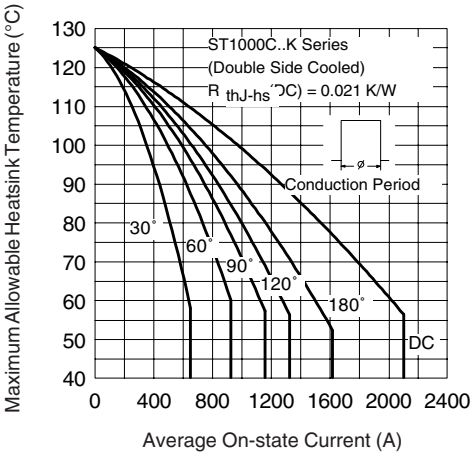


Fig. 4 - Current Ratings Characteristics

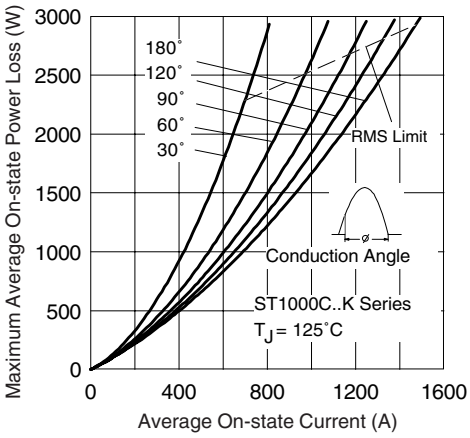


Fig. 5- On-state Power Loss Characteristics

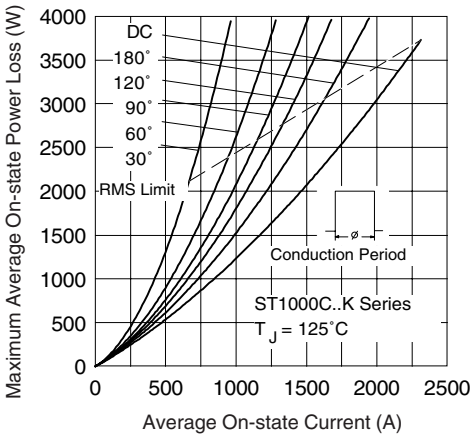


Fig. 6- On-state Power Loss Characteristics

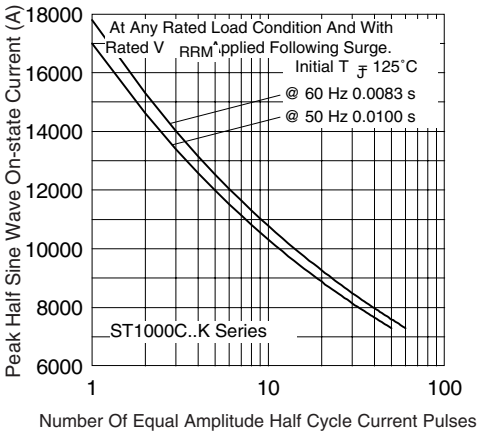


Fig. 7 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

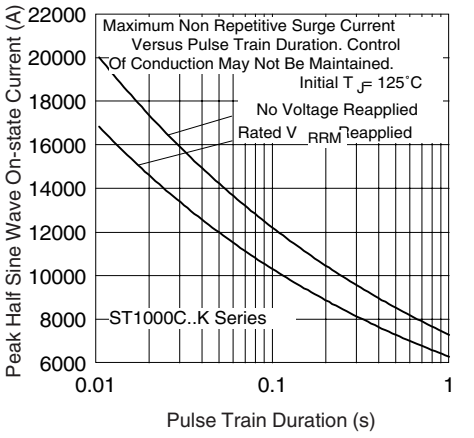


Fig. 8 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

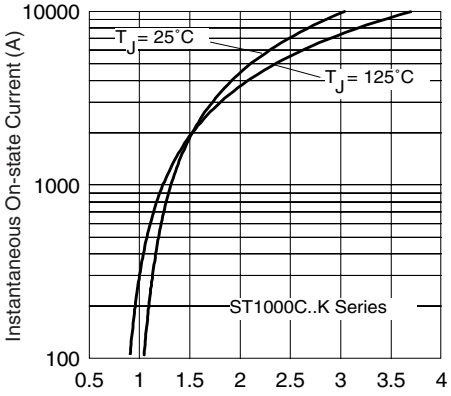


Fig. 9 - On-state Voltage Drop Characteristics

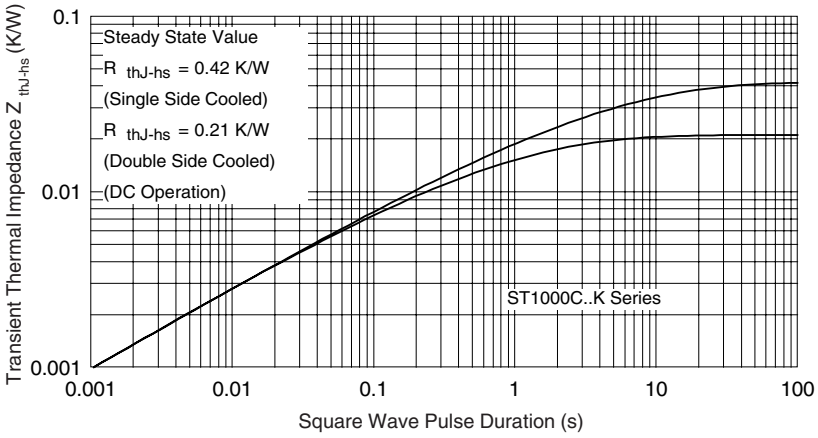


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

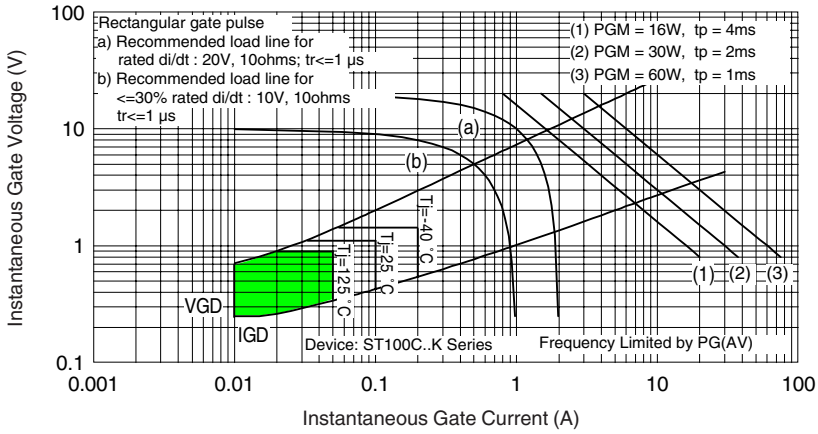


Fig. 11 - Gate Characteristics