MOTOROLA
SEMICONDUCTOR ▄▄▄▄▄▄▄
TECHNICAL DATA

Advance Information
H4C SERIES™ CMOS ARRAYS
and the CDA™ ARCHITECTURE

**H4C
SERIES**

**HIGH PERFORMANCE
TRIPLE LAYER METAL**

**SUB−MICRON
CMOS ARRAYS**

The H4C Series is Motorola's highest performance, sub-micron family of CMOS arrays with a typical gate delay of 365 picoseconds and low power dissipation of only 3µW/gate/MHz. The H4C Series triple-layer metal arrays range in density from 18,080 to 317,968 gates with package pins counts ranging from an 80 QFP to a 447 PGA, see Table 1.

The channelless arrays of the H4C Series can be used to build Motorola's Customer Defined Array™ (CDA™) in which large, complex functions are diffused into the array structure. The CDA architecture combines into one technology the benefits of high-performance complex functions (usually associated with custom cells) with the fast turnaround and lower-cost manufacture of gate arrays. Motorola's first diffused functions are single- and dual-port SRAMs (user compilable up to 256Kbits) and in development is an embedded MC68000 microprocessor core.
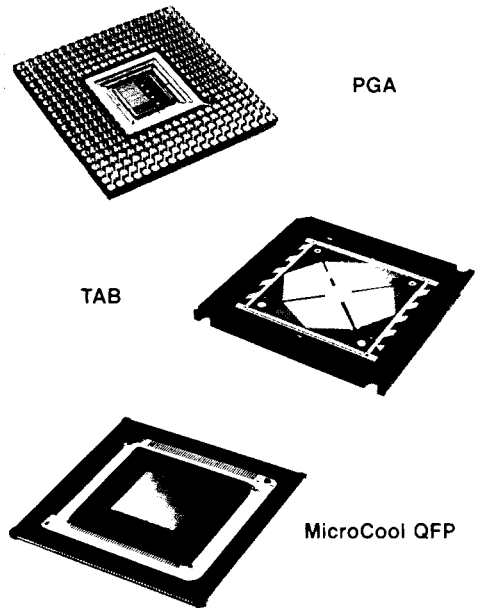
Recent additions to the H4C Series feature list include three new arrays (H4C018, H4C267, and H4C318), new packages, several new macrocells, 3.3 volt I/O buffers, and new design tools for greater design efficiency.

PGA

TAB

MicroCool QFP

TYPICAL H4C SERIES PACKAGES

H4C Series™ Features
* 18,080 to 317,968 available gates
* Channelless, sea-of-gates and diffused CDA™ architectures
* 0.7 micron effective gate length
* Triple-layer metal for signal routing and power distribution
* 365 ps typical gate delay (NAN2, fanout=2, with interconnect metal)
* Low power consumption: 3µW/gate/MHz for internal macrocells
* 3.3 V and 5.0 V CMOS and TTL configurable I/O cells up to 48 mA.
* Up to 256 Kbits available in compiled, fully-diffused SRAMs with BIST ports
* Fully-digital PLL macro functions for up to 75 MHz clocks
* BIST, JTAG boundary scan, and ESSD/LSSD scan
* High-performance packaging

Table 1. H4C Series Arrays

Array Name	Available Gates*	Die Size (mil/side)	Core Size		Die Pads Wirebond	Package Pins
			x (µm)	y (µm)		
H4C018	18,080	189	3200	3164	136	80-120
H4C027	27,048	217	3920	3864	160	80-128
H4C035	35,392	239	4480	4424	176	80-160
H4C057	57,368	287	5680	5656	216	80-208
H4C086	86,956	337	6960	6916	256	120-232
H4C123	123,136	391	8320	8288	304	160-299
H4C161	161,364	438	9520	9492	344	160-304
H4C195	195,452	476	10480	10444	376	160-375
H4C267	266,832	545	12240	12208	432	304, 447
H4C318	317,968	589	13360	13328	464	447

*Actual usable gates varies with design.

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PRODUCT DESCRIPTION

HIGH-PERFORMANCE TECHNOLOGY

The fabrication of the H4C Series CMOS arrays uses a 0.7 μm L_{eff} channel, self-aligned, twin tub process, Figure 1. Both n-type and p-type well implants are driven together to form deep, balanced wells which improve short n-channel transistor performance. Also, a lightly doped drain (LDD) diffusion is used to reduce hot carrier injection effects caused by a high electric field in the short channel transistors. A highly-reliable multi-layer metal structure is achieved by a planarization technique using tapered contacts and vias.

The combination of a small feature size and a thin oxide coating provides both high gate density and low power dissipation. The typical power dissipation for internal gates with a load of 0.06 pF (fanout = 1) is only 3 μW/gate/MHz.

The quality of Motorola's CMOS process is evident in the low 2.54 worst- to best-case PVT (process/voltage/temperature) ratio used in derating propagation delays. In comparison, some ASIC vendors can only achieve a ratio of 3 to 4. This means that Motorola's process is highly controlled and predictable.
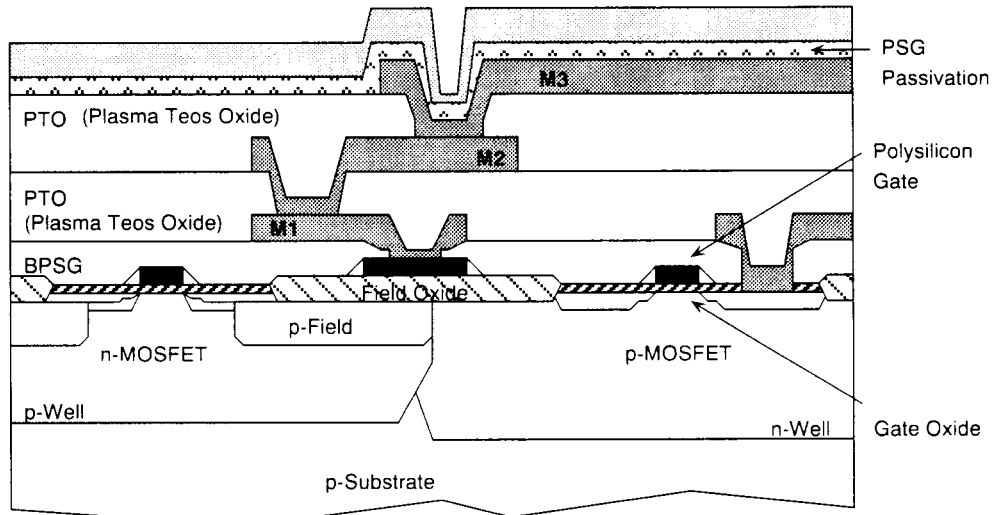

Figure 1. H4C Series CMOS Device Cross-Section

The H4C Primary Cell

The primary cell consists of four pairs of n- and p-type transistors. The transistors are the same size to optimize both gate density and routability. The primary cell is used to configure all of the H4C Series macrocells. Figure 2 shows half of a

primary cell (two p-type and two n-type transistors) configured as a 2-input NAND gate (NAN2). The typical gate delay for a 2-input NAND at 25°C, 5.0V is 365 picoseconds with a fanout of 2, including interconnect metal.
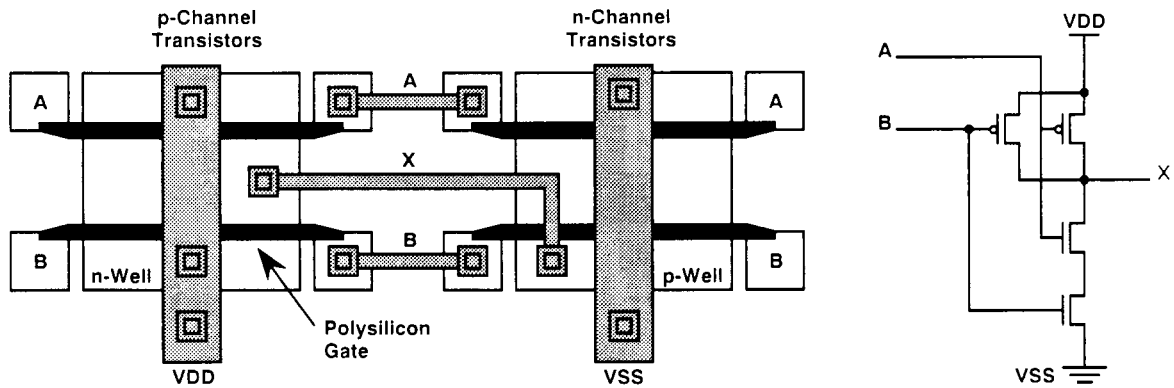

Figure 2. 2-Input NAND Gate Implementation Within Half an Eight Transistor Primary Cell

Triple-Layer Metal Routing

A triple-layer metal (TLM) structure provides superior routing access to configure and connect macrocells and distribute power and ground, see Figure 3.
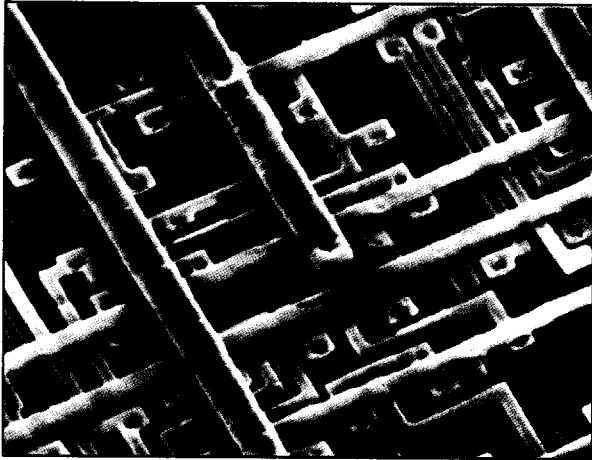

Figure 3. Triple-Layer Metallization (Photo)

One important benefit of TLM routing is improved routability for higher gate utilization. TLM also provides improved clock distribution by moving the clock signals to the top metal layer where the capacitance per unit length is at least 30% less than the lower metal layers due to the thicker dielectric layer. In addition, TLM's shorter interconnect lines reduces delays by 10% versus two-layer metal routing and improves power distribution.

GATE ENSEMBLE™ PLACE AND ROUTE - The layout of the routing layers is accomplished with Cadence's Gate Ensemble place and route system. Some of Gate Ensemble's capabilities include timing driven layout (net and path constrained), soft/firm grouping of macros, clock-tree synthesis, incremental layout changes, and highly accurate distributed RC calculations. In addition, the power-bus router automatically uses single-, double-, or quadruple-width power tracks to optimize performance while minimizing spent routing channel.

PrediX™ FLOORPLANNING - Motorola has developed PrediX, an efficient floorplanning tool that is easy to learn and use. PrediX enables you to define groups and regions, to floorplan your design to optimize die area and data path performance. PrediX has a graphical user interface which enhances productivity.

THE H4C SERIES LIBRARY

The H4C Series library contains a complete suite of I/O functions, combinatorial and sequential functions, and a growing list of megafunctions. Many basic logic functions come in several versions including standard/high-drive capacity and scan/non-scan to provide you with the widest choice of functions.

Also, the mature HDC Series library is fully upward compatible with the H4C Series library.

I/O Functions

Motorola's I/O cell is configurable into any I/O function including inputs, outputs, bidirectionals, oscillators, JTAG I/O buffers, and power and ground connections. Varieties of I/O functions include 3.3 volt, 5.0 volt, CMOS-level, TTL-level, 3-state, open drain and Schmitt triggered I/O, see Figure 4.

3.3V I/O BUFFERS - Motorola's new 3.3V I/O buffers are specially designed for low-voltage applications to reduce power consumption while maintaining a high level of performance.
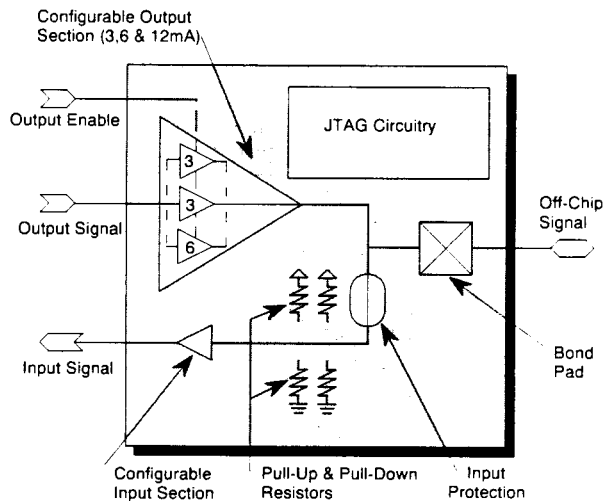

Figure 4. H4C Series I/O Cell

JTAG Boundary Scan I/O - The I/O cells of the H4C Series arrays have JTAG logic already built-in to minimize the impact on performance and gate overhead. An application note (AN1500) will be available for designing with JTAG, contact factory for availability.

SELECTABLE OUTPUT DRIVE - For increased output current capacity, up to 4 output drivers may be paralleled from adjacent I/O cells to deliver as much as 48 mA of current to a single output or bidirectional output pin. (JTAG outputs and bidirectionals are not parallelable, but have higher current capacity versions available.) Unused output drivers may also be used to drive highly loaded internal signals such as clock networks.

SLEW RATE CONTROL - Slew rate control outputs are available to reduce system noise due to over- and undershoot of output signals caused by fast rise and fall times. All 4 and 8 mA output buffers have a moderate (10%) and slow (30%) slew control version.

OSCILLATORS - Three different oscillator I/O macros are available on the H4C Series arrays: non-inverting buffer, clock buffer, and Schmitt trigger versions. These macros can be configured for ceramic resonators from 32 KHz to above 60 MHz with quartz crystals.

Macrocells

Internal macrocells include both combinatorial and sequential functions with complexities ranging from simple logic gates to larger functions such as adders and decoders. A summary of internal macrocell functionality is shown in Table 2.

Table 2. Summary of Macrocells

Library Functions	# of Macros
AND	7
NAND	12
OR	7
NOR	12
EXOR	8
EXNOR	5
A/N, A/O, O/N, O/A	26
Inverting Buffer	12
Non-Inverting Buffer	13
3-State Buffer	8
Schmitt Trigger Buffer	4
D Flip-Flop	44
JK Flip-Flop	12
Toggle Flip-Flop	4
Latch	26
Multiplexer	20
Decoder	8
Arithmetic	16
Misc.	10

Many of the macrocells include high-drive, balanced slew rate, and complementary output versions. The benefit of high-drive over standard drive is a greater fanout capacity with reduced impact on propagation delay, see Figure 5.
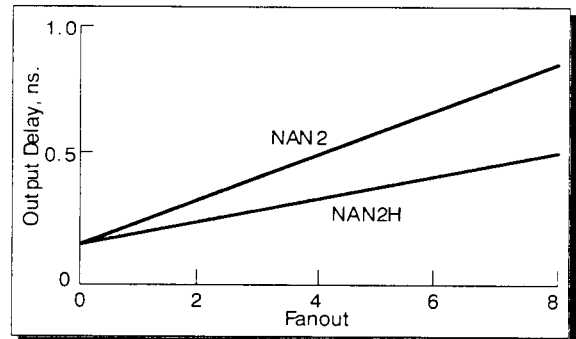
Figure 5. Output Delay of High-Drive (NAN2H) vs. Standard-Drive (NAN2)

Balanced slew rate versions of macrocells provide near symmetrical rise and fall slew rates.

Also, ESSD/LSSD (see page 6) scan macrocells are available for designs requiring internal scan for testability.

Special Functions

Special functions include all non-standard logic functions designed for a specific use. Examples of special functions include PLL, SRAM, BIST, and JTAG functions.

Table 3. Summary of Special Functions

Special Function	# of Macros
Metallized SRAMs	24
Diffused SRAMs	user defined
BIST	5
PLL	4
Internal JTAG	7

METALLIZED SRAMS - The H4C Series library includes a family of asynchronous single, dual, and quad-port metallized SRAM blocks up to 2304 bits. Single-port SRAMs are designed for low-power and dual-port SRAMs are optimized for high-speed.

Table 4. Sizes of Metallized SRAMs

Single-Port, Low-Power	Dual-Port, High-Speed	Quad-Port
8x18	8x9	16x18
16x18	8x18	16x36
16x36	8x36	32x18
32x8	8x72	32x36
32x18	16x9	
32x36	16x18	
64x18	16x36	
64x36	16x72	
	32x9	
	32x18	
	32x36	
	32x72	

DIFFUSED SRAMS - Synchronous, single- and dual-port, diffused SRAMs up to 256 Kbits are user definable when using the Memorist SRAM Compiler. Presently Memorist is available as a service through Motorola's Regional Design Centers (RDCs). Memorist generates several versions of a given SRAM size, each with different performance, gate counts, and physical configurations. The diffused SRAMs also feature BIST ports to simplify your design. See Table 5 for a comparison of metal and diffused SRAMs.

Table 5. Comparison of Metallized and Diffused SRAMs

Feature	Metal RAM	Diffused RAM
Technology	HDC, H4C	H4C
Strobe	asynchronous	synchronous
Ports	1, 2, 4	1, 2
Max. Size	2.3 Kbits	256 Kbits
Gate Density*	~3 gates/bit	~1 gate/bit
Construction	gate array	diffused
Routing Impact	M2 part, M3 open	M3 restricted
Availability	fixed sizes	user defined
BIST Ports	no	yes
Access Time†	14.8 ns	11.1 ns

* Average gate densities, actual gate count varies.

† Single-port, 64x36 SRAM at 135°C, 4.5V, worst process.

SPECIAL DESIGN FEATURES

The H4C Series offers solutions to many of today's design problems. The increasing complexities of applications places higher demands on performance, clock skew management, testability, I/O capability and workstation based design environments. This section describes some of the special features of the H4C Series that provide solutions to these issues.

The CDA Architecture

The H4C Series can be implemented in either a conventional gate array or a Customer Defined Array (CDA). The CDA was developed to satisfy the most demanding requirements for high performance applications.

The CDA is an architectural hybrid, taking the best of both gate array and standard cell methodologies, see Figure 6.
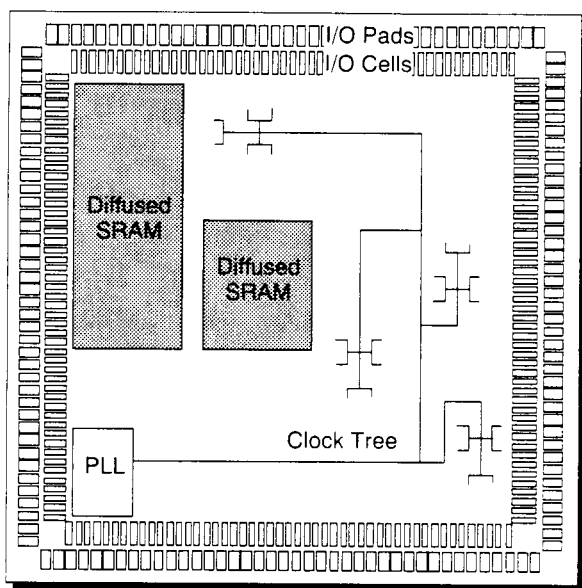
Figure 6. The CDA Concept: Large Diffused Functions Within a Gate Array

As in the standard cell methodology, the CDA can use large diffused functions to provide a higher-level of performance and functionality which is difficult to attain in gate array implementations. On the other hand, the CDA exploits the cycle time and low cost of manufacturing usually associated with gate arrays, by using fixed I/O ring and die sizes.

The CDA, therefore, combines high-performance and complex functions with cost-efficient manufacturing.

CDA Benefits:
* System-level designs on a single chip
* Diffused megafunctions for optimal performance and silicon area
* Fixed I/O locations and die size minimizes manufacturing costs and turnaround time
* Re-usable base arrays for fast, cost-effective redesigns

Design for Testability

The time and cost to test an ASIC increases exponentially as the complexity and size of the ASIC grows. Using a design for test (DFT) methodology allows large, complex ASICs to be efficiently and economically tested.

Motorola supports several DFT methodologies, including ESSD/LSSD scan, JTAG boundary scan, and BIST for memories. To take full advantage of these DFT methodologies, Motorola has supported the development of a low-cost, high-speed scan tester.

ESSD/LSSD SCAN - Motorola offers Edge Sensitive Scan Design and Level Sensitive Scan Design (ESSD/LSSD) versions of flip-flops, latches and other functions in the H4C Series library. The Mustang™ ATPG (Automatic Test Pattern Generation) tool, available with Motorola's OACS™ CAD system, performs fault grading and test vector generation on ESSD/LSSD designs.

AUTOMATIC SCAN STITCHING - Using the Synopsys Test Compiler™ scan stitching feature saves you time in your design cycle by inserting scan macros into your design and linking the scan chains automatically.

JTAG BOUNDARY SCAN - Motorola has specially designed JTAG I/O and JTAG control macrocells to conform to the IEEE 1149.1 JTAG boundary scan standard. The JTAG I/O macrocells are designed to optimize performance and minimize silicon overhead by embedding all sequential and multiplexing logic within the I/O sites of the array.

BUILT-IN SELF TEST FOR MEMORY - We offer two versions of Built-in-Self-Test (BIST) for memories.

"Simplified" BIST is relatively easy to implement, requires few gates, and can achieve fault coverage up to 99%.

"Comparator" BIST, on the other hand, is more complicated to design and requires more gate overhead, but can usually achieve 100% fault coverage.

Each type of BIST may be used to test either metallized or diffused SRAMs. Application note (AN1502) is available to assist you in using either BIST versions in your design.

THE ISS2000™ TESTER - In 1988 Motorola entered into partnership with Schlumberger Technologies', ATE Division, to develop the ISS2000 tester™. The ISS2000 is a high pin count, scan-based, cost-efficient tester for ASICs, and features up to 1024 signal pins with 64 scan channels that supports scan data rates up to 40MHz. The ISS2000 also supports a high-speed clock burst pin to take full advantage of BIST circuitry for testing SRAMs.

Clock Distribution and Management

ASICs are becoming an integral part of system design and are regularly found interfacing with multiple chips including other ASICs, microprocessors and memories. Optimizing performance of such systems depends on maximizing communication between chips using synchronous interfaces. Clock skew control and distribution, both on-chip and between chips, is of critical importance. Motorola's solution to clock management is to balance clock trees to control skew on-chip and a digital PLL to control clock skew between ASICs, see Figure 7.

CLOCK TREE SYNTHESIS - Motorola offers clock tree synthesis during layout to build balanced clock distribution networks or clock trees. Clock trees balance on-chip clock load requirements so that the clock signal arrives at all sequential elements at the same time. Clock trees have a minimal effect on design routability, critical data paths, timing driven layout and floorplanning.

PHASE LOCKED LOOP (PLL) - To control chip-to-chip clock skew problems Motorola has developed a unique, fully digital PLL. The PLL synchronizes internal ASIC clocks with the external system clock up to 75MHz. The PLL is configured from three specially designed macrocells: a phase detector, a counter, and a delay line. There are two delay lines to choose from depending on your clock network.
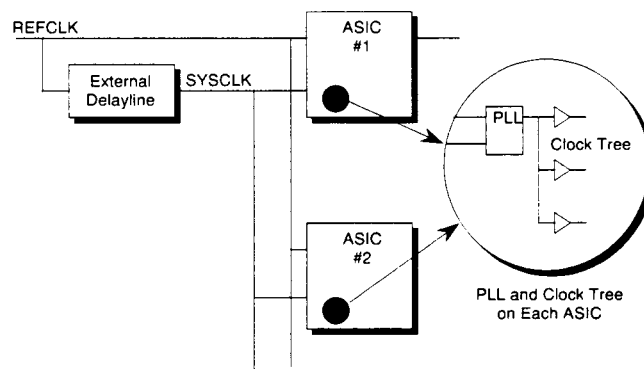

Figure 7. Example of Clock Management of Multiple ASICs using the Digital PLL and Clock Tree Distribution

THE MACROCELL LIBRARY

The following tables detail the elements which make up the H4C Series library. The elements are organized into five categories Input/Output and Power/Ground Macrocells, Internal Macrocells, Soft/Firm/PLL Clock Skew Management Macrocells, JTAG Macrocells, and Metallized RAM Macrocells.

Bold Macros = New Macros in OACS 2.1

S = Sections used (I/O macros)
G = Physical gate count (Internal Macrocells)
R = Recommended Use Internal Macros (**X**)
These Macros will be upward compatible with OACS releases after 2.1 and new technologies.

Note: All Peripheral macros are upward compatible.

#	ARRAYS PERIPHERAL MACROS		S
	INPUTS		
1	ICI	CMOS, Inverting Input	1/0
2	BICI	CMOS, Inverting Input (Input part of Bidirectional)	1/0
3	ICIH	CMOS, Inverting, Clock Driver Input	1/1
4	ICN	CMOS, Non-inverting Input	1/0
5	BICN	CMOS, Non-inverting Bidirectional Input	1/0
6	ICNH	CMOS, Non-inverting Clock Driver Input	1/1
7	ISN	CMOS Schmitt, Non-inverting Input	1/0
8	BISN	CMOS Schmitt, Non-inverting Bidirectional Input	1/0
9	ISNH	CMOS Schmitt, Non-inverting Clock Driver Input	1/1
10	ITN	TTL, Non-inverting Input	1/0
11	BITN	TTL, Non-inverting Bidirectional Input	1/0
12	ITNH	TTL, Non-inverting Clock Driver Input	1/1
13	ITSN	TTL Schmitt, Non-inverting Input	1/0
14	BITSN	TTL Schmitt, Non-inverting Input (Input part of Bidirectional)	1/0
15	ITSNH	TTL Schmitt, Non-inverting Clock Driver Input	1/1
	OUTPUTS		
1	ON2	3mA Standard Output	0/1
2	ON4	6mA Standard Output	0/1
3	*ON4L*	*6mA (3.3 V) Standard Output*	*0/1*
4	ON8	12mA Standard Output (Can be paralleled up to 4X = 48 mA)	0/1
5	ON4S2	6mA Standard Output with Slew Control	0/1
6	ON8S2	12mA Standard Output with Slew Control (Can be paralleled up to 4X = 48 mA)	0/1
7	ON4S4	6mA Standard Output with Slew Control	0/1
8	ON8S4	12mA Standard Output with Slew Control (Can be paralleled up to 4X = 48 mA)	0/1
9	ON2T	3mA 3-State Output	0/1
10	BON2T	3mA 3-State Bidirectional Output	0/1
11	ON4T	6mA 3-State Output	0/1
12	*ON4TL*	*6mA (3.3 V) 3-State Output*	*0/1*
13	BON4T	6mA 3-State Bidirectional Output	0/1
14	*BON4TL*	*6mA (3.3 V) 3-State Bidirectional*	*0/1*
15	ON8T	12mA 3-State Output (Can be paralleled up to 4X = 48 mA)	0/1
16	BON8T	12mA 3-State Bi-directional Output (Can be paralleled up to 4X = 48 mA)	0/1
17	ON4TS2	6mA 3-State Output with Slew Control	0/1
18	BON4TS2	6mA 3-State Output with Slew Control (Output part of Bidirectional)	0/1
19	ON8TS2	12mA 3-State Output with Slew Control (Can be paralleled up to 4X = 48 mA)	0/1
20	BON8TS2	12mA 3-State Output with Slew Control (Output part of Bidirectional) (Can be paralleled up to 4X = 48 mA)	0/1
21	ON4TS4	6mA 3-State Output with Slew Control	0/1

#	ARRAYS PERIPHERAL MACROS		S
	OUTPUTS (Continued)		
22	BON4TS4	6mA 3-State Output with Slew Control (Output part of Bidirectional)	0/1
23	ON8TS4	12mA 3-State Output with Slew Control (Can be paralleled up to 4X = 48 mA)	0/1
24	BON8TS4	12mA 3-State Output with Slew Control (Output part of Bidirectional) (Can be paralleled up to 4X = 48 mA)	0/1
25	ON2OD	3mA (Sink) Open-Drain Output	0/1
26	BON2OD	3mA (Sink) Open-Drain Output (Output part of Bidirectional)	0/1
27	ON4OD	6mA (Sink) Open-Drain Output	0/1
28	BON4OD	6mA (Sink) Open-Drain Output (Output part of Bidirectional)	0/1
29	ON8OD	12mA (Sink) Open-Drain Output (Can be paralleled up to 4X = 48 mA)	0/1
30	BON8OD	12mA (Sink) Open-Drain Output (Output part of Bidirectional) (Can be paralleled up to 4X = 48 mA)	0/1
31	ON4ODS2	6mA (Sink) Open-Drain Output W/Slew Control	0/1
32	BON4ODS2	6mA (Sink) Open-Drain Output W/Slew Control (Output part of Bidirectional)	0/1
33	ON8ODS2	12mA (Sink) Open-Drain Output W/Slew Control (Can be paralleled up to 4X = 48 mA)	0/1
34	BON8ODS2	12mA (Sink) Open-Drain Output with Slew Control (Output part of Bidirectional) (Can be paralleled up to 4X = 48 mA)	0/1
35	ON4ODS4	6mA (Sink) Open-Drain Output W/Slew Control	0/1
36	BON4ODS4	6mA (Sink) Open-Drain Output with Slew Control (Output part of Bidirectional)	0/1
37	ON8ODS4	12mA (Sink) Open-Drain Output W/Slew Control (Can be paralleled up to 4X = 48 mA)	0/1
38	BON8ODS4	12mA (Sink) Open-Drain Output with Slew Control (Output part of Bidirectional) (Can be paralleled up to 4X = 48 mA)	0/1

Note: Any of the "B" prefix Outputs may be used with any of the "B" prefix Inputs (above) to form a unique Bidirectional combination (with or without any of the four "pull" resistors).

	OSCILLATORS		
1	OSCPB	Standard Oscillator	2/2
2	OSCPHB	Oscillator with Clock Driver Buffer	2/2
3	OSCPSB	Oscillator with Schmitt Trigger Buffer	2/2

	RESISTORS		
1	PUL	Pull-Up, Low current/speed Resistor	N/A
2	PUH	Pull-Up, High current/speed Resistor	N/A
3	PDL	Pull-Down, Low current/speed Resistor	N/A
4	PDH	Pull-Down, High current/speed Resistor	N/A

Note: Any of these four resistors may be used with any of the above Inputs.

#	PERIPHERAL MACROS	
	POWER & GROUND MACROS	
1	BOTHVDD	Core & I/O Supply Pad
2	BOTHVSS	Core & I/O Ground Pad
3	BUSTIE	Bus Tie
4	INPVDD	Core Supply Pad
5	INPVSS	Core Ground Pad
6	OUTVDD	I/O Supply Pad
7	OUTVSS	I/O Ground Pad
	BUS SEGMENTATION MACROS	
1	ISO	Isolation to Power
2	ISOP	Isolation to Shared Power
3	OSVDDL	Left Supply End
4	OSVDDR	Right Supply End
5	OSVSSL	Left Ground End
6	OSVSSR	Right Ground End
7	OUTSVDDL	Supply Left Cut
8	OUTSVDDR	Supply Right Cut
9	OUTSVSSL	Ground Left Cut
10	OUTSVSSR	Ground Right Cut
11	OVDDL	Left Supply End with Pad
12	OVDDR	Right Supply End with Pad
13	OVSSL	Left Ground End without Pad
14	OVSSR	Right Ground End without Pad

#	INTERNAL MACROS		G	R
	AND GATES			
1	AND2	2-Input AND Gate	2	X
2	AND2H	2-Input AND Gate, 2X Drive	2	X
3	AND3	3-Input AND Gate	2	X
4	AND3H	3-Input AND Gate, 2X Drive	3	X
5	AND4	4-Input AND Gate	3	X
6	AND4H	4-Input AND Gate, 2X Drive	3	X
7	AND8H	8-Input AND Gate, 2X Drive	6	X
	NAND GATES			
1	NAN2	2-Input NAND Gate	1	X
2	NAN2H	2-Input NAND Gate, 2X Drive	2	X
3	NAN2B	2-Input NAND Gate, Balanced	2	X
4	NAN3	3-Input NAND Gate	2	X
5	NAN3H	3-Input NAND Gate, 2X Drive	3	X
6	NAN4	4-Input NAND Gate	2	X
7	NAN4H	4-Input NAND Gate, 2X Drive	4	X
8	NAN5	5-Input NAND Gate	4	X
9	NAN5H	5-Input NAND Gate, 2X Drive	5	X
10	NAN6CH	6-Input NAND Gate, 2X Drive, 1X Complementary Output	6	X
11	NAN8H	8-Input NAND Gate, 2X Drive	7	X
12	NAN8CH	8-Input NAND Gate, 2X Drive, 1X Complementary Output	7	
	OR GATES			
1	OR2	2-Input OR Gate	2	X
2	OR2H	2-Input OR Gate, 2X Drive	2	X
3	OR3	3-Input OR Gate	2	X
4	OR3H	3-Input OR Gate, 2X Drive	3	X
5	OR4	4-Input OR Gate	3	X
6	OR4H	4-Input OR Gate, 2X Drive	3	X
7	OR8H	8-Input OR Gate, 2X Drive	8	X

#	INTERNAL MACROS		G	R
	NOR GATES			
1	NOR2	2-Input NOR Gate	1	X
2	NOR2H	2-Input NOR Gate, 2X Drive	2	X
3	NOR2B	2-Input NOR Gate, Balanced	2	X
4	NOR3	3-Input NOR Gate	2	X
5	NOR3H	3-Input NOR Gate, 2X Drive	4	X
6	NOR4	4-Input NOR Gate	4	X
7	NOR4H	4-Input NOR Gate, 2X Drive	4	X
8	NOR5	5-Input NOR Gate	4	X
9	NOR5H	5-Input NOR Gate, 2X Drive	5	X
10	NOR6CH	6-Input NOR Gate, 2X Drive, 1X Complementary Output	6	X
11	NOR8H	8-Input NOR Gate, 2X Drive	7	X
12	NOR8CH	8-Input NOR Gate, 2X Drive, 1X Complementary Output	7	
	EXCLUSIVE OR & EXCLUSIVE NOR GATES			
1	EXNOR	2-Input Exclusive NOR	4	
2	EXNORH	2-Input Exclusive NOR, 2X Drive	4	
3	EXNORA	2-Input Ex NOR, Unbuffered Inputs	3	X
4	EXNOR3	3-Input Exclusive NOR	7	
5	EXNOR3H	3-Input Exclusive NOR, 2X Drive	8	X
6	EXOR	2-Input Exclusive OR	4	
7	EXORH	2-Input Exclusive OR, 2X Drive	4	
8	EXORA	2-Input Exclusive OR, Unbuffered Inputs	3	X
9	EXOR3	3-Input Exclusive OR	7	
10	EXOR3H	3-Input Exclusive OR, 2X Drive	8	X
11	EXOR4	4-Input Exclusive OR	9	
12	EXOR4H	4-Input Exclusive OR, 2X Drive	10	X
13	EXOR9H	9-Input Exclusive OR	24	
	AND/NOR, AND/OR, OR/NAND, & OR/AND GATES			
1	ANDOI22	2-Input AND + 2-Input NOR, into 2-Input NOR	3	X
2	ANDOI22H	2-Input AND+2-Input NOR,→2-Input NOR 2X Drive	4	X
3	AO21H	2-Input AND, 1-Wide,→2-Input OR, 2X	3	X
4	AO22H	2-Input AND, 2-Wide, into 2-Input OR, 2X	3	X
5	AO321H	3,2,1-input AND-OR Gate, 2X Drive	5	X
6	AO4321H	4,3,2,1-input AND-OR Gate, 2X Drive	8	X
7	AOI21	2-Input AND, 1-Wide, into 2-input NOR	2	X
8	AOI21H	2-Input AND, 1-Wide, into 2-input NOR, 2X	3	X
9	AOI211	2-Input AND, 1-Wide, into 3-input NOR	2	X
10	AOI211H	2-Input AND, 1-Wide, into 3-input NOR, 2X	4	X
11	AOI22	2-Input AND, 2-Wide, into 2-input NOR	2	X
12	AOI22H	2-Input AND, 2-Wide, into 2-input NOR, 2X	4	X
13	MAJ3	2 of 3 Majority, Inverting Output	3	
14	MAJ3H	2 of 3 Majority, Inverting Output, 2X Drive	4	
15	NR24	2-Input, 4-wide, NOR (Partial Product Generator)	4	
16	OA21H	2-Input OR, 1-Wide, into 2-input AND, 2X	3	X
17	OA22H	2-Input OR, 2-Wide, into 2-input AND, 2X	3	X
18	OA211H	2-Input OR, 1-Wide, into 3-input AND, 2X	3	
19	OAI21	2-Input OR, 1-Wide, into 2-input NAND	2	X
20	OAI21H	2-Input OR, 1-Wide, into 2-input NAND, 2X	3	X
21	OAI211	2-Input OR, 1-Wide, into 3-input NAND	2	X
22	OAI211H	2-Input OR, 1-Wide, into 3-input NAND, 2X	4	X
23	OAI22	2-Input OR, 2-Wide, into 2-input NAND	2	X
24	OAI22H	2-Input OR, 2-Wide, into 2-input NAND, 2X	4	X
25	ONDAI22	2-Input OR + 2-Input NAND, into 2-Input NAND	3	X
26	ONDAI22H	2-Input OR + 2-Input NAND, into 2-Input NAND, 2X Drive	4	X

#	INTERNAL MACROS		G	R
	INVERTING BUFFERS			
1	INV	Inverter	1	X
2	INVB	Inverter, Balanced (Symmetrical Rise & Fall)	1	X
3	INV2	2-Inverters in parallel	1	X
4	INV2B	2-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	2	X
5	INV3	3-Inverters in parallel	2	
6	INV3B	3-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	3	
7	INV4	4-Inverters in parallel	2	X
8	INV4B	4-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	4	X
9	INV8	8-Inverters in parallel	4	X
10	INV8B	8-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	8	X
11	INVX	Inverted Buffer (used to drive internal logic from an I/O Site)	--	X
12	INVXP	Inverted Buffer (used to drive internal logic from an Power/GND Site)	--	X
	NON-INVERTING BUFFERS			
1	BUF	1X drive Buffer	1	X
2	BUF2	2X drive Buffer	2	X
3	BUF2B	2X drive Buffer, Balanced (Symmetrical Rise & Fall)	3	X
4	BUF2C	2X drive Buffer, 1x Complementary Output	2	
5	BUF3	3X drive Buffer	2	
6	BUF3B	3X drive Buffer, Balanced (Symmetrical Rise & Fall)	4	
7	BUF3C	3X drive Buffer, 1x Complementary Output	2	
8	BUF4	4X drive Buffer	3	X
9	BUF4B	4X drive Buffer, Balanced (Symmetrical Rise & Fall)	5	X
10	BUF8	8X drive Buffer	5	X
11	BUF8B	8X drive Buffer, Balanced (Symmetrical Rise & Fall)	9	X
12	BUFX	Non-Inverting Buffer (used to drive internal logic from an I/O Site)	--	X
13	BUFXP	Non-Inverting Buffer (used to drive internal logic from an Power/GND Site)	--	X
	3-STATE BUFFERS			
1	TBUF	3-state Buffer, Active Low Enable	4	X
2	TBUFH	3-state Buffer, Active Low Enable, 2X Drive	5	X
3	TBUFP	3-state Buffer, Active High Enable	4	X
4	TBUFPH	3-state Buffer, Active High Enable, 2X Drive	5	X
5	INVT	Inverting 3-state Buffer, Active Low Enable	2	X
6	INVTH	Inverting 3-state Buffer, Active Low Enable, 2X Drive	3	X
7	INVTP	Inverting 3-state Buffer, Active High Enable	3	X
8	INVTPH	Inverting 3-state Buffer, Active High Enable, 2x Drive	4	X
	SCHMITT TRIGGER BUFFERS			
1	DS1536	Schmitt Trigger Buffer	3	
2	DS1536H	Schmitt Trigger Buffer, 2X Drive	3	
3	DS1536I	Inverting Schmitt Trigger Buffer	3	
4	DS1536IH	Inverting Schmitt Trigger Buffer, 2X Drive	4	
	D TYPE FLIP-FLOPS			
1	DFF1A	Scan D Flip-Flop	15	X
2	DFF4A	4-Bit Scan D Flip-Flop	48	X
3	DFF8A	8-Bit Scan D Flip-Flop	96	
4	*DFFGLP*	*D Flip-Flop, Multiplexed (or Scan) Input with HOLD function*	13	X

#	INTERNAL MACROS		G	R
	D TYPE FLIP-FLOPS (Continued)			
5	*DFFMX1A*	*Scan D Flip-Flop with Multiplexed Input*	15	
6	DFFMX4A	4-Bit Scan D Flip-Flop W/Multiplexed Input	56	
7	DFFP	D Flip-Flop	8	X
8	DFFPH	DFFP, 2X Drive	8	X
9	DFFP4	4-Bit DFFP	23	
10	DFFP4H	DFFP4, 2X Drive	24	
11	DFFLP	D Flip-Flop, Multiplexed (or Scan) Input	11	X
12	DFFLPH	DFFLP, 2X Drive	11	X
13	DFFLPA	DFFLP W/Unbuffered Input /Clock	8	
14	DFFLPAH	DFFLPA, 2X Drive	9	
15	DFFLPB	D Flip-Flop	10	
16	DFFLPBH	DFFLPB, 2X Drive	11	
17	DFFR1	1-Bit D Flip Flop with Reset, 1X Drive	13	
18	DFFR1H	1-Bit D Flip Flop with Reset, 2X Drive	13	
19	DFFR4	4-Bit D Flip Flop with Reset, 1X Drive	41	
20	DFFR4H	4-Bit D Flip Flop with Reset, 2X Drive	45	
21	DFFRP	D Flip-Flop with Reset	8	X
22	DFFRPH	DFFRP, 2X Drive	10	X
23	DFFRP4	D Flip-Flop with Reset	28	
24	DFFRP4H	DFFRP, 2X Drive	32	
25	DFFRLP	D Flip-Flop W/Reset, Multiplexed (or Scan) Input	11	X
26	DFFRLPH	DFFRLP, 2X Drive	11	X
27	DFFRSPB	D Flip-Flop with Set and Reset	10	
28	DFFRSPHB	DFFRSP, 2X Drive	10	
29	DFFRSLPB	D Flip-Flop with Set and Reset, Multiplexed (or Scan) Input	14	
30	DRSLPHB	DFFRSLP, 2X Drive	14	
31	DFFSC	Scan D Flip-Flop	16	
32	DFFSCH	DFFSC, 2X Drive	18	X
33	DFFSCA	Muxed DFFSC	18	
34	DFFSCAH	DFFSCA, 2X Drive	20	X
35	DFFSP	D Flip-Flop with Set	8	X
36	DFFSPH	DFFSP, 2X Drive	10	X
37	DFFSLP	D Flip-Flop w/Set, Multiplexed (or Scan) Input	12	X
38	DFFSLPH	DFFSLP, 2X Drive	12	X
39	*DFFSRP*	*D Flip-Flop with Synchronous Reset*	9	X
40	*DFFSRLP*	*D Flip-Flop, Multiplexed (or Scan) Input with Synchronous Reset*	12	X
41	*DFFSSP*	*D Flip-Flop with Synchronous Set*	9	X
42	*DFFSSLP*	*D Flip-Flop, Multiplexed (or Scan) Input with Synchronous Set*	12	X
43	DFFRTPA	D Flip-Flop W/Reset, Q & 3-State Q Outputs	10	
44	DFFRTPHA	DFFRTPA, 2X Drive	12	
	JK TYPE FLIP-FLOPS			
1	JKFFP	J-K Flip-Flop	10	
2	JKFFPH	JKFFP, 2X Drive	10	
3	JKFFLP	J-K Flip Flop, Multiplexed (or Scan) Input	14	
4	JKFFLPH	JKFFLP, 2X Drive	14	
5	JKFFRP	J-K Flip Flop with Reset	12	
6	JKFFRPH	JKFFRP, 2X Drive	12	
7	JKFFRLP	J-K Flip Flop W/Reset, Multiplexed (or Scan) Input	14	
8	JKFFRLPH	JKFFRLPH, 2X Drive	14	
9	JKFFRSPB	J-K Flip Flop with Set and Reset	12	
10	JKRSPHB	JKFFRSPB, 2X Drive	13	
11	JKRSLPB	J-K Flip Flop W/Set and Reset, Multiplexed (or Scan) Input	16	
12	JKRSLPHB	JKFFRSLPB, 2X Drive	16	

#	INTERNAL MACROS		G	R
	TOGGLE FLIP-FLOPS			
1	TFFRPA	Toggle Flip-Flop with Reset	8	
2	TFFRPHA	TFFRPA, 2X Drive	10	
3	TFFSP	Toggle Flip-Flop with Set	8	
4	TFFSPH	TFFSP, 2X Drive	10	
	LATCHES			
1	CCNDRS	S-R Latch W/Set, Reset & Separate Gated Inputs	4	
2	CCNDRSG	S-R Latch W/Set, Reset & Common Gated Inputs	4	
3	L1LSSD	D-Type Latch with Scan Test Inputs	8	
4	L1LSSDH	L1LSSD, 2X Drive	8	
5	LATN	D-Type Latch, Neg Gate Latched	5	X
6	LATNH	LATN, 2X Drive	6	X
7	LATP	D-Type Latch, Pos Gate Latched	5	X
8	LATPH	LATP, 2X Drive	6	X
9	LATPA	Non-Inverting Latch, Pos Gate Latched	4	
10	LATPAH	LATPA, 2X Drive	5	
11	LATP4	4-Bit Latch with Non-Inverting Output	14	
12	LATP4H	LATP4, 2X Drive	14	
13	LATPI4	4-Bit Latch with Inverting Output	14	
14	LATPI4H	LATPI4, 2X Drive	14	
15	LATRN	D-Type Latch W/Reset, Neg Gate Latched	6	X
16	LATRNH	LATRN, 2X Drive	7	X
17	LATRP	D-Type Latch W/Reset, Pos Gate Latched	6	X
18	LATRPH	LATRP, 2X Drive	7	X
19	LAT4T	4-Bit D-Type Latch with 3-State Output	19	
20	LAT4TH	LAT4TH, 2X Drive	23	X
21	LSSD1A	D-Type Latch with Scan Test Inputs	12	
22	LSSD1AH	LSSD1A, 2X Drive	14	X
23	LSSD2	D-Type Latch with Scan Test Inputs	16	
24	LSSD2H	LSSD2, 2X Drive	18	
25	SRLSSD1	D-Type Latch W/ Scan into D-Type Latch	12	
26	SRLSSD1H	SRLSSD1, 2X Drive	13	X
	MULTIPLEXERS			
1	MUL8X8	8X8 - Bit Unsigned Multiplier	1106	
2	MUX2A	2-1 Multiplexer, 1X Drive	3	X
3	MUX2H	2-Input Multiplexer, 2X Drive	3	X
4	MUX2I	2-Input Multiplexer, Inverted Output	3	
5	MUX2IH	MUX2I, 2X Drive	3	X
6	MUX4	4-1 Multiplexer, 1X Drive	8	
7	MUX4H	4-Input Multiplexer, 2X Drive	7	X
8	*MUX8AH*	*8-Input Multiplexer, 2X Drive*	*16*	*X*
9	MUX41A	Four 2-1 MUX with Common Select	12	X
10	MUX41AH	MUX41A, 2X Drive	14	X
11	MUXE41	MUX41 with Common Enable	12	
12	MUXE41H	MUXE41, 2X Drive	14	
13	MUX41I	4-Bit, 2-1 Inverting Multiplexer with Common Select, 1X Drive	8	
14	MUX41IH	4-Bit, 2-1 Inverting Multiplexer with Common Select, 2X Drive	10	
15	MX41	4-Input Multiplexer with individual Selects, 2X Drive	5	X
16	MX41H	MX41, 2X Drive	6	X
17	MX61	7-Input MultiplexerW/ Individual Selects	8	X
18	MX61H	MX61, 2X Drive	9	X
19	MX81	8-Input Multiplexer W/Individual Selects	10	X
20	MX81H	MX81, 2X Drive	12	X

#	INTERNAL MACROS		G	R
	DECODERS			
1	DEC4	1 of 4 Decoder, Active Low Outputs	5	
2	DEC4H	DEC4, 2X Drive	9	X
3	DEC4A	1 of 4 Decoder, Active High Outputs	10	
4	DEC4AH	1 of 4 Decoder, Active High Outputs, 2X Drive	14	X
5	DEC1OF8	1 of 8 Decoder with Enable, Active Low Outputs	16	X
6	DEC8	1 of 8 Decoder, Active High Outputs	16	
7	DEC8A	1 of 8 Decoder with Enable, Active High Outputs	30	
8	DEC8AH	1 of 8 Decoder with Enable, Active High Outputs, 2X Drive	30	X
	ARITHMETIC CIRCUITS			
1	AD4FUL	4-Bit Full Adder, 2X Drive	40	
2	AD4FULA	4-Bit Full Adder, 2X Drive	40	X
3	AD4PG	4-Bit Full Adder with Propagate & Generate, 2X Drive	94	X
4	ADD5	Add 5-Bits, 2X Drive	20	
5	ADD5A	Add 5-Bits, 2X Drive	20	
6	ADFUL	Full Adder	10	
7	ADFULH	ADFUL, 2X Drive	10	X
8	ADFULHA	Full Adder, 2X Drive	10	X
9	ADHALF	Half Adder	6	
10	ADHALFH	ADHALF, 2X Drive	6	X
11	ECOMP4	4-Bit Equality Comparator	16	X
12	LACG4	4-bit Look-Ahead-Carry Generator	32	X
13	MCOMP2	2-bit Magnitude Comparator	18	
14	MCOMP4	4-bit Magnitude Comparator	35	X
15	SBHALF	Half Subtracter	6	
16	SBHALFH	Half Subtracter, 2X Drive	6	
	MISCELLANEOUS			
1	DCR4	4-Bit Decrementer	26	
2	DCR4H	4-Bit Decrementer, 2X Drive	28	X
3	DLY8	8-Stage Inverter Delay	4	X
4	DLY100	100-Stage Inverter Delay	50	
5	INC4	4-Bit Incrementer	27	
6	INC4H	4-Bit Incrementer, 2X Drive	28	X
7	PAR4	4-Bit Parity Checker	14	
8	ROT8A	8-Bit Rotate, 1X Drive	54	X
9	ROT8	8-Bit Rotate, 4X Drive	72	
10	SHIFT8	8-Bit Shift Register	45	X
	BIST SOFT MACROS			
1	ADDR_CELL	Address Counter Cell for Simplified BIST	20	X
2	DATA_CELL	Pattern generator & Signature Analysis	27	X
3	COMPA CELL	Address Cell for Comparator BIST	34	X
4	COMPD CELL	Data Cell for Comparator BIST	54	X
5	COMP BISTCNTL	BIST Controller for Comparator BIST	780	X
	PHASE LOCKED LOOP MACROCELLS			
1	DLYLN6	6-Bit Delay	462	X
2	DLYLN7	7-Bit Delay	702	X
3	PHSDET	Phase Detector	162	X
4	PLLCTR7	7-Bit Counter	288	X

#	ARRAYS JTAG MACROS		S
JTAG 1149.1 INPUTS			
1	ICNCKHJ	Non-Inverting CMOS Clock Buffer	1/1
2	ICNJ	Non-Invering CMOS Input	1/0
3	ICNJA	Non-Inverting CMOS Input	1/0
4	ISNCKHJ	Non-Invert CMOS Schmitt Trigger Clk Buffer	1/1
5	ISNJ	Non-Invering CMOS Schmitt Trigger Input	1/0
6	ITNCKHJ	Non-Invering TTL Clock Buffer	1/1
7	ITNJ	Non-Invering TTL Input	1/0
8	ITSNCKHJ	Non-Invert TTL Schmitt Trigger Clk Buffer	1/1
9	ITSNJ	Non-Inverting TTL Schmitt Trigger Input	1/0
JTAG 1149.1 OUTPUTS			
1	ON2J	Non-Inverting Output Buffer	0/1
2	ON4J	Non-Inverting Output Buffer	0/1
3	ON8J*	Non-Inverting Output Buffer	0/1
4	ON2TJ	Non-Inverting 3-State Output Buffer	0/1
5	ON4TJ	Non-Inverting 3-State Output Buffer	0/1
6	ON8TJ*	Non-Inverting 3-State Output Buffer	0/1
7	ON2ODJ	Non-Inverting Open Drain Output Buffer	0/1
8	ON4ODJ	Non-Inverting Open Drain Output Buffer	0/1
9	ON8ODJ*	Non-Inverting Open Drain Output Buffer	0/1
10	ON4S2J	Non-Inverting Output Buffer, with Slew Rate Control (S2)	0/1
11	ON8S2J*	Non-Inverting Output Buffer, Slew Rate Control (S2)	0/1
12	ON4S4J	Non-Inverting Output Buffer, Slew Rate Control (S4)	0/1
13	ON8S4J*	Non-Inverting Output Buffer, Slew Rate Control (S4)	0/1
14	ON4TS2J	Non-Inverting 3-State Output Buffer, Slew Rate Control (S2)	0/1
15	ON8TS2J*	Non-Inverting 3-State Output Buffer, Slew Rate Control (S2)	0/1
16	ON4TS4J	Non-Inverting 3-State Output Buffer, Slew Rate Control (S4)	0/1
17	ON8TS4J*	Non-Inverting 3-State Output Buffer, Slew Rate Control (S4)	0/1
18	ON4ODS2J	Non-Inverting Open Drain Output Buffer, Slew Rate Control (S2)	0/1
19	ON8ODS2J*	Non-Inverting Open Drain Output Buffer, Slew Rate Control (S2)	0/1
20	ON4ODS4J	Non-Inverting Open Drain Output Buffer, Slew Rate Control (S4)	0/1
21	ON8ODS4J*	Non-Inverting Open Drain Output Buffer, Slew Rate Control (S4)	0/1
JTAG 1149.1 Bidirectionals			
1	BICNJ	Non-Invetring CMOS Bidirectional Input Buffer	1/0
2	BITNJ	Non-Inverting CMOS Bidirectional Input Buffer	1/0
3	BISNJ	Non-Inverting CMOS Schmitt Trigger Bidirectional Input Buffer	1/0
4	BITSNJ	Non-Inverting CMOS Schmitt Trigger Bidirectional Input Buffer	1/0
5	BN2TJ	Non-Inverting TTL Bidirectional Output Buffer	0/1
6	BN4TJ	Non-Inverting TTL Bidirectional Output Buffer	0/1
7	BN8TJ*	Non-Inverting TTL Bidirectional Output Buffer	0/1
8	BN2ODJ	Non-Inverting CMOS Open Drain Bidirectional Output Buffer	0/1
9	BN4ODJ	Non-Inverting CMOS Open Drain Bidirectional Output Buffer	0/1
10	BN8ODJ*	Non-Inverting CMOS Open Drain Bidirectional Output Buffer	0/1
11	BN4TS2J	Non-Inverting CMOS 3-State Bidirectional Output Buffer, Slew Rate Control (S2)	0/1

#	ARRAYS JTAG MACROS		S
12	BN8TS2J*	Non-Inverting CMOS 3-State Bidirectional Output Buffer, Slew Rate Control (S2)	0/1
13	BN4TS4J	Non-Inverting CMOS 3-State Bidirectional Output Buffer, Slew Rate Control (S2	0/1
14	BN8TS4J* See NOTE	Non-Inverting CMOS 3-State Bidirectional Output Buffer, Slew Rate Control (S4)	0/1
15	BN4ODS2J	Non-Inverting CMOS Open Drain Bidirectional Output Buffer, Slew Rate Control (S4)	0/1
16	BN8ODS2J*	Non-Inverting CMOS Open Drain Bidirectional Output Buffer, Slew Rate Control (S2)	0/1
17	BN4ODS4J	Non-Inverting CMOS Open Drain Bidirectional Output Buffer, Slew Rate Control (S4)	0/1
18	BN8ODS4J*	Non-Inverting CMOS Open Drain Bidirectional Output Buffer, Slew Rate Control (S4)	0/1

*Versions up to 4X

#	ARRAYS JTAG TAP I/O MACROS		I/O*
TAP Inputs/Outputs Functions			
1	TCK	Test Clock	1/0
2	TCKH	Test Clock, High Drive	1/1
3	TCKT	Test Clock, TTL Levels	1/0
4	TCKHT	Test Clock, TTL Levels, High Drive	1/1
5	TDI	Test Data Input	1/0
6	TDIT	Test Data Input, TTL Levels	1/0
7	TDO	Test Data Output	1/1
8	TDOA	Test Data Output	1/1
9	TMS	Test Mode Select	1/0
10	TMST	Test Mode Select, TTL Levels	1/0
11	TRSTB	Test Reset (Bar)	1/0
12	TRSTBT	Test Reset (Bar), TTL Levels	1/0
Miscellaneous Boundary-Scan Macrocells			
1	CKDR,	B-S Register Clock Driver -JTAG	0/1
2	CKDRP	(Pwr/Gnd Site)	
3	CKDRMID	B-S Register Clock Driver -JTAG	0/1
4	CKDRMIDP	(Pwr/Gnd Site)	
5	CKDRCC1	B-S Register Clock Driver -JTAG	0/1
6	CKDRCC1P	(Pwr/Gnd Site)	
7	CKDRCC2	B-S Register Clock Driver -JTAG	0/1
8	CKDRCC2P	(Pwr/Gnd Site)	
9	ENSCANJ	B-S Register Enable Scan Macro -JTAG	0/1
10	ENSCANP	(Pwr/Gnd Site)	
11	IMCDR	B-S Register Input Mode Control Driver -JTAG	0/1
12	IMCDRP	(Pwr/Gnd Site)	
13	OMCDR	B-S Register Output Mode Control Driver -JTAG	0/1
14	OMCDRP	(Pwr/Gnd Site)	
15	OSCPBJ	B-S Register Oscillator W/Non-Inverting	2/2
16	OSCPHBJ	Input/Oscillator W/Clock Buffer Input	2/2
17	OSCPSBJ	Oscillator W/Schmitt Trigger Input -JTAG	2/2
18	SHDR,	B-S Register Shift Driver -JTAG	0/1
19	SHDRP	(Pwr/Gnd Site)	
20	UDDR	B-S Register Update Driver -JTAG	0/1
21	UDDRP	(Pwr/Gnd Site)	

#	ARRAYS JTAG TAP I/O MACROS		I/O*
22	TDBUF	B-S Register Test Data Buffer -JTAG	0/1
23	TDBUFP	(Pwr/Gnd Site)	

#	ARRAYS JTAG MACROS		G
	TAP CONTROL MACRO FUNCTIONS		
1	BPREG	1-bit Bypass Register	10
2	ENSCANI	Enable Boundary Scan Macro (Internal)	20
3	IDREG	32-bit Device Identification Code Register	256
4	MC_IREG	1-bit of Instruction Register (Soft Macro)	25
5	MC_IREG4	4-bit of Instruction Register(Soft Macro)	124
6	FMC_TAPC	TAP Controller (FIRM Macro)	276
7	MC_TAPC*	TAP Controller (Soft Macro)	-

*Number of input/output drivers used for function.
•The TAP Controller (Soft Macro) is not included in the recommended use list.

MEMORY BLOCKS			
#	Name	RAM Size	Gate Count
SINGLE-PORT RAM's (LOW Power)			
1	RSA8X18	8 word X 18bit	440
2	RSA16X18	16 word X 18bit	760
3	RSA16X36	16 word X 36 bit	1440
4	RSA32X8	32 word X 8bit	630
5	RSA32X18	32 word X 18 bit	1400
6	RSA32X36	32 word X 36 bit	2660
7	RSA64X18	32 word X 18 bit	2680
8	RSA64X36	64 word X 36 bit	5092
DUAL-PORT RAM's (HIGH Speed)			
1	RDA8X9	8 word X 9 bit	356
2	RDA8X18	8 word X 18 bit	608
3	RDA8X36	8 word X 36 bit	1112
4	RDA8X72	8 word X 72 bit	2156
5	RDA16X9	16 word X 9 bit	725
6	RDA16X18	16 word X 18 bit	1193
7	RDA16X36	16 word X 36 bit	2129
8	RDA16X72	16 word X 72 bit	4050
9	RDA32X9	32 word X 9 bit	1400
10	RDA32X18	32 word X 18 bit	2300
11	RDA32X36	32 word X 36 bit	4100
12	RDA32X72	32 word X 72 bit	7798
QUAD PORT RAM's			
1	RQA16X18	16 word X 18 bit	2200
2	RQA16X36	16 word X 36 bit	3766
3	RQA32X18	32 word X 18 bit	4762
4	RQA32X36	32 word X 36 bit	7738

LIBRARY SUMMARY		
Internal Macros	Macros	Recommended Use Macros
Inverters	12	10
Non-Inverting Buffers	13	9
3-State Inverters and Buffers	8	8
Schmitt Trigger Buffers	4	0
AND & NAND Gates	19	18
OR & NOR Gates	19	18
Exor & Exnor Gates	13	5
AND/NOR,AND/OR,OR/NAND & OR/AND Gates	26	22
D Flip-flops	44	21
JK Flip-flops	12	0

LIBRARY SUMMARY		
Internal Macros	Macros	Recommended Use Macros
Toggle Flip-flops	4	0
Latches	26	11
Multiplexers	20	13
Decoders	8	4
Arithmetic Functions	16	8
Miscellaneous	10	5
RAMs (Metallized)	24	24
Clock Skew Management (Phase Locked Loop)	4	4
Soft Macros	5	5
JTAG Control Functions	7	6
JTAG Boundary Scan Functions	23	23

Total number of Internal Library Cells: **317**

Total number of Recommended Use Internal Library Cells: **214**

Total number of Non-JTAG periphery cell combinations: **423**
* Input Cell Combinations: 50
* Output Cell Combinations: 23
* Bidirectional Cell Combinations: 350

Total number of JTAG periphery cell combinations: **356**
* Input Cell Combinations: 45 + 10
* Output Cell Combinations: 21
* Bidirectional Cell Combinations: 280

Total number of Recommended Use Non-JTAG periphery cell combinations:**104**
* Input Cell Combinations: 35
* Output Cell Combinations: 9
* Bidirectional Cell Combinations: 60

Total number of Recommended Use JTAG periphery cell combinations: **62**
* Input Cell Combinations: 10 + 7
* Output Cell Combinations: 5
* Bidirectional Cell Combinations: 40

MACROCELL EXAMPLES

## INPUT/OUTPUT MACROCELLS

BON8T/BICI - Non-Inverting Bidirectional Buffer

with CMOS Input Switching Levels

The BON8T and BICI cells are used together to form a complete bidirectional macrocell. A "weak" or "strong" pullup/pulldown resistor can optionally be attached (at the dotted line) during schematic capture.

Nom. V_{DD}= 5.0 V, T_J= 25.0°C

Sym	Parameter	Typ.	Unit
t_{PLH}	Propagation Delay,	3.10	ns
t_{PHL}	BON8T: DO to PAD C_L = 50 pF	2.67	ns
t_{PLH}		3.16	ns
t_{PHL}	Propagation Delay,	2.32	ns
t_{PLZ}	BON8T: EN to PAD	1.01	ns
t_{PZL}	C_L = 50 pF R_L= 500 Ω	2.30	ns
t_{PZH}		3.14	ns
t_{PHZ}		1.13	ns
t_{PLH}	Propagation Delay,	0.24	ns
t_{PHL}	BICI: PAD to DI C_L = 13 pF	0.19	ns

BON8T

Normal Bidirectional
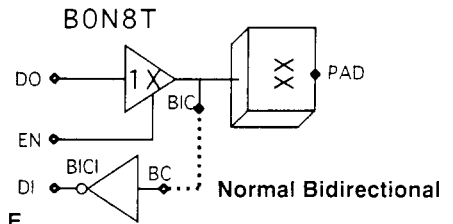
FUNCTION TABLE

EN	PAD	DO	DI	PAD	FUNCTION
L	L/H	X	H/L	Z	The pin functions as an input. Data from the internal array is disabled and data from the PAD input is enabled.
H	L/H	L/H	L/H	L/H	The pin functions as an output, with data originating from the internal array at point DO. The data at point DO appears at the PAD output and at point DI.

INTERNAL MACROCELLS (COMBINATIONAL)

2-Input NAND Gate

NAN2 - 1/2 Cell - 1 Equivalent Gate

NAN2H - 1 Cell -2 Equivalent Gate (High Drive)

NAN2B - 1 Cell -2 Equivalent Gate (Balanced Drive)

FUNCTION TABLE

A	B	X
L	L	H
L	H	H
H	L	H
H	H	L

CMOS SWITCHING CHARACTERISTICS (Input Edge Rate t_r, t_f=1.0ns)

Rev. 2.10

Sym	Parameter	Nom. V_{DD}= 5.0 V, T_J= 25.0°C						
		FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K (ns/pF)
NAN2								
t_{PLH}	Propagation Delay,	0.17	0.26	0.34	0.50	0.84	ns	1.38
t_{PHL}	A to X	0.12	0.18	0.24	0.35	0.57	ns	0.94
t_{PLH}	Propagation Delay,	0.20	0.29	0.37	0.53	0.86	ns	1.37
t_{PHL}	B to X	0.11	0.17	0.23	0.34	0.56	ns	0.94
t_r	Output Rise Time, X	0.14	0.31	0.49	0.84	1.55	ns	2.94
t_f	Output Fall Time, X	0.08	0.19	0.30	0.52	0.97	ns	1.86
NAN2H								
t_{PLH}	Propagation Delay,	0.16	0.21	0.25	0.33	0.50	ns	0.69
t_{PHL}	A to X	0.12	0.15	0.18	0.23	0.35	ns	0.47
t_{PLH}	Propagation Delay,	0.20	0.24	0.29	0.37	0.54	ns	0.69
t_{PHL}	B to X	0.11	0.14	0.16	0.22	0.33	ns	0.47
t_r	Output Rise Time, X	0.16	0.24	0.33	0.51	0.86	ns	1.46
t_f	Output Fall Time, X	0.10	0.16	0.21	0.32	0.54	ns	0.90
NAN2B								
t_{PLH}	Propagation Delay,	0.15	0.19	0.23	0.32	0.48	ns	0.69
t_{PHL}	A to X	0.17	0.22	0.28	0.39	0.62	ns	0.94
t_{PLH}	Propagation Delay,	0.17	0.21	0.25	0.33	0.50	ns	0.69
t_{PHL}	B to X	0.15	0.20	0.26	0.37	0.60	ns	0.94
t_r	Output Rise Time, X	0.12	0.21	0.30	0.47	0.82	ns	1.46
t_f	Output Fall Time, X	0.10	0.21	0.33	0.55	0.99	ns	1.86

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.06pF).

INTERNAL MACROCELLS (SEQUENTIAL)
DFFRP - D Flip Flop with Reset
DFFRLP - Scan D Flip Flop with Reset

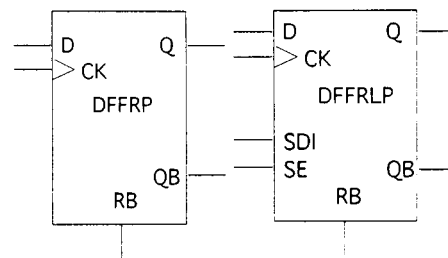| MACRO	EQUIV. GATES
DFFRP	8
DFFRLH	11

Rev. 2.10

MACRO	OUTPUTS/INPUTS
DFFRP	Q,QB / RB,D,CK
DFFRLH	Q,QB / D,CK,SDI,SE,RB

FUNCTION TABLE

D	SDI*	SE*	CK	RB	Q	QB
L	X	L	$\llcorner$	H	L	H
H	X	L	$\llcorner$	H	H	L
X	L	H	$\llcorner$	H	L	H
X	H	H	$\llcorner$	H	H	L
X	X	X	$\lrcorner$	H	Q	QB
X	X	X	X	L	L	H

* SDI & SE not applicable on DFFRP

CMOS SWITCHING CHARACTERISTICS (Input Edge Rate $t_r, t_f = 1.0$ns)

Rev. 2.10

Sym	Parameter	Nom. $V_{DD} = 5.0$ V, $T_J = 25.0$°C						
		FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K (ns/pF)
	DFFRP							
t_{PLH}	Propagation Delay, CK to Q	0.87	0.95	1.03	1.20	1.53	ns	1.38
t_{PHL}		0.96	1.00	1.03	1.10	1.24	ns	0.58
t_{PLH}	Propagation Delay, CK to QB	1.09	1.17	1.26	1.42	1.75	ns	1.38
t_{PHL}		1.08	1.12	1.15	1.22	1.35	ns	0.56
t_{PHL}	Propagation Delay, RB to Q	0.48	0.51	0.55	0.62	0.76	ns	0.58
t_{PLH}	Propagation Delay, RB to QB	0.62	0.70	0.79	0.95	1.28	ns	1.38
t_r	Output Rise Time, Q	0.11	0.29	0.46	0.81	1.52	ns	2.93
t_f	Output Fall Time, Q	0.16	0.22	0.28	0.40	0.64	ns	1.00
t_r	Output Rise Time, QB	0.07	0.25	0.43	0.78	1.49	ns	2.94
t_f	Output Fall Time, QB	0.12	0.18	0.24	0.36	0.60	ns	1.01
	DFFRLP							
t_{PLH}	Propagation Delay, CK to Q	0.85	0.94	1.02	1.18	1.52	ns	1.38
t_{PHL}		1.05	1.09	1.12	1.19	1.33	ns	0.58
t_{PLH}	Propagation Delay, CK to QB	1.19	1.27	1.35	1.52	1.85	ns	1.38
t_{PHL}		1.03	1.06	1.10	1.17	1.30	ns	0.56
t_{PHL}	Propagation Delay, RB to Q	0.43	0.47	0.50	0.57	0.71	ns	0.58
t_{PLH}	Propagation Delay, RB to QB	0.57	0.65	0.74	0.90	1.23	ns	1.38
t_r	Output Rise Time, Q	0.11	0.29	0.46	0.81	1.52	ns	2.93
t_f	Output Fall Time, Q	0.15	0.21	0.27	0.39	0.63	ns	1.01
t_r	Output Rise Time, QB	0.07	0.25	0.43	0.78	1.49	ns	2.94
t_f	Output Fall Time, QB	0.10	0.16	0.22	0.34	0.59	ns	1.02

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.06pF).

TIMING REQUIREMENTS (Input Edge Rate $t_r, t_f = 1.0$ns)

Sym	Parameter	Minimum Requirement	
		Nom. 5 V, 25°C	Unit
	DFFRP		
t_{su}	Set Up Time, D to CK	0.48	ns
t_h	Hold Time, CK to D	0.10	ns
t_{rec}	Recovery Time, RB to CK	-0.12	ns
t_w	Pulse Width, CK(L)	0.90	ns
t_w	Pulse Width, CK(H)	0.67	ns
t_w	Pulse Width, RB(L)	0.64	ns

Sym	Parameter	Minimum Requirement	
		Nom. 5V, 25°C	Unit
	DFFRLP		
t_{su}	Set Up Time, D,SDI,SE to CK	0.80	ns
t_h	Hold Time, CK to D,SDI	-0.14	ns
t_h	Hold Time, CK to SE	-0.05	ns
t_{rec}	Recovery Time, RB to CK	-0.13	ns
t_w	Pulse Width, CK(L)	1.00	ns
t_w	Pulse Width, CK(H)	0.71	ns
t_w	Pulse Width, RB(L)	0.61	ns

INTERNAL MACROCELLS (SEQUENTIAL)

DFFSC - D Flip Flop with Scan Latch

MACRO	EQUIV. GATES
DFFSC	16

Rev. 2.10

MACRO	OUTPUTS/INPUTS
DFFSC	Q,QB,SQ / D,CK,SDI,BCLK,ACLK,EN

FUNCTIONAL DESCRIPTION:

This macro consists of a D type Flip Flop with Q feedback (hold) capability. It allows scan data to be muxed into the slave stage and contains a separate scan latch for storing scan data independent of Q. CK clocks the Flip Flop, BCLK controls latching scan data into the slave stage and ACLK controls the final scan data latch.

FUNCTION TABLE

D	EN	CK	SDI	BCLK	ACLK	Q	QB	SQ	Notes
X	X	L	X	L	L	Q	QB	SQ	1
X	L	/	X	L	L	Q	QB	SQ	2
L	H	/	X	L	L	L	H	SQ	3
H	H	/	X	L	L	H	L	SQ	3
X	X	L	X	L	H	Q	QB	QB	4
X	X	L	L	H	L	H	L	SQ	5
X	X	L	H	H	L	L	H	SQ	5
X	X	L	L	H	H	H	L	L	6
X	X	L	H	H	H	L	H	H	6

1. No Clock 2. Active Clock, disabled 3. Active Clock, enabled
4. Scan-out Clock applied 5. Scan-in Clock applied 6. Flush or Ring-oscillate

CMOS SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.0ns)

Rev. 2.10

| Sym	Parameter	Nom. V_{DD}= 5.0 V, T_J= 25.0°C						
		FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K (ns/pF)
		DFFSC						
t_{PLH}	Propagation Delay,	0.60	0.68	0.77	0.93	1.27	ns	1.38
t_{PHL}	ACLK to SQ	0.55	0.59	0.62	0.69	0.83	ns	0.57
t_{PLH}	Propagation Delay,	0.47	0.52	0.56	0.64	0.81	ns	0.71
t_{PHL}	BCLK to Q	0.75	0.79	0.83	0.91	1.07	ns	0.68
t_{PLH}	Propagation Delay,	0.98	1.02	1.06	1.14	1.31	ns	0.69
t_{PHL}	BCLK to QB	0.96	1.00	1.04	1.11	1.25	ns	0.59
t_{PLH}	Propagation Delay,	1.61	1.70	1.78	1.94	2.27	ns	1.37
t_{PHL}	BCLK to SQ	1.49	1.52	1.56	1.63	1.76	ns	0.57
t_{PLH}	Propagation Delay,	0.96	1.00	1.04	1.13	1.30	ns	0.71
t_{PHL}	CK to Q	0.95	0.99	1.03	1.12	1.28	ns	0.68
t_{PLH}	Propagation Delay,	1.19	1.23	1.28	1.36	1.53	ns	0.70
t_{PHL}	CK to QB	1.46	1.50	1.54	1.61	1.75	ns	0.59
t_{PLH}	Propagation Delay,	1.95	2.03	2.11	2.28	2.61	ns	1.37
t_{PHL}	CK to SQ	2.06	2.09	2.13	2.20	2.34	ns	0.57
t_{PLH}	Propagation Delay,	0.46	0.51	0.55	0.63	0.80	ns	0.71
t_{PHL}	SDI to Q	0.63	0.67	0.71	0.79	0.95	ns	0.68
t_{PLH}	Propagation Delay,	0.84	0.88	0.92	1.01	1.18	ns	0.70
t_{PHL}	SDI to QB	0.96	0.99	1.03	1.10	1.24	ns	0.59
t_{PLH}	Propagation Delay,	1.47	1.55	1.64	1.80	2.13	ns	1.38
t_{PHL}	SDI to SQ	1.48	1.51	1.55	1.62	1.75	ns	0.57
t_r	Output Rise Time, Q	0.18	0.26	0.35	0.52	0.86	ns	1.43
t_f	Output Fall Time, Q	0.35	0.41	0.47	0.59	0.83	ns	1.01
t_r	Output Rise Time, QB	0.14	0.23	0.32	0.49	0.83	ns	1.43
t_f	Output Fall Time, QB	0.20	0.26	0.32	0.44	0.68	ns	0.99
t_r	Output Rise Time, SQ	0.11	0.29	0.47	0.82	1.52	ns	2.93
t_f	Output Fall Time, SQ	0.15	0.21	0.27	0.39	0.63	ns	1.01

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.06pF).

CMOS TIMING REQUIREMENTS (Input Edge Rate $t_r, t_f = 1.0ns$)   Rev. 2.10

Sym	Parameter	Nom. $V_{DD}= 5.0$ V, $T_J= 25.0°C$	
		Minimum Requirement	Unit
DFFSC			
t_{su}	Set Up Time, BCLK,SDI to ACLK	1.44	ns
t_{su}	Set Up Time, CK to ACLK	1.77	ns
t_{su}	Set Up Time, SDI to BCLK	1.11	ns
t_{su}	Set Up Time, D to CK	0.26	ns
t_{su}	Set Up Time, EN to CK	0.55	ns
t_h	Hold Time, ACLK to BCLK	-0.99	ns
t_h	Hold Time, ACLK to CK	-1.07	ns
t_h	Hold Time, ACLK to SDI	-0.94	ns
t_h	Hold Time, BCLK to CK	-0.97	ns
t_h	Hold Time, BCLK to SDI	0.16	ns
t_h	Hold Time, CK to BCLK	-0.91	ns
t_h	Hold Time, CK to D	0.41	ns
t_h	Hold Time, CK to EN	0.18	ns
t_{rec}	Recovery Time, CK to ACLK	-1.48	ns
t_{rec}	Recovery Time, ACLK to CK	1.97	ns
t_w	Pulse Width, ACLK(H)	0.31	ns
t_w	Pulse Width, BCLK(H)	0.99	ns
t_w	Pulse Width, CK(L)	0.84	ns
t_w	Pulse Width, CK(H)	1.16	ns

FUNCTIONAL DIAGRAM: DFFSC
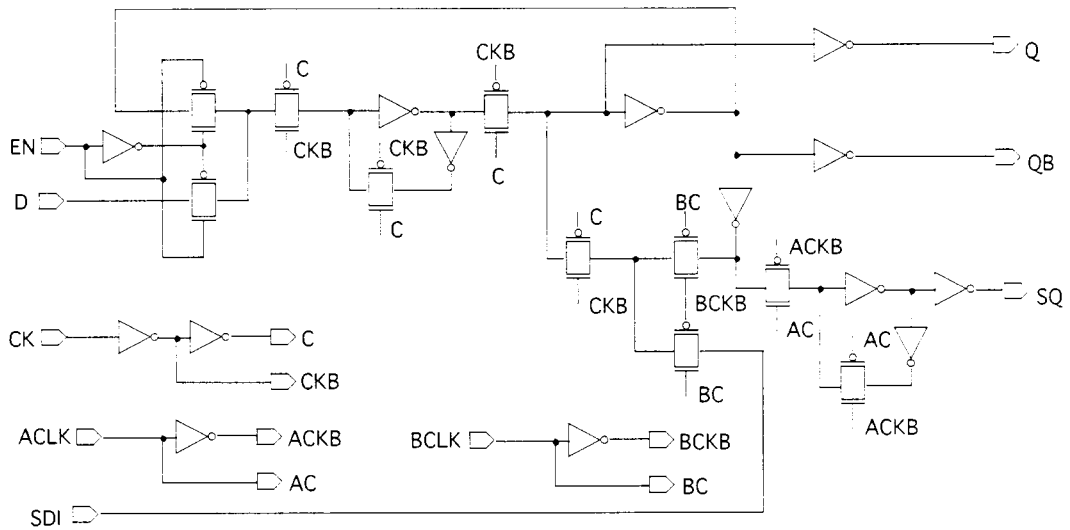
Note: Outputs have balanced drive

METALLIZED SRAM BLOCKS

Random Access Memories

Motorola offers 26 different building blocks that can be used to construct Single, Dual and Four Port memories. A comprehensive guide to using these blocks and their performance is shown in the H4C Series Design Reference Guide. (H4CDM/D)

Multiple Memory Blocks

It is possible to combine two or more memory blocks to create larger memory blocks. When multiple blocks are used,

the user is responsible for creating the external decoder logic needed. The maximum number of SRAM blocks on an array is restricted to 16, depending on array/SRAM sizes.

Array Sizing

To choose an array into which a design with SRAM will fit, two considerations must be evaluated: the physical size/layout of the SRAM or SRAMs and the gate utilization.

RDAXXxXX -High Speed Dual Port SRAM

Equivalent Gates: see below

Pin names:

A_A(0-m) - address bus for Port A

A_B(0-m) - address bus for Port B

DIN_A(0-n) -input data

WB_B - Write enable bus or Port A

DO_B(0-n) - data output

```
 ┌──────────────────────────────┐
 │        RDAXXxXX              │
 │── A_A(0-m)      DO_B(0-n) ───│
 │── A_B(0-m)                   │
 │                             │
 │── DIN_A(0-n)                │
 │                             │
 │── WB_A                      │
 └──────────────────────────────┘
```
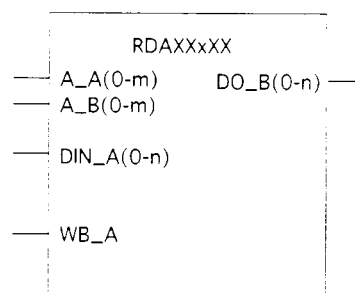
Size (Words X Bits)	Name	Size (Columns X Rows)	Total Gate Count	Port A Input Capacitance Per Address Line	Port A Input Capacitance WB_A Line	Port B Input Capacitance Per Address Line
8-WORD BLOCK						
8X9	RDA8X9	13X14	356			
8X18	RDA8X18	22X14	608			
8X36	RDA8X36	40X14	1112	0.15 pF	0.18 pF	0.15 pF
8X72	RDA8X72	77X14	2156			

CMOS SWITCHING CHARACTERISTICS (Input Edge Rate $t_r, t_f = 1.0$ns)

Rev. 2.10

| Sym	Parameter	Nom. V_{DD}= 5.0 V, T_J= 25.0°C							
		Abbr.	FO=0	FO=1	FO=2	FO=4	FO=8	Unit	K (ns/pF)
8-WORD BLOCK									
t_{PLH}	Address Access Time, 9-Bits	t_{AA}	2.67	2.75	2.84	3.02	3.37	ns	1.47
t_{PHL}		t_{AA}	1.88	1.92	1.95	2.02	2.15	ns	0.56
t_{PLH}	Address Access Time, 18-Bits	t_{AA}	2.93	3.02	3.11	3.28	3.63	ns	1.47
t_{PHL}		t_{AA}	1.98	2.02	2.05	2.12	2.25	ns	0.56
t_{PLH}	Address Access Time, 36-Bits	t_{AA}	3.45	3.54	3.63	3.81	4.16	ns	1.47
t_{PHL}		t_{AA}	2.23	2.26	2.29	2.36	2.49	ns	0.56
t_{PLH}	Address Access Time, 72-Bits	t_{AA}	4.06	4.14	4.23	4.41	4.76	ns	1.47
t_{PHL}		t_{AA}	2.72	2.76	2.79	2.86	2.99	ns	0.56
t_{PLH}	Propagation Delay, WBA to DOB (n) (WL = 9)	t_{WDO}	3.95	4.04	4.12	4.30	4.65	ns	1.47
t_{PHL}		t_{WDO}	2.98	3.01	3.04	3.11	3.24	ns	0.56
t_{PLH}	Propagation Delay, WBA to DOB (n) (WL = 18)	t_{WDO}	4.35	4.44	4.53	4.70	5.05	ns	1.47
t_{PHL}		t_{WDO}	3.17	3.20	3.24	3.30	3.44	ns	0.56
t_{PLH}	Propagation Delay, WBA to DOB (n) (WL = 36)	t_{WDO}	5.00	5.09	5.17	5.35	5.70	ns	1.47
t_{PHL}		t_{WDO}	3.73	3.76	3.79	3.86	3.99	ns	0.56
t_{PLH}	Propagation Delay, WBA to DOB (n) (WL = 72)	t_{WDO}	5.63	5.72	5.81	5.98	6.33	ns	1.47
t_{PHL}		t_{WDO}	4.23	4.26	4.30	4.36	4.50	ns	0.56
t_{PLH}	Propagation Delay, DINA(n) to DOB(n)	t_{DDO}	2.34	2.42	2.51	2.69	3.04	ns	1.47
t_{PHL}		t_{DDO}	2.04	2.08	2.11	2.18	2.31	ns	0.56
t_r	Output Rise Time, DOB (n)	N/A	1.22	1.41	1.61	2.01	2.80	ns	3.29
t_f	Output Fall Time, DOB (n)	N/A	0.58	0.66	0.74	0.90	1.23	ns	1.36

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.06pF).

MACROCELL EXAMPLES (Continued)

CMOS TIMING REQUIREMENTS (Input Edge Rate: $t_r, t_f = 1.0ns$)

Sym.	Parameter		Nom.V_{DD}=5.0V,T_J= 25 °C	
			8-WORD BLOCK	Unit
t_{DSU}	Set Up Time,	DIN_A(n) to WB_A (WL = 9)	2.06	ns
		DIN_A(n) to WB_A (WL = 18)	2.24	ns
		DIN_A(n) to WB_A (WL = 36)	2.46	ns
		DIN_A(n) to WB_A (WL = 72)	3.15	ns
t_{AWB}	Set Up Time,	A_A to WB_A	0.25	ns
t_{DH}	Hold Time,	WB_A to DIN_A(n) (WL = 9)	1.08	ns
		WB_A to DIN_A(n) (WL = 18)	1.22	ns
		WB_A to DIN_A(n) (WL = 36)	1.34	ns
		WB_A to DIN_A(n) (WL = 72)	1.82	ns
t_{AH}	Hold Time,	WB_A to A_A(n)	0.09	ns
t_{WP}	Pulse Width	WB_A (L) (WL = 9)	2.86	ns
		WB_A (L) (WL = 18)	3.19	ns
		WB_A (L) (WL = 36)	3.86	ns
		WB_A (L) (WL = 72)	5.13	ns
		WB_A (H) (WL = 9)	1.42	ns
		WB_A (H) (WL = 18)	1.57	ns
		WB_A (H) (WL = 36)	2.03	ns
		WB_A (H) (WL = 72)	2.61	ns

FUNCTIONAL DIAGRAM of High Speed Dual-Port RAM
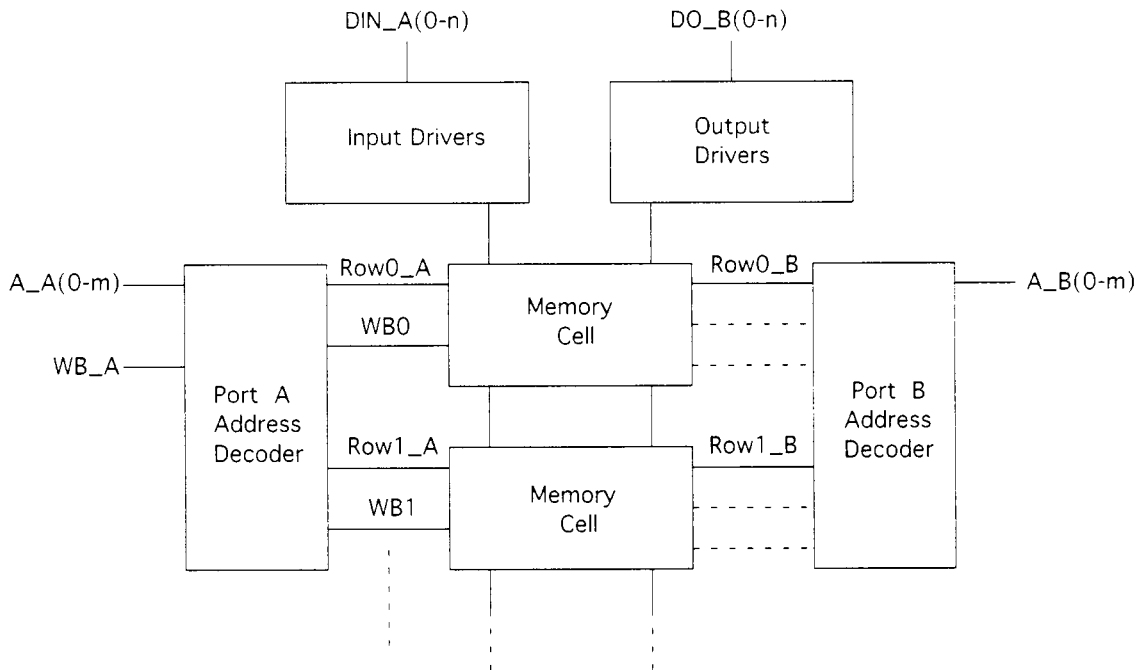
COMPILED, DIFFUSED SRAM BLOCKS

Why Diffused SRAMs?

Why use Memorist diffused SRAMs rather than selecting a metallized SRAM from the standard H4C Library?

- Memorist diffused SRAM's are more efficient than metallized SRAMs (above 2K bits): Metallized SRAMs are about 3 gates/bit, while Memorist SRAMs are about 1 gate/bit.
- The performance is better than conventional gate array metallized SRAM implementation.
- Memorist allows flexible implementation of fully diffused SRAMs with many different configuations.

Memorist Compiler

Motorola's Memorist SRAM Compiler tool automates the creation of fully-diffused single- and dual-port, synchronous SRAM blocks. Memorist creates the necessary symbols, files and entries to enable it to be embedded in the gate array environment as if it were an element in the standard library. The available word lengths are 1 to 256 bits/word and the available word blocks are16 to 16,384 words/block.

Access Time vs. Number of Words/Word Lengths

Given an SRAM configuration, such as 1Kx8, there can be up to 40 different implementations. These reflect the different aspect ratios and multi-block configurations. Thus, for each configuration, there can be a range of possible performance and area values.

In general, as the performance increases, power and area also increases, and vice versa. Due to the large number of SRAMs available, specific information of performance and layout parameters are available only by using the Memorist SRAM Compiler.

The following graphs (Figure 8 to Figure 10) show estimated minimum cycle time, read access time, and equivalent gate count for various number of words and word lengths of the single port memories at typical conditions (typical process, $V_{DD} = 5.0V$, $T_J = 25°C$). These graphs do not show the upper limit of the performance range and physical size.
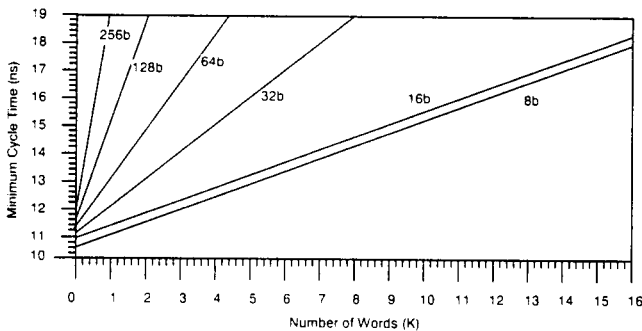
Figure 8. Estimated Minimum Cycle Time vs. Number of Words and Bits/Word (b)
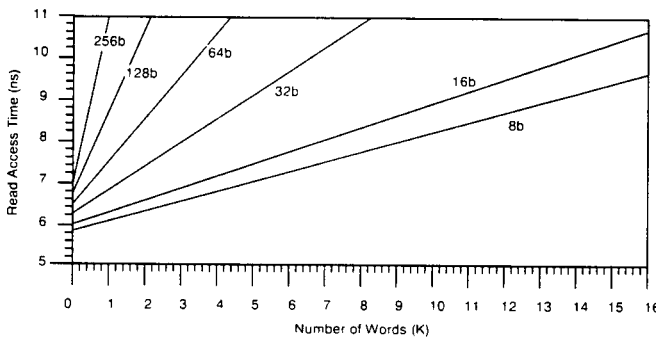
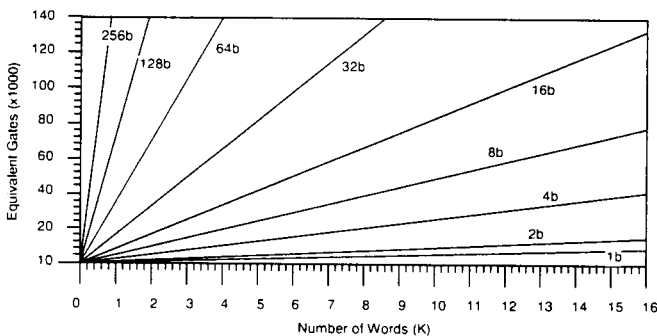**Figure 9. Estimated Read Access Time vs. Number of Words and Bits/Word (b)**

Figure 10. Estimated Equivalent Gates Used vs. Number of Words and Bits/Word (b)

Note: In all the above graphs b = bits

Table 6. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to 7.0	V
V_{in}	DC Input Voltage	-1.5 to V_{DD} + 1.5	V
Vout	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Pin, Any Single Input or Output	50	mA
	DC Current Drain per Pin, Any Paralleled Outputs	100	mA
	DC Current Drain VDD and VSS Pins	75	mA
T_{stg}	Storage Temperature	-65 to + 150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

Note: Maximum ratings are those values beyond which damage to the device may occur.

RECOMMENDED OPERATING CONDITIONS (to guarantee functionality)

Symbol	Parameter	Min	Max	Unit
V_{DD}	DC Supply Voltage	3.0	6.0	V
V_{in}, V_{out}	Input Voltage, Output Voltage	0.0	V_{DD}	V
T_A	Commercial Operating Temperature	0	+70	°C
	Industrial Operating Temperature	-40	+85	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.
For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq$ (V_{in} or V_{out})$\leq V_{DD}$
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{ss} or V_{DD}).

Sym.	Parameter	Condition	25°C, 5.0V Typical	0 to 70°C Guaranteed Min.	0 to 70°C Guaranteed Max.	-40 to +85°C Guaranteed Min.	-40 to +85°C Guaranteed Max.	Unit
V_{IH}	Input High Voltage, CMOS Inputs	V_{out}=0.1V or V_{DD}-0.1V $|I_{out}|$=20μA	2.4	0.7 V_{DD}	-	0.7 V_{DD}	-	V
	Input High Voltage, TTL Inputs	V_{out}=0.1V or VDD-0.1V $|I_{out}|$=20μA	1.6	2.0	-	2.0	-	
V_{IL}	Input Low Voltage, CMOS Inputs	V_{out}=0.1V or V_{DD}-0.1V $|I_{out}|$=20μA	2.4	-	0.3 V_{DD}	-	0.3 V_{DD}	V
	Input Low Voltage, TTL Inputs	V_{out}=0.1V or V_{DD}-0.1V $|I_{out}|$=20μA	1.5	-	0.8	-	0.8	
I_{OH}	Output High Current							mA
	ON8 Output Type	V_{OH} = 3.7 Volts	>20.0	-12.0	-	-10.0	-	
	ON4 Output Type		>10.0	-6.0	-	-6.0	-	
	ON2 Output Type		>5.0	-3.0	-	-3.0	-	
I_{OL}	Output Low Current							mA
	ON8 Output Type	V_{OL} = 0.4 Volts	>20.0	12.0	-	10.0	-	
	ON4 Output Type		>10.0	6.0	-	6.0	-	
	ON2 Output Type		>5.0	3.0	-	3.0	-	
V_{T+}	Positive Threshold Voltage							V
	CMOS Schmitt Trigger	V_{out} = 0.1V or V_{DD}-0.1 $|I_{out}|$ = 20μA	3.15	-	-	-	-	
	TTL Schmitt Trigger		1.77	-	-	-	-	
V_{T-}	Negative Threshold Voltage							V
	CMOS Schmitt Trigger	V_{out} = 0.1V or VDD-0.1 $|I_{out}|$ = 20μA	2.32	-	-	-	-	
	TTL Schmitt Trigger		1.35	-	-	-	-	
V_{Hy}	Hysteresis - CMOS Schmitt Trigger	V_{T+} to V_{T-}	0.83	-	-	-	-	V
	Hysteresis - TTL Schmitt Trigger		0.42	-	-	-	-	
I_{in}	Input Leakage Current, No Pull Resistor	V_{in} = V_{DD} or V_{SS}	±0.15	-1.0	+1.0	-1.0	+1.0	μA
	Input Leakage Current, with Pullup Resistor	PUH; V_{in} = V_{SS}	-100	-50	-180	-50	-200	
		PUL; V_{in} = V_{SS}	-55	-20	-100	-20	-120	
	Input Leakage Current, with Pulldown Resistor	PDH; V_{in} = V_{DD}	175	70	310	70	380	
		PDL; V_{in} = V_{DD}	110	40	200	40	240	
I_{oz}*	Output Leakage Current, 3-State Output	Output = Hi Impedance V_{out} = V_{DD} or V_{SS}	±1.5	-1.0	+1.0	-1.0	+1.0	μA
	Output Leakage Current, Open Drain Output (Device Off)	Output = Hi Impedance V_{out} = V_{DD}	±1.5	-1.0	+1.0	-1.0	+1.0	
I_{DD}	Max Quiescent Supply Current	I_{out} = 0mA V_{in} = V_{DD} or V_{SS}	DESIGN DEPENDENT					mA

* Single-Drive Output

PACKAGING

Motorola offers three high performance, surface and through-hole mounted packages to complement the H4C Series arrays.

QFP in the MOLDED CARRIER RING

Motorola currently offers the popular EIAJ standard Plastic Quad Flat Package (QFP) in the Molded Carrier Ring (MCR). The MCR is a coplanarity and lead protection device for QFP packages, developed as an extension of the TAPE-PAK™ license and registered as a JEDEC standard. The MCR provides lead protection during manufacturing/testing and shipping (optional) for the fragile fine pitch QFP leads; e.g.: the 28mm square 208 QFP has a 0.50mm pitch with lead thickness of 0.15mm.

At this time there are plans for three sizes, AA: 36 mm ^{2}, five units per strip (max = 192 pins, rectangular packages), AB: 46 mm^2, four units per strip (max = 256 pins, square packages, and AC: 56 mm^2, three units per strip (max =312 pins, square package). Another advantage of the MCR is that it allows the use of thermally superior copper, and provides up to 1.5 Watts of power to be dissipated (dependent on temperature and ambient conditions). The MCR enables common manufacturing across the range of packages and a single test socket per ring size because of standardized ring dimensions.

After the manufacturing and testing processes the customer may elect to do trim and form by receiving the QFP in the molded carrier ring. If the customer chooses to receive the parts excised, Motorola will trim and form the parts and ship in an industry standard QFP packing tray for lead protection.

All QFPs (with or without an MCR) will be shipped by Motorola baked and drypacked. The trend towards Surface Mount Technology (SMT) with high density, thinner packages (which are more sensitive to thermal stress failure during board mounting) has led Motorola to conduct numerous studies. The resultant action is a slow bake of moisture from the SMT package and shipping in drypack bags to shield the unit from moisture absorption. Units are baked at 125 °C for 24 hours, cooled and placed in a vacuum sealed drypack with desiccant bags, humidity indicator card, and lot identification stickers.

MicroCool™ QUAD FLAT PACK

The MicroCool QFP is a new QFP compatible plastic package with higher heat dissipation capacity. It has a heat slug attached to a printed circuit board which supports a copper lead frame. The package is supported within an MCR to maintain pin coplanarity. The MicroCool is a cost effective and high pin density package that is capable of meeting the higher power dissipation (up to 3 W, depending on temperature and ambient conditions) and higher performance requirements of the H4C Series.

PGA

Motorola will continue to support PGA (Pin Grid Array) packages for thru-hole mounting. Multiple power plane construction is especially important for high performance applications.
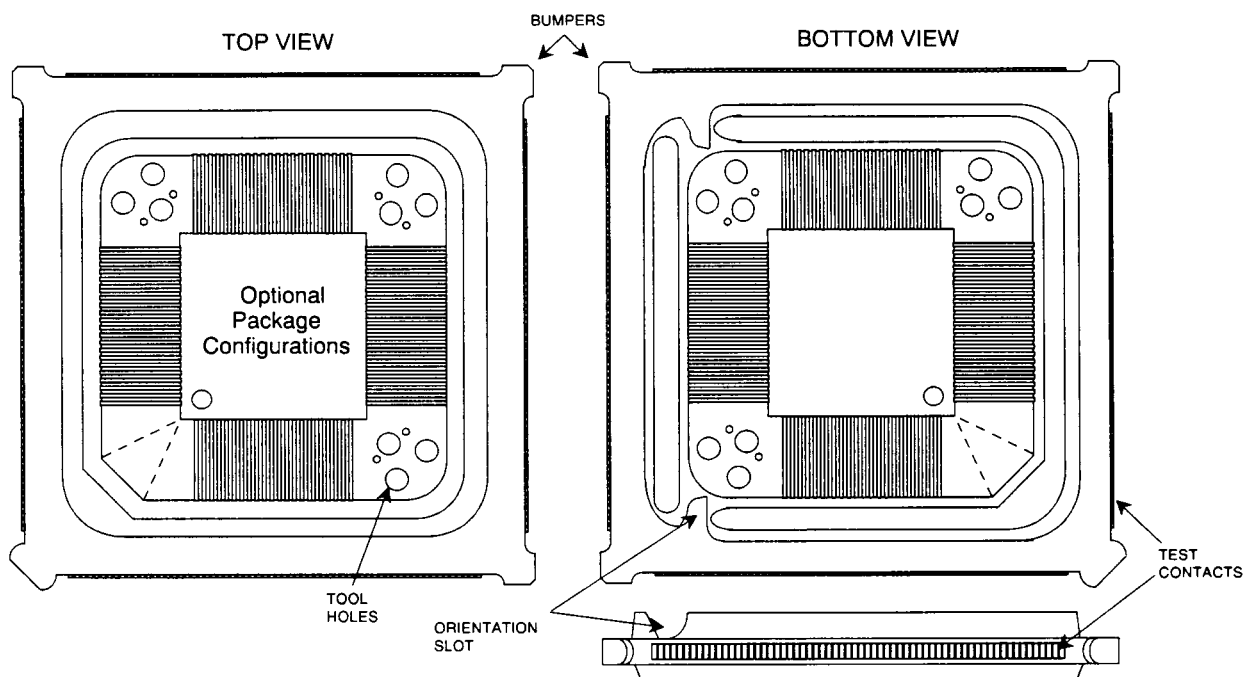

Figure 11. Sample of a Molded Carrier Ring

MCR and MicroCool are trademarks of Motorola, Inc.
TAPEPAK is a trademark of National Semiconductor, Inc.

Table 8. Package Selection

ARRAY		H4C018	H4C027	H4C035	H4C057	H4C086	H4C123	H4C161	H4C195	H4C267	H4C318
CDA Array (Die Size)		189	217	239	287	337	391	438	476	545	589
# of I/O Cells		160	196	224	284	334	416	476	524	612	668
# of Programmable Signal	WB	120	144	160	188	220	230	284	308	356	380
or Power & Ground Pads*	TAB	172	172	184	220	256	304	336	372	440	456
# of Dedicated Power	WB	16	16	16	28	40	48	60	68	84	84
& Ground Pads*	TAB	16	16	24	36	48	56	72	72	72	100
80 QFP (CU)		P,H,Q	A,H,Q	A,H,Q	A,H,Q						
100 QFP (CU)		P,H,Q	A,H,Q	A,H,Q	A,H,Q						
120 QFP (CU)		P,H,Q	A,H,Q	A,H,Q	A,H,Q	A,H,Q					
128 QFP (CD)				A,F,Q	A,F,Q						
160 QFP (CD)					A,F,Q	A,F,Q	A,F,Q	A,F,Q			
208 QFP (CD)					A,Q	A,F,Q	A,F,Q				
160 MicroCool (MCR)					A,F	A,F	A,F	A	A		
208 MicroCool (MCR)					A	A,F	A,F	A	A		
232 MicroCool (MCR)						A	A				
304 MicroCool (MCR)							A	A	A	A	
223 PGA (CD)						P,Q					
299 PGA (CD)							A,Q				
375 PGA (CD)									A,Q		
447 PGA (CD)										P	P

PGA: Ceramic Pin Grid Array   QFP: Plastic Quad Flat Pack   MCR: Molded Carrier Ring(CD)

WB: WireBond   (CU) denotes Cavity UP   (CD) denotes Cavity Down

MicroCool™ : QFP-type package with heat slug.   TAB: Tape Automated Bonding (Consult Motorola)

*Numbers indicate Wire Bond and TAB pads availability

Q = Qualified

A = Available for Option Development in OACS 2.0 release

P = Planned (consult factory for CAD availability) for OACS 2.1 release.

F = Flexible power pin assignment

H = HDCMOS Compatible

Fixed Power Pads:

    All QFP (CU) packages have completely flexible power pin assignment.

    Ceramic PGAs have some fixed power pads due to power & ground package plane requirements

AN INTEGRATED DESIGN SYSTEM SOLUTION

THE OPEN ARCHITECTURE CAD SYSTEM™

Motorola's Open Architecture CAD System (OACS™) offers a highly versatile and powerful design environment for the H4C Series, including logic synthesis, memory compilation, event-driven simulation, ATPG/fault simulation, static timing analysis and other sophisticated design tools. The OACS system integrates several of the industry's most powerful design tools and Motorola's high-performance tools in an industry standard, EDIF based CAD environment.

OACS™ FEATURES:

- Supported on HP-Apollo® and SPARC SUN®workstations
- Supports multiple technologies
- Industry standard EDIF 2.0.0 based netlist
- Synopsys' Design Compiler™ and HDL Compiler™ logic synthesis tools
- Mentor Graphics' NetEd™ (HP) and Cadence's GED™ (SUN) schematic capture packages
- Supports ESSD/LSSD SCAN, JTAG, BIST
- Sophisticated propagation delay and timing limits calculations for accurate simulation
  - Estimated and actual (back-annotated) wire capacitances
  - Includes intrinsic as well as slew rate, output pin loading and distributed RC delays
  - Continuous process, temperature, and voltage variation
- Functional, pre- and post-layout (back-annotated) delay simulations through:
  - Cadence's Verilog-XL™ (HP-Apollo and SUN)
  - Mentor Graphics' QuickSim™ (HP-Apollo)
- Comprehensive Electrical Rules Checking (ERC)
- Cadence's Veritime™ Static Timing Analysis
- Quad Design's MOTIVE™ Static Timing Analysis
- Motorola's Mustang™ Automatic Test Pattern Generation
- Motorola's TestPAS™ test vector validation and extraction
- Motorola's PrediX™ floorplanning tool
- Clock-tree synthesis, clock skew management, timing driven layout

THE OACS DESIGN FLOW

From the conception of the design to fabrication of the product, Motorola's design process flow is efficient, flexible and accurate. The design flow (see Figure 12) has three basic phases: pre-layout design, physical design, and post-layout design.

Pre-Layout Design Phase

Pre-layout design is performed by the customer using OACS tools to develop and simulate the ASIC product. In addition to schematic capture, designs can be synthesized using a hardware description language (HDL), equations, or truth tables. After the design has been described, an EDIF netlist is generated from the design database. At this point in the design phase, delay and timing calculations, netlist verification, automatic test pattern generation, or static timing analysis and fault grading can be performed. Pre-layout simulations use estimated best/typical/worst-case delays based on gate, load, slew rate, and estimated RC delays. Prior to the release of the design to layout, the test vectors created by the customer must pass specific rules to take full advantage of Motorola's production test equipment.
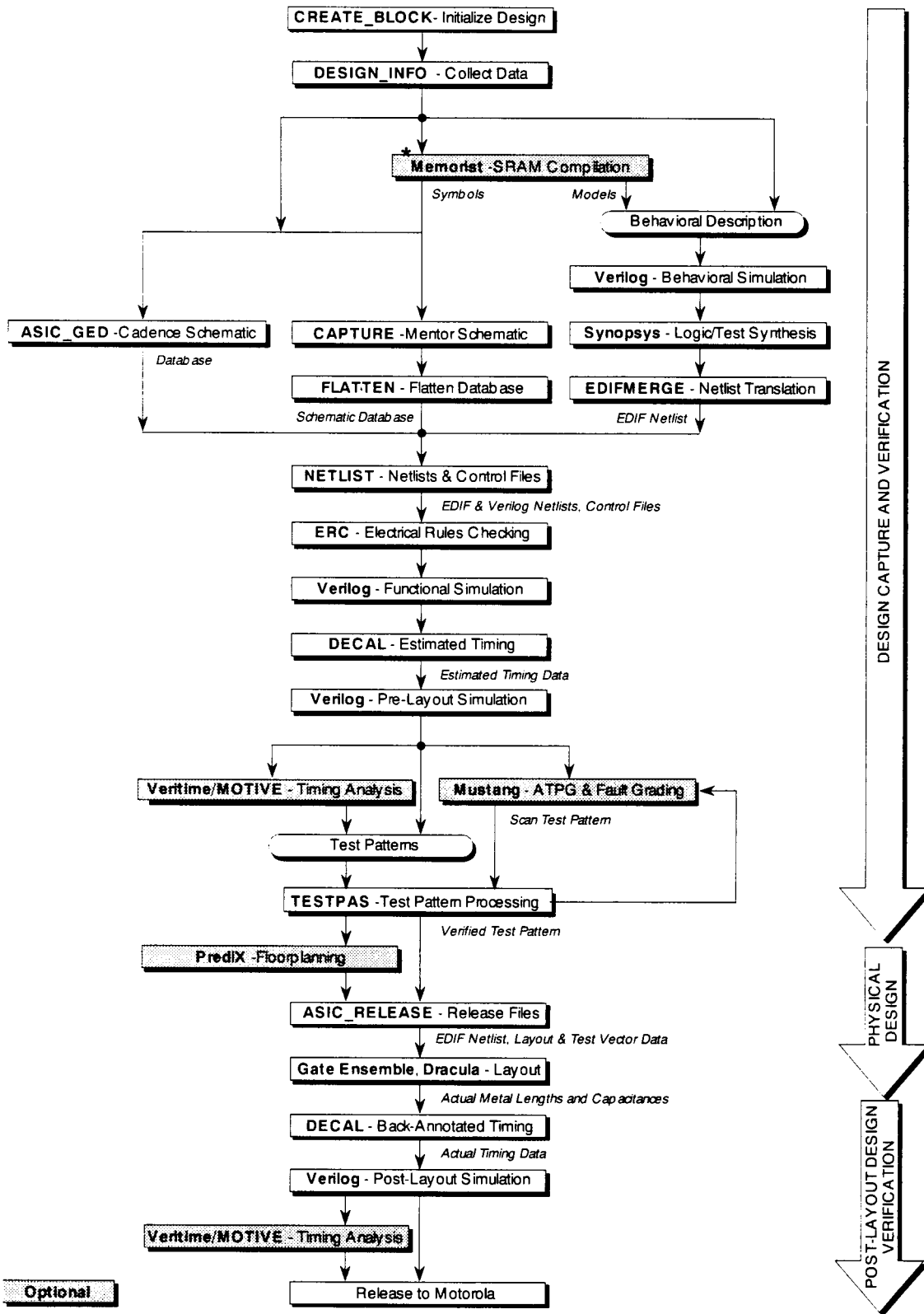
Physical Design Phase

Prior to design release, the customer may choose to floorplan the design using PrediX. Physical design is performed by Motorola's Option Development Engineers (ODE). An ODE is dedicated to each option and works directly with the customer to satisfy their layout requirements. Options such as timing driven layout and clock tree synthesis are available to optimize silicon performance. Upon completion of the physical design, back-annotation data of actual wire routing lengths and RC parasitics is provided to the customer for post-layout verification.

Post-Layout Design Phase

The post-layout design is performed by the customer to assure that the physical layout of the design satisfies all performance and timing requirements. Post-layout simulations use the actual wire lengths and RC parasitics obtained from the physical layout to provide simulations that represent the circuit's behavior in silicon. Following a successful post-layout design verification and customer sign off, Motorola will manufacture the ASIC design.

Figure 12. OACS 2.1 Design Flow

The flow chart contains the following blocks and annotations:

CREATE_BLOCK - Initialize Design

DESIGN_INFO - Collect Data

Memorist -SRAM Compilation
*

Symbols   Models

Behavioral Description

Verilog - Behavioral Simulation

ASIC_GED -Cadence Schematic

CAPTURE -Mentor Schematic

Synopsys - Logic/Test Synthesis

Database

FLAT-TEN - Flatten Database

EDIFMERGE - Netlist Translation

Schematic Database   EDIF Netlist

NETLIST - Netlists & Control Files

EDIF & Verilog Netlists, Control Files

ERC - Electrical Rules Checking

Verilog - Functional Simulation

DECAL - Estimated Timing

Estimated Timing Data

Verilog - Pre-Layout Simulation

Veritime/MOTIVE - Timing Analysis

Mustang - ATPG & Fault Grading

Scan Test Pattern

Test Patterns

TESTPAS -Test Pattern Processing

Verified Test Pattern

PredIX -Floorplanning

ASIC_RELEASE - Release Files

EDIF Netlist, Layout & Test Vector Data

Gate Ensemble, Dracula - Layout

Actual Metal Lengths and Capacitances

DECAL - Back-Annotated Timing

Actual Timing Data

Verilog - Post-Layout Simulation

Veritime/MOTIVE - Timing Analysis

Optional

Release to Motorola

* Memorist is provided
as a service

DESIGN CAPTURE AND VERIFICATION

PHYSICAL DESIGN

POST-LAYOUT DESIGN VERIFICATION

ASIC Regional Design Centers

U.S.A

California, San Jose	(408) 749-0510
Illinois, Chicago	(708) 490-9500
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International

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France, Vanves	(01) 40355877
Germany, Munich	(089) 92103-0
Holland, Eindhoven.	(04998) 61211
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1PHX33006-4 PRINTED IN USA 10/92 IMPERIAL LITHO 88612 8,000 ASIC YNAROO

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