

8-Lane 2-Port Non-Transparent PCI Express® Switch

89HPES8NT2 Product Brief

Device Overview

The 89HPES8NT2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions offering the next-generation I/O interconnect standard. The PES8NT2 is a 8-lane, 2-port peripheral chip that provides high-performance switching and non-transparent bridging (NTB) functions between a PCIe® upstream port and an NTB downstream port. The PES8NT2 is a part of the IDT PCIe System Interconnect Products and is intended to be used with IDT PCIe System Interconnect Switches. Together, the chipset targets multi-host and intelligent I/O applications such as communications, storage, and blade servers where inter-domain communication is required.

Features

- High Performance PCI Express Switch
 - Eight PCI Express lanes (2.5Gbps), two switch ports
 - Delivers 32 Gbps (4 GBps) of aggregate switching capacity
 - Low latency cut-through switch architecture
 - Support for Max Payload size up to 2048 bytes
 - Supports one virtual channel and eight traffic classes
- PCI Express Base specification Revision 1.0a compliant
- **♦** Flexible Architecture with Numerous Configuration Options
 - Supports automatic per port link width negotiation (x8, x4, x2, or x1)
 - Static lane reversal on all ports
 - Automatic polarity inversion on all lanes
 - Supports locked transactions, allowing use with legacy software

- Ability to load device configuration from serial EEPROM
- Ability to control device via SMBus

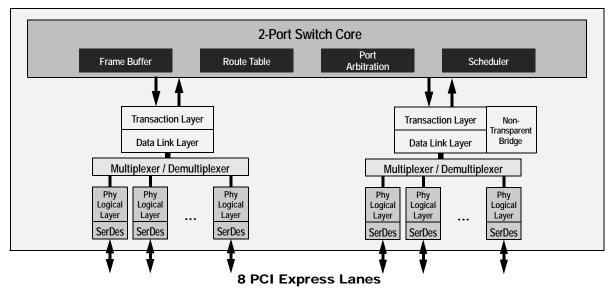
Non-Transparent Port

- Crosslink support on NTB port
- Four mapping windows supported
 - Each may be configured as a 32-bit memory or I/O window
 - May be paired to form a 64-bit memory window
- Interprocessor communication
 - · Thirty-two inbound and outbound doorbells
 - Four inbound and outbound message registers
 - Two shared scratchpad registers
- Allows up to sixteen masters to communicate through the nontransparent port
- No limit on the number of supported outstanding transactions through the non-transparent bridge
- Completely symmetric non-transparent bridge operation allows similar/same configuration software to be run
- Supports direct connection to a transparent or non-transparent port of another switch

Highly Integrated Solution

- Requires no external components
- Incorporates on-chip internal memory for packet buffering and queueing
- Integrates eight 2.5 Gbps embedded full duplex SerDes, 8B/ 10B encoder/decoder (no separate transceivers needed)

Block Diagram



x4 Upstream Port and One x4 Downstream Port

Figure 1 Internal Block Diagram

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Reliability, Availability, and Serviceability (RAS) Features

- Internal end-to-end parity protection on all TLPs ensures data integrity even in systems that do not implement end-to-end CRC (ECRC)
- Supports ECRC pass-through
- Supports Hot-Swap

Power Management

- Supports PCI Power Management Interface specification, Revision 1.1 (PCI-PM)
- Unused SerDes are disabled

Testability and Debug Features

- Built in SerDes Pseudo-Random Bit Stream (PRBS) generator
- Ability to read and write any internal register via the SMBus
- Ability to bypass link training and force any link into any mode
- Provides statistics and performance counters

Two SMBus Interfaces

- Slave interface provides full access to all software-visible registers by an external SMBus master
- Master interface provides connection for an optional serial EEPROM used for initialization
- Master interface is also used by an external Hot-Plug I/O expander
- Master and slave interfaces may be tied together so the switch can act as both master and slave
- Eight General Purpose Input/Output pins
- Packaged in 19x19mm 324 ball BGA with 1mm ball spacing

Product Description

Utilizing standard PCI Express interconnect, the PES8NT2 provides the most efficient high-performance I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. With support for non-transparent bridging, the PES8NT2 is part of the IDT PCIe System Interconnect Products that target multi-host and intelligent I/O applications requiring inter-domain communication. The PES8NT2 provides 32 Gbps (4 GBps) of aggregated, full-duplex switching capacity through 8 integrated serial lanes, using proven and robust IDT technology. Each lane provides 2.5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base specification 1.0a.

The PES8NT2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link, and Transaction layers in compliance with PCI Express Base specification Revision 1.0a. The PES8NT2 can operate either as a store and forward or cut-through switch depending on the packet size and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management.

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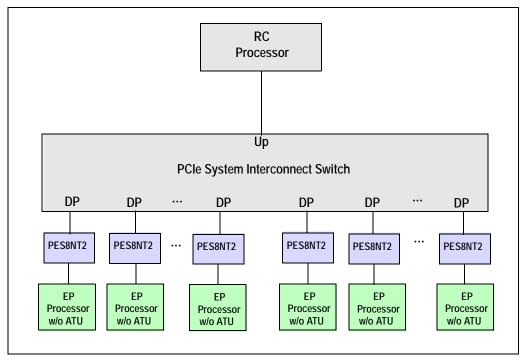


Figure 2 Embedded Compute Application - Processors With and Without Address Translation Unit (ATU) Functionality



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