REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Wanda L. Meadows

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
92-12-01

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, MICROPROCESSOR, 16-BIT AND 8/16-BIT, HCMOS, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89462
A	67268	

SHEET 1 OF 34

DESC FORM 193
JUL 91

5962-E543-92

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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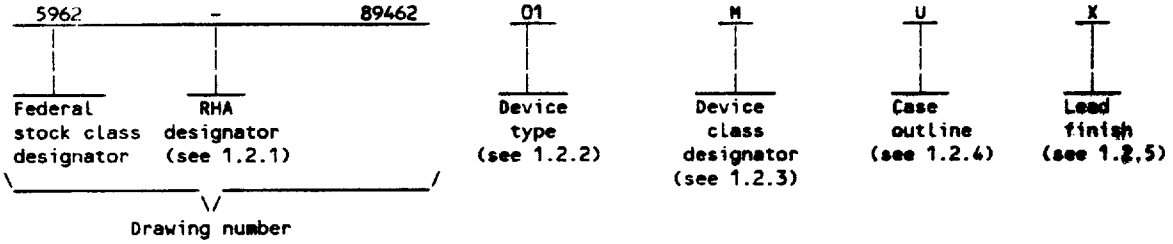
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Speed
01	68HC000-8	16-bit fixed instruction microprocessor	8 MHz
02	68HC000-10	16-bit fixed instruction microprocessor	10 MHz
03	68HC000-12	16-bit fixed instruction microprocessor	12.5 MHz
04	68HC001-8	8/16-bit fixed instruction microprocessor	8 MHz
05	68HC001-10	8/16-bit fixed instruction microprocessor	10 MHz
06	68HC001-12	8/16-bit fixed instruction microprocessor	12.5 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	CMGA2-P68	68	Grid array
X	CQCC1-N68	68	Square leadless chip carrier
Y	CDIP1-T64	64	Dual-in-line
Z	See figure 1	68	Leaded chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +6.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Storage temperature range (T_{stg})	-65°C to +150°C
Maximum power dissipation (P_D)	0.28 W
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case Z	10°C/W
Cases U, X, and Y	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage range (logic inputs) (V_{IH})	2.0 V dc to V_{CC}
Low level input voltage range (logic inputs) (V_{IL})	GND - 0.3 V to 0.8 V dc
Minimum high level output voltage (V_{OH})	V_{CC} - 0.75 V dc
Maximum low level output voltage (V_{OL})	0.55 V dc
Frequency of operation:	
Device type 01, 04	4.0 to 8.0 MHz
Device type 02, 05	4.0 to 10.0 MHz
Device type 03, 06	4.0 to 12.5 MHz
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510	-	Microcircuits, General Specification for.
MIL-I-38535	-	Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480	-	Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-1835	-	Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103	-	List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780	-	Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Input high voltage	V_{IH}	All inputs		All	1,2,3	2.0	V_{CC}	V
Input low voltage	V_{IL}			All	1,2,3	GND-0.3	0.8	V
Output high voltage, A1-A23, AS, BG, D0-D15, E, FC0-FC2, LDS, R/W, UDS, VMA	V_{OH}	V_{CC} = 4.5 V, V_{IN} = 0.8 V, 2.0 V	I_{OH} = -400 µA	All	1,2,3	V_{CC} - 0.75		V
Output low voltage, HALT	V_{OL}	V_{CC} = 4.5 V, V_{IN} = 0.8 V, 2.0 V	I_{OL} = 1.6 mA	All	1,2,3		0.55	V
Output low voltage A1-A23, BG, FC0-FC2			I_{OL} = 3.2 mA	All	1,2,3		0.55	V
Output low voltage RESET			I_{OL} = 5.0 mA	All	1,2,3		0.55	V
Output low voltage E, AS, D0-D15, LDS, R/W UDS, VMA			I_{OL} = 5.3 mA	All	1,2,3		0.55	V
Three-state (off-state) input current AS, A1-A23, D0-D15, FC0-FC2, LDS, R/W, UDS, VMA	I_{TSI}	V_{IN} = 0.5 V, 2.4 V		All	1,2,3		20	µA
Input leakage current; BERR, BGACK, BR, DTACK, CLK, IPL0-IPL2, VPA	I_{IN}	V_{IN} = 5.5 V		All	1,2,3		2.5	µA
Input leakage current; HALT, RESET				All	1,2,3		20	µA
Current dissipation	I_D	V_{CC} = 5.5 V 1/	f = 6 MHz	All	1,2,3		40	mA
			f = 8 MHz	All	1,2,3		42	
			f = 10 MHz	02,03 05,06	1,2,3		45	
			f = 12.5 MHz	05,06	1,2,3		50	
Input capacitance	C_{IN}	V_{IN} = 0 V, frequency = 1 MHz, T_C = +25°C, see 4.4.1c		All	4		20	pF
Functional tests		See 4.4.1b		All	7,8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Waveform number (see figure 4)	Group A subgroups	Device type 01,04 8 MHz		Device type 02,05 10 MHz		Device type 03,06 12.5 MHz		Unit
					Min	Max	Min	Max	Min	Max	
Frequency of operation	f	V_{CC} = 4.5 V C_L = 70 pF for $\overline{HALT}$, 130 pF all others See figure 4	---	9,10,11	4.0	8.0	4.0	10.0	4.0	12.5	MHz
Cycle time	t_{cyc}		1	9,10,11	125	250	100	250	80	250	ns
Clock pulse width (measured from 1.5 V to 1.5 V for 12 MHz)	t_{CL}		2	9,10,11	55	125	45	125	35	125	ns
	t_{CH}		3	9,10,11	55	125	45	125	35	125	ns
Clock fall time	t_{Cf}		4	9,10,11		10		10		5	ns
Clock rise time	t_{Cr}		5	9,10,11		10		10		5	ns
Clock low to address valid	t_{CLAV}		6	9,10,11		70		60		55	ns
Clock high to FC valid	t_{CHFCV}		6A	9,10,11		70		60		55	ns
Clock high to address, data bus high impedance (maximum)	t_{CHADZ}		7 2/	9,10,11		80		70		60	ns
Clock high to address/FC invalid (minimum)	t_{CHAFI}		8 3/	9,10,11	0		0		0		ns
Clock high to $\overline{AS}$, $\overline{DS}$ asserted	t_{CHSL}		9 4/	9,10,11	0 5/	60	0 5/	55	0 5/	55	ns
Clock high to $\overline{AS}$, $\overline{DS}$ negated	t_{CHSLn}		6/	9,10,11							
Address valid to $\overline{AS}$, $\overline{DS}$ asserted (read)/ $\overline{AS}$ asserted (write)	t_{AVSL}		11 7/	9,10,11	30		20		0		ns
FC valid to $\overline{AS}$, $\overline{DS}$ asserted (read)/ $\overline{AS}$ asserted (write)	t_{FCVSL}		11A 7/ 8/	9,10,11	60		50		40		ns
Clock low to $\overline{AS}$, $\overline{DS}$ negated	t_{CLSH}		12 4/	9,10,11		70		55		50	ns
$\overline{AS}$, $\overline{DS}$ negated to address/FC invalid	t_{SHAFI}		13 7/ 8/	9,10,11	30		20		10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Waveform number (see figure 4)	Group A subgroups	Device type 01,04 8 MHz		Device type 02,05 10 MHz		Device type 03,06 12.5 MHz		Unit
					Min	Max	Min	Max	Min	Max	
$\overline{AS}$, (and $\overline{DS}$ read) width asserted	t_{SL}	V_{CC} = 4.5 V C_L = 70 pF for $\overline{HALT}$, 130 pF all others See figure 4	14 7/ 8/	9,10,11	240		195		160		ns
$\overline{DS}$ width asserted (write)	t_{DSL}		14A 7/ 8/	9,10,11	115		95		80		ns
$\overline{AS}$, $\overline{DS}$ width negated	t_{SH}		15 7/ 8/	9,10,11	150		105		65		ns
Clock high to control bus high impedance	t_{CHCZ}		16 2/	9,10,11		80		70		60	ns
$\overline{AS}$, $\overline{DS}$ negated to R/$\overline{W}$ invalid	t_{SHRH}		17 7/ 8/	9,10,11	40		20		10		ns
Clock high to R/$\overline{W}$ high (read)	t_{CHRH}		18 4/	9,10,11	0	70	0	60	0	60	ns
Clock high to R/$\overline{W}$ high (read) (minimum)	t_{CHRHn}		6/	9,10,11							ns
Clock high to R/$\overline{W}$ low (write)	t_{CHRL}		20 4/	9,10,11		70		60		60	ns
$\overline{AS}$ asserted to R/$\overline{W}$ valid (write)	t_{ASRV}		20A 7/ 8/ 9/	9,10,11		20		20		20	ns
Address valid to R/$\overline{W}$ low (write)	t_{AVRL}		21 7/ 8/	9,10,11	20		0		0		ns
FC valid to R/$\overline{W}$ low (write)	t_{FCVRL}		21A 7/ 8/	9,10,11	60		50		30		ns
R/$\overline{W}$ low to $\overline{DS}$ asserted (write)	t_{RLSL}		22 7/ 8/	9,10,11	80		50		30		ns
Clock low to data out valid (write)	t_{CLDO}		23	9,10,11		70		55		55	ns
Clock high to R/$\overline{W}$, $\overline{VMA}$ high impedance	t_{CHRZ}		10/	9,10,11							ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Waveform number (see figure 4)	Group A subgroups	Device type 01,04 8 MHz		Device type 02,05 10 MHz		Device type 03,06 12.5 MHz		Unit
					Min	Max	Min	Max	Min	Max	
$\overline{AS}$, $\overline{DS}$ negated to data-out invalid (write)	t_{SHDOI}	V_{CC} = 4.5 V C_L = 70 pF for $\overline{HALT}$, 130 pF all others	25 7/ 8/	9,10,11	30		20		15		ns
Data-out valid to $\overline{DS}$ asserted (write)	t_{DOSL}	See figure 4	26 7/	9,10,11	30		20		15		ns
Data-in to clock low (setup time) on read)	t_{DICL}		27 8/ 11/	9,10,11	15		10		10		ns
$\overline{AS}$, $\overline{DS}$ negated to $\overline{DTACK}$ negated (asynchronous hold)	t_{SHDAH}		28 7/ 8/	9,10,11	0	245	0	190	0	150	ns
$\overline{AS}$, $\overline{DS}$ negated to data-in invalid (hold time on read)	t_{SHDII}		29 8/	9,10,11	0		0		0		ns
$\overline{AS}$, $\overline{DS}$ negated to $\overline{BERR}$ negated	t_{SHBEH}		30 8/	9,10,11	0		0		0		ns
$\overline{DTACK}$ asserted to data-in valid setup time)	t_{DALDI}		31 7/ 8/ 11/	9,10,11		90		65		50	ns
$\overline{HALT}$ and $\overline{RESET}$ input transition time	$t_{RHr,f}$		32 2/	9,10,11	0	200	0	200	0	200	ns
Clock high to $\overline{BG}$ asserted	t_{CHGL}		33	9,10,11		70		60		50	ns
Clock high to $\overline{BG}$ negated	t_{CHGH}		34 8/	9,10,11		70		60		50	ns
$\overline{BR}$ asserted to $\overline{BG}$ asserted	t_{BRLGL}		35 8/	9,10,11	1.5	3.5 +90 ns	1.5	3.5 +80 ns	1.5	3.5 +70 ns	Clk. per.
$\overline{BR}$ negated to $\overline{BG}$ negated	t_{BRHGH}		36 8/ 12/	9,10,11	1.5	3.5 +90 ns	1.5	3.5 +80 ns	1.5	3.5 +70 ns	Clk. per.
$\overline{BGACK}$ asserted to $\overline{BG}$ negated	t_{GALGH}		37 8/	9,10,11	1.5	3.5 +90 ns	1.5	3.5 +80 ns	1.5	3.5 +70 ns	Clk. per.
$\overline{BGACK}$ asserted to $\overline{BR}$ negated	t_{GALBRH}		37A 8/	9,10,11	20 ns	1.5	20 ns	1.5	20 ns	1.5	Clk. per.

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Waveform number (see figure 4)	Group A subgroups	Device type 01,04 8 MHz		Device type 02,05 10 MHz		Device type 03,06 12.5 MHz		Unit
					Min	Max	Min	Max	Min	Max	
$\overline{BG}$ asserted to control, address, data bus high impedance (AS negated)	t_{GLZ}	V_{CC} = 4.5 V C_L = 70 pF for $\overline{HALT}$, 130 pF all others See figure 4	38 2/	9,10,11		80		70		60	ns
$\overline{BG}$ width negated	t_{GH}		39 8/	9,10,11	1.5		1.5		1.5		Clk. per.
Clock low to $\overline{VMA}$ asserted	t_{CLVML}		40	9,10,11		70		70		70	ns
Clock low to E transition	t_{CLET}		41	9,10,11		70		55		45	ns
E output rise and fall time	$t_{Er,f}$		42 8/	9,10,11		25		25		25	ns
$\overline{VMA}$ asserted to E high	t_{VMLEH}		43 8/	9,10,11	200		150		90		ns
$\overline{AS}$, $\overline{DS}$ negated to $\overline{VPA}$ negated	t_{SHVPH}		44 8/	9,10,11	0	120	0	90	0	70	ns
E low to control, address bus invalid (address hold time)	t_{ELCAI}		45 8/	9,10,11	30		10		10		ns
$\overline{BGACK}$ width low	t_{GAL}		46 8/	9,10,11	1.5		1.5		1.5		Clk. per.
Asynchronous input setup time	t_{ASI}		47 11/	9,10,11	20		20		20		ns
$\overline{BERR}$ asserted to $\overline{DTACK}$ asserted	t_{BELDAL}		48 8/ 13/	9,10,11	20		20		20		ns
$\overline{AS}$, $\overline{DS}$ negated to E low	t_{SHEL}		49 8/ 14/	9,10,11	-70	+70	-55	+55	-45	+45	ns
E width high	t_{EH}		50 8/	9,10,11	450		350		280		ns
E width low	t_{EL}		51 8/	9,10,11	700		550		440		ns
E executed rise time	t_{EICHX}		8/ 15/	9,10,11							ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Waveform number (see figure 4)	Group A subgroups	Device type 01,04 8 MHz		Device type 02,05 10 MHz		Device type 03,06 12.5 MHz		Unit
					Min	Max	Min	Max	Min	Max	
Data-out hold from clock high	t_{CHDOI}	V_{CC} = 4.5 V C_L = 70 pF for $\overline{HALT}$, 130 pF all others See figure 4	53 8/	9,10,11	0		0		0		ns
E low to data-out invalid	t_{ELDOI}		54 8/ 16/	9,10,11	30		20		15		ns
R/$\overline{W}$ asserted to data bus impedance change	t_{RLDBD}		55 8/	9,10,11	30		20		10		ns
$\overline{HALT}$, $\overline{RESET}$ pulse width	t_{HRPW}		56 8/ 13/ 17/	9,10,11	10		10		10		Clk. per.
$\overline{BGACK}$ negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ driven	t_{GASD}		57 8/	9,10,11	1.5		1.5		1.5		Clk. per.
$\overline{BGACK}$ negated to FC, VMA driven	t_{GAFD}		57A 8/	9,10,11	1.0		1.0		1.0		Clk. per.
$\overline{BR}$ negated to $\overline{AS}$, $\overline{DS}$ R/$\overline{W}$ driven	t_{RHSD}		58 8/ 12/	9,10,11	1.5		1.5		1.5		Clk. per.
$\overline{BR}$ negated to FC, VMA driven	t_{RHFD}		58A 8/ 12/	9,10,11	1.0		1.0		1.0		Clk. per.

1/ Currents listed are with no loading.
2/ Guaranteed to the limits specified in table I, if not tested. Available upon request.
3/ FC invalid; as a minimum, tested initially and for process and design changes only.
4/ For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the value given in the maximum column.
5/ Not tested, for system design purposes only.
6/ Combined with the above parameter. Previous specification of 0 ns was theoretical and not attainable.
7/ Actual value depends on clock period.
8/ As a minimum, tested initially and for process or design changes only.
9/ When AS and R/W are equally loaded (±20 percent), subtract 10 nanoseconds from the values given for these parameters.
10/ Combined with 16, control bus specification.
11/ If the asynchronous setup time (47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (31) requirement can be ignored. The data must only satisfy the data-in clock-low setup time (27) for the following cycle.
12/ The processor will negate BG and begin driving the bus again if external arbitration logic negates BR before asserting BGACK.
13/ If 47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, 48 may be 0 nanoseconds.
14/ The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification 49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of the E clock.
15/ Deleted.
16/ After V_{CC} has been applied for 100 ms.
17/ For power up, the device must be held in $\overline{RESET}$ state for 100 ms to all stabilization of on-chip circuitry. After the system is powered up, 56 refers to the minimum pulse width required to reset the system.

Device types 01, 02, and 03

Case outline Z

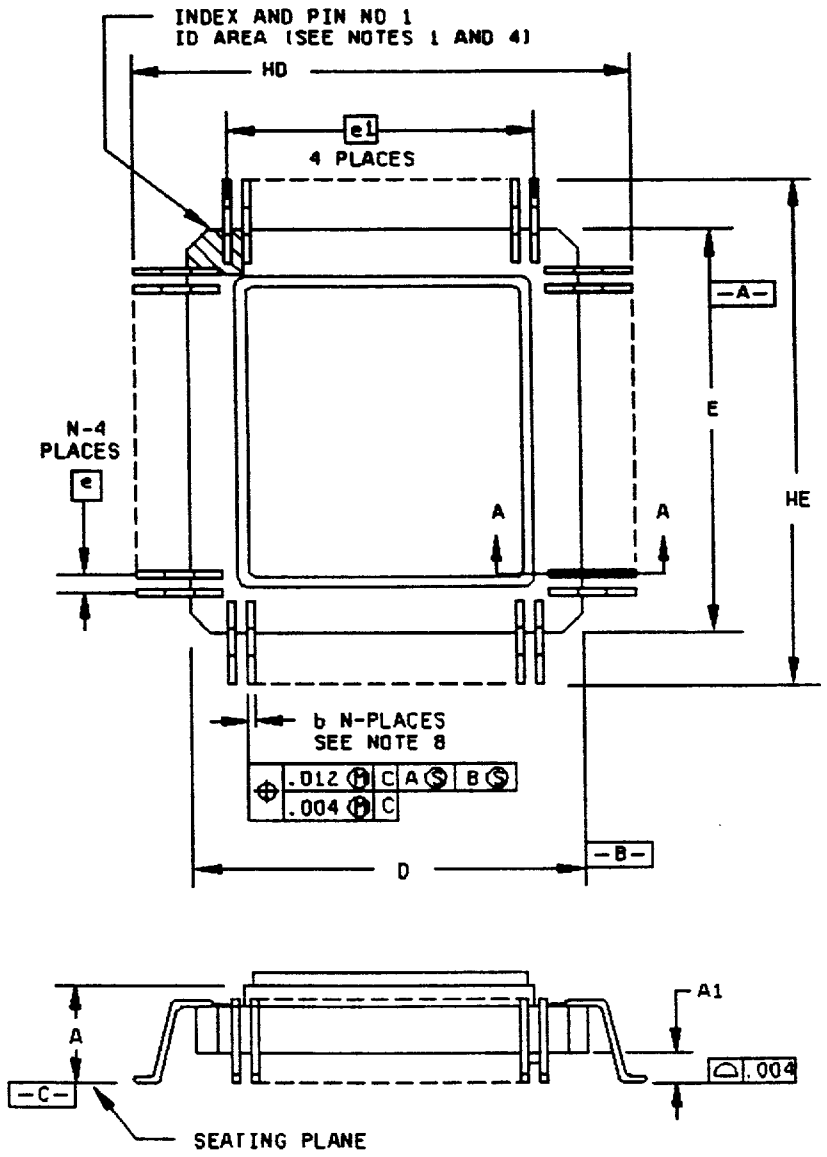


FIGURE 1. Case outline.

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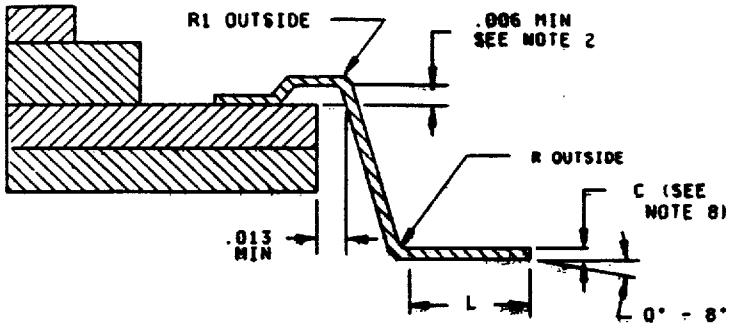
DESC FORM 193A
JUL 91

9004708 0004818 668

Case outline Z



SECTION A-A

Case Z				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.125		3.175
A1	.018	.035	0.457	0.889
b	.018	.030	0.457	0.762
c	.005	.010	0.127	0.254
D/E	.940	.960	23.88	24.38
e	.050 BSC		---	
e1	.800 BSC		---	
HD/HE	1.133	1.147	28.78	29.13
L	.024	.040	0.610	1.016
N	68		68	
R	.011	.034	0.279	0.864
R1	.009	---	0.229	---

NOTES:
1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction.
3. Dimension N: Number of terminals.
4. Corner shapes (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
5. Metric equivalents are given for general information only.
6. Controlling dimension: Inch.
7. Datums X and Y to be determined where center leads exit the body.
8. Dimensions b and c include lead finish.

FIGURE 1. Case outline - Continued.

Device types 01, 02, and 03

Case outline U (bottom view)

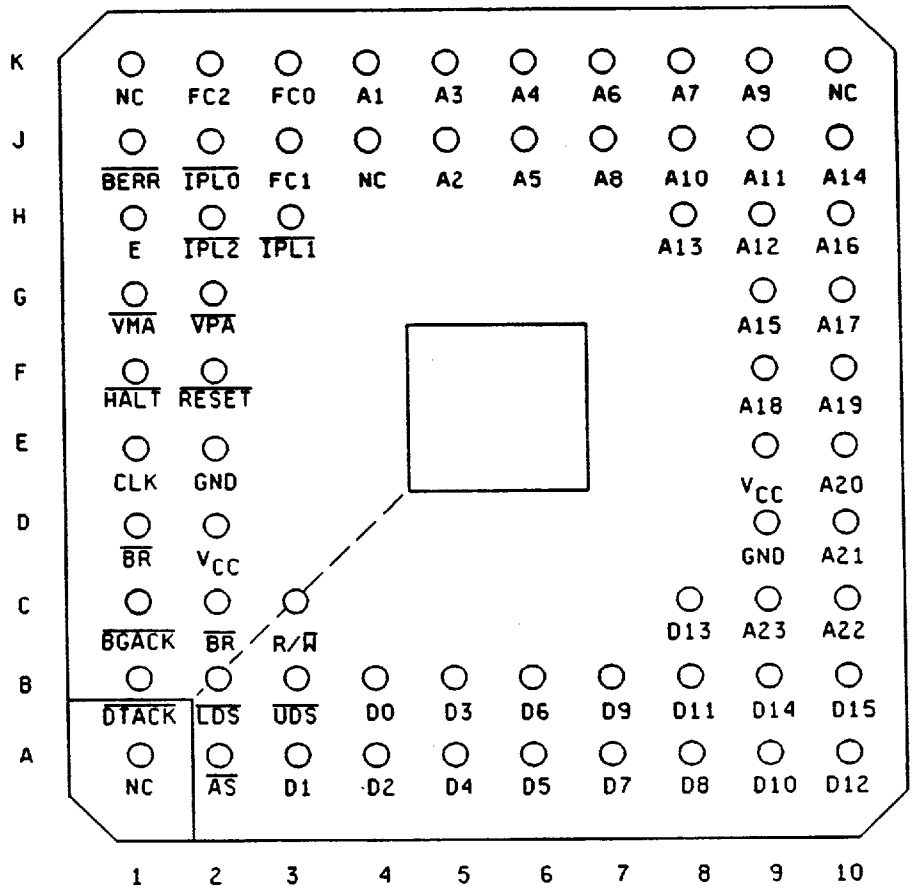


FIGURE 2. Terminal connections.

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Device types 04, 05, and 06

Case outline U (bottom view)

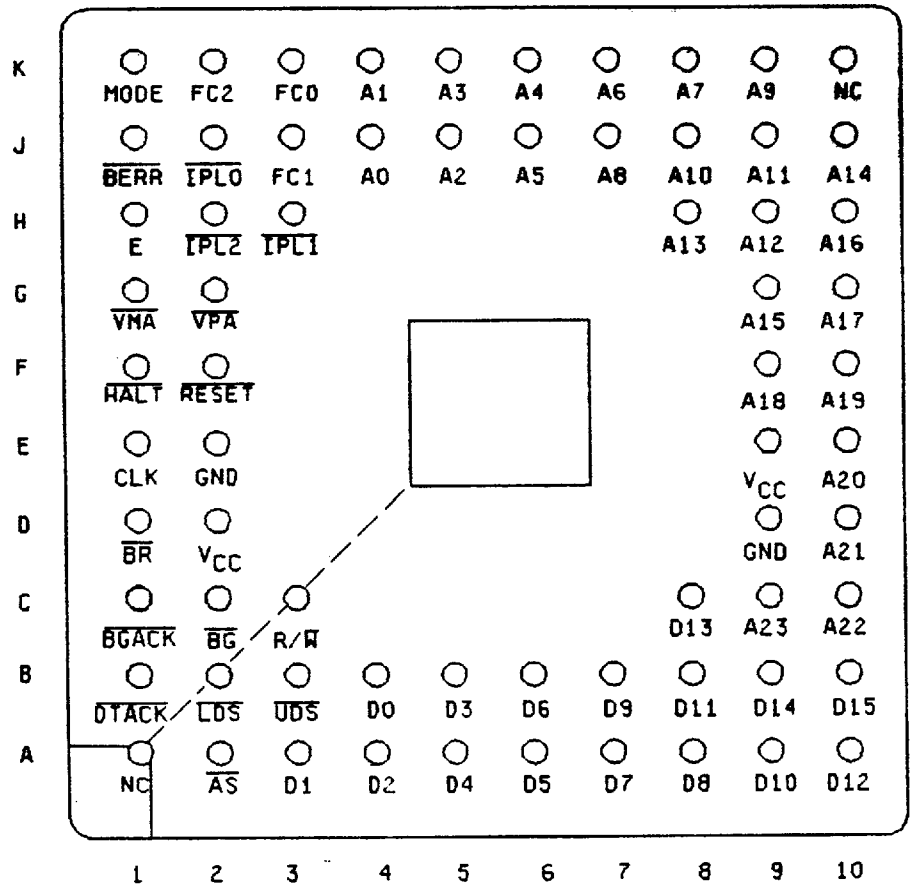

FIGURE 2. Terminal connections - Continued.

Device types 01, 02, and 03

Case outline X (top view)

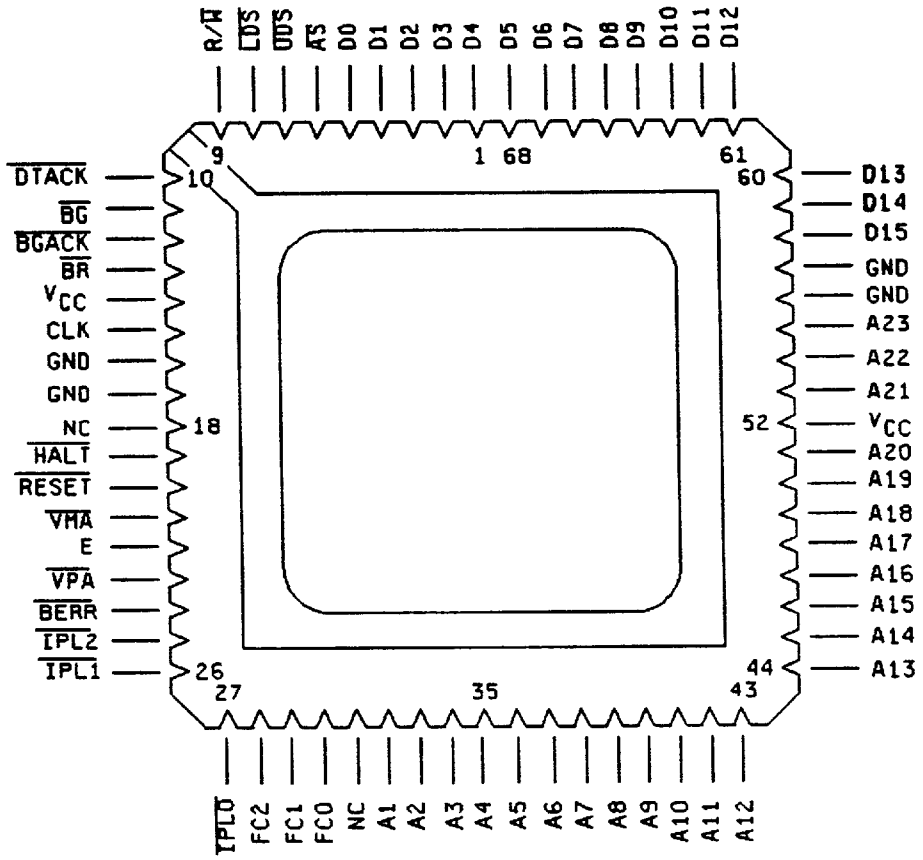

FIGURE 2. Terminal connections - Continued.

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Device types 01, 02, and 03

Case outline Y (top view)

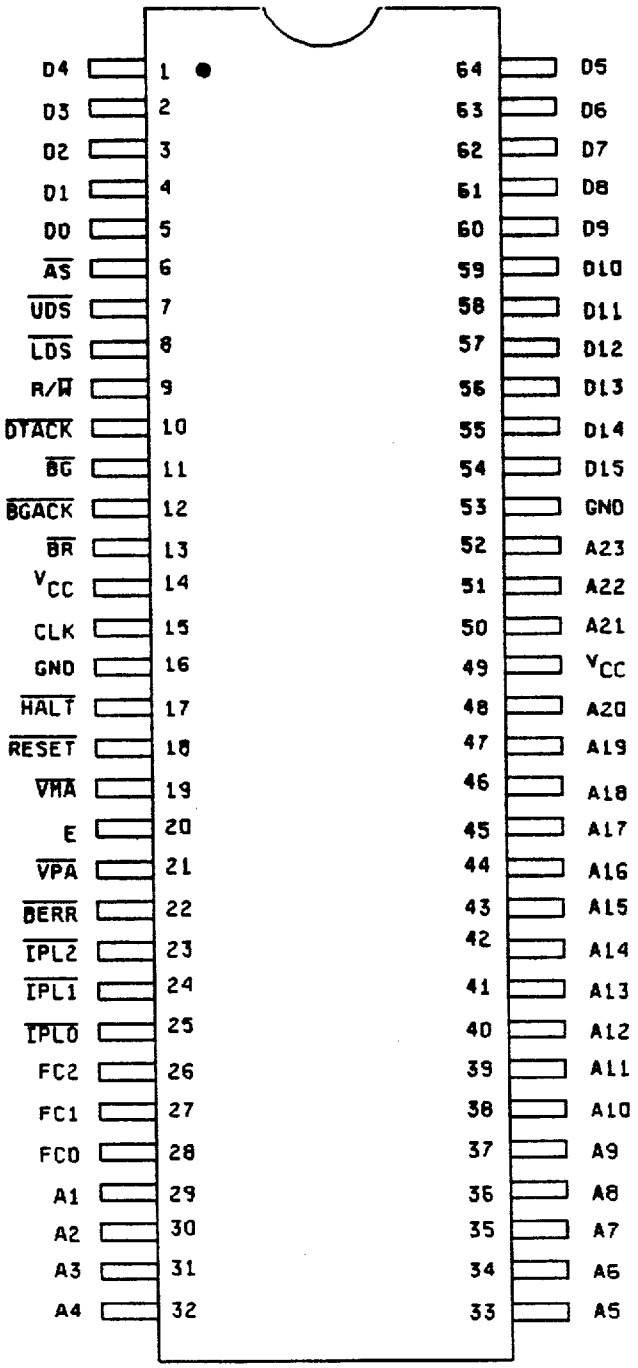
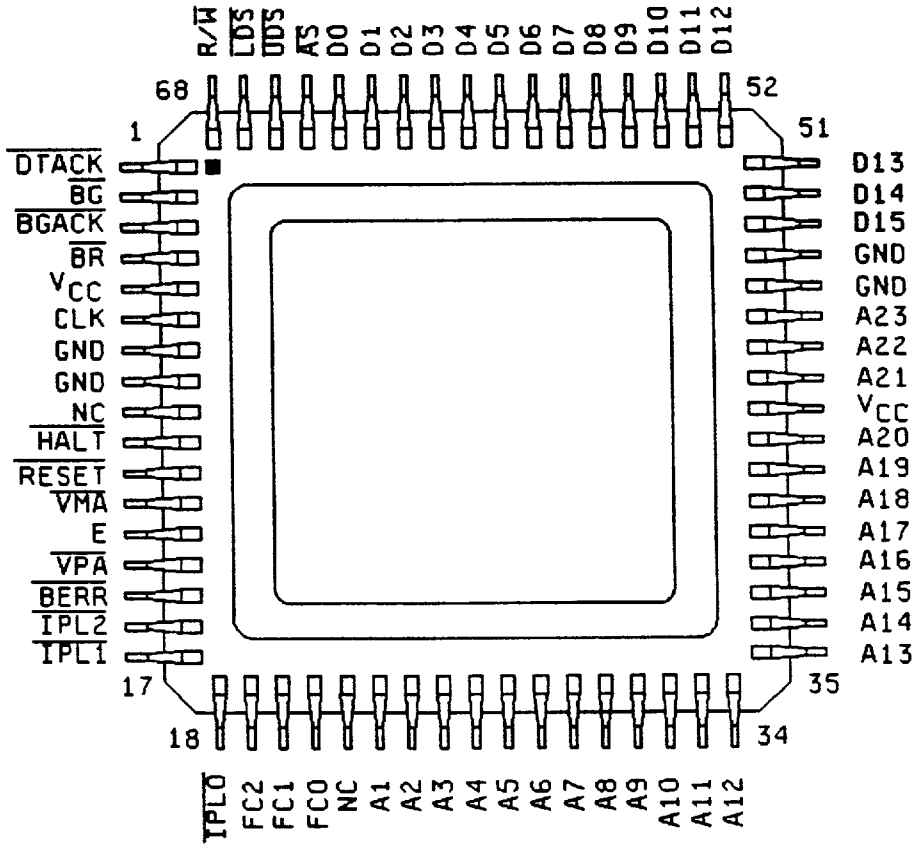


FIGURE 2. Terminal connections - Continued.

Device types 01, 02, and 03

Case outline Z (top view)



NOTE: NC = no connection.

FIGURE 2. Terminal connections - Continued.

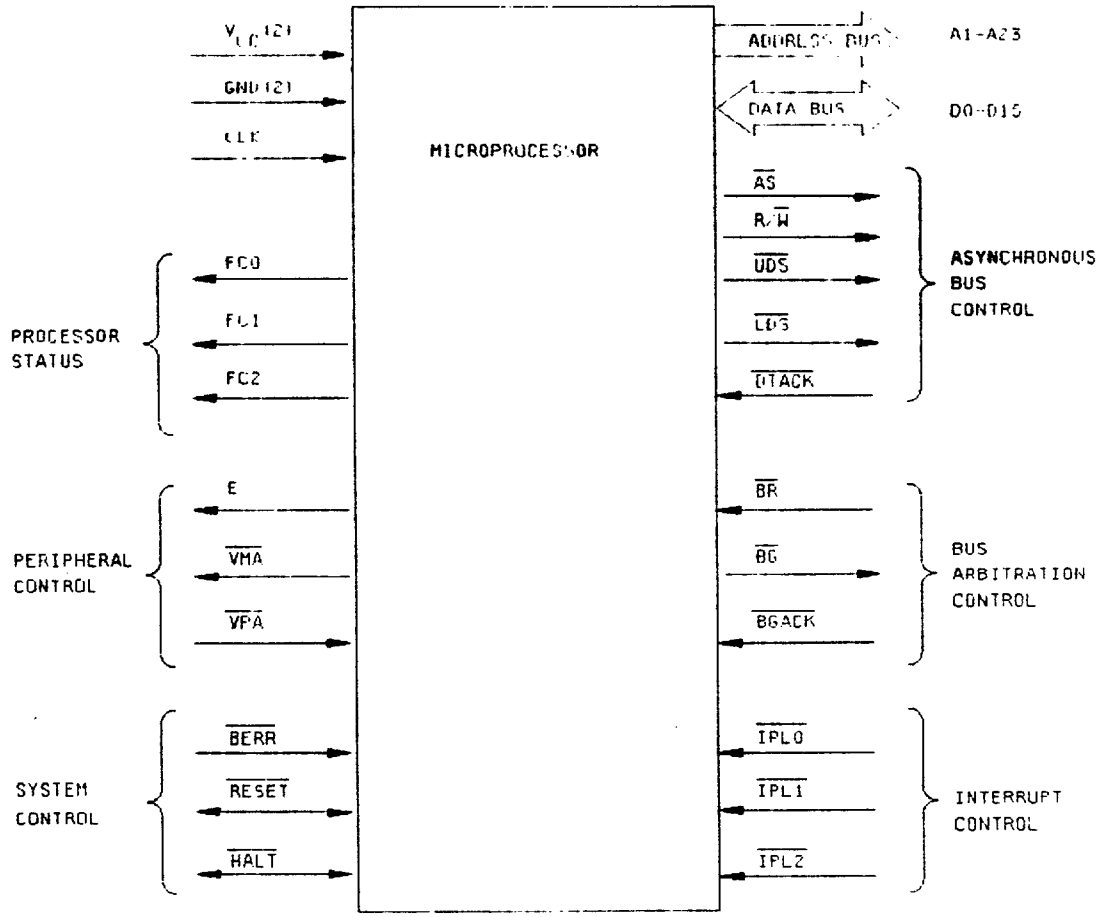


FIGURE 3. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89462
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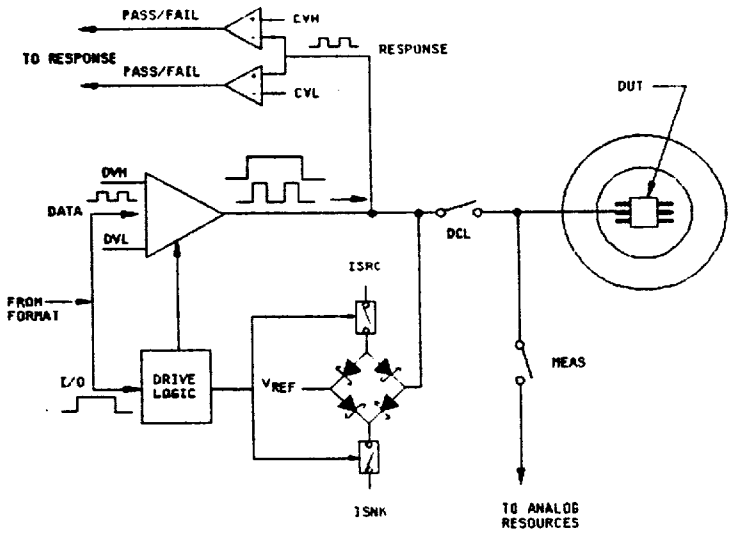
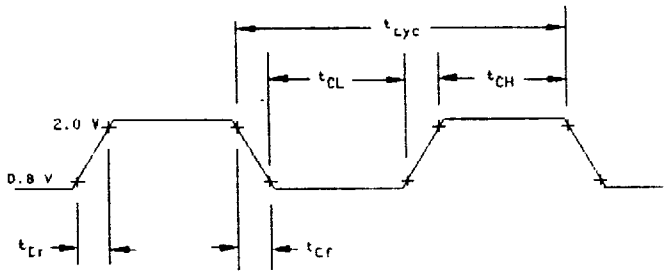


Test circuit



Input clock waveform

FIGURE 4. Switching test circuit and waveforms.

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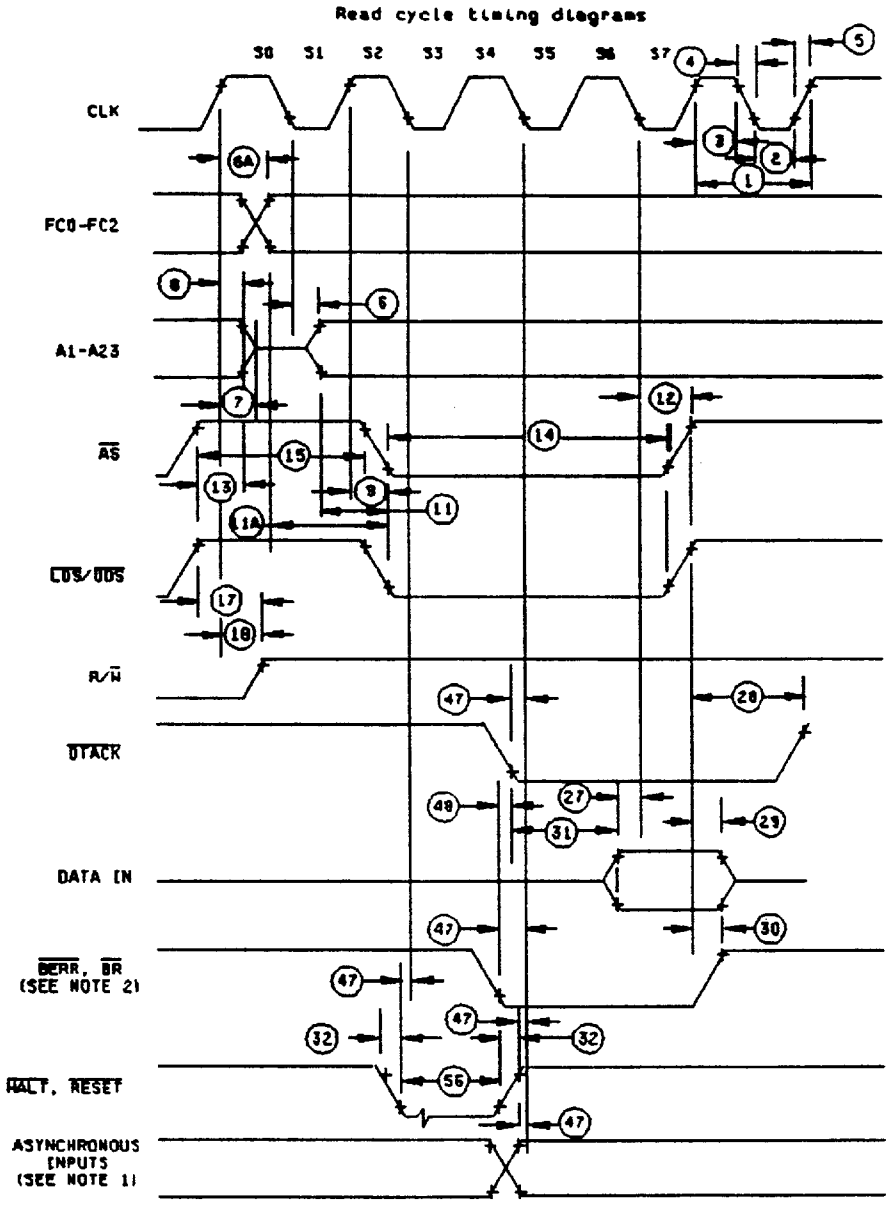
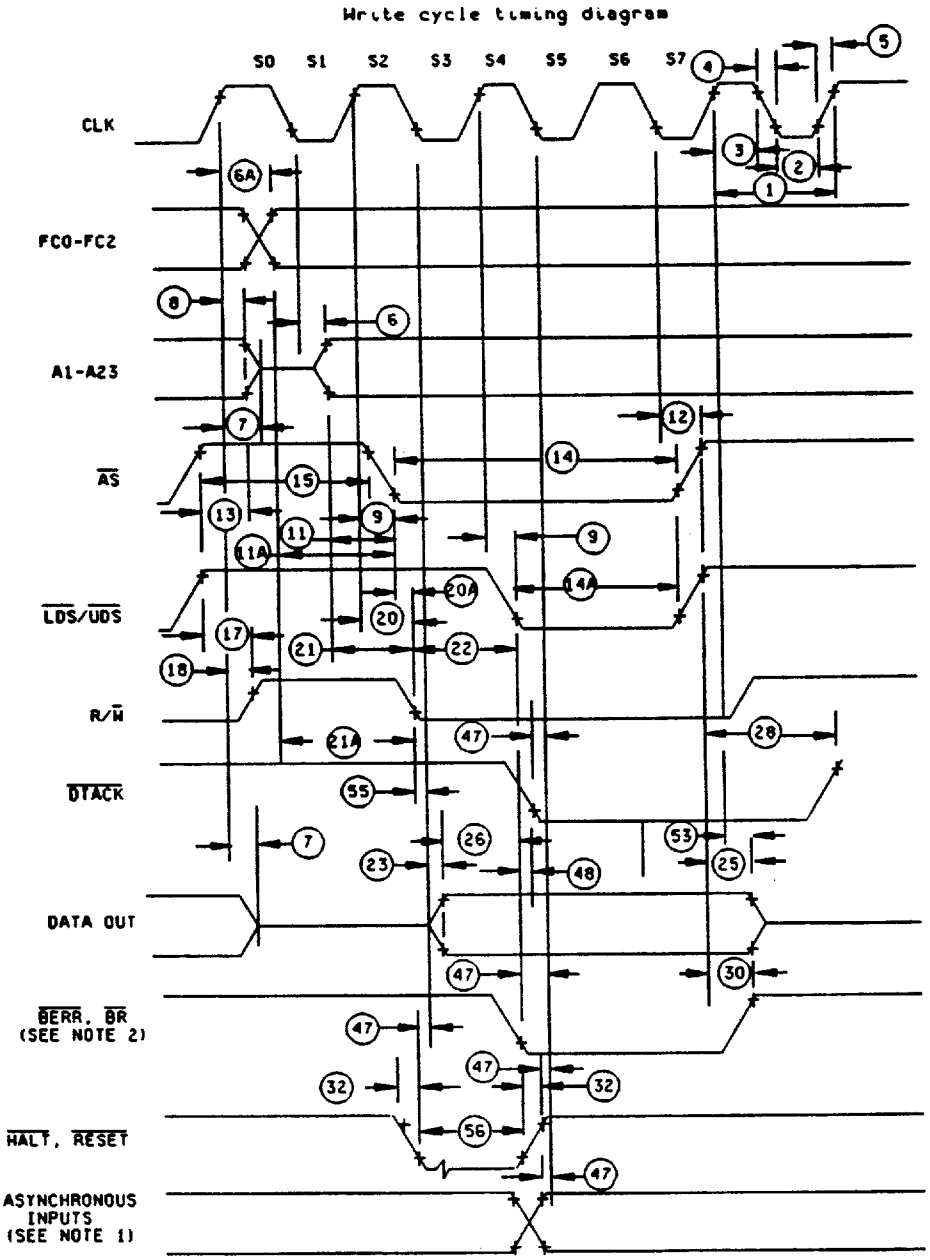
		REVISION LEVEL	SHEET 19



NOTES:
1. Setup time for the asynchronous input $\overline{\text{BGACK}}$, $\overline{\text{IPL0}}$-$\overline{2}$, and $\overline{\text{VPA}}$ guarantees their recognition at the next falling edge of the clock.
2. BR need fall at this time only to insure being recognized at the end of this bus cycle.
3. Unless otherwise noted, timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 and 2.0 volts.

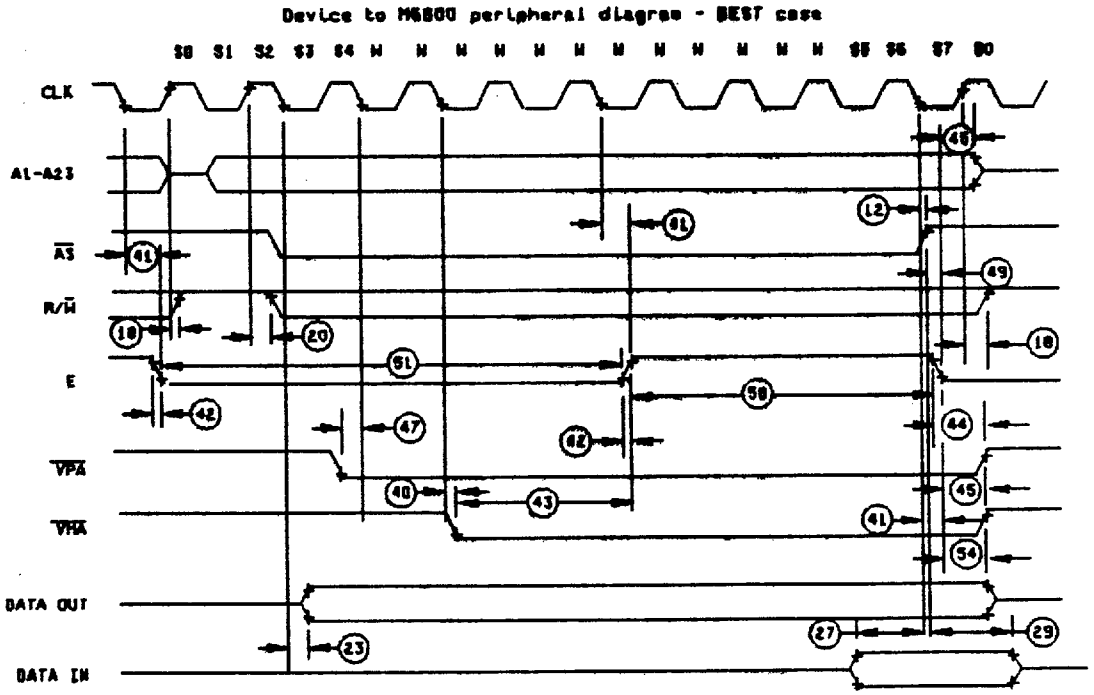
FIGURE 4. Switching test circuit and waveforms - Continued.



NOTES:

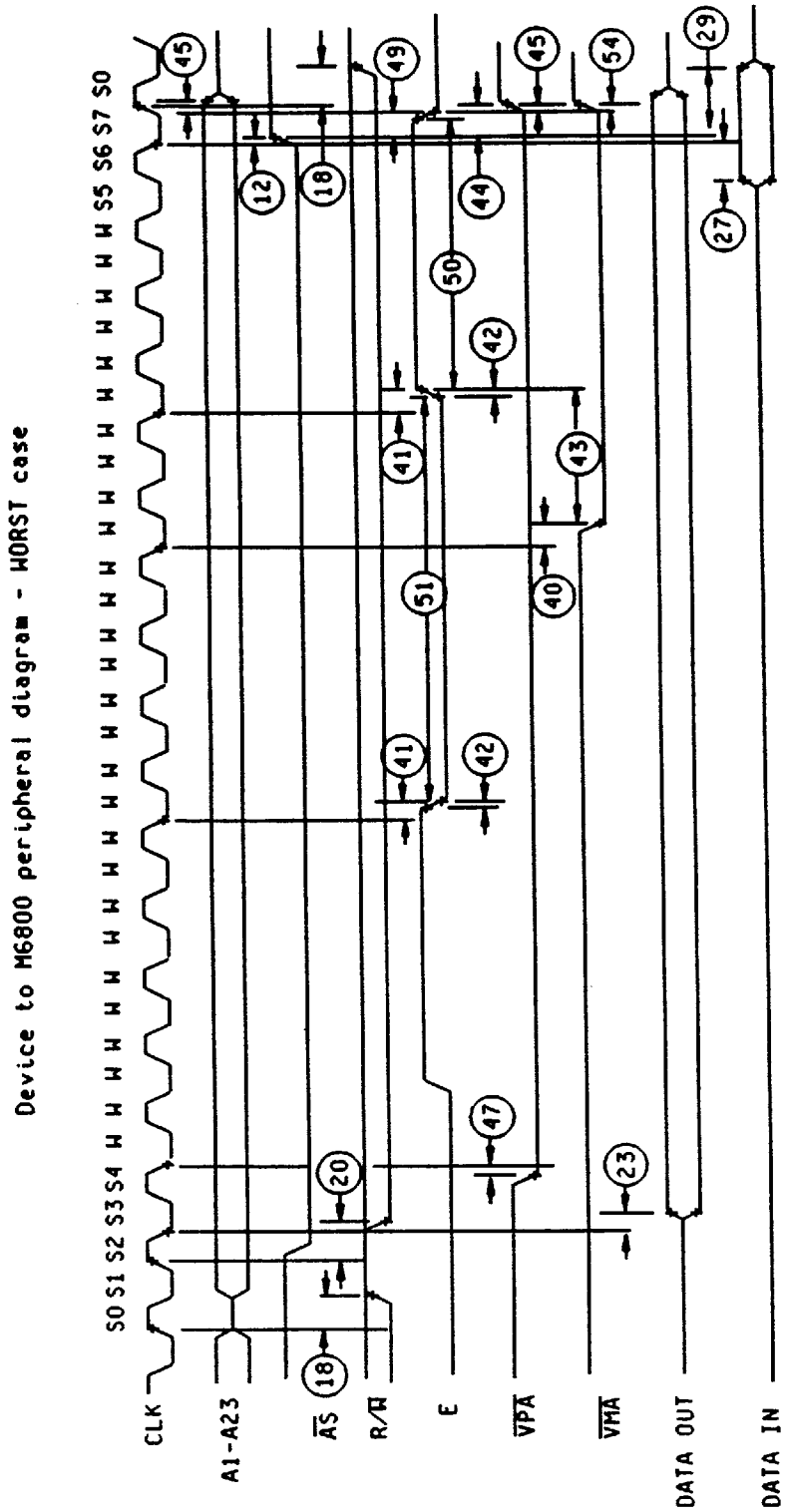
1. Unless otherwise noted, timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 volts and 2.0 volts.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (specification 20A).

FIGURE 4. Switching test circuit and waveforms - Continued.



NOTE: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the best case possibly attainable.

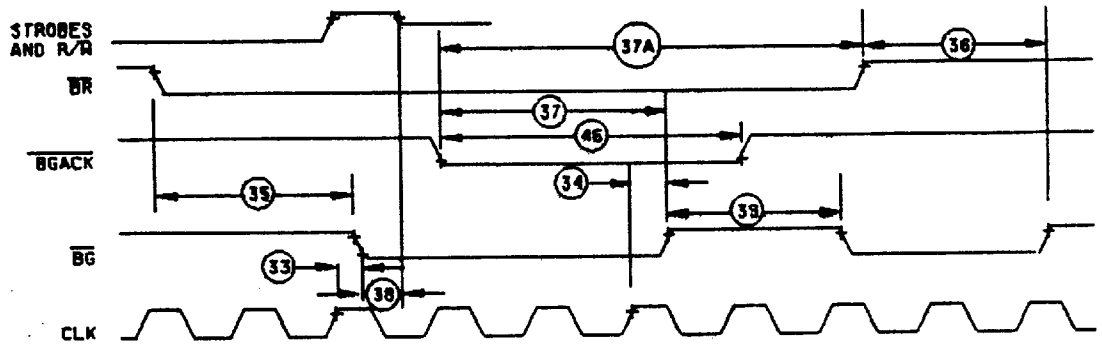
FIGURE 4. Switching test circuit and waveforms - Continued.



NOTE: This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the worst case possible attainable.

FIGURE 4. Switching test circuit and waveform - Continued.

Bus arbitration timing diagram



NOTE: Setup time to the clock (47) for the asynchronous inputs $\overline{\text{BERR}}$, $\overline{\text{BGACK}}$, $\overline{\text{BR}}$, $\overline{\text{DTACK}}$, $\overline{\text{IPL0}}$-$\overline{\text{IPL2}}$, and $\overline{\text{VPA}}$ guarantees their recognition at the next falling edge of the clock.

FIGURE 4. Switching test circuit and waveforms - Continued.

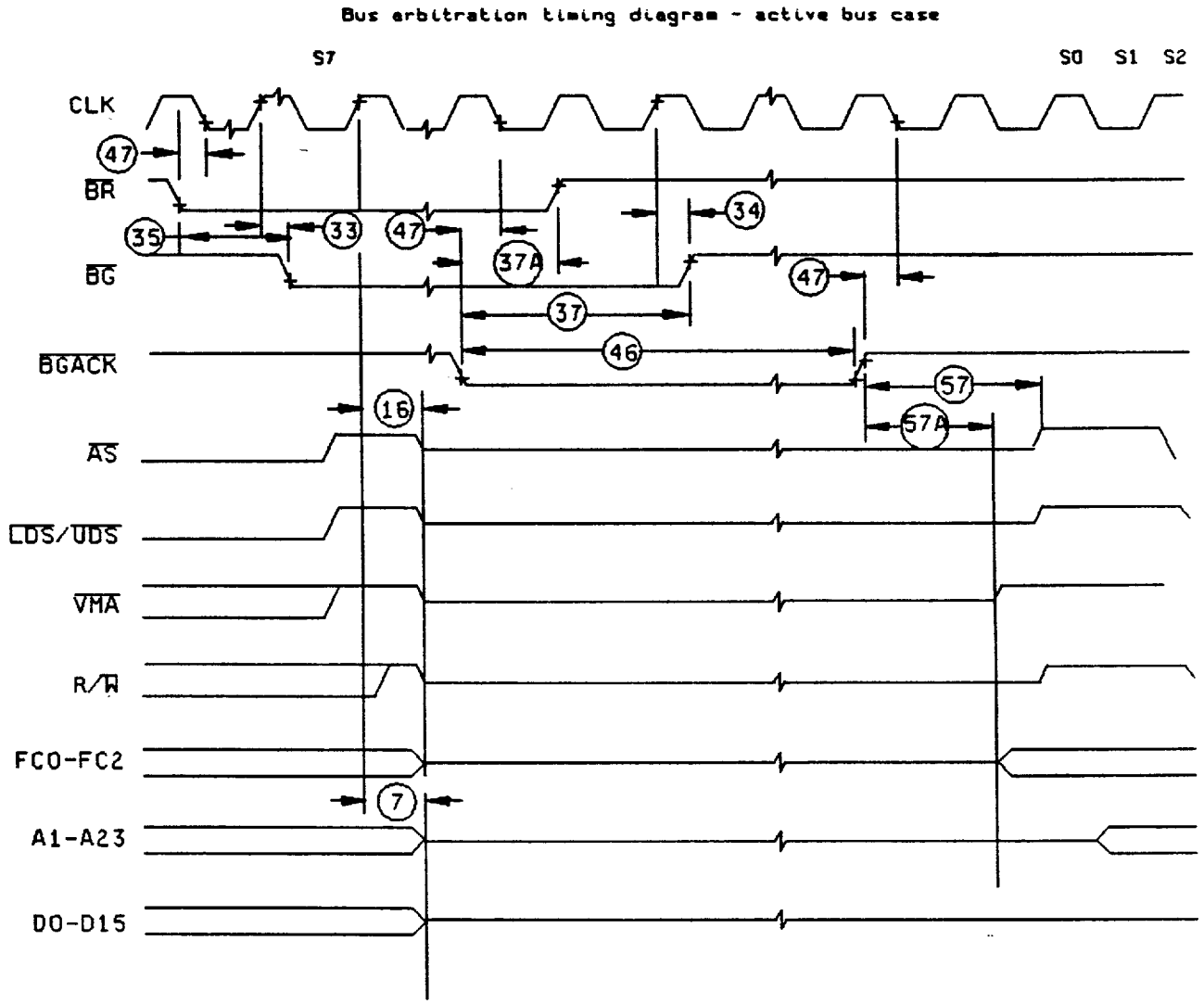


FIGURE 4. Switching test circuit and waveforms - Continued.

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Bus arbitration timing diagram - idle bus case

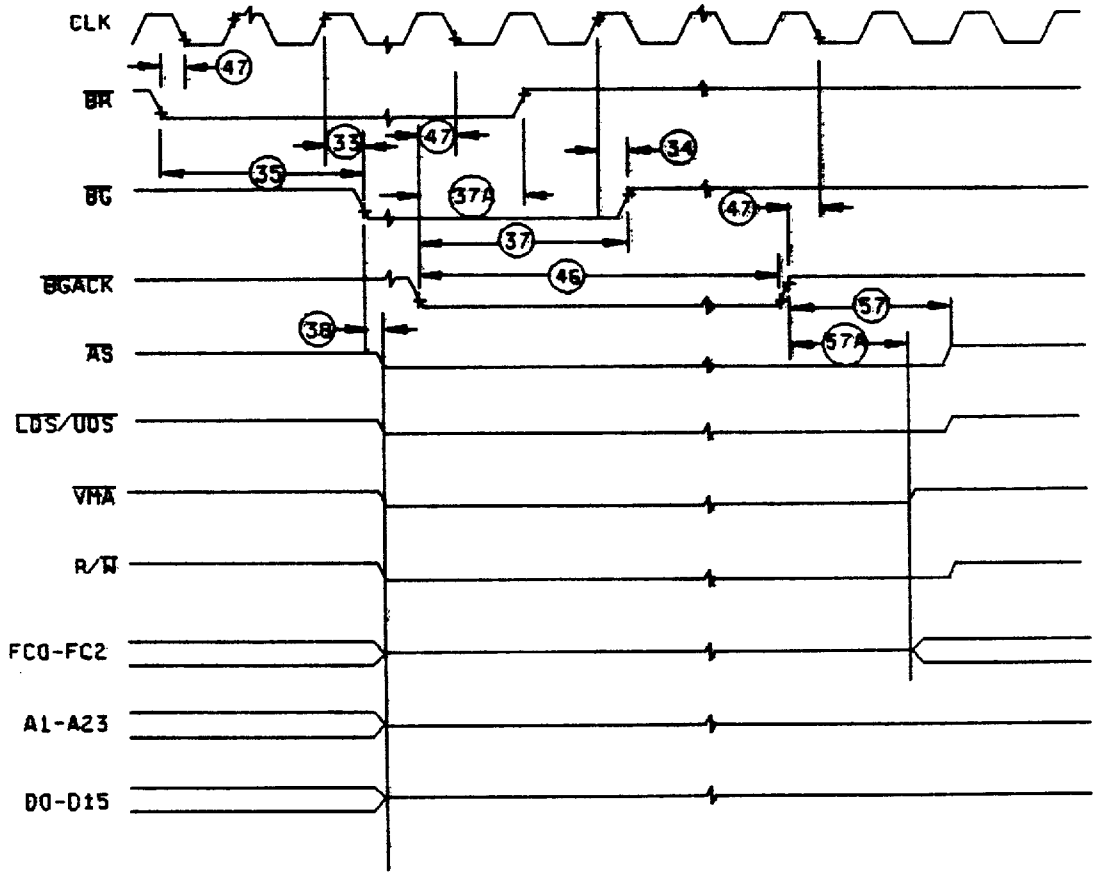

FIGURE 4. Switching test circuit and waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89462
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Bus arbitration timing diagram - multiple bus requests

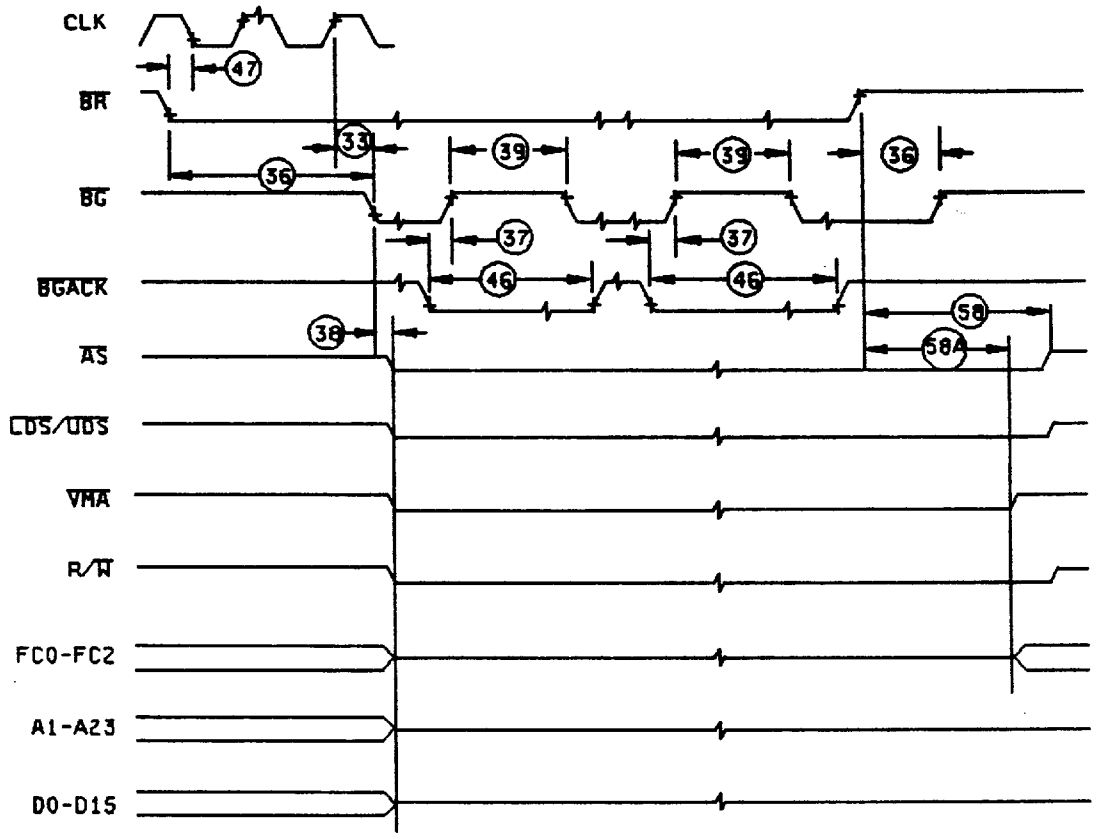

FIGURE 4. Switching test circuit and waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1/ 1,2,3,7,8,9,10,11	1/ 1,2,3,7,8,9,10,11	2/ 1,2,3,7,8,9,10,11	1/ 1,2,3,7,8,9,10,11	2/ 1,2,3,7,8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,7,9		
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11		1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11
Group D end-point electrical parameters (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11	1,2,3,7,8,9,10,11
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4 3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-S D-883:

a. Test condition A or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331. The input and output signals can be functionally organized into groups as shown on figure 4 and table III.

TABLE III. Signal summary.

Signal function	Signal name	Input/output	Active state	Three-state	
				On $\overline{\text{HALT}}$	On $\overline{\text{BGACK}}$
Address bus	A1-A23 (A0-A23 2/)	Output	High	Yes	Yes
Data bus	D0-D15	Input/output	High	Yes	Yes
Address strobe	$\overline{\text{AS}}$	Output	Low	No	Yes
Read/write	R/$\overline{\text{W}}$	Output	Read-high Write-low	No	Yes
Upper and lower data strobes	$\overline{\text{UDS}}$, $\overline{\text{LDS}}$	Output	Low	No	Yes
Data transfer acknowledge	$\overline{\text{DTACK}}$	Input	Low	No	No
Bus request	$\overline{\text{BR}}$	Input	Low	No	No
Bus grant	$\overline{\text{BG}}$	Output	Low	No	No
Bus grant acknowledge	$\overline{\text{BGACK}}$	Input	Low	No	No
Interrupt priority level	$\overline{\text{IPL0}}$, $\overline{\text{IPL1}}$, $\overline{\text{IPL2}}$	Input	Low	No	No
Bus error	$\overline{\text{BERR}}$	Input	Low	No	No
Reset	$\overline{\text{RESET}}$	Input/output	Low	No 1/	No 1/
Halt	$\overline{\text{HALT}}$	Input/output	Low	No 1/	No 1/
Enable	E	Output	High	No	No
Valid memory address	$\overline{\text{VMA}}$	Output	Low	No	Yes
Valid peripheral address	$\overline{\text{VPA}}$	Input	Low	No	No
Function codes	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	No	No
Mode 2/	MODE	Input	High/Low	No	No
Power supply	V_{CC}	Input			
Ground	GND	Input			

1/ Open drain.
2/ Applies to device types 04, 05, and 06 only.

Address bus (A1 through A23 for device types 01, 02, and 03; A0 through A23 for device types 04, 05 and 06). The unidirectional, three-state address bus is capable of addressing 8 megawords of data in devices 01, 02, and 03, and 16 megawords of data in devices 04, 05, and 06. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while the remaining address lines are all set to a logic high.

Data bus (D0 through D15). This 16-bit, bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0 through D7.

For device types 04, 05, and 06, the data bus may operate in either 8-bit or 16-bit mode. When the processor is in the 16-bit mode, the data bus transfers and accepts data in either word or byte length. When in the 8-bit mode, the processor drives the entire bus during writes, but only the lower eight bits (D0 through D7) contain valid data; data on lines D8 through D15 is ignored during read cycles.

Asynchronous bus control. Asynchronous data transfers are handled using the following control signals: Address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

Address strobe ($\overline{AS}$). This signal indicates that there is a valid address on the address bus.

Read/write (R/$\overline{W}$). This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper and lower data strobes ($\overline{UDS}$, $\overline{LDS}$). These signals control the data on the data bus as shown in table IV. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/$\overline{W}$ line is low, the processor will write to the data bus as shown.

When the processor is operating in the 8-bit mode (device types 04, 05, and 06 only), $\overline{UDS}$ is always forced high.

TABLE IV. Data strobe control of data bus.

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8-D15	D0-D7
High	High		No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15

Data transfer acknowledge ($\overline{DTACK}$). This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

Bus arbitration control. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus request ($\overline{BR}$). This input is wired OR with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

Bus grant ($\overline{BG}$). This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus grant acknowledge ($\overline{\text{BGACK}}$). This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

a. A bus grant has been received.

b. Address strobe is inactive which indicates that the microprocessor is not using the bus.

c. Data transfer acknowledge is inactive which indicates that either memory or the peripherals are not using the bus.

d. Bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

Interrupt control ($\overline{\text{IPL0}}$, $\overline{\text{IPL1}}$, $\overline{\text{IPL2}}$). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is contained in $\overline{\text{IPL0}}$ and the most significant bit is contained in $\overline{\text{IPL2}}$.

System control. The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus error ($\overline{\text{BERR}}$). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

a. Nonresponding devices.

b. Interrupt vector number acquisition failure.

c. Illegal access request as determined by a memory management unit.

d. Other application dependent errors.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retired.

Reset ($\overline{\text{RESET}}$). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of a $\overline{\text{RESET}}$ instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external halt and reset signals applied at the same time.

Halt ($\overline{\text{HALT}}$). When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their impedance state.

When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

Peripheral control. These control signals are used to allow the interfacing of synchronous peripheral devices with the asynchronous processor. These signals are explained in the following paragraphs.

Enable (E). This signal is the standard enable signal common to all peripheral devices. The period for this output is ten clock periods (six clocks low; four clocks high).

Valid peripheral address ($\overline{\text{VPA}}$). This input indicates that the device or region addressed is a family device and that data transfer should coincide with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt.

Valid memory address ($\overline{\text{VMA}}$). This output is used to indicate to peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address (VPA) input which indicates that the peripheral is a family device.

Processor status (FC0, FC1, FC2). These function code outputs indicate the mode (user or supervisor) and the cycle type currently being executed as shown in table V. The information indicated by the function code outputs is valid whenever address strobe (AS) is active.

TABLE V. Function code outputs.

FC2	FC1	FC0	Cycle type
Low	Low	Low	(Undefined, reserved)
Low	Low	High	User data
Low	High	Low	User program
Low	High	High	(Undefined, reserved)
High	Low	Low	(Undefined, reserved)
High	Low	High	Supervisor data
High	High	Low	Supervisor program
High	High	High	Interrupt acknowledge

Clock (CLK). The clock input is a TTL compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input shall be a constant frequency.

Mode (MODE). Available on device types 04, 05, and 06 only; this input selects between the 8-bit and 16-bit operating modes. If this input is grounded at reset, the processor will come out of reset in the 8-bit mode. If this input is tied high or floating at reset, the processor will come out of reset in the 16-bit mode. This input should be changed only at reset and must be stable two clocks after RESET is negated. Changing this input during normal operation may produce unpredictable results.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.