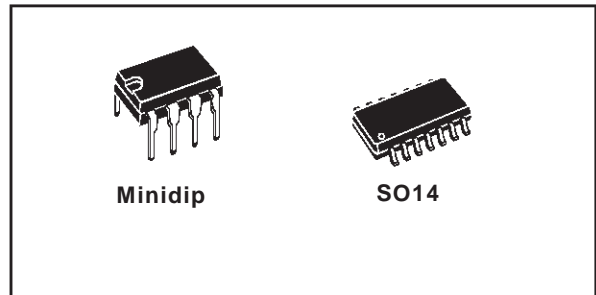




UC2842/3/4/5 UC3842/3/4/5

CURRENT MODE PWM CONTROLLER

- OPTIMIZED FOR OFF-LINE AND DC TO DC CONVERTERS
- LOW START-UP CURRENT (< 1 mA)
- AUTOMATIC FEED FORWARD COMPENSATION
- PULSE-BY-PULSE CURRENT LIMITING
- ENHANCED LOAD RESPONSE CHARACTERISTICS
- UNDER-VOLTAGE LOCKOUT WITH HYSTERESIS
- DOUBLE PULSE SUPPRESSION
- HIGH CURRENT TOTEM POLE OUTPUT
- INTERNALLY TRIMMED BANDGAP REFERENCE
- 500 KHz OPERATION
- LOW R_o ERROR AMP



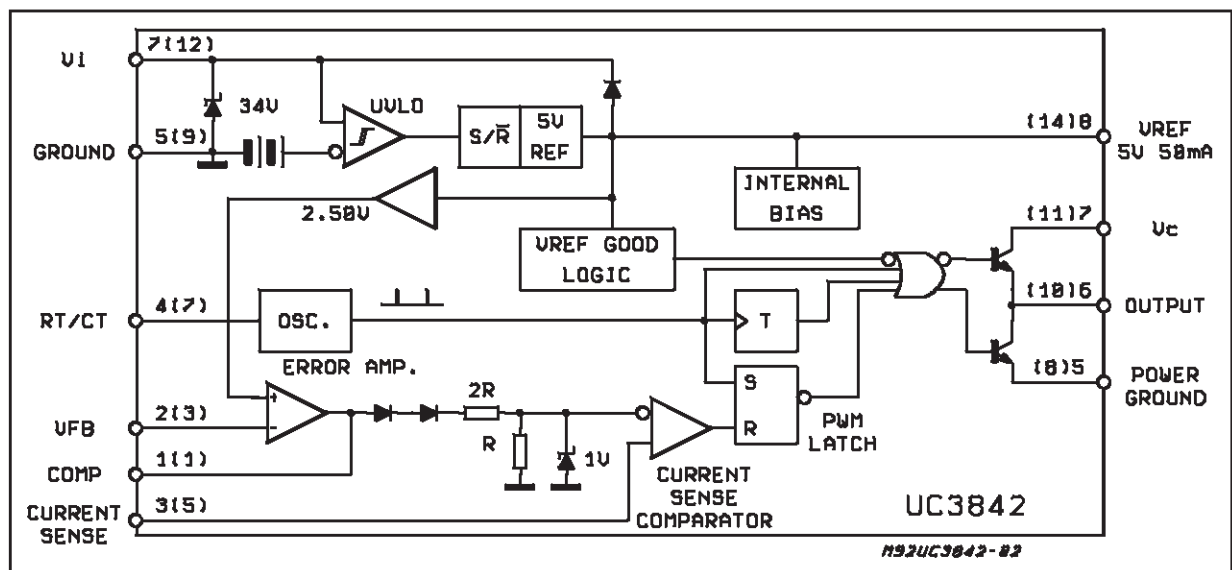
logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842 and UC3844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications. The corresponding thresholds for the UC3843 and UC3845 are 8.5 V and 7.9 V. The UC3842 and UC3843 can operate to duty cycles approaching 100%. A range of the zero to < 50 % is obtained by the UC3844 and UC3845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

DESCRIPTION

The UC3842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include undervoltage lockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input,

BLOCK DIAGRAM (toggle flip flop used only in U3844 and UC3845)



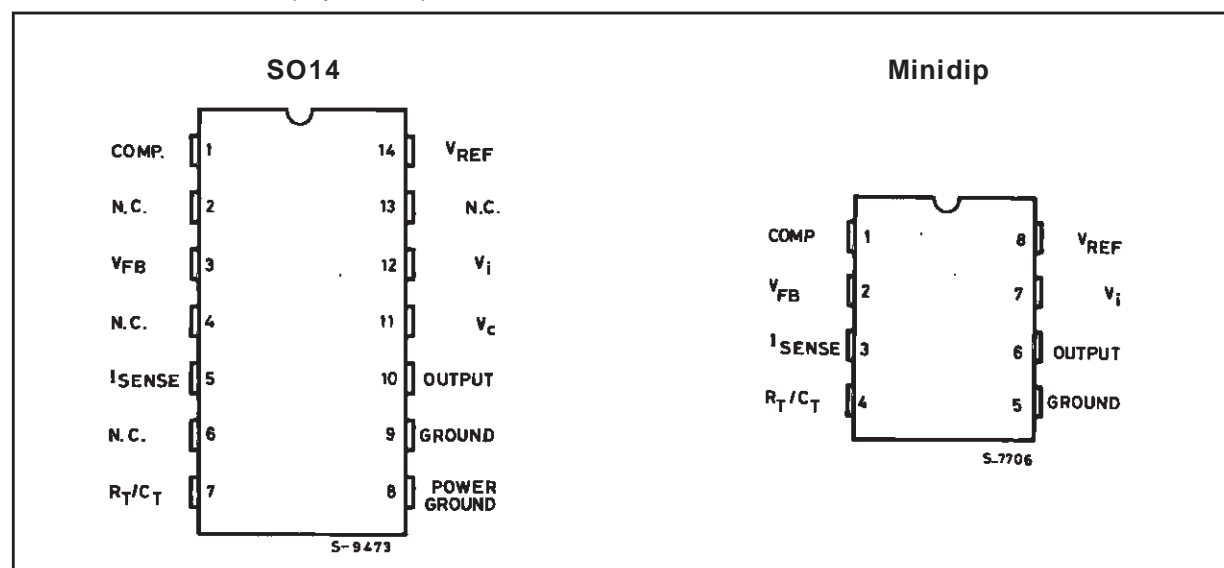
UC2842/3/4/5-UC3842/3/4/5

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------|---|---------------|------------------|
| V_i | Supply Voltage (low impedance source) | 30 | V |
| V_i | Supply Voltage ($I_i < 30\text{mA}$) | Self Limiting | |
| I_o | Output Current | ± 1 | A |
| E_o | Output Energy (capacitive load) | 5 | μJ |
| | Analog Inputs (pins 2, 3) | - 0.3 to 6.3 | V |
| | Error Amplifier Output Sink Current | 10 | mA |
| P_{tot} | Power Dissipation at $T_{\text{amb}} \leq 50^\circ\text{C}$ (minidip, DIP-14) | 1 | W |
| P_{tot} | Power Dissipation at $T_{\text{amb}} \leq 25^\circ\text{C}$ (SO14) | 725 | mW |
| T_{stg} | Storage Temperature Range | - 65 to 150 | $^\circ\text{C}$ |
| T_L | Lead Temperature (soldering 10s) | 300 | $^\circ\text{C}$ |

* All voltages are with respect to pin 5, all currents are positive into the specified terminal.

PIN CONNECTIONS (top views)



ORDERING NUMBERS

| Type | Minidip | SO14 |
|--------|---------|---------|
| UC2842 | UC2842N | UC2842D |
| UC3843 | UC2843N | UC2843D |
| UC2844 | UC2844N | UC2844D |
| UC2845 | UC2845N | UC2845D |
| UC3842 | UC3842N | UC3842D |
| UC3843 | UC3843N | UC3843D |
| UC3844 | UC3844N | UC3844D |
| UC3845 | UC3845N | UC3845D |

THERMAL DATA

| Symbol | Description | Minidip | SO14 | Unit |
|----------------------|--------------------------------------|----------|------|------------------|
| $R_{\text{thj-amb}}$ | Thermal Resistance Junction-ambient. | max. 100 | 165 | $^\circ\text{C}$ |

UC2842/3/4/5-UC3842/3/4/5

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $-25 \leq T_{amb} \leq 85^{\circ}\text{C}$ for UC2824X; $0 \leq T_{amb} \leq 70^{\circ}\text{C}$ for UC384X; $V_i = 15\text{V}$ (note 5); $R_T = 10\text{K}$; $C_T = 3.3\text{nF}$)

| Symbol | Parameter | Test Conditions | UC284X | | | UC384X | | | Unit |
|------------------------------|--------------------------|--|--------|------|------|--------|------|------|------------------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| REFERENCE SECTION | | | | | | | | | |
| V_{REF} | Output Voltage | $T_j = 25^{\circ}\text{C}$ $I_o = 1\text{mA}$ | 4.95 | 5.00 | 5.05 | 4.90 | 5.00 | 5.10 | V |
| ΔV_{REF} | Line Regulation | $12\text{V} \leq V_i \leq 25\text{V}$ | | 6 | 20 | | 6 | 20 | mV |
| ΔV_{REF} | Load Regulation | $1 \leq I_o \leq 20\text{mA}$ | | 6 | 25 | | 6 | 25 | mV |
| $\Delta V_{REF}/\Delta T$ | Temperature Stability | (Note 2) | | 0.2 | 0.4 | | 0.2 | 0.4 | mV/ $^{\circ}\text{C}$ |
| | Total Output Variant | Line, Load, Temperature (2) | 4.9 | | 5.1 | 4.82 | | 5.18 | V |
| e_N | Output Noise Voltage | $10\text{Hz} \leq f \leq 10\text{KHz}$ $T_j = 25^{\circ}\text{C}$ (2) | | 50 | | | 50 | | μV |
| | Long Term Stability | $T_{amb} = 125^{\circ}\text{C}$, 1000Hrs (2) | | 5 | 25 | | 5 | 25 | mV |
| I_{SC} | Output Short Circuit | | -30 | -100 | -180 | -30 | -100 | -180 | mA |
| OSCILLATOR SECTION | | | | | | | | | |
| f_s | Initial Accuracy | $T_j = 25^{\circ}\text{C}$ (6) | 47 | 52 | 57 | 47 | 52 | 57 | KHz |
| | Voltage Stability | $12 \leq V_i \leq 25\text{V}$ | | 0.2 | 1 | | 0.2 | 1 | % |
| | Temperature Stability | $T_{MIN} \leq T_{amb} \leq T_{MAX}$ (2) | | 5 | | | 5 | | % |
| V_4 | Amplitude | V_{PIN4} Peak to Peak | | 1.7 | | | 1.7 | | V |
| ERROR AMP SECTION | | | | | | | | | |
| V_2 | Input Voltage | $V_{PIN1} = 2.5\text{V}$ | 2.45 | 2.50 | 2.55 | 2.42 | 2.50 | 2.58 | V |
| I_b | Input Bias Current | | | -0.3 | -1 | | -0.3 | -2 | μA |
| | A_{VOL} | $2 \leq V_o \leq 4\text{V}$ | 65 | 90 | | 65 | 90 | | dB |
| B | Unity Gain Bandwidth | (2) | 0.7 | 1 | | 0.7 | 1 | | MHz |
| SVR | Supply Voltage Rejection | $12\text{V} \leq V_i \leq 25\text{V}$ | 60 | 70 | | 60 | 70 | | dB |
| I_o | Output Sink Current | $V_{PIN2} = 2.7\text{V}$ $V_{PIN1} = 1.1\text{V}$ | 2 | 6 | | 2 | 6 | | V |
| I_o | Output Source Current | $V_{PIN2} = 2.3\text{V}$ $V_{PIN1} = 5\text{V}$ | -0.5 | -0.8 | | -0.5 | -0.8 | | mA |
| | V_{OUT} High | $V_{PIN2} = 2.3\text{V}$; $R_L = 15\text{K}\Omega$ to Ground | 5 | 6 | | 5 | 6 | | V |
| | V_{OUT} Low | $V_{PIN2} = 2.7\text{V}$; $R_L = 15\text{K}\Omega$ to Pin 8 | | 0.7 | 1.1 | | 0.7 | 1.1 | V |
| CURRENT SENSE SECTION | | | | | | | | | |
| G_V | Gain | (3 & 4) | 2.85 | 3 | 3.15 | 2.8 | 3 | 3.2 | V/V |
| V_3 | Maximum Input Signal | $V_{PIN1} = 5\text{V}$ (3) | 0.9 | 1 | 1.1 | 0.9 | 1 | 1.1 | V |
| SVR | Supply Voltage Rejection | $12 \leq V_i \leq 25\text{V}$ (3) | | 70 | | | 70 | | dB |
| I_b | Input Bias Current | | | -2 | -10 | | -2 | -10 | μA |
| | Delay to Output | | | 150 | 300 | | 150 | 300 | ns |
| OUTPUT SECTION | | | | | | | | | |
| I_{OL} | Output Low Level | $I_{SINK} = 20\text{mA}$ | | 0.1 | 0.4 | | 0.1 | 0.4 | V |
| | | $I_{SINK} = 200\text{mA}$ | | 1.5 | 2.2 | | 1.5 | 2.2 | V |
| I_{OH} | Output High Level | $I_{SOURCE} = 20\text{mA}$ | 13 | 13.5 | | 13 | 13.5 | | V |
| | | $I_{SOURCE} = 200\text{mA}$ | 12 | 13.5 | | 12 | 13.5 | | V |
| t_r | Rise Time | $T_j = 25^{\circ}\text{C}$ $C_L = 1\text{nF}$ (2) | | 50 | 150 | | 50 | 150 | ns |
| t_f | Fall Time | $T_j = 25^{\circ}\text{C}$ $C_L = 1\text{nF}$ (2) | | 50 | 150 | | 50 | 150 | ns |

UC2842/3/4/5-UC3842/3/4/5

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | UC284X | | | UC384X | | | Unit |
|--------------------------------------|-------------------------------------|--|--------|------|------|--------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| UNDER-VOLTAGE LOCKOUT SECTION | | | | | | | | | |
| | Start Threshold | X842/4 | 15 | 16 | 17 | 14.5 | 16 | 17.5 | V |
| | | X843/5 | 7.8 | 8.4 | 9.0 | 7.8 | 8.4 | 9 | V |
| | Min Operating Voltage After Turn-on | X842/4 | 9 | 10 | 11 | 8.5 | 10 | 11.5 | V |
| | | X843/5 | 7.0 | 7.6 | 8.2 | 7.0 | 7.6 | 8.2 | V |
| PWM SECTION | | | | | | | | | |
| | Maximum Duty Cycle | X842/3 | 93 | 97 | 100 | 93 | 97 | 100 | % |
| | | X844/5 | 46 | 48 | 50 | 47 | 48 | 50 | % |
| | Minimum Duty Cycle | | | 0 | | | 0 | % | |
| TOTAL STANDBY CURRENT | | | | | | | | | |
| I _{st} | Start-up Current | | | 0.5 | 1 | | 0.5 | 1 | mA |
| I _i | Operating Supply Current | V _{PIN2} = V _{PIN3} = 0V | | 11 | 20 | | 11 | 20 | mA |
| V _{iz} | Zener Voltage | I _i = 25mA | | 34 | | | 34 | | V |

- Notes :**
- These parameters, although guaranteed, are not 100% tested in production.
 - Parameter measured at trip point of latch with V_{PIN2} = 0.
 - Gain defined as :

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8V$$
 - Adjust V₁ above the start threshold before setting at 15 V.
 - Output frequency equals oscillator frequency for the UC3842 and UC3843.
Output frequency is one half oscillator frequency for the UC3844 and UC3845.

Figure 1 : Error Amp Configuration.

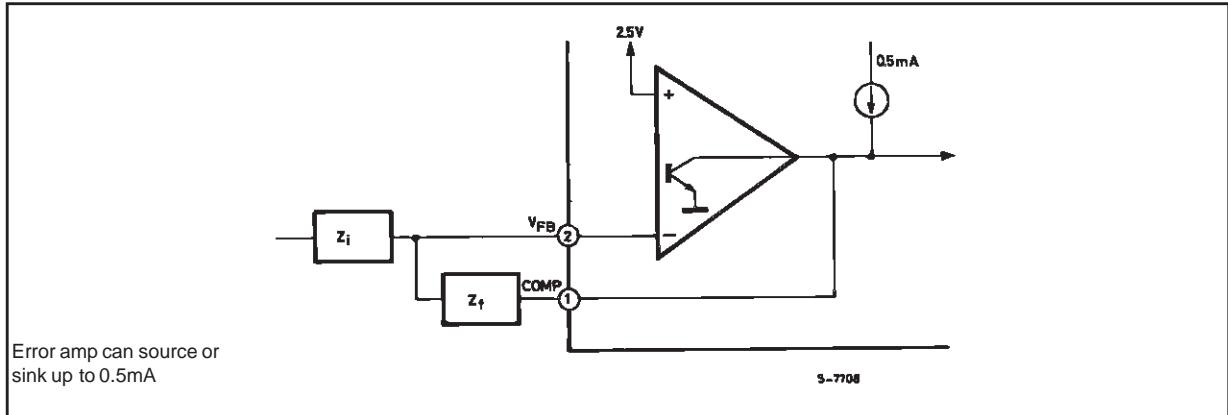
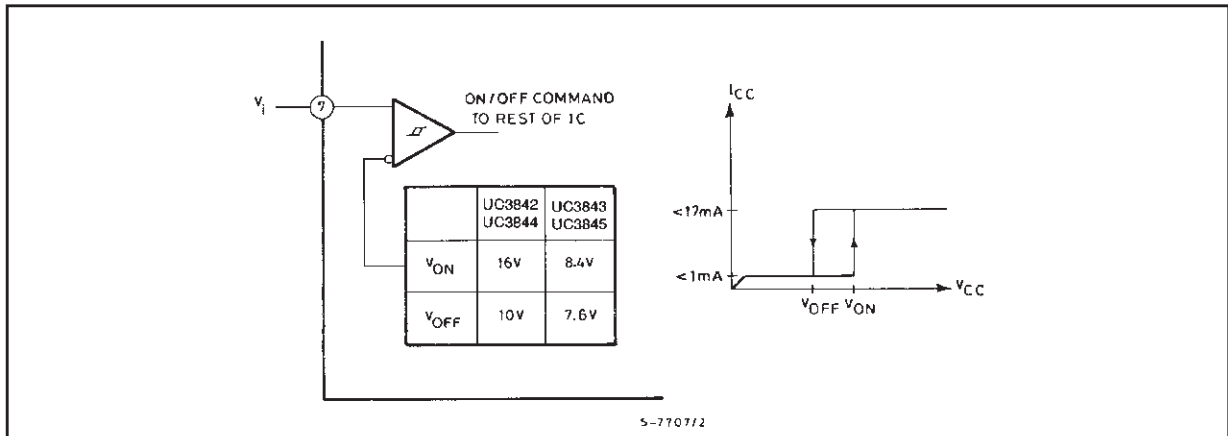


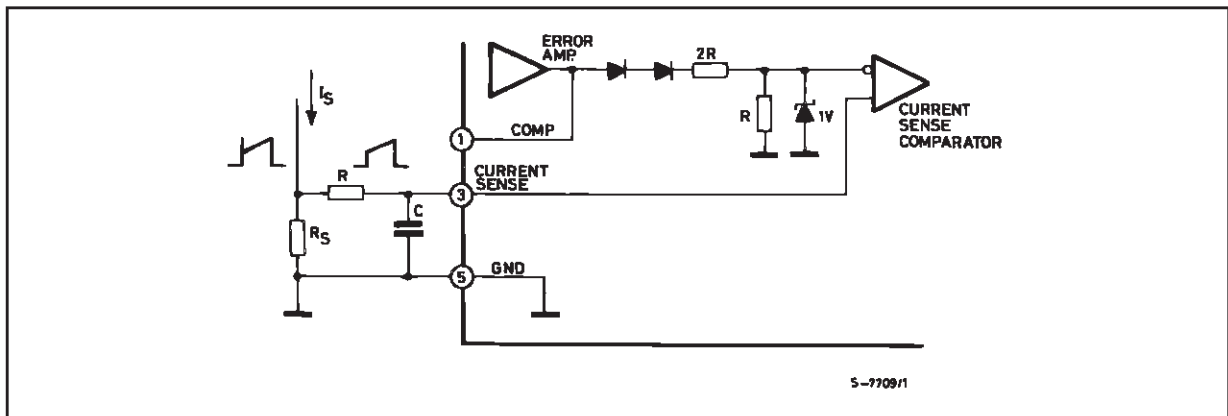
Figure 2 : Under Voltage Lockout.



During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor

to prevent activating the power switch with extraneous leakage currents.

Figure 3 : Current Sense Circuit .



Peak current (i_s) is determined by the formula

$$I_{s \max} \approx \frac{1.0 \text{ V}}{R_s}$$

A small RC filter may be required to suppress switch transients.



UC2842/3/4/5-UC3842/3/4/5

Figure 4.

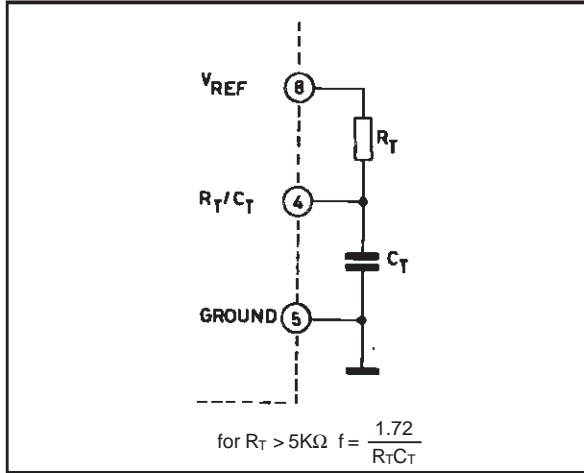


Figure 5 : Deadtime vs. C_T ($R_T > 5K\Omega$).

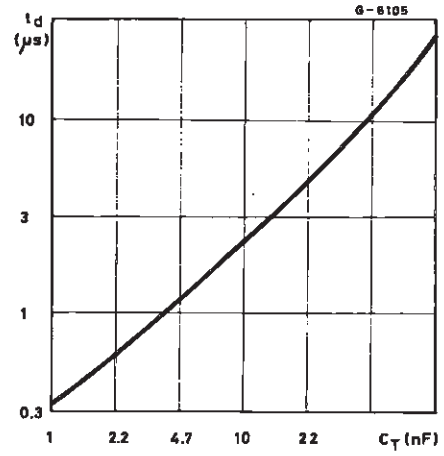


Figure 6 : Timing Resistance vs. Frequency.

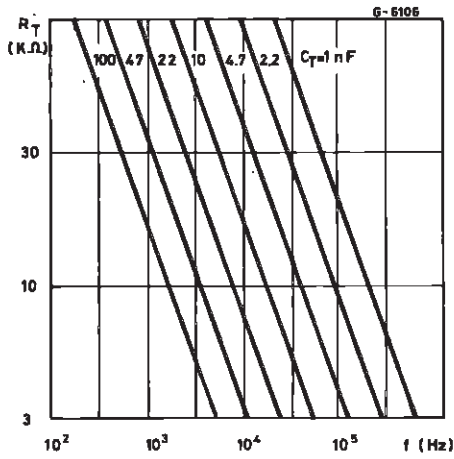


Figure 7 : Output Saturation Characteristics.

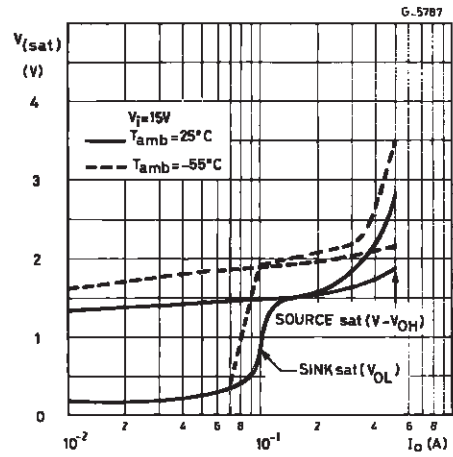


Figure 8 : Error Amplifier Open-loop Frequency Response.

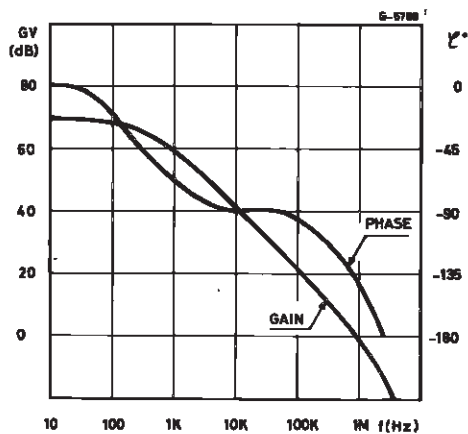
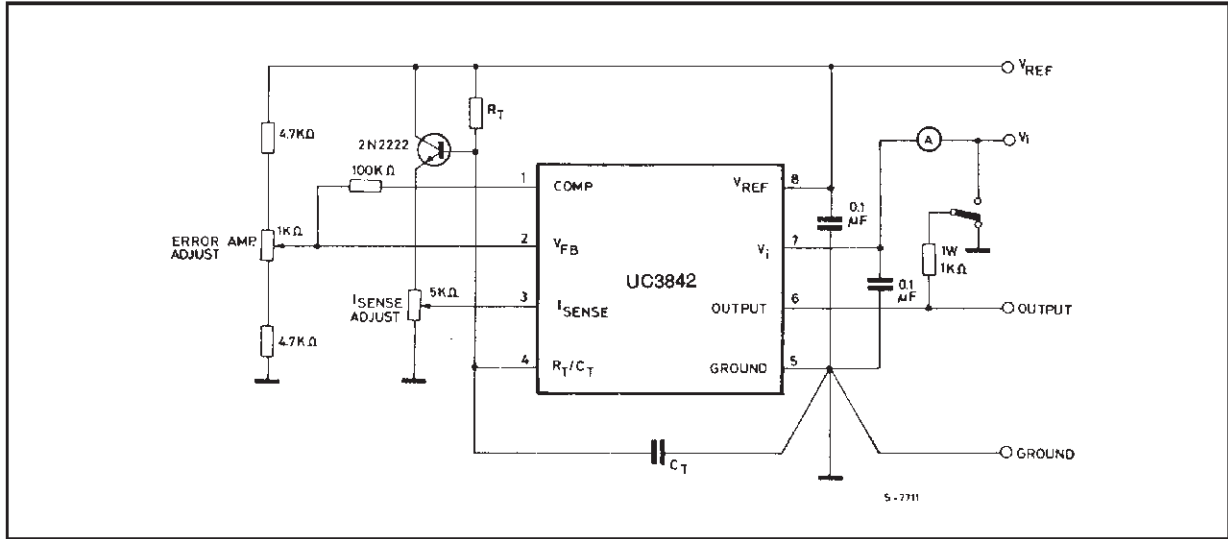


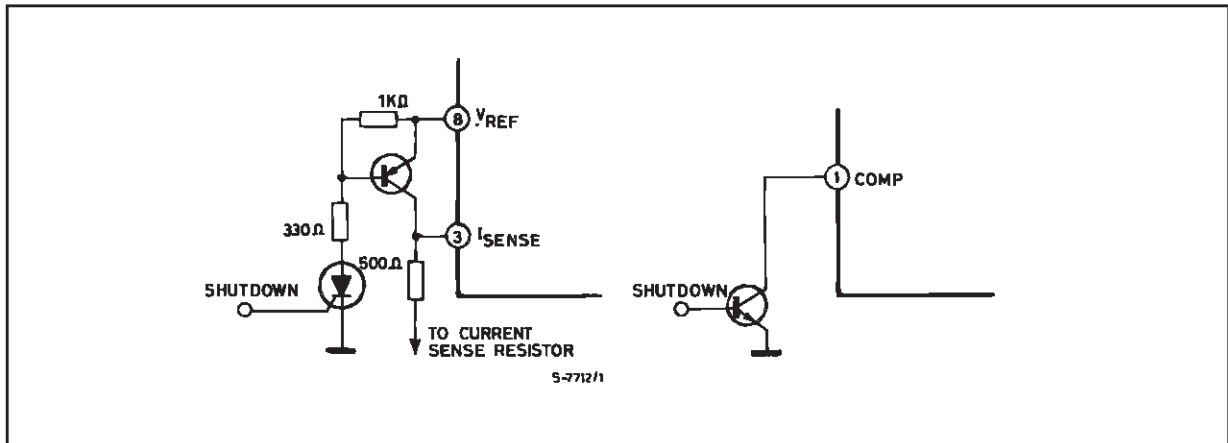
Figure 9 : Open Loop Test Circuit.



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close

to pin 5 in a single point ground. The transistor and 5 KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 10 : Shutdown Techniques.

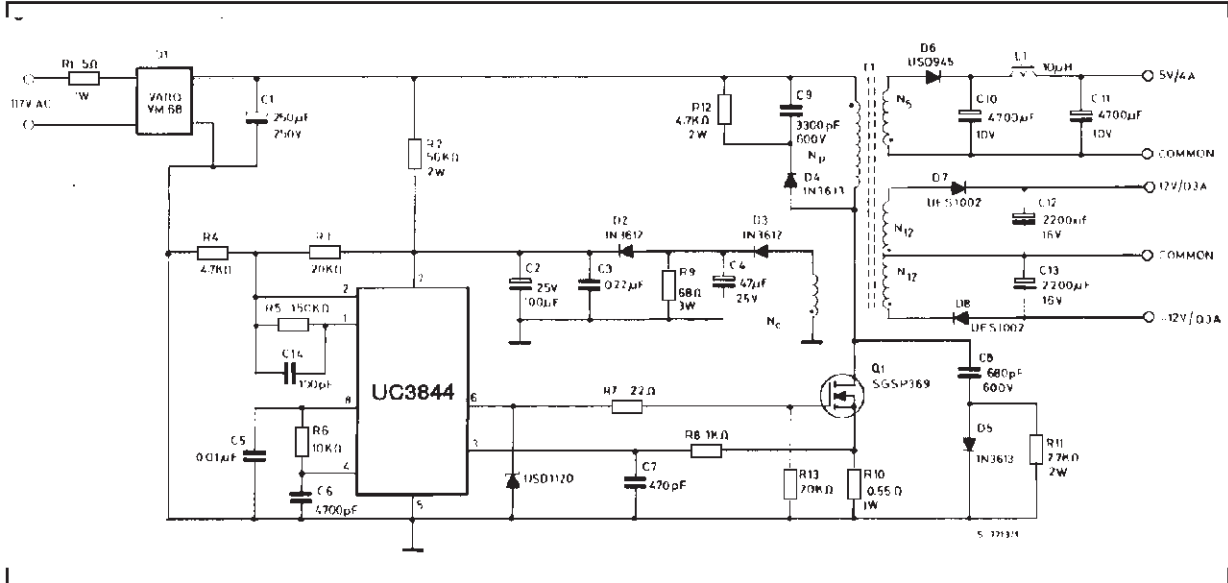


Shutdown of the UC2842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method cause the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shut-

down condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_i below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

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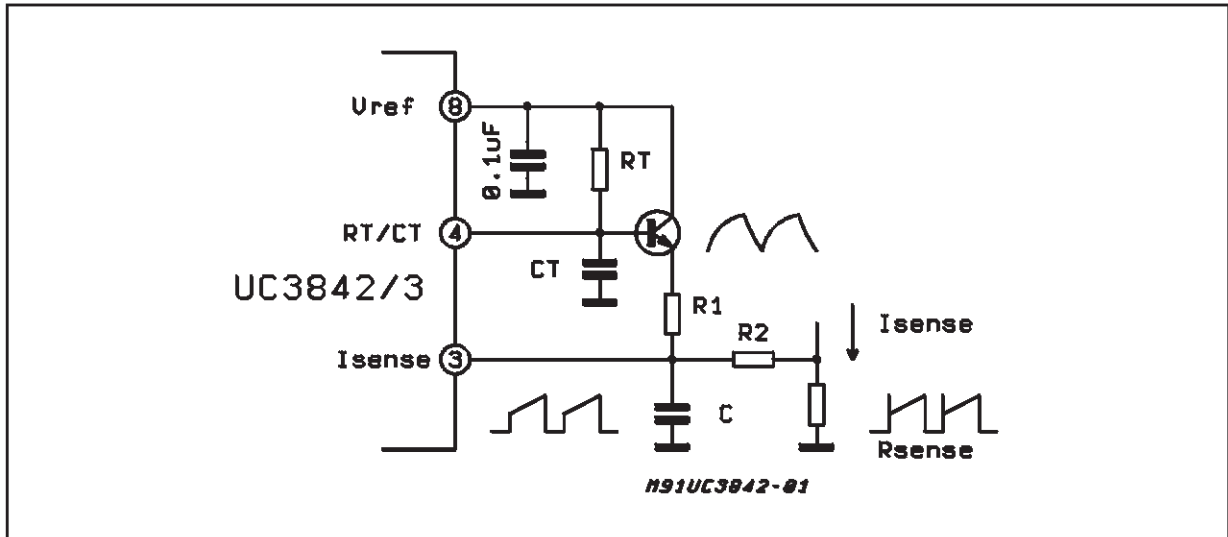
Figure 11 : Off-line Flyback Regulator.



Power Supply Specifications

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. Input Voltage : 95 VAC to 130 VAC (50 Hz/60 Hz) 2. Line Isolation : 3750 V 3. Switching Frequency : 40 KHz 4. Efficiency @ Full Load : 70 % | <ol style="list-style-type: none"> 5. Output Voltage : <ul style="list-style-type: none"> A. + 5 V, ± 5 % : 1 A to 4 A load Ripple voltage : 50 mV P-P Max. B. + 12 V, ± 3 % : 0.1 A to 0.3 A load Ripple voltage : 100 mV P-P Max. C. - 12 V, ± 3 % : 0.1 A to 0.3 A load Ripple voltage : 100 mV P-P Max. |
|---|--|

Figure 12 : Slope Compensation.



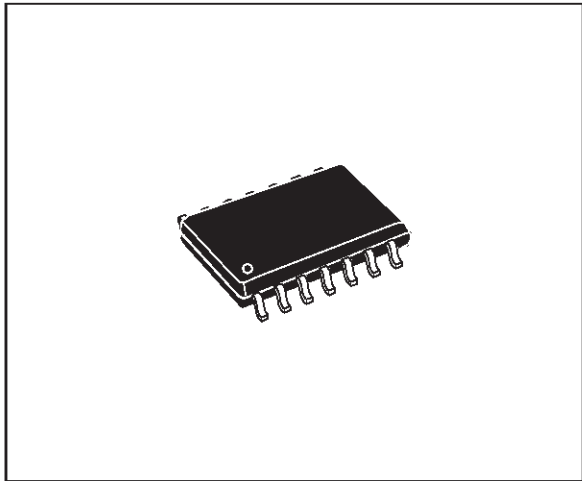
A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50 %.

Note that capacitor, C, forms a filter with R₂ to suppress the leading edge switch spikes.



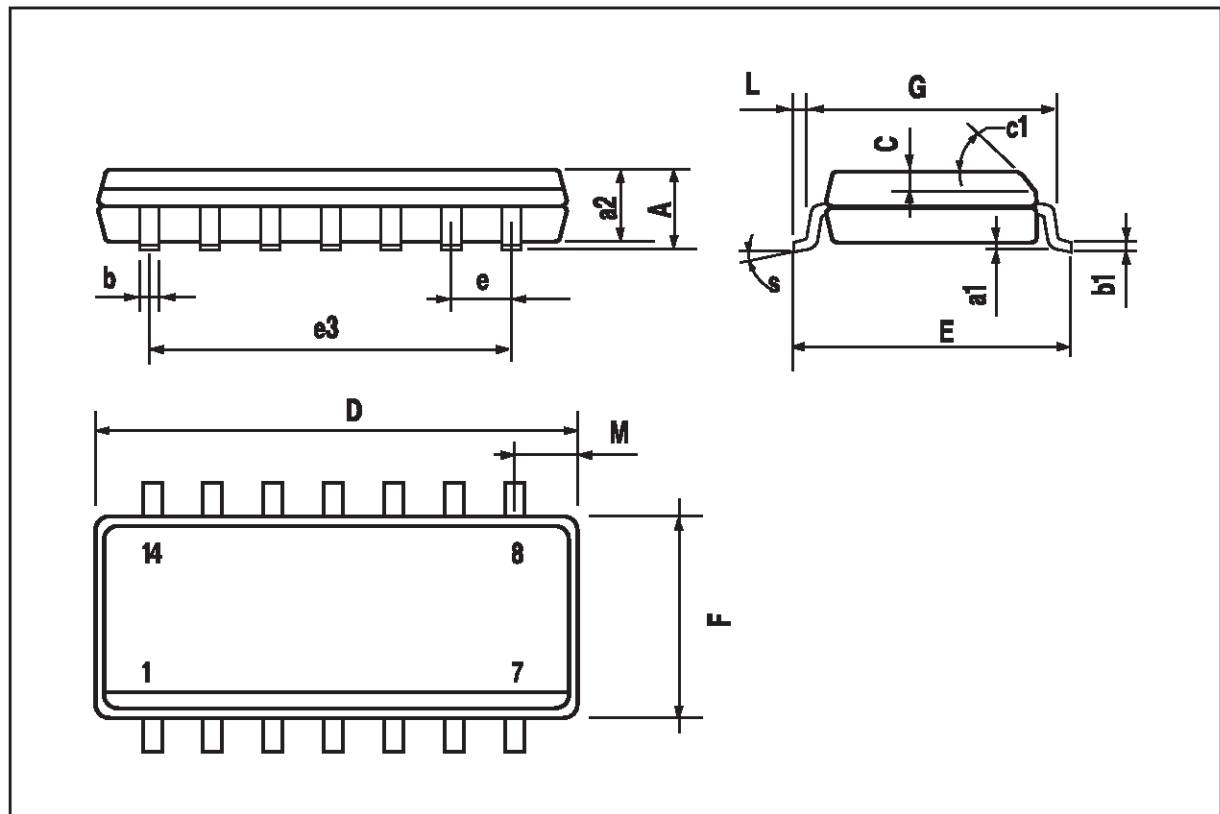
| DIM. | mm | | | inch | | |
|-------|------------|------|-------|-------|-------|-------|
| | MIN.. | TYP. | MAX.. | MIN.. | TYP.. | MAX.. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.009 |
| a2 | | | 1.6 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.014 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D (1) | 8.55 | | 8.75 | 0.336 | | 0.344 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 7.62 | | | 0.300 | |
| F (1) | 3.8 | | 4 | 0.150 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.209 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| M | | | 0.68 | | | 0.027 |
| S | 8° (max) | | | | | |

OUTLINE AND MECHANICAL DATA



SO14

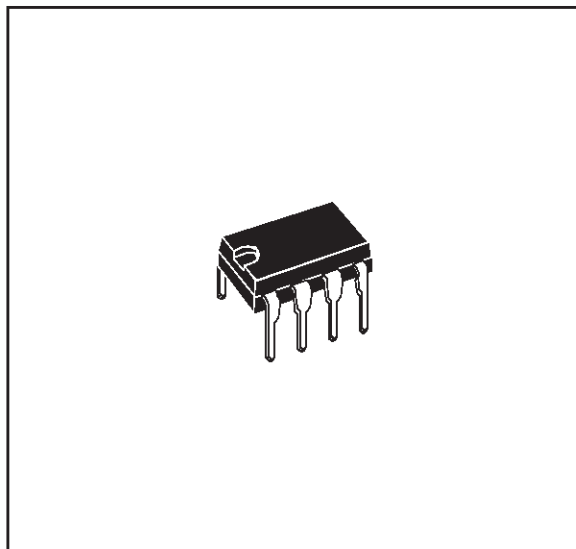
(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).



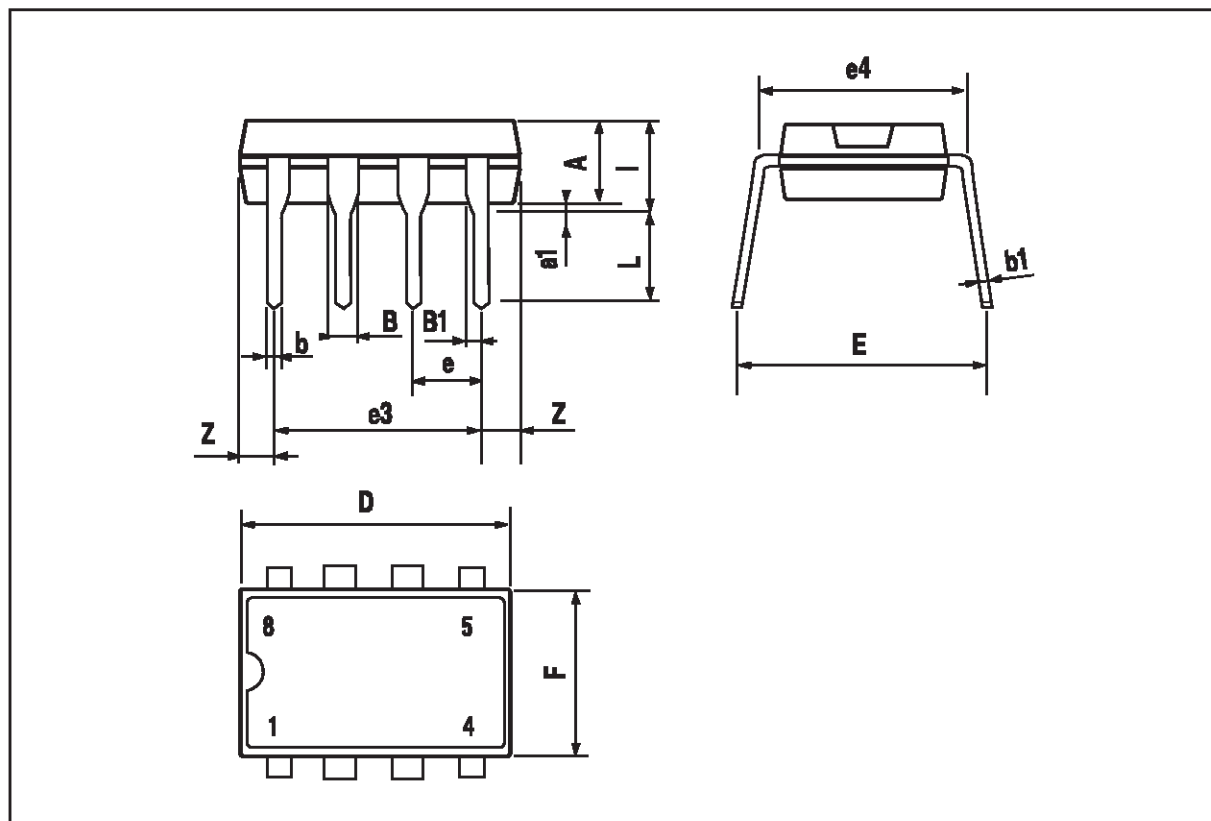
UC2842/3/4/5-UC3842/3/4/5

| DIM. | mm | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | 3.3 | | | 0.130 | |
| a1 | 0.7 | | | 0.028 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| B1 | 0.91 | | 1.04 | 0.036 | | 0.041 |
| b | | 0.5 | | | 0.020 | |
| b1 | 0.38 | | 0.5 | 0.015 | | 0.020 |
| D | | | 9.8 | | | 0.386 |
| E | | 8.8 | | | 0.346 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 7.62 | | | 0.300 | |
| e4 | | 7.62 | | | 0.300 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 4.8 | | | 0.189 |
| L | | 3.3 | | | 0.130 | |
| Z | 0.44 | | 1.6 | 0.017 | | 0.063 |

OUTLINE AND MECHANICAL DATA



Minidip 0.300''



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