

# Dual Output Driver

## FEATURES

- Dual, 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog, Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiescent Current
- 5 to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin Surface Mount Package

## DESCRIPTION

The UC1706 family of output drivers are made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFET's. These devices implement three generalized functions as outlined below.

First: They accept a single-ended, low-current digital input of either polarity and process it to activate a pair of high-current, totem pole outputs which can source or sink up to 1.5A each.

Second: They provide an optional single-ended to push-pull conversion through the use of an internal flip-flop driven by double-pulse-suppression logic. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Third: Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control, and thermal shutdown.

These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount Q and L packages.

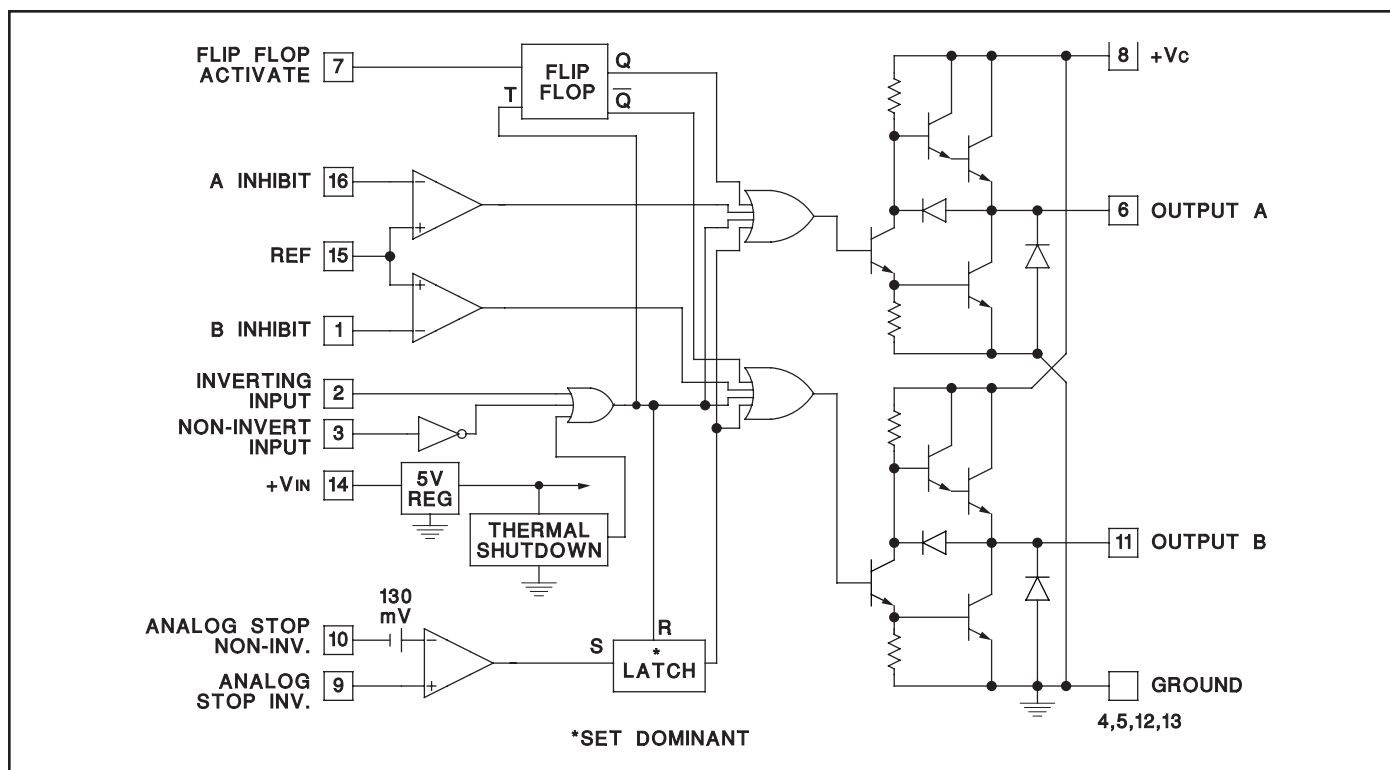
## TRUTH TABLE

| INV | N.I | OUT |
|-----|-----|-----|
| H   | H   | L   |
| L   | H   | H   |
| H   | L   | L   |
| L   | L   | L   |

$\overline{\text{OUT}} = \overline{\text{INV}}$  and N.I.

$\overline{\text{OUT}} = \text{INV}$  or N.I.

## BLOCK DIAGRAM

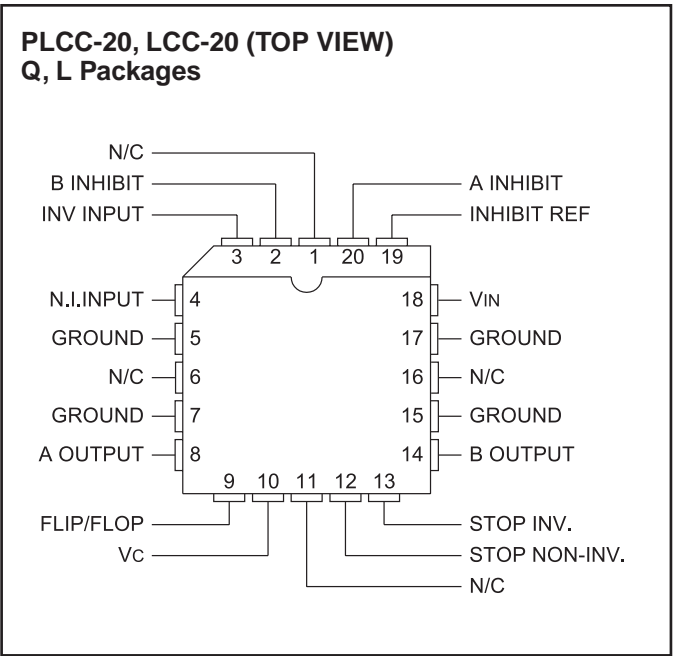
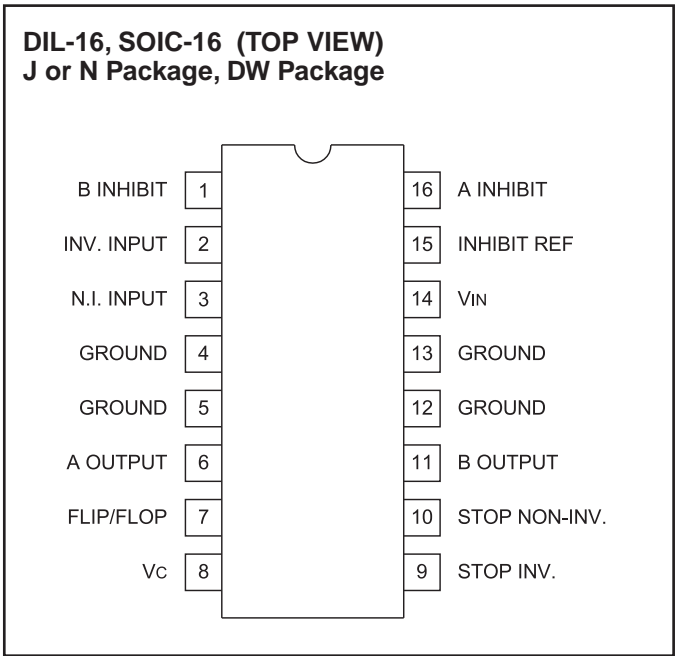


# ABSOLUTE MAXIMUM RATINGS

|  | N--Pkg                                      | J--Pkg             |
|--|---|--------------------|
| Supply Voltage, $V_{IN}$                                   | 40V   | 40V                |
| Collector Supply Voltage, $V_c$                            | 40V   | 40V                |
| Output Current (Each Output, Source or Sink)               |   |                    |
| Steady--State  | $\pm 500\text{mA}$                          | $\pm 500\text{mA}$ |
| Peak Transient   | $\pm 1.5\text{A}$                           | $\pm 1.0\text{A}$  |
| Capacitive Discharge Energy                                | 20 $\mu\text{J}$                            | 15 $\mu\text{J}$   |
| Digital Inputs   | 5.5V  | 5.5V               |
| Analog Stop Inputs   | $V_{IN}$                                    | $V_{IN}$           |
| Power Dissipation at $T_A = 25^\circ\text{C}$ (See Note)   | 2W  | 1W                 |
| Power Dissipation at $T$ (Leads/Case) = $25^\circ\text{C}$ | 5W  | 2                  |
| (See Note)   |   |                    |
| Operating Temperature Range                                | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |                    |
| Storage Temperature Range                                  | $-65^\circ\text{C}$ to $+150^\circ\text{C}$ |                    |
| Lead Temperature (Soldering, 10 Seconds)                   | 300 $^\circ\text{C}$                        |                    |

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Consult Packaging sections of the Databook for thermal limitations and considerations of package.

# CONNECTION DIAGRAMS



Note: All four ground pins must be connected to a common ground.

**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  for the UC1706,  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for the UC2706 and  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for the UC3706;  $V_{IN} = V_c = 20\text{V}$ .  $T_A = T_J$ .

| PARAMETERS               | TEST CONDITIONS                             | MIN | TYP  | MAX  | UNITS |
|--------------------------|---|-----|------|------|-------|
| $V_{IN}$ Supply Current  | $V_{IN} = 40\text{V}$                       |     | 8    | 10   | mA    |
| $V_c$ Supply Current     | $V_c = 40\text{V}$ , Outputs Low            |     | 4    | 5    | mA    |
| $V_c$ Leakage Current    | $V_{IN} = 0$ , $V_c = 30\text{V}$ , No Load |     | .05  | 0.1  | mA    |
| Digital Input Low Level  |   |     |      | 0.8  | V     |
| Digital Input High Level |   | 2.2 |      |      | V     |
| Input Current            | $V_i = 0$                                   |     | -0.6 | -1.0 | mA    |
| Input Leakage            | $V_i = 5\text{V}$                           |     | .05  | 0.1  | mA    |

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| PARAMETERS                    | TEST CONDITIONS              | MIN | TYP | MAX | UNITS              |
|-------------------------------|------------------------------|-----|-----|-----|--------------------|
| Output High Sat., $V_{C-V_O}$ | $I_O = -50\text{mA}$         |     |     | 2.0 | V                  |
| Output Low Sat., $V_O$        | $I_O = 50\text{mA}$          |     |     | 0.4 | V                  |
|                               | $I_O = 500\text{mA}$         |     |     | 2.5 | V                  |
| Inhibit Threshold             | $V_{REF} = 0.5\text{V}$      | 0.4 |     | 0.6 | V                  |
|                               | $V_{REF} = 3.5\text{V}$      | 3.3 |     | 3.7 | V                  |
| Inhibit Input Current         | $V_{REF} = 0$                |     | -10 | -20 | $\mu\text{A}$      |
| Analog Threshold              | $V_{CM} = 0$ to $15\text{V}$ | 100 | 130 | 160 | mV                 |
| Input Bias Current            | $V_{CM} = 0$                 |     | -10 | -20 | $\mu\text{A}$      |
| Thermal Shutdown              |                              |     | 155 |     | $^{\circ}\text{C}$ |

**TYPICAL SWITCHING CHARACTERISTICS:**  $V_{IN} = V_C = 20\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ . Delays measured to 10% output change.

| PARAMETERS                                 | TEST CONDITIONS  | OUTPUT $C_L =$ |     |     | UNITS |
|--|--|----------------|-----|-----|-------|
| <b>From Inv. Input to Output:</b>          |  | open           | 1.0 | 2.2 | nF    |
| Rise Time Delay                            |  | 110            | 130 | 140 | ns    |
| 10% to 90% Rise                            |  | 20             | 40  | 60  | ns    |
| Fall Time Delay                            |  | 80             | 90  | 110 | ns    |
| 90% to 10% Fall                            |  | 25             | 30  | 50  | ns    |
| <b>From N. I. Input to Output:</b>         |  |                |     |     |       |
| Rise Time Delay                            |  | 120            | 130 | 140 | ns    |
| 10% to 90% Rise                            |  | 20             | 40  | 60  | ns    |
| Fall Time Delay                            |  | 100            | 120 | 130 | ns    |
| 90% to 10% Fall                            |  | 25             | 30  | 50  | ns    |
| Vc Cross-Conduction Current Spike Duration | Output Rise  | 25             |     |     | ns    |
|  | Output Fall  | 0              |     |     | ns    |
| Inhibit Delay                              | Inhibit Ref. = $1\text{V}$ , Inhibit Inv. = $0.5$ to $1.5\text{V}$ | 250            |     |     | ns    |
| Analog Shutdown Delay                      | Stop Non-Inv. = $0\text{V}$ , Stop Inv. = $0$ to $0.5\text{V}$     | 180            |     |     | ns    |

## CIRCUIT DESCRIPTION

### Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common  $V_C$  pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

### Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at least  $200\text{nsec}$  must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

### Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs—the threshold is approximately  $1.2\text{V}$  with no hysteresis; and external pull-up resistors are not required.

### Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning-on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from  $0.5$  to  $3.5\text{V}$ . When this circuit is not used, ground pin 15 and leave 1 and 16 open.

## CIRCUIT DESCRIPTION (cont.)

### Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to ( $V_{IN} - 3V$ ). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

### Supply Voltage

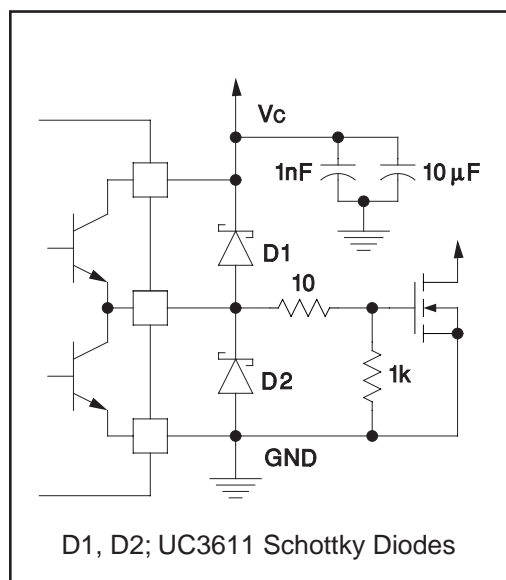
With an internal 5V regulator, this circuit is optimized for

use with a 7 to 40V supply; however, with some slight response time degradation, it can also be driven from 5V. When  $V_{IN}$  is low, the entire circuit is disabled and no current is drawn from  $V_C$ . When combined with a UC1840 PWM, the Driver Bias switch can be used to supply  $V_{IN}$  to the UC1706.  $V_{IN}$  switching should be fast as if  $V_C$  is high, undefined operation of the outputs may occur with  $V_{IN}$  less than 5V.

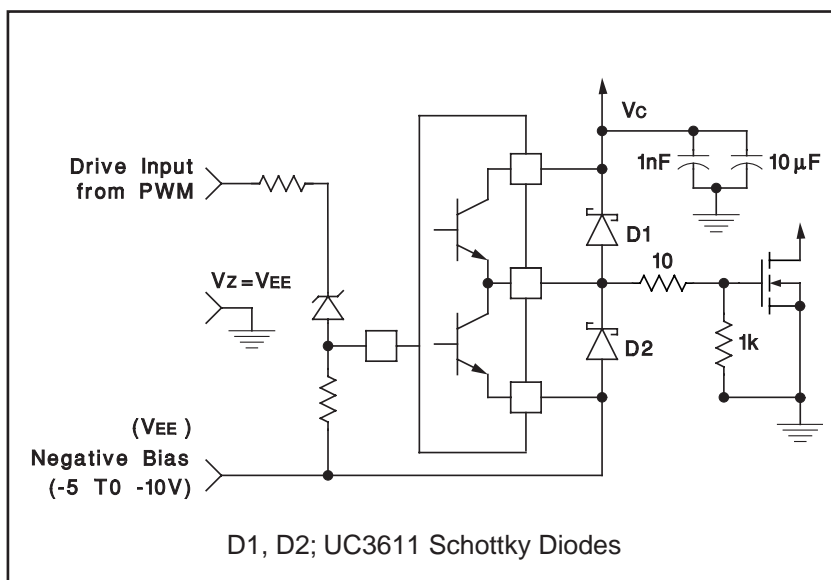
### Thermal Considerations

Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

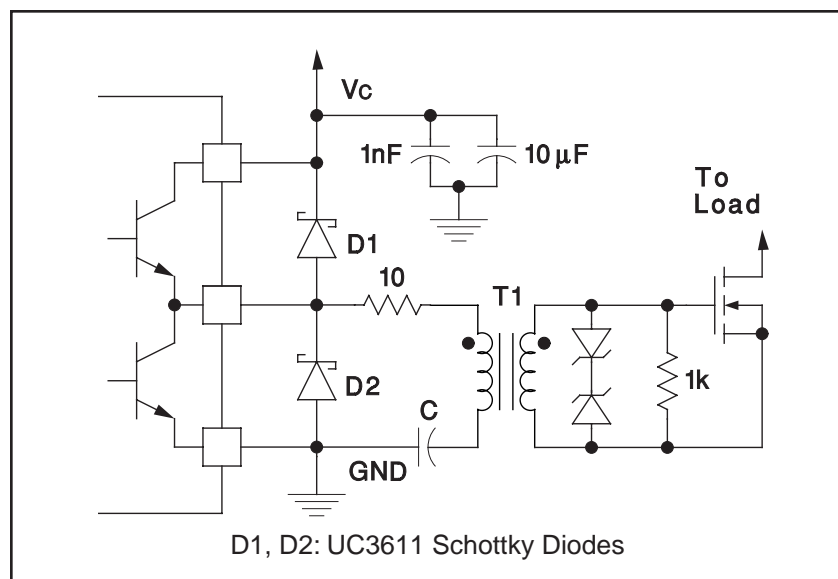
## APPLICATIONS



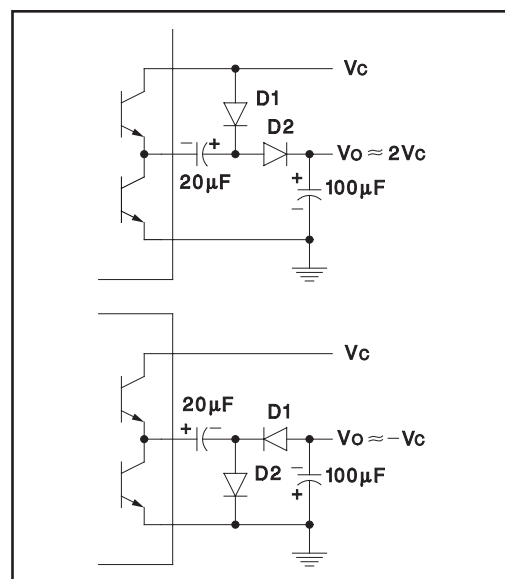
Power MOSFET Drive Circuit



Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs

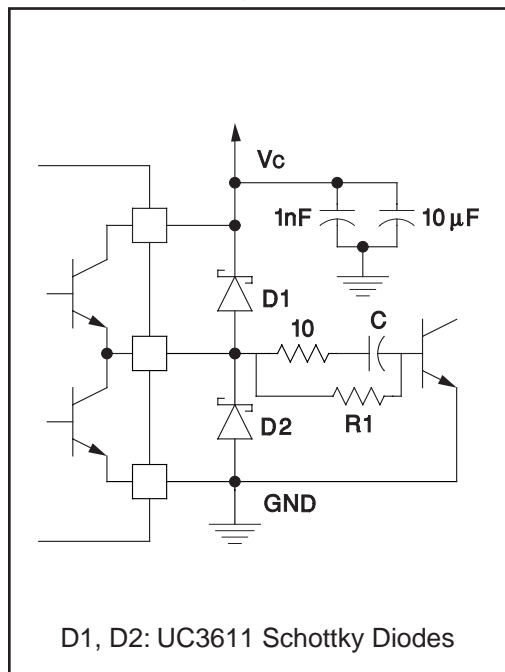


Transformer Coupled MOSFET Drive Circuit

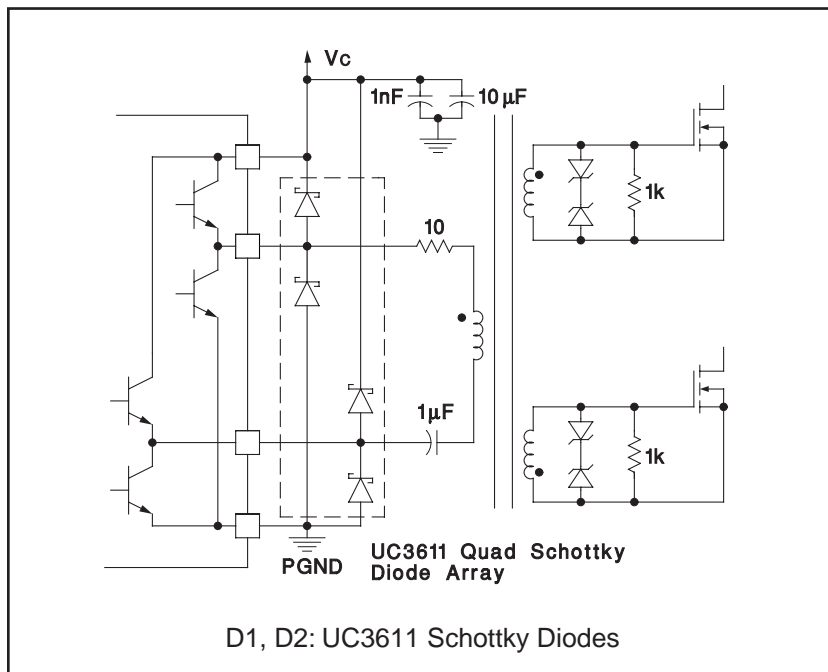


Charge Pump Circuits

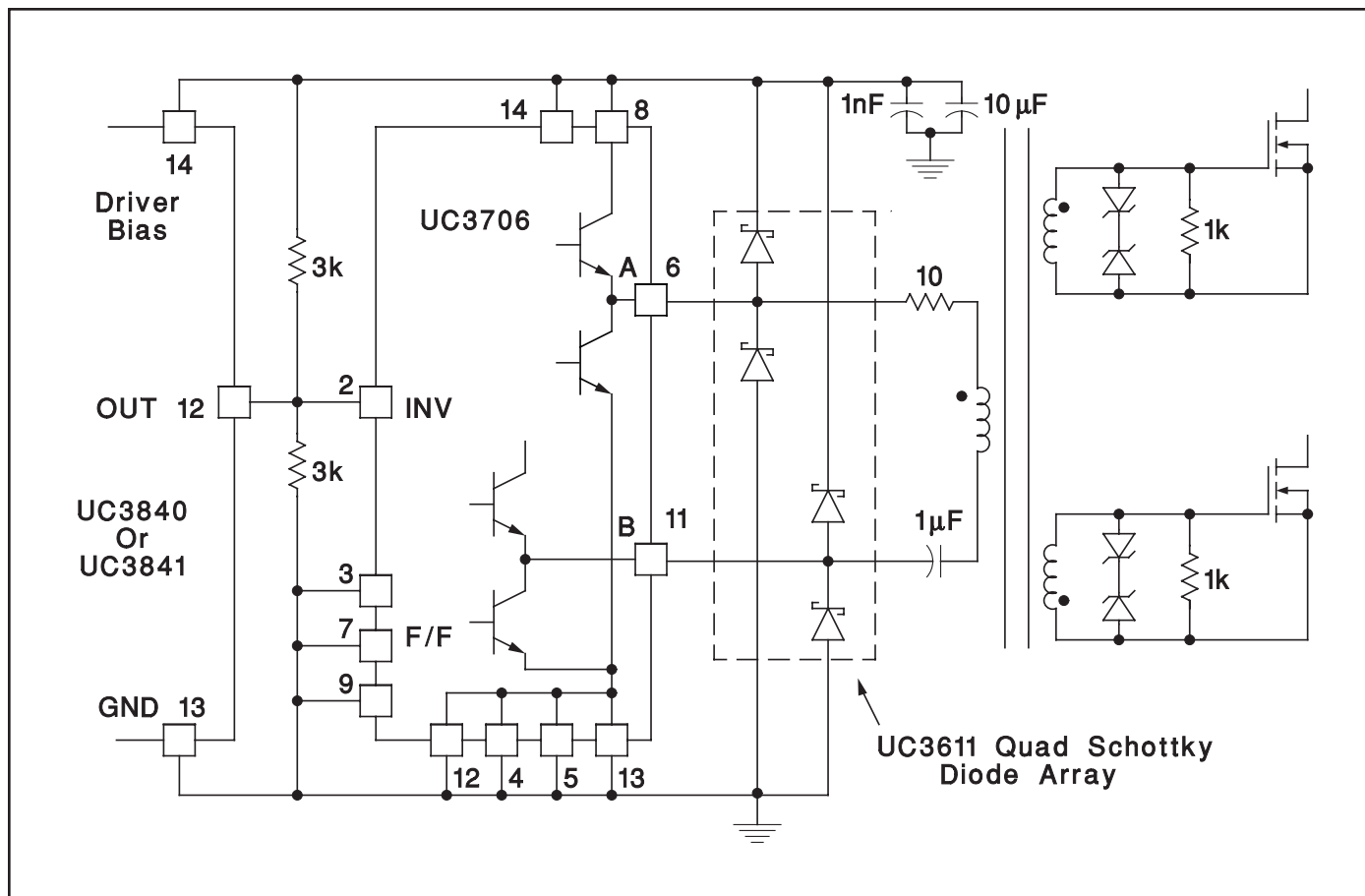
# APPLICATIONS (cont'd)



Power Bipolar Drive Circuit



Transformer Coupled Push-Pull MOSFET Drive Circuit



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