CSC™ CHERRY SEMICONDUCTOR

CS-2706
CS-3706

DUAL OUTPUT DRIVER

DESCRIPTION

The CS-2706/CS-3706 series of integrated circuits provide an interface between low-level TTL inputs and high-power switching devices such as power MOSFETs. A typical application is single-ended PWM control to push-pull power control conversion.

The primary function of these devices is to convert a bipolar single-ended low current digital input to a pair of totem pole outputs which can source or sink up to 1.5A each. An internal flip-flop, driven by double-pulse suppression logic, can be enabled to provide single-ended to push-pull conversion. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control and thermal shutdown.

FEATURES:

- Dual 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiesent Current
- 5V to 40V Operation
- Thermal Shutdown Protection

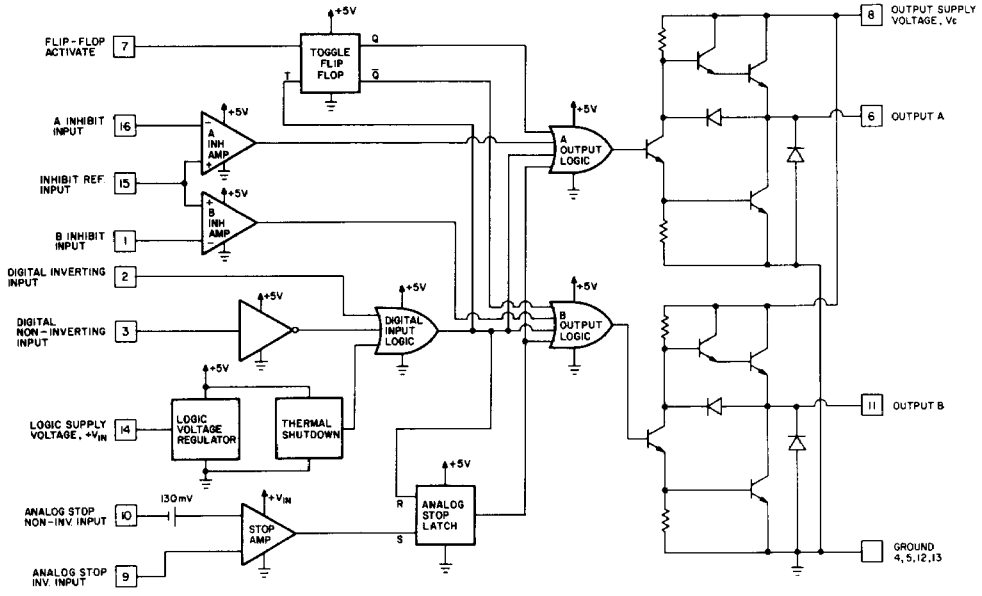
TRUTH TABLE

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV}}$ and N.I.

$\overline{\text{OUT}}$ = INV or $\overline{\text{N.I.}}$

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

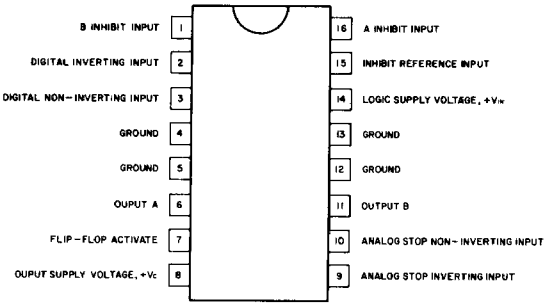
	N-PACKAGE (Plastic)	UNITS
Logic Supply Voltage (Vin, Pin 14)	40.0	V
Output Supply Voltage (Vc, Pin 8)	40.0	V
Output Current (each output, source, or sink) (pins 6 & 11)		
Steady State	±500	mA
Peak Transient for Less Than 100us	±1.5	A
capacitive discharge energy	20.0	uJ
Digital Inputs (pins 2 & 3)	5.5	V
Analog Inputs (pins 9 & 10)	Vin	V
Inhibit Inputs (pins 1, 15, & 16)	5.5	V
Power Dissipation at TA=25°C	2.0	W
Derate Above 50°C	20.0	mW/°C
Power Dissipation at T (leads and case)=25°C	5.0	W
Derate for Ground Lead Temperature Above 25°C	40.0	mW/°C
Derate for Case Temperature above 25°C	—	mW/°C

Operating Temperature Range	
CS-2706	-25 to 85°C
CS-3706	0 to 70°C
Storage Temperature Range	-65 to 150°C
Lead Temperature (soldering, 10 sec)	300 °C

NOTES: All voltages are with respect to the four ground pins which must be connected together.

All currents are positive into, negative out of the specified terminal.

PIN CONNECTIONS



NOTE: ALL FOUR GROUND PINS MUST BE CONNECTED TO A COMMON GROUND.

ELECTRICAL CHARACTERISTICS These specifications apply over the operating temperature range of the IC. ($V_{IN} = V_C = 20V$, $V_4 = V_5 = V_{12} = V_{13} = 0V$ unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V, V_C = 20V, V_2 = 0V, Unused pins = open.		8	12	mA
V_C Supply Current	V_{IN} = 20V, V_C = 40V, Outputs low		3	5	mA
V_C Leakage Current	V_{IN} = 0V, V_C = 40V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Digital Input Current	V_I = 0V		-0.6	-1.0	mA
Digital Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_O = -50mA			2.0	V
Output High Sat., V_C-V_O	I_O = -500mA			2.5	V
Output Low Sat., V_O	I_O = 50mA			0.4	V
Output Low Sat., V_O	I_O = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
Inhibit Threshold	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0V		-10	-20	μA
Analog Threshold	V_{CM} = 0V to 15V	100	130	150	mV
Analog input bias current	V_I = 0V, V_{CM} = 15V		-10	-20	μA
Thermal Shutdown	Turn on (TA)		155		°C
Thermal Shutdown	Turn off (TA)		125		°C

TYPICAL SWITCHING CHARACTERISTICS (V_{IN} = V_C = 20V, T_A = 25°C. Delays measured 50% in to 50% out.)

PARAMETER	TEST CONDITIONS	OUTPUT C_L =			UNITS
		open	1.0	2.2	nF
From Inv. Input to Output:					
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N.I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_c Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V Inhibit = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop (+) Ref. = 0 Stop (–) Input = 0 to 0.5V	180			ns

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CIRCUIT DESCRIPTION

Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast. high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_C pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at least 200nsec. must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs—the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} - 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

Supply Voltage

With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply, however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_C. When combined with a CS-384X PWM, the Driver Bias switch can be used to supply V_{IN} to the CS-3706. V_{IN} switching should be fast as undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations

Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

PACKAGE/TEMPERATURE RANGE OPTIONS

Part Number	Package	Temperature Range	Power @ 25°C
CS-3706N	16 Pin Plastic Batwing DIP	0°C to 70°C	2W
CS-2706N	16 Pin Plastic Batwing DIP	-25°C to +85°C	2W