ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply	
		Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	GND -0.3Vto VCC +0.3V	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	TEMP & VCC = OPERATING RANGE MAX	TEMP=25°C VCC=5.0 (1) TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = GND OR VCC
ICCOP	Operating Supply Current (2)		10	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND≤VI≤VCC
IOZ	Output Leakage Current	-1.0	+1.0	±0.5	μA	GND≤VO≤VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.1	V	IOL = 3.2mA
VOH	Output High Voltage	2.4		4.25	V	IOH = -1.0mA
CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance (3)		10.0	8.0	pF	VO = VCC OR GND f = 1MHz
TELQV	Chip Enable Access Time		200	120	ns	(4)
TAVQV	(TAVQV = TELQV + TAVEL) Address Access Time		220	120	ns	(4)
TELQX	Chip Enable Output Enable Time	20	100	40	ns	(4)
TGVQX	Output Enable Output Enable Time	20	100	40	ns	(4)
TGVQZ	Output Enable Output Disable Time	20	100	40	ns	(4)
TELEH	Chip Enable Pulse Negative Width	200		120	ns	(4)
TELEL	Read Cycle Time	350		200	ns	(4)
TEHEL	Chip Enable Pulse Positive Width	150		80	ns	(4)
TAVEL	Address Set-up Time	20		0	ns	(4)
TELAX	Address Hold Time	60		40	ns	(4)

NOTES:

(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information - not guaranteed.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed - not 100% tested.
(4) AC Test Conditions: Inputs-TRISE = TFALL = 20nsec; Outputs -CLOAD = 50pF. All timing measurements at 1.5V.

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6. The address of the bit is again presented, and latched by a second chip enable falling edge.

7. The data outputs are enabled, and read, to verify that the bit was successfully programmed.
   a). If verified, two post programming pulses are applied (the bit is programmed twice more). Then the next bit to be programmed is addressed and programmed .

   b). If not verified, the program/verify sequence is repeated up to 8 times total, at the programming voltage level, 12.5 volts.

8. After all bits to be programmed have been verified at 6.0 volts, the VCC is lowered to 4.0 volts and all bits are verified.
   a). If all bits verify, the device is properly programmed.

   b). If any bit fails to verify, the device is rejected.

PROGRAMMING SYSTEM REQUIREMENTS

1. The power supply for the device to be programmed must be able to be set to four voltages; 4.0V, 6.0V, +12.5V. This supply must be able to supply 500mA average, and 1A dynamic, currents to the PROM during programming. The power supply rise fall times when switching between voltages must be no quicker than 1μ s.

2. The address drivers must be able to maintain input voltage levels $\geq$70% VCC for VIH, and $\leq$ 20% VCC for VIL. The programming system designer has a choice between buffers that will track VCC up and down (e.g. open collector buffers with pull up resistors) or buffers used for VIH only at 4.0V and 6.0V and returned to VIL when the system is at programing voltages.*

3. The control input buffers have the same 70% and 20% VCC requirements as the address buffers. Notice that chip enable ($\overline{E}$) does not require a pull up to programming voltage levels, but that the output enable ($\overline{G}$) must have a pull up to track VCC up and down. The program control (P) must switch from ground to programming VCC level.*

4. The data input buffers must be able to sink up to 3mA from the PROM's output pins without rising more than 0.7 volts above ground, be able to hold the other outputs high with a current source capability of 0.5mA to 2.0mA, and not interfere with the reading and verifying of the data output of the PROM. Notice that a bit to be programmed is changed from a low state (VOL) to high (VOH) by pulling low on the output pin. A suggested implementation is open collector TTL buffers (or inverters) with 4.7KΩ pull up resistors to VCC.*

*Note: Never allow any input or output pin to rise more than 0.3 volts above VCC, or fall more than 0.3 volts below ground.

PROGRAMMING SYSTEM CHARACTERISTICS

PARAMETER	NAME	MIN	TARGET	MAX	UNITS
VCCN	Normal VCC	5.75	6.0	6.25	volts
VCC PGM	Programming Voltage	12.0	12.5	13.0	volts
VCC LV	Low Voltage Verify VCC	3.75	4.0	4.25	volts
ICC	System ICC Capability	500			mA
ICC Peak	Transient ICC Capability	1.0			A
	For PROM Input Pins:				
VOL	Output Low Voltage (to PROM)	-0.3	GND	20% VCC	volts
VOH	Output High Voltage (to PROM)	70% VCC	VCC	VCC +0.3	volts
IOL	Output Sink Current (at VOL)	.01			mA
IOH	Output Source Current (At VOH)	0.1			mA
	For PROM Data Output Pins:				
VOL	Output Low Voltage (to PROM)	-0.3	GND	0.7	volts
VOH	Output High Voltage (to PROM)	70% VCC	VCC	VCC +0.3	volts
IOL	Output Sink Current (at VOL)	3.0			mA
IOH	Output Source Current (at VOH)	0.5	1.0	2.0	mA