Empowered by Innovation

NEC

DSP
Digital Signal Processor

Digital Signal Processor

me
digital

24hour

Upward Mobility: Add value to mobile products with DSP from NEC

Our advanced DSP architecture is capable of executing both audio and video codecs.

How to be top banana in your mobile market

Now that consumers are demanding mobile access to the full range of web services, designers of cell phones, PDAs and other mobile terminals face some daunting challenges. There's a great big market out there. But success is reserved for those who can design subcompact handsets with super-sized features such as downloading music and video on the go.

DSP solutions from NEC are the simple, flexible way to develop multi-function mobile products. Our DSP solutions incorporate application middleware, including software libraries with voice, audio and video codecs. Middleware enhances your design flexibility because it allows you to add innovative applications without dedicated LSIs or additional hardware.

Implemented with the world's finest process technology, our DSP devices achieve the industry's lowest levels of power consumption without any sacrifice of performance. They feature a unique and ultra-efficient signal processing architecture, which is capable of executing both audio and video codecs.

NEC offers advanced DSP cores for system LSIs, application middleware and development tools. Our DSP solutions are based on rich experience and success in Japan, one of the world's most sophisticated and competitive markets for Internet mobile phones.

As the industry leader in process technology, application middleware and overall mobile experience, NEC is your ideal partner for timely development of value-added mobile products.

DSP solutions from NEC

Upward Mobility: Add value to mobile products with DSP from NEC

Enhance features and performance while reducing power consumption with our industry-leading DSP technology
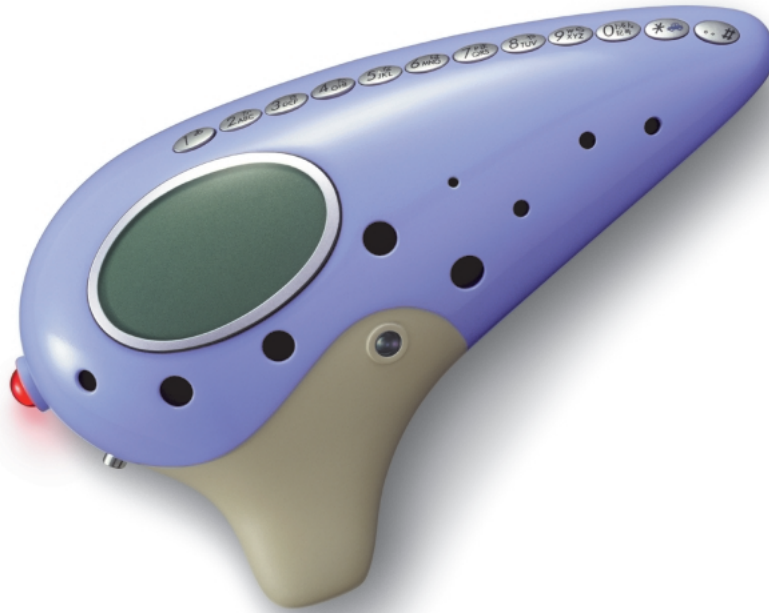
## Make your mobile systems sing with DSP from NEC

Internet connectivity is a must for today's mobile products. To impress contemporary consumers, mobile systems need media-rich performance. But building voice, data, audio and video capabilities into a single compact unit is a real challenge for designers.

If you're looking for ways to raise performance and process large volumes of data while lowering power requirements, take a close look at NEC's 16-bit, fixed-point DSP families (µPD77111, and µPD77210). The µPD77111 Family, implemented with a 0.25-micron process, offers power/performance ratings from 0.8 to 1.25mW/MIPS. The µPD77210 Family raises the bar even higher. Implemented with a 0.13-micron process, this family achieves power/performance of 0.5mW/MIPS.

NEC's unique combination of advanced DSP devices and application middleware helps you develop multi-function mobile products in a hurry. If you want to load lots of features onto a single chip, let us help you with system LSI development. Our system LSI solutions incorporate the industry's most advanced ASIC technology and the expertise we've acquired as one of the world's leading ASIC vendors.

With the most advanced DSP devices, a wide range of application middleware, high-level skills in system LSI design, sophisticated development tools and comprehensive expertise in mobile applications, NEC offers everything you need to succeed in today's mobile markets. If you want to add value to your products, add a valuable partner to your program.
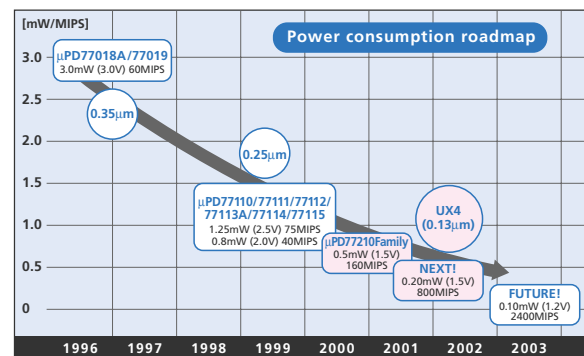
DSP solutions from NEC

Upward Mobility:
Add value to mobile products with
DSP from NEC

If time-to-market is your issue, our DSP development tools are your answer

Tools rule when you're designing
mobile products under deadline pressure

Consumers keep demanding more from mobile products. Today they want PDAs with enhanced communications and cell phones with more computing clout. Tomorrow, they may want interactive gaming or some other hot new feature added to the mix.

Cramming multi-function capability into a compact unit is quite a challenge. And development cycles are shrinking all the time. To succeed in the face of all these pressures, you need the most efficient development tools, the best DSP devices and libraries of advanced middleware.

That's exactly what you get from NEC. To speed up the process of DSP programming, we offer GUI-based development tools. To save you the time and trouble of learning specialized skills for signal processing, we provide a familiar C compiler. We've even developed a DSP-specific operating system that handles multi-task scheduling and memory management with ease. By providing better development tools, we let you concentrate on the many other challenges of mobile-product design.

Our DSP solutions include a wide range of DSP cores, system LSI skills, application middleware, efficient development tools and expertise in mobile applications. As the industry leader in process technology, application middleware and overall mobile experience, NEC is your ideal partner for timely development of value-added mobile products.

DSP solutions from NEC

μPD77111 Family

The μPD77111 Family (μPD77110, 77111, 77112, 77113A, 77114, 77115) is group of low-power-consuming, high-performance DSPs developed for mobile applications.

- Minimum instruction cycle: 13.3 ns (@ 75 MHz operation (MAX))
- Low power consumption: 0.4 to 0.5 mA/MHz (TYP)
- Low-voltage operation: 1.8(2.3**Note**) to 2.7 V (**Note** μPD77110)
- Memory variation: The product that best suits the requirements of the application (low cost, upgradable in the field, etc.) can be selected.
  - ➢ High-capacity RAM: μPD77110
  - ➢ Mask ROM: μPD77111, 77112
  - ➢ ROM/RAM hybrid: μPD77113A, 77114
- Software compatibility with the μPD77016: Instructions compatible with μPD77016 Family. Speech codecs and other middleware provided for the μPD77016 Family can be used.
- Compact package
  The package can be selected to suit the application.
  - ➢ 9 mm $\times$ 9 mm fine-pitch BGA (μPD77111, 77113A)
  - ➢ 12 mm $\times$ 12 mm fine-pitch TQFP (μPD77111)
  - ➢ 14 mm $\times$ 14 mm fine-pitch TQFP (μPD77110, 77112, 77114)

μPD77115

The μPD77115 is a μPD77111 Family DSP designed specifically for audio applications.

- Identical architecture to μPD77111 Family
- Peripheral functions aimed at audio applications
  - ➢ On-chip SD (Secure Digital) card interface
  - ➢ On-chip audio serial interface
  - ➢ DMA transfer between SD card interface and memory
- Compact package
  - ➢ 9 mm $\times$ 9 mm fine-pitch BGA
  - ➢ 12 mm $\times$ 12 mm fine-pitch TQFP

DSP audio decoder middleware utilizing the MP3, MPEG-2 AAC, and Windows Media™ Audio technologies is also available, with ATRAC3 middleware now under development.

μPD77210 Family

As the successor to the μPD77111 Family, the μPD77210 Family (μPD77210, 77213) features higher speed and lower power consumption, achieved through the employment of a UX4 process (0.13 μm rule).

- Instruction cycle: 6.25 ns (@ 160 MHz operation (MAX))
- Low power consumption: 0.3 mA/MHz (TYP)
- Software compatibility with the μPD77016: Instructions compatible with μPD77016 Family. Speech codecs, audio decoders, and other middleware provided for the μPD77016 Family can be used.
- Wide range of peripherals
  - ➢ Audio serial interface
  - ➢ Time division serial interface
  - ➢ 16-bit host interface
  - ➢ 16-bit resolution timer
  - ➢ DMA transfer between peripherals and memory
  - ➢ SD card interface (μPD77213)
- Package
  The package can be selected to suit the application.
  - ➢ 10 mm $\times$ 10 mm fine-pitch BGA
  - ➢ 20 mm $\times$ 20 mm fine-pitch LQFP

List of μPD77111 and μPD77210 Family Functions

	Product Name / Item	μPD77110	μPD77111	μPD77112	μPD77113A	μPD77114	μPD77115	μPD77210	μPD77213
	Maximum operating frequency (MHz)	65	40				50	160	120
		75 (operation @ 2.5 V or over)	75 (operation @ 2.3 V or over)				75 (operation @ 2.3 V or over)		
	Minimum instruction cycle	15.4	13.3				13.3	6.25	8.33
Memory — Internal	Instruction RAM (K words x 32 bits)	35.5	1		3.5		11.5	31.5	15.5
	Instruction ROM (K words x 32 bits)	—	31.75		48		—	—	64
	Data RAM (K words x 16 bits)	48	6		32		32	60	36
	Data ROM (K words x 16 bits)	—	32		64		—	—	64
Memory — External	Instruction area (K words x 32 bits)	—	—	—	—	—	—	—	—
	Data area (K words x 16 bits)	64	—	32	—	16	—	1024	
Peripherals	Audio serial interface (channels)	—	—	—	—	—	1	1	1
	Time division serial interface (channels)	—	—	—	—	—	—	1	1
	Standard serial interface (channels)	2					1 (shared with audio serial interface)	2 (shared with audio and time division serial interfaces)	
	Host interface (bus width)	1 (8 bits)					1 (8/16 bits)		
	General-purpose I/O ports (bits)	4					8	16 (MAX)	
	Timer (channels)	—	—	—	—	—	1	2	
	DMA transfer (channels)	—	—	—	—	—	1 (SD card interface → Internal data RAM)	8 (Peripherals ↔ Internal data RAM)	
	Other	—	—	—	—	—	SD card interface (1 bit)	—	SD card interface (1 bit)
	Clock circuit (on-chip PLL)	External clock multiplied by 1 to 8	External clock multiplied by 1 to 16					External clock multiplied by 10 to 64	
	Standby modes	HALT/STOP							
Operating voltage	DSP core (V)	2.3 to 2.7	1.8 to 2.7				2.0 to 2.7	1.5±5%	
	I/O (V)	2.7 to 3.6							
	Package	100-pin TQFP	80-pin FBGA 80-pin TQFP	100-pin TQFP	80-pin FBGA	100-pin TQFP	80-pin FBGA 80-pin TQFP	161-pin FBGA 144-pin LQFP	

Concept

Power performance targeting mobile applications

With the rapid advances being made in the mobile device field and consequent expansion of broadband mobile communication, the potential for broadening the application area in mobile devices such as cellular phones and PDAs is huge.

NEC is therefore focussing on the development of DSP devices with a power performance that satisfies the low-power-consumption requirements of mobile applications, as well as the provision of an optimized DSP software environment.

System-level integration

NEC is one of the top ASIC vendors in the world and boasts a large customer base. NEC is now offering its customers DSP cores for cell-based ICs to enable the development ASICs that realize system-level integration on a single chip, which is now essential in the development of mobile applications.

Comprehensive DSP programming development environment

However excellent the DSP, if there are too many programming restrictions or the development procedure is too complicated, a considerable amount of time and labor will be required to produce an efficient application. NEC provides its customers with total development support, starting with a device architecture that facilitates efficient DSP programming and a user-friendly GUI-based development environment. Moreover, the availability of a DSP-dedicated C compiler and middleware environment makes DSP programming easy, even for first timers, leaving customers to concentrate time and resources on application development.

Basic architecture (μPD77210 Family)

Some peripherals may differ in the μPD77111 Family.
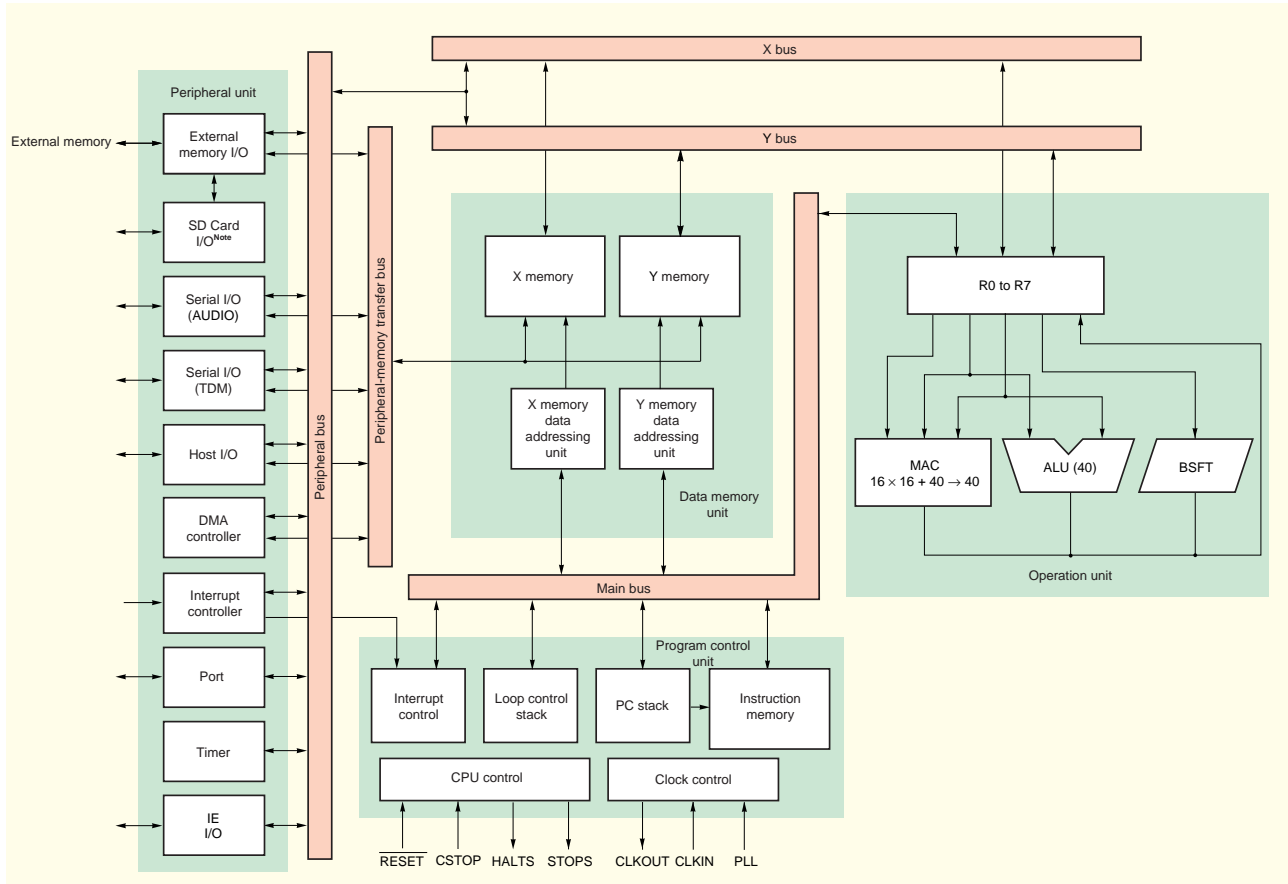
Note μPD77213 only

Use of Harvard architecture and parallel processing

By employing Harvard architecture, in which separate memory spaces are provided for instructions and data, each with an independent bus, and then dividing the data space into two further spaces, again each with an independent bus, NEC is able to provide a DSP that can read instructions, execute operations, and transfer two sets of data simultaneously, thus enabling efficient program writing.

In the μPD77210 Family, moreover, the incorporation of a bus for DMA transfers between the peripherals and the memory enables data I/O with an external interface with no adverse effect on the execution of DSP processing.

Efficient programming operation and language

Programmers are able to write code with superior legibility thanks to the employment of an arithmetic assembler that features C-language-like descriptions.

NEC's DSPs offer easy data handling and efficient programming due to the employment of a pipeline architecture that enhances the execution speed and allows users to design programs that do not have to be aware of the pipeline. With this pipeline architecture, all instructions, except branch and loop instructions, can be executed in one cycle, and the processing result of the previous cycle can be used in the subsequent cycle. A further feature of these DSPs is that the general-purpose registers to which the input operands are written do not have to be specified: any one of 8 general-purpose registers can be used.

On-chip peripherals

- Serial interface: 2 channels in the μPD77110 to 77114, 1 channel supporting an audio codec in the μPD77115, and 1 channel supporting an audio codec and a 1-channel time division serial interface supporting switching applications in the μPD77210 Family.
- Host interface: Parallel bus with a width of 8 bits in the μPD77110 to 77114, and 16 bits in the μPD77115 and 77210 Family.
- General-purpose I/O ports: General-purpose ports $\times$ 4 bits in the μPD77110 to 77114, 8 bits in the μPD77115, and up to 16 bits in the μPD77210 Family.
- Timer: 16-bit timer $\times$ 1 channel in the μPD77115, and 2 channels in the μPD77210 Family.
- Dedicated peripherals: SD card interface in the μPD77115 and μPD77213.
- DMA transfer function: DMA controller for 1-channel transfers between SD card interface and memory in the μPD77115, and 8-channel transfers between peripherals and memory in the μPD77210 Family.

On-chip emulation function

An in-circuit emulation function is provided in each DSP device, through which the delay and noise problems that occur with conventional emulators can be avoided. Also, the use of a dedicated in-circuit emulator and debugger control software facilitates function evaluation.

Harvard Architecture and Efficient Programming System

M-tap FIR filter

Input data X[n]

X[n] Z^{-1} X[n-1] Z^{-1} X[n-2] Z^{-1} X[n-M]

A_0 A_1 A_2 .... A_M

+ + + → Output data Y[n]

Z^{-1} :Delay element A_0 :Constant multiplier   + :Adder

DSP memory

X data memory (input data)

X_n	← dp0
X_{n-1}	
X_{n-2}	
⋮	
X_{n-M}	

Y data memory (co-effiecient data)

A_0	← dp4
A_1	
A_2	
⋮	
A_M	
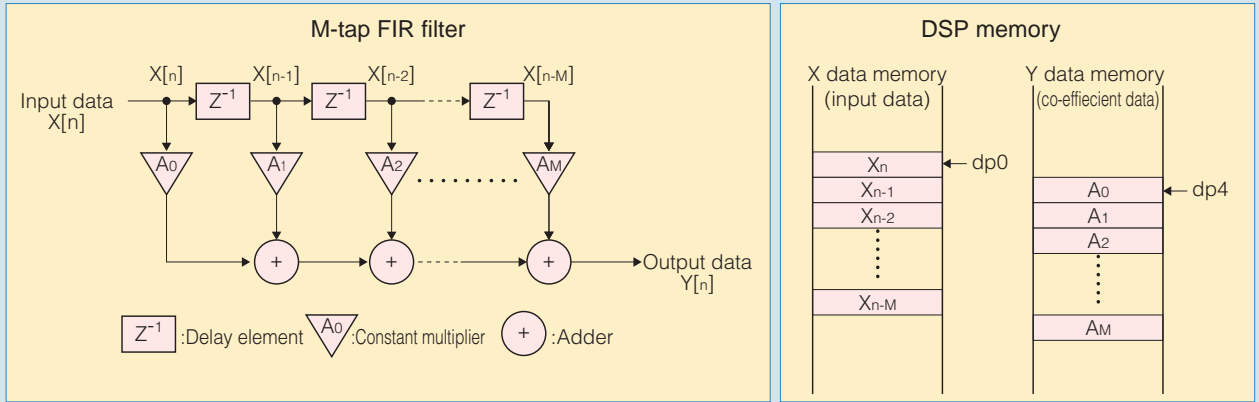
Example of FIR realized using DSP

Hardware loop mechanism with no overhead

8 x 40-bit general-purpose registers (no restictions on operator input)

Arithemetic assembler with excellent legiblity

```
rep M;
r0 = r0 + r1H*r2H   r1 = *dp0++   r2 = *dp4++;
```

Multiply accumulator operations, 2-data transfers, and data pointer updates executed in 1 instruction cycle

Data pointer updated after data transfer

16 bits x 16 bits + 40 bits→ 40 bits multiply accumulator

Operation results can be used in next cycle

4 data pointers each for X and Y memories

Multiplication executed 256 or more times continuously by 40-bit register with no overflow

- Using the higher 8 bits of a 40-bit register as head room, multiply accumulator operations can be executed continuously at least 256 times with the same precision, without having to perform overflow detection.
- Processing results can be used as operator inputs in the next cycle, facilitating data handling in programming.
- Data handling while programming is made easy by using 8 general-purpose registers to remove restrictions on operator input.
- All instructions (except branch and loop instructions) are executed in one cycle.

Road Map

* :Under development

High-performance DSP

μPD77xxx*

High-performance
1000 MIPS DSP

μPD77210 Family

Low power consumption DSP

μPD77yyy*

0.9 V drive DSP

μPD77111 Family

μPD77115

Audio decoder DSP
using μPD77111 architecture

μPD77213

Large-capacity RAM/mask ROM
hybrid product
Includes dedicated peripherals
for audio decoders
and video codecs

Application Specific DSP

μPD77533

GPS signal processing LSI

μPD775xx*

μPD77110,
77111, 77112,
77113A, 77114

0.25 μm process full RAM
and mask ROM products
Max. 75 MHz operation

μPD77210

UX4 (0.13 μm process)
full RAM process
160 MHz operation
Instruction RAM: 31.5 Kwords
Data RAM: 60 Kwords

2001

2002

Development Tools

Software development tools

• Software tool package (SP77016[Note 1])
• Software tool package (SP77210[Note 2])
• C compiler (CC77016)

The SP77016 is a package that includes the WB77016, HSM77016 and ID77016 software tools in a CD-ROM. Each software tool can also be supplied separately.
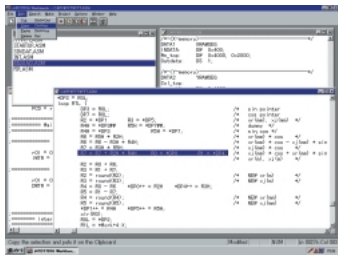
■ Workbench (WB77016)
This is an integrated program development environment package that includes a relocatable assembler, a linker, an editor, and a Make utility, enabling efficient development, from program editing to object code generation.
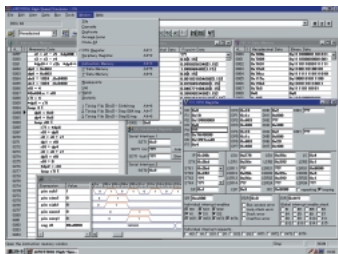
■ High-speed simulator (HSM77016)
This device enables simulation of DSP operations, both those executed internally and those executed via an external interface, in a PC environment. As source code simulation is also supported, simulation can be performed in C-language instruction units using a C compiler.
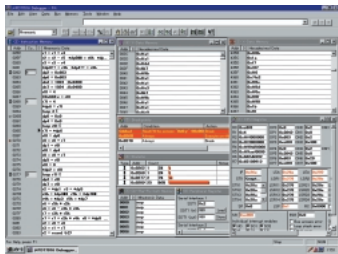
■ Debugger control software (ID77016)
This software is used to control an in-circuit emulator (NDSP_ICE001 or NDSP_ICE002).
With this software, the operation of the target device can be verified using the same user interface as the high-speed simulator (HSM77016).

■ C compiler (CC77016)
The CC77016 is an ANSI-compliant C compiler that compiles C-source program into WB77016 assembly language. Efficient compilation results are obtainable through support of DSP-C (a C language extension supporting DSP architecture).

Notes 1. The software tool for μPD7701x, and μPD77111 Family.
　　　 2. The software tool for μPD77210 Family. This package includes assembler/linker, software simulator, hardware debugger in a CD-ROM. These software tools cannot be supplied separately.

Remark The SP77016 and SP77210 are only available in Japan. Overseas customers wishing to purchase these products are requested to contact an NEC distributor or sales office.

Hardware development tools

- USB interface in-circuit emulator (NDSP_ICE001)[Notes 1, 2]
- PCMCIA interface in-circuit emulator (NDSP_ICE002)[Note 1]

NDSP_ICE001

USB interface in-circuit emulator

Host machine

+

NDSP_ICE002

PCMCIA interface in-circuit emulator

+

User target board

The DSP is mounted on the user target board, from which debug pins must be derived.
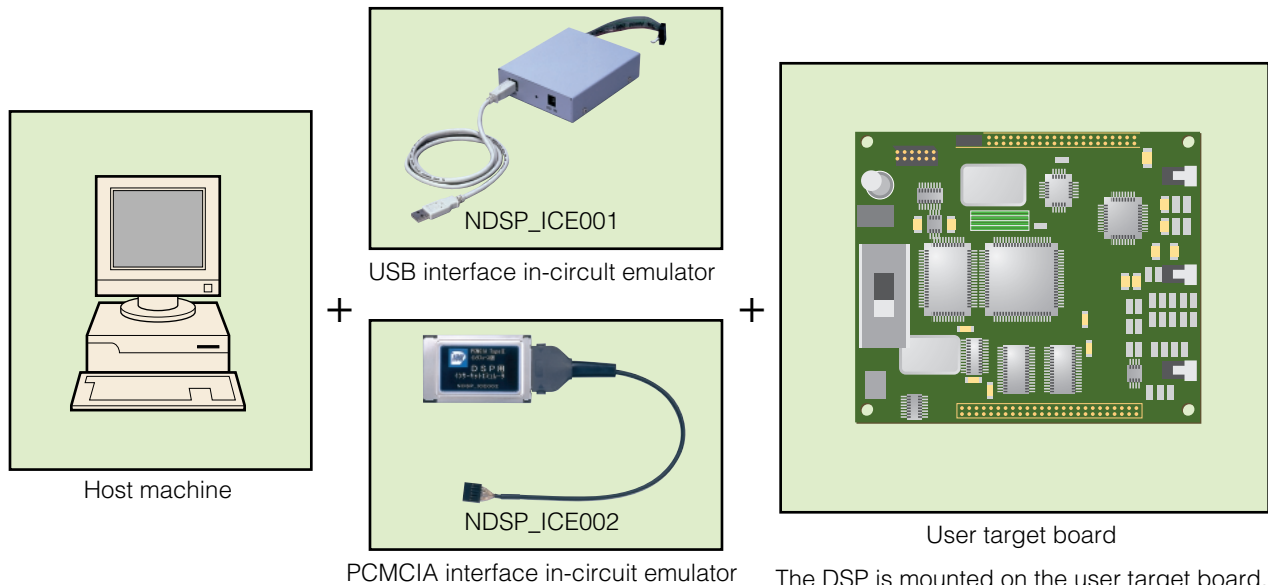
Notes 1. Product of ANDOR System Support, Co., Ltd.
2. Under development

The NDSP_ICE001 and NDSP_ICE002 are devices for interfacing between the host machine and the in-circuit emulator function incorporated in the DSP device. The interfaces on the host machine side are USB and PCMCIA respectively. On the DSP device side, an interface for debugging (using JTAG pins) is used. Windows® 95/98/2000 is the OS used in the host machine, which must also support a USB or PCMCIA interface.
Separate debugger control software (ID77016) is required to operate the NDSP_ICE001 and NDSP_ICE002.

The following product is also provided as a simple evaluation board.
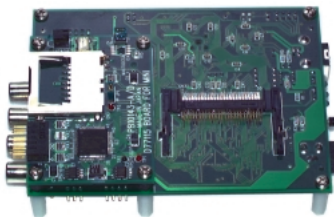
■ **Application board mini**[Note]

This board includes a DSP, stereo sound codec, and microcontroller (V850/SA1™). The μPD77110 and μPD77210 are provided as the DSP. The μPD77110 incorporates a CompactFlash™ card adapter, enabling data I/O with a CompactFlash card, and the μPD77210 incorporates an SD card adapter, enabling data I/O with an SD card.

Note Product of ANDOR System Support, Co., Ltd.

Remark Software development tools and an in-circuit emulator are separately required for this board.

Development tool information

Product Name		Target Device	
		μPD77111 Family	μPD77210 Family
SP77016	Software package	○	—
WB77016	Workbench	○	—
HSM77016	High-speed simulator	○	—
ID77016	Debugger control software	○	—
SP77210	Software package	—	○
CC77016	C compiler	○	○
USB interface in-circuit emulator[Notes1,2,3]		○	○
PCMCIA interface in-circuit emulator[Notes1,3]		○	○
Application board mini (Simplified evaluation board)[Note3]		○	○

Notes 1. The ID77016 or software tool package (SP77210) is also necessary.
     2. Under development
     3. This product is sold and supported by ANDOR System, Support, Co., Ltd.
       For further information, please contact:
        ANDOR System Support Co., Ltd.
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        Shinagawa 2-15-8, Shinagawa-ku, Tokyo 140-0004
        Phone: +81-3-3450-8101, http://www.sys-andor.co.jp/kaisha/enframe.htm   E-mail: esda@sys-andor.co.jp

Remark Customers wishing to purchase software development tools are requested to contact an NEC distributor, our sales
        office, or ATAIR SOFTWARE.
        ATAIR SOFTWARE G.M.B.H
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        Phone: +43-1-535-9913,   http://www.atair.co.at,   E-mail: office@atair.co.at

Middleware

NEC provides the following middleware library for its DSP products.

Notes 1. Decoder
     2. Encoder

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