FULLY DECODED 8192 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

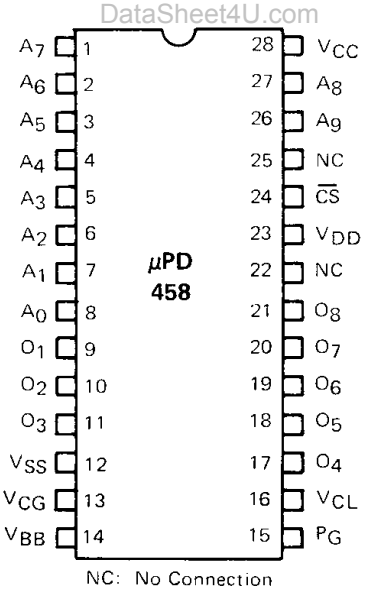
The μPD458 is an Electrically Erasable and Reprogrammable Read Only Memory (EEPROM), organized as 1024 words by 8 bits.

The μPD458 is fabricated with N-channel MOS technology and is packaged in a 28 pin ceramic DIP.

FEATURES

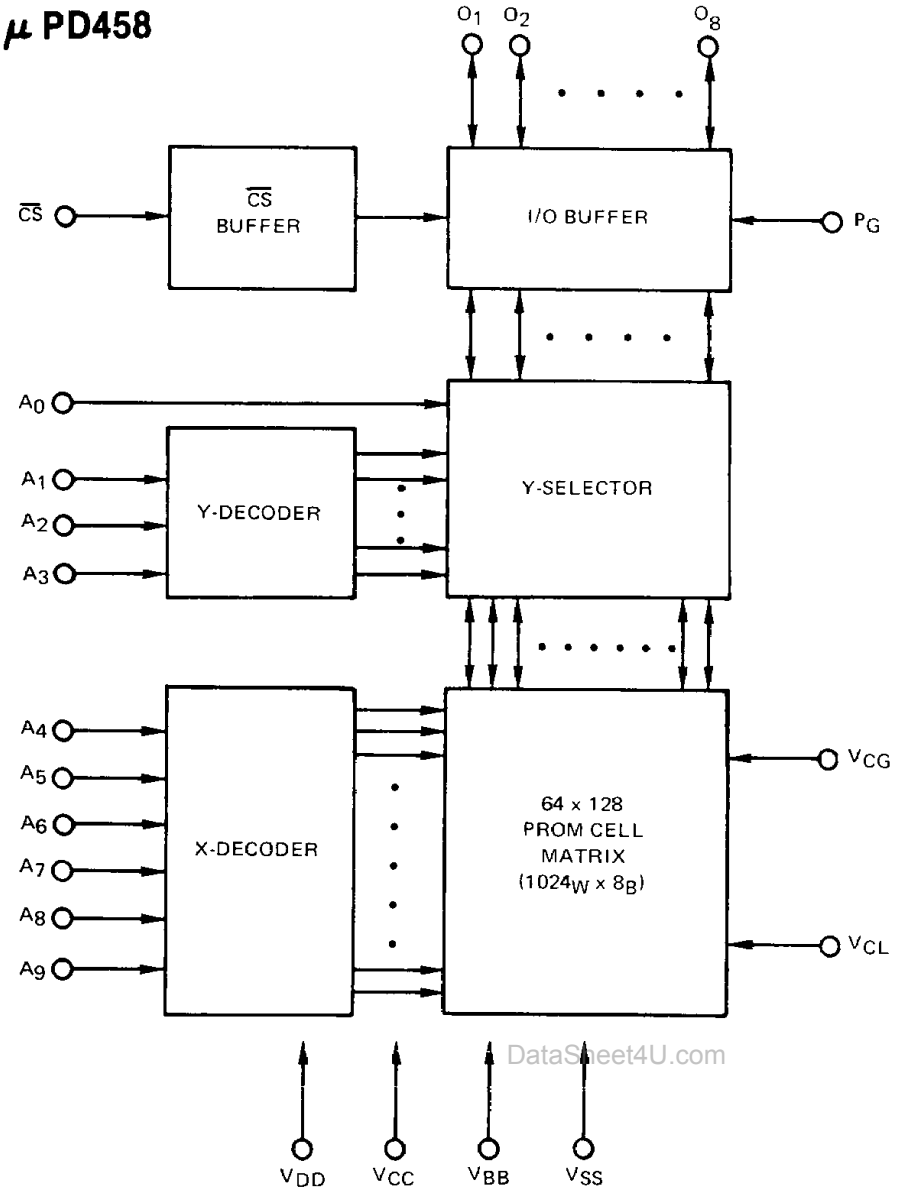
- Electrically Erasable and Reprogrammable
- Fully Decoded, 1024 Words x 8 Bits Organization
- Access Time – 450 ns max.
- Fast Programming and Erasure Speed
- Simple Worst-case Verification of Programmed Data and Erasure
- Static, No Clock Required
- Input/Output TTL Compatible for Read and Programming Operation
- Three-State Output, OR-Tie Capability
- N-Channel MOS
- Two Power Supplies, +12V and +5V for Read
- 28 Pin Ceramic DIP

PIN CONFIGURATION



NC: No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.3 to +11 Volts①
All Input Voltages	−0.3 to +11 Volts①
Supply Voltage V_{DD}	−0.3 to +15 Volts①
Supply Voltage V_{CC}	−0.3 to +7 Volts①
Supply Voltage V_{BB}	V_{SS} to −7 Volts②
Supply Voltage P_G	−0.3 to +30 Volts①②
Supply Voltage V_{CL}	−0.3 to +43 Volts①②
Supply Voltage V_{CG}	−44 to +30 Volts①②

Notes: ① Relative to V_{BB}.

② Data in the memory cell is not guaranteed to be preserved.
Specifies ratings which will not cause permanent damage to the device.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

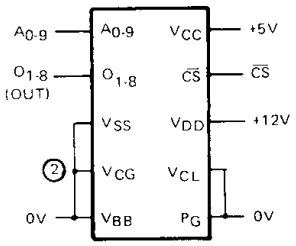
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	f = 1 MHz

SUPPLY VOLTAGES

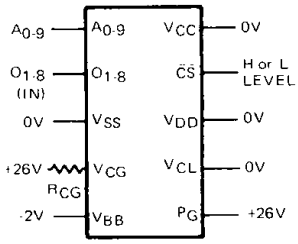
Typical values. Unit – Voltage.

MODE \ PIN	V_{DD}(23)	V_{CC}(28)	V_{BB}(14)	P_G(15)	V_{CL}(16)	V_{CG}(13)	V_{SS}(12)
Read	+12	+5	0	0	0	0	0
Program	0	0	-2	+26	0	+26	0
Erase	0	0	-5	0	+36	-40	0 or Open
Verify "0"	+12	+5		0	0	+3	0
Verify "1"	+12	+5		0	0		0

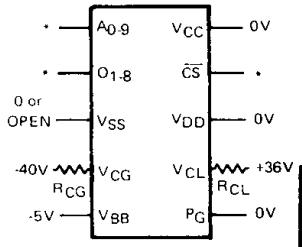
READ



PROGRAM



ERASE



Notes: * = Either High or Low Level, or Open.

① R_{CG} and R_{CL} are Protection Resistors
R_{CG} = 10 kΩ ± 10%, 1/4W
R_{CL} = 200Ω ± 10%, 10W

② R_{CG} may be left connected in Read Mode.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	INPUT/ OUTPUT	FUNCTION
1 – 8, 26, 27	A_0 – A_9	Input	Address Input
24	$\overline{CS}$	Input	Chip Select Input (Active Low)
9 – 11, 17 – 21	O_1 – O_8	Output	Data Out for Read Operation
		Input	Data Input for Programming Operation
15	P_G	Power Supply	Power Supply for Programming Operation
16	V_{CL}	Power Supply	Power Supply for Erasure Operation
13	V_{CG}	Power Supply	Power Supply for Control Gate for Programming and Erasure Operation
14	V_{BB}	Power Supply	Power Supply for Substrate Bias
23	V_{DD}	Power Supply	+12V Power Supply for Read Operation
28	V_{CC}	Power Supply	+5V Power Supply for Read Operation
12	V_{SS}	GND	Ground Reference

READ OPERATION

DC CHARACTERISTICS

T_a = -10 to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%,
V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V

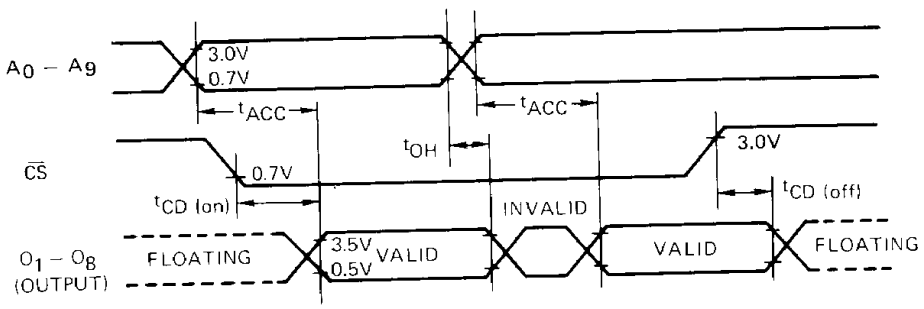
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Output High Voltage	V_{OH}	3.5			V	I_{OH} = -2.0 mA
Output Low Voltage	V_{OL}			0.5	V	I_{OL} = 1.7 mA
Input Leakage Current High	I_{LIH}			+10	μA	V_I = +3.0V
Input Leakage Current Low	I_{LIL}			-10	μA	V_I = +0.7V
Output Leakage Current High	I_{LOH}			+20	μA	$\overline{CS}$ = "1" V_O = 3.5V
Output Leakage Current Low	I_{LOL}			-10	μA	$\overline{CS}$ = "1" V_O = 0.4V
V_{DD} Supply Current	I_{DD}		55	80	mA	
V_{CC} Supply Current	I_{CC}		20	30	mA	with no load

AC CHARACTERISTICS

T_a = -10 to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%,
V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Access Time	t_{ACC}			450	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	$t_{CD(on)}$			200	ns	
$\overline{CS}$ to Output Off Delay	$t_{CD(off)}$	0		200	ns	
Output Hold Time	t_{OH}	0			ns	

TIMING WAVEFORMS



PROGRAMMING OPERATION

Programming is performed word by word and one word at a time. Address and an 8 bit programming word for that address should be input at the same time. High level data "1" given through one of Data Input terminals (O_1 – O_8) writes a high level data "1" into the memory cell specified with the address input and its bit position.

After erasure, all memory cells of the μPD458 contain cleared data "0". By this programming operation, only the memory cells which contain data "0" are programmed to high level data "1" by high level input. Thus before normal programming operation, the μPD458 should undergo erasure operation to clear all bits to "0".

DC CHARACTERISTICS

T_a = 25°C ± 2°C, V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V. $\overline{CS}$ = Either HIGH or LOW level.

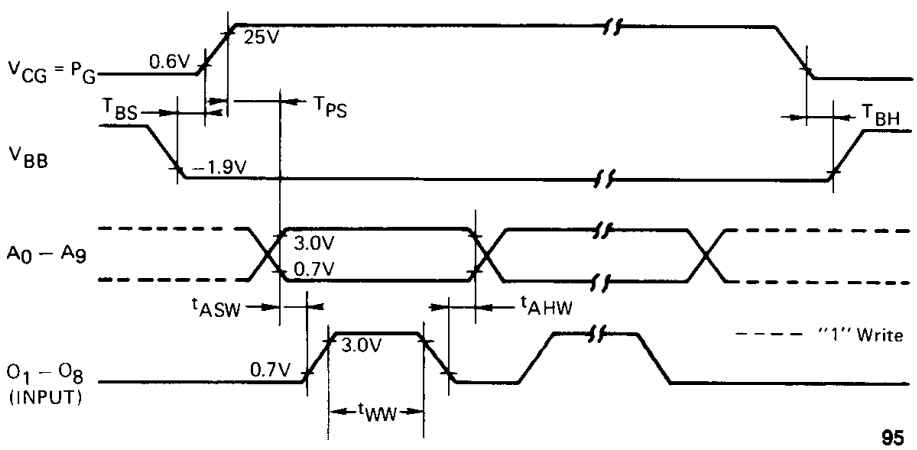
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		5.25	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Supply Voltage	V_{BB}	-1.9	-2.0	-2.1	V	
Supply Voltage	P_G	25	26	27	V	
Supply Voltage	V_{CG}	25	26	27	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}		-8	-15	mA	
Supply Current (P_G)	I_G		+30	+50	mA	
Supply Current (V_{CG})	I_{CG}			+20	μA	

AC CHARACTERISTICS

T_a = 25°C ± 2°C, V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V. $\overline{CS}$ = Either HIGH or LOW level.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Setup Time	t_{ASW}	10			μs	
Address Hold Time	t_{AHW}	10			μs	
Write Data Width	t_{WW}	40		100	ms	per one word
V_{BB} Setup Time	T_{BS}	1.0			μs	
V_{BB} Hold Time	T_{BH}	1.0			μs	
P_G, V_{CG} Setup Time	T_{PS}	10			μs	

TIMING WAVEFORMS



ERASURE OPERATION*

DC CHARACTERISTICS

T_a = 25°C ± 2°C, V_{DD} = V_{CC} = P_G = 0V, V_{SS} = 0V or Open
$\overline{CS}$, A_0 – A_9 and O_1 – O_8 = Either HIGH or LOW level, or non-connected

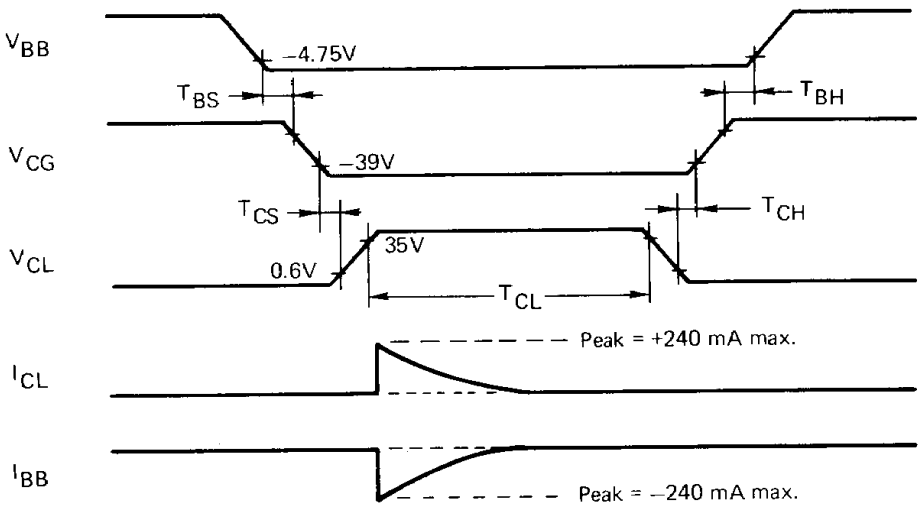
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{BB}	−4.75	−5.0	−5.25	V	
Supply Voltage	V_{CL}	+35	+36	+37	V	through R_{CL}
Supply Voltage	V_{CG}	−39	−40	−41	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}			−240	mA	Initial peak current. See timing chart.
Supply Current (V_{CL})	I_{CL}			+240	mA	
Supply Current (V_{CG})	I_{CG}			−20	μA	

AC CHARACTERISTICS

T_a = 25°C ± 2°C, V_{DD} = V_{CC} = P_G = 0V, V_{SS} = 0V or Open
$\overline{CS}$, A_0 – A_9 and O_1 – O_8 = Either HIGH or LOW level, or non-connected

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP	MAX		
Clear Time	T_{CL}		60		sec	
V_{BB} Setup Time	T_{BS}	0			μs	
V_{BB} Hold Time	T_{BH}	0			μs	
V_{CG} Setup Time	T_{CS}	1.0			μs	
V_{CG} Hold Time	T_{CH}	1.0			μs	

TIMING WAVEFORMS



Note: The supply currents I_{BB} and I_{CL} diminish to almost zero within T_{CL}.

*Erasure operation clears all 8192 bits to Logic "0" simultaneously.

APPENDIX PROM PROGRAMMER DESIGN

To insure integrity and retention of data programmed in the μPD458, the following requirements are specified for the μPD458 supply voltage and current levels. The PROM PROGRAMMER should be designed such that voltages provided to the PROM socket be within the range specified on any occasion including power on/off to the programmer, power on/off to the μPD458, and in READ, WRITE or ERASE operation. Surge or noise voltages beyond the specified range are to be avoided.

Setting V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5% and V_{CG} = +3V ± 0.1V after erasure and comparing data read from the μPD458 with zero effectively tests for proper erasure.

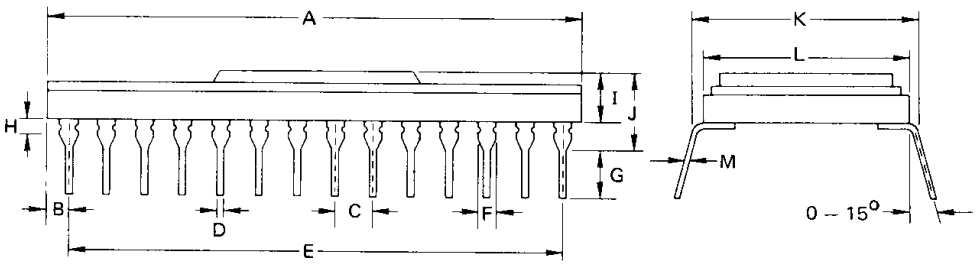
Setting V_{DD}= +12V ± 5%, V_{CC} = +5V ± 5% and V_{CG} = −3V ± 0.1V after programming and comparing data read from the μPD458 with the desired data coupled with erase verification, provides a simple test of worst-case temperature and long-term data retention.

Under normal Read Mode conditions, V_{CG} should either be grounded directly or held at 0V ± 0.1V through R_{CG}. R_{CG} is required when any non-zero voltage is applied to V_{CG}.

SYMBOL	LIMITS ②									UNIT	TEST CONDITIONS
	READ			PROGRAM			ERASE				
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{DD}	+11.4	+12	+12.6	−0.3	0	+0.3	0.3	0	+0.3	V	
V_{CC}	+4.75	+5	+5.25	−0.3	0	+0.3	−0.3	0	+0.3	V	
V_{CG}	−0.1	0	+0.1	+25	+26	+27	−39	−40	−41	V	
V_{BB}	−0.1	0	+0.1	−1.9	−2	−2.1	−4.75	−5	−5.25	V	
P_G	−0.3	0	+0.3	+25	+26	+27	−0.3	0	+0.3	V	
V_{CL}	−0.1	0	+0.1	−0.1	0	+0.1	+35	+36	+37	V	
I_{CC}		+20	+30			−0.2			0.2	mA	①
I_{DD}		+55	+80			−0.2			−0.2	mA	①
I_{CG}			+10			+20			−20	μA	①
I_{BB}			−0.2		−8	15			−240	mA	①
I_{PG}			−0.2		+30	+50			−0.2	mA	①
I_{CL}			−0.5			−10			+240	mA	①

Notes: ① At typical supply voltage
② All voltages relative to VSS = 0V.

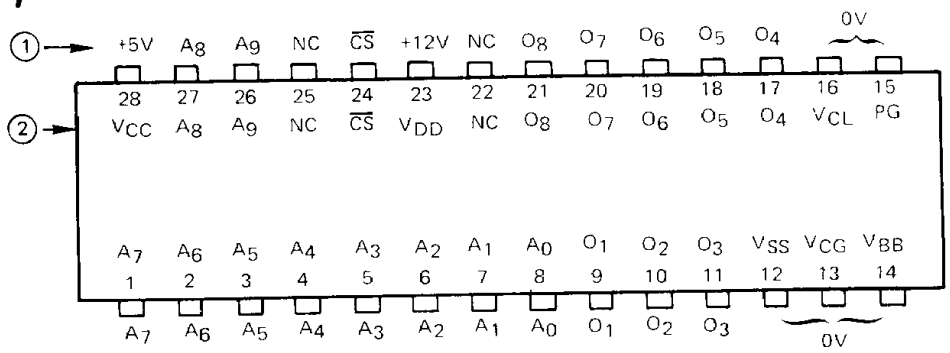
PACKAGE OUTLINE μPD458D



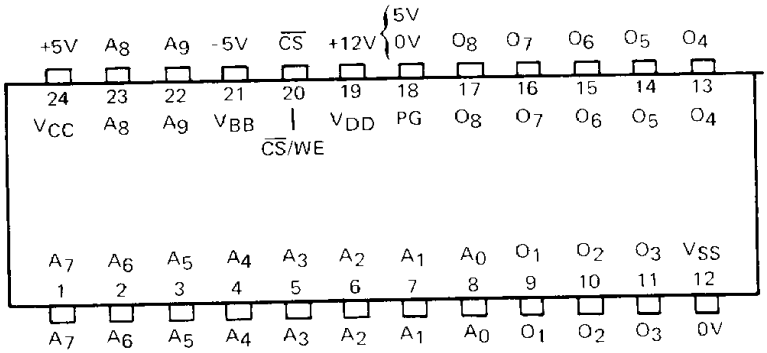
ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.41 MAX.
B	1.5 MAX.	0.059 MAX.
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

μ PD458

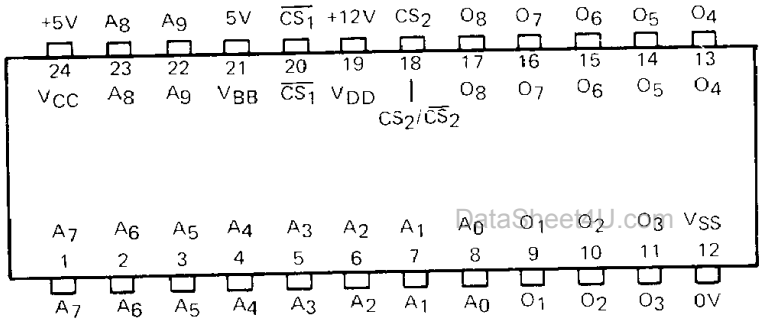
μPD458D (EEPROM)



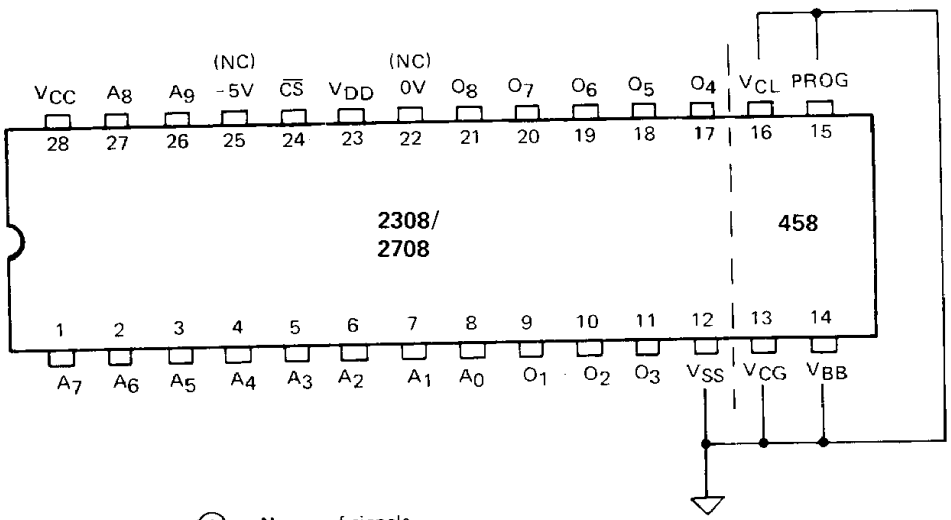
2708 (PROM ERASABLE WITH ULTRAVIOLET)



μPD2308C/D – 2308 (MASK ROM)



COMMON PIN CONFIGURATION



Notes: ① Names of signals.
② Names of the terminal.

SP458-4-77-GY-CAT