



# ICs for Communications

Analog Line Interface Solution - ALIS  
ALIS V3

PSB 4595 Version 2.1

PSB 4596 Version 3.1

Preliminary Data Sheet 04.99

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## Preface

This document, the *Preliminary Data Sheet*, describes the functionality, application and software issues of the Infineon Technologies Analog Line Interface Solution (ALIS) chipset, ALIS-A and ALIS-D. It is intended to provide as well a hardware as a software design engineer with the most important information needed to evaluate and use the ALIS chipset for an application.

## Organization of this Document

This *Preliminary Data Sheet* is organized as follows:

- Chapter 1, Overview  
Includes the general description, features list, logic symbol, and summary of typical applications.
- Chapter 2, Pin Descriptions  
Includes the configuration of pins, descriptions of their functions, and the interconnection of the ALIS-A with the ALIS-D.
- Chapter 3, Functional Description  
Summarizes the functional architecture and operating modes of the ALIS.
- Chapter 4, Operational Description  
Summarizes the different operating states, and the performance of the ALIS as a Data Access Arrangement (DAA).
- Chapter 5, Interface Descriptions  
Summarizes the hardware and software aspects of the Serial Control Interface (SCI), Serial Data Interface (SDI), telephone line connection, and Caller-ID interface.
- Chapter 6, Register Description  
Contains a map of registers and their descriptions.
- Chapter 7, Programming  
Describes how to address the registers of the ALIS-D for programming.
- Chapter 8, Timing Diagrams  
Contains the timing parameters for all signals.
- Chapter 9, Electrical Characteristics  
States the recommended operating conditions, absolute extreme range, DC and AC characteristics.
- Chapter 10, Package Outlines  
Includes package outlines for both ALIS-A and ALIS-D components.
- Chapter 11, Appendix  
Includes a glossary.
- Chapter 12, Index

## Related Documentation

Additional documentation for the ALIS chipset includes a “*Product Brief*”, “*Product Overview*” and assorted “*Application Notes*”.



## **1 Overview**

The Analog Line Interface Solution (ALIS) chipset is a complete analog modem front-end that integrates a fully programmable Data Access Arrangement (DAA) with a high quality codec. It can be used for analog subscriber equipment, such as modems, fax, or voice appliances. It provides:

- Modem performance improved by digital isolation interface: greater linearity, reduced noise;
- Adaptation to different countries' line requirements by downloading of coefficients;
- Form-factor and power consumption optimized for portable and battery-operated equipment;
- Conformance with PC 98/PC 99 on Caller-ID storage, wake-up on incoming calls, and power-saving modes; and
- Demonstrated worldwide compliance to telecom and safety standards with pre-homologated reference systems.

The ALIS chipset consists of an analog component—the ALIS-A (PSB 4595)—and a digital part—the ALIS-D (PSB 4596). The ALIS-A, which is powered by the loop current of the telephone line, implements the line interface, ring detector, hybrid, filters and the codec. The ALIS-D incorporates programmable digital filter structures that allow very flexible line adaptation. It provides dialing functions, captures Caller-ID information and stores it in a register, even when the device is in power-down state. The ALIS chipset uses small 24- and 28-pin packages and conforms to PC-Card standards.

## Analog Line Interface Solution - ALIS ALIS V3

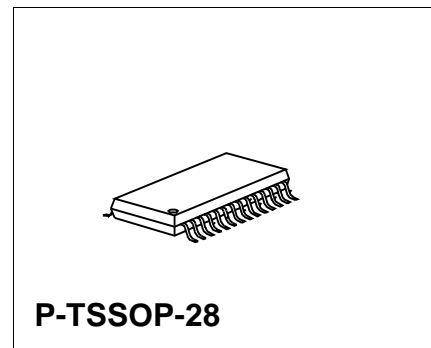
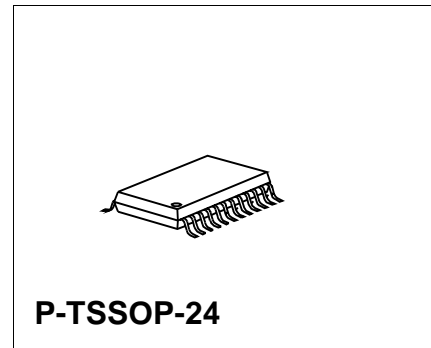
PSB 4595  
PSB 4596

### ALIS-A Version 2.1 ALIS-D Version 3.1

#### 1.1 Features

##### *Cost savings features*

- Integrates two-wire Tip/Ring interface, hybrid, codec, and digital filter structures for flexible line adaptation.
- Integrates ring detector, DTMF and pulse dialing.
- Digital isolation interface between ALIS-A and ALIS-D chips eliminates voice band transformer.
- Reduces Bill of Materials (BOM).
- Phase-Locked Loop allows sampling rates from 7.2 to 32 kHz.
- Eliminates requirement for country-specific designs and optimization.
- Reference approvals reduce expenses and time for homologations.



##### *World-wide compliance features*

- Provides a Data Access Arrangement (DAA) configurable for international application.
- Fully programmable subscriber line characteristics: Transhybrid loss, AC impedance, DC characteristics, receive and transmit levels.
- Telco reference approvals according to FCC Part 68 (USA), CTR-21 (UK, future European Standard), B-11 23A (France), BAPT 223 ZV5 (Germany), JATE (Japan), TS002 (Australia).
- Safety reference approval according to IEC 950, EN 60 950, covering: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Portugal, Spain, Switzerland, United Kingdom.

Type	Package
PSB 4595	P-TSSOP-24
PSB 4596	P-TSSOP-28

- Programmable Caller-ID receiver conforms to Bell 202, CCITT V.23, and Bellcore specifications TR-NWT-000030 and SR-TSV-002476.

*Performance features*

- 16-bit linear codec meets V.34 and V.90 modem requirements.
- Programmable symbol and data rates.
- Reduced noise due to a short analog signal path.
- Excellent transmission quality (even in low-frequency range) provides superior modem performance, particularly for V.90 modems.
- Provides Caller-ID storage.

*Time-to-market*

- Requires only one hardware design for the global market.
- Predefined country-specific coefficient sets available.
- Evaluation system available.
- Excellent development tool support.

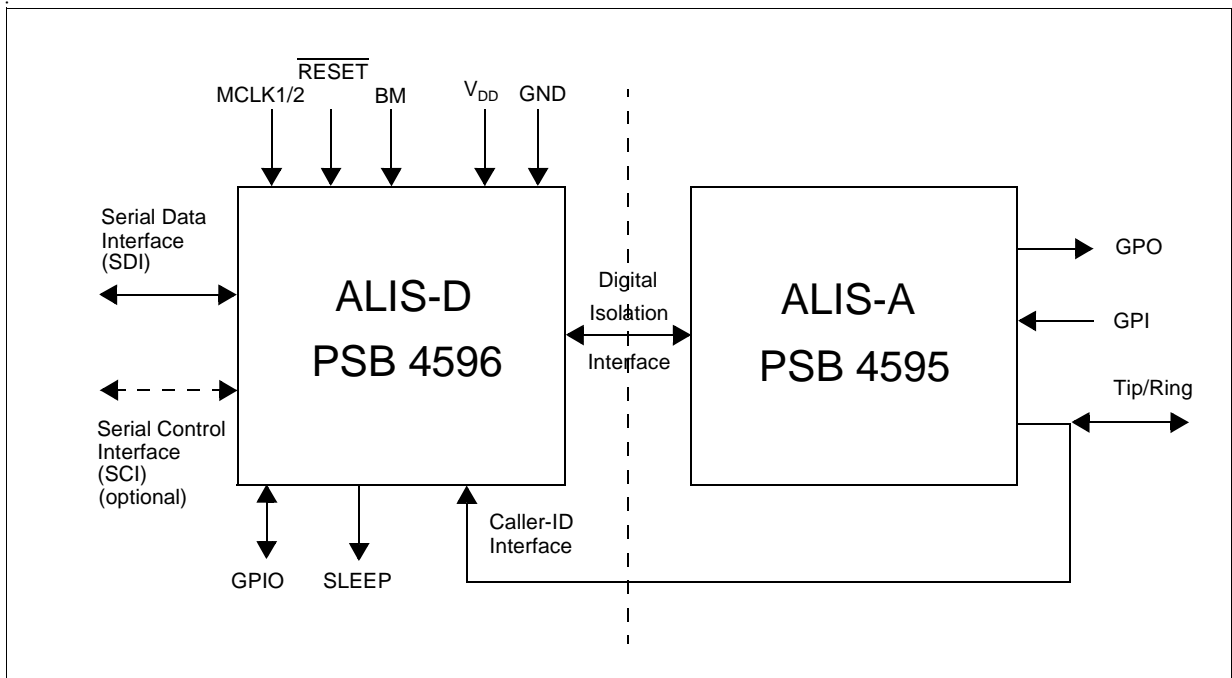
*Form factor*

- Small, PC-Card compliant packages (P-TSSOP24, P-TSSOP28).
- Ideal for PC-Card applications (no bulky voice band transformer).
- Minimizes the number of discrete components.

*Power saving features*

- ALIS-A is powered by the Tip/Ring loop current.
- ALIS-D supports two power management states to reduce power consumption.
- Supports PC power management functions with wake-up signal and Caller-ID storage (PC 98 ready).

## 1.2 Logic Symbol



**Figure 1-1 Logic Symbol of the ALIS Chipset**

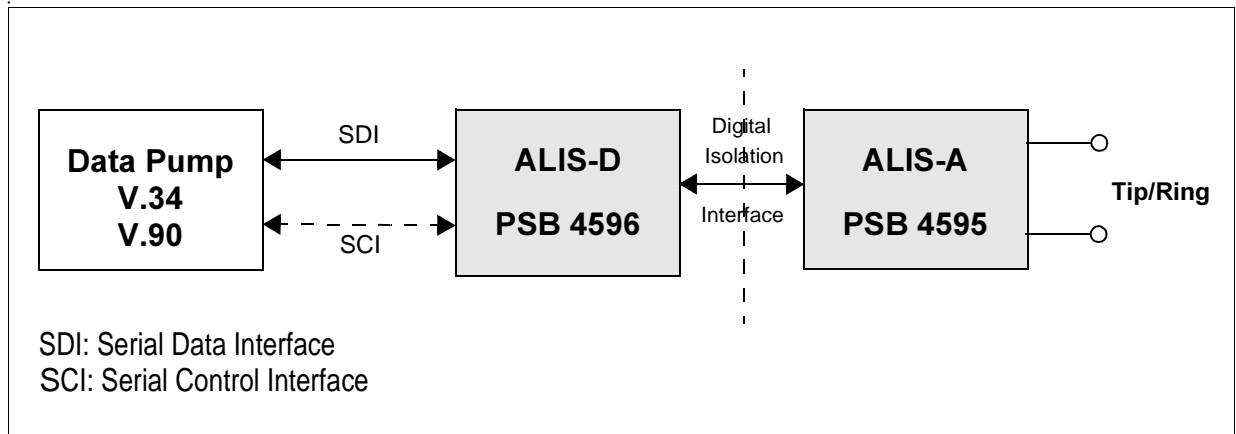
*Note: The Serial Control Interface SCI can optionally be used for programming the chipset (see **Chapter 5.1.1.1**).*

### 1.3 Typical Applications

The ALIS can be used in different modem applications to connect the data pump to the Tip/Ring wire.

#### 1.3.1 ALIS with DSP-based Modem

For a modem data pump, the ALIS provides the front-end to the Tip/Ring.



**Figure 1-2 DSP-based Modem Application**

Isolation is provided by a digital Isolation interface between the ALIS-A and the ALIS-D (see **Chapter 5.1.5**). This allows very flat frequency response over the entire voice band, even at low frequencies.

### 1.3.2 ALIS with Software Modem

The ALIS can also be used in software modems, in which V.34 or the V.90 modem algorithms are run on the host. In this application, the Serial Data Interface (SDI) is connected to the USB or PCI interface via a FIFO structure.

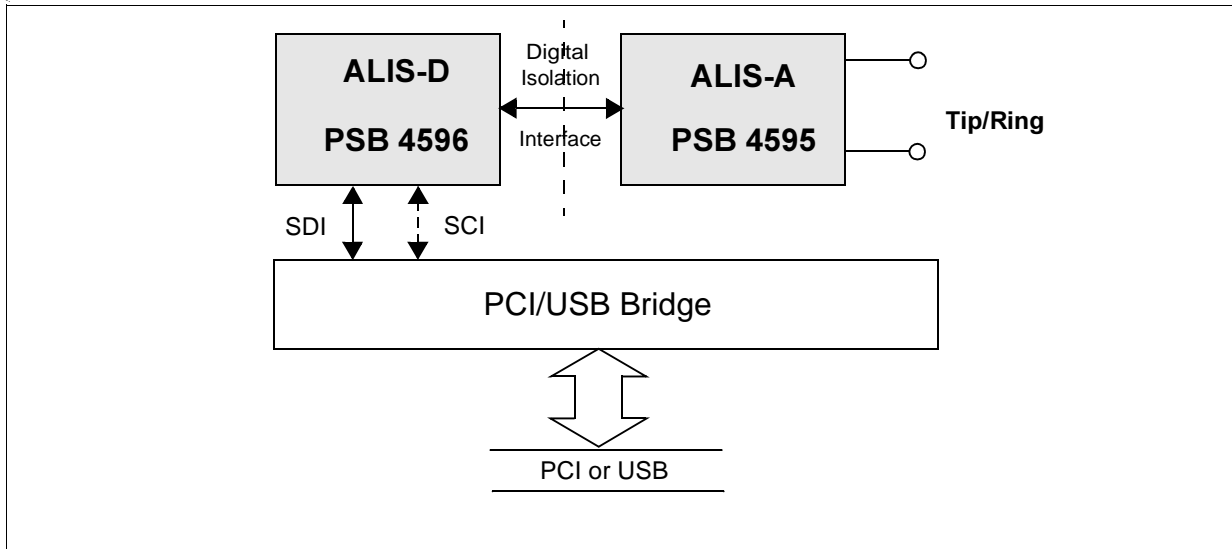


Figure 1-3 Software Modem Application

## 2 Pin Descriptions

### 2.1 Pin Configurations

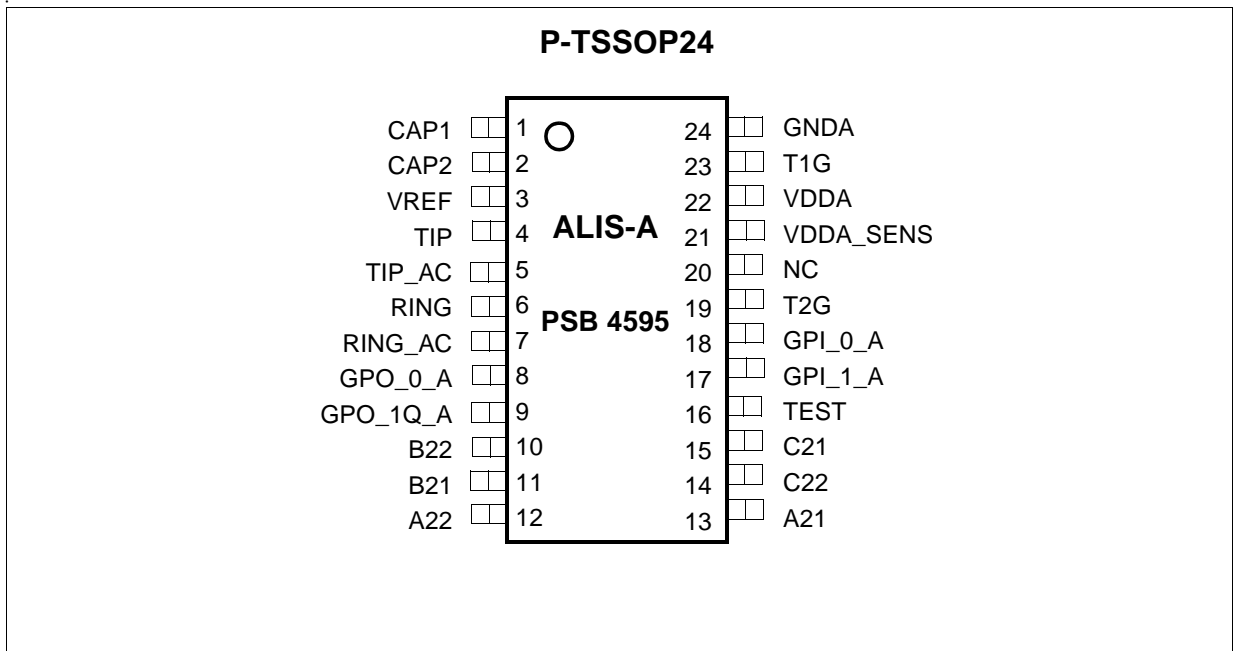


Figure 2-1 Pin Configuration of the ALIS-A (PSB 4595) (Top View)

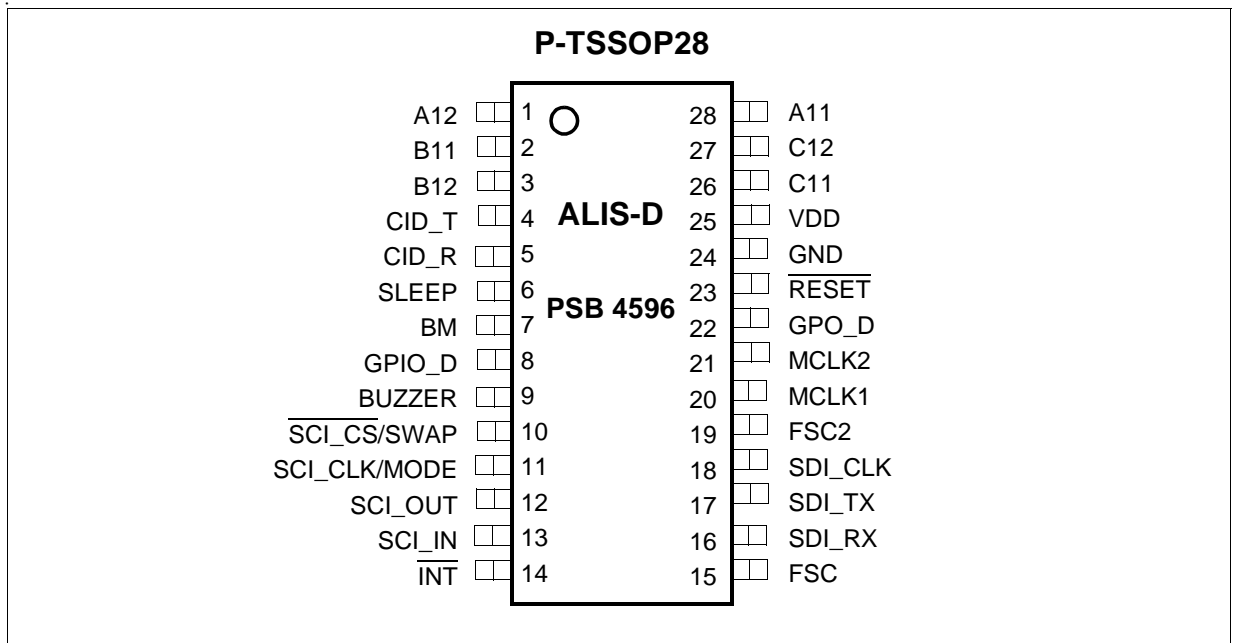


Figure 2-2 Pin Configuration of the ALIS-D (PSB 4596) (Top View)

## 2.2 Pin Definitions of ALIS-A (PSB 4595)

**Table 2-1 ALIS-A Pin Definitions**

<b>Symbol</b>	<b>Pin</b>	<b>Type</b>	<b>Description</b>
VDDA	22	Power	<b>V<sub>DDA</sub></b> Analog supply voltage.
GNDA	24	Power	<b>Analog ground</b> All signals are referenced to this pin.
TIP	4	I	<b>Tip</b> Tip AC+DC input.
TIP_AC	5	I	<b>Tip AC</b> Tip AC input.
RING	6	I	<b>Ring</b> Ring AC+DC input.
RING_AC	7	I	<b>Ring</b> Ring AC input.
T1G	23	O	<b>Transistor 1 Gate</b> Gate for external transistor T1 (AC/DC control).
T2G	19	O	<b>Transistor 2 Gate</b> Gate for external transistor T2 (V <sub>DDA</sub> control).
VDDA_SENS	21	I	<b>Supply Voltage Sense</b> V <sub>DDA</sub> sense input.
VREF	3	I/O	<b>Reference Voltage</b> Must connect to GNDA via an external capacitor.
CAP1	1	I/O	<b>Capacitance 1</b> Must connect to pin CAP2 via an external capacitor for DC filtering.
CAP2	2	I/O	<b>Capacitance 2</b> Must connect to pin CAP1 via an external capacitor for DC filtering.
GPI_0_A	18	I	<b>General Purpose Input 0</b> Auxiliary input pin 0. Tied to GNDA or VDDA if not in use.
GPI_1_A	17	I	<b>General Purpose Input 1</b> Auxiliary input pin 1. Tied to GNDA or VDDA if not in use.
GPO_0_A	8	O	<b>General Purpose Output 0</b> Auxiliary output pin 0. Disconnected if not in use.



**Table 2-1 ALIS-A Pin Definitions (cont'd)**

<b>Symbol</b>	<b>Pin</b>	<b>Type</b>	<b>Description</b>
GPO_1Q_A	9	O	<b>General Purpose Output 1</b> Auxiliary output pin 1. Disconnected if not in use.
TEST	16	I	<b>Test</b> Must connect to GNDA.
A21	13	I	<b>Digital Isolation Interface</b> to ALIS-D: Must be connected to pin A11 of ALIS-D (see <b>Chapter 3.3.5</b> )
A22	12	I	<b>Digital Isolation Interface</b> to ALIS-D: Must be connected to pin A12 of ALIS-D (see <b>Chapter 3.3.5</b> )
B21	11	O	<b>Digital Isolation Interface</b> to ALIS-D: Must be connected to pin B11 of ALIS-D (see <b>Chapter 3.3.5</b> )
B22	10	O	<b>Digital Isolation Interface</b> to ALIS-D: Must be connected to pin B12 of ALIS-D (see <b>Chapter 3.3.5</b> )
C21	15	I	<b>Digital Isolation Interface</b> to ALIS-D: Must be connected to pin C11 of ALIS-D (see <b>Chapter 3.3.5</b> )
C22	14	I	<b>Digital Isolation Interface</b> to ALIS-D: Must be connected to pin C12 of ALIS-D (see <b>Chapter 3.3.5</b> )
NC	20	n/a	<b>Not Connected</b> Reserved.

## 2.3 Pin Definitions of ALIS-D (PSB 4596)

Table 2-2 ALIS-D Pin Definitions

Symbol	Pin	Type	Description
VDD	25	Power	$V_{DD}$ Digital supply voltage. Power supply for the digital circuitry: + 3.3 $V_{DC}$ .
GND	24	Power	<b>Digital Ground</b> All signals are referenced to this pin.
MCLK1	20	I	<b>Master Clock 1</b> Either connected to one pin of an external crystal or driven by an external clock.
MCLK2	21	O	<b>Master Clock 2</b> When MCLK1 is connected to an external clock, MCLK2 is left open; when MCLK1 is connected to an external crystal, MCLK2 is connected to the second pin.
$\overline{\text{RESET}}$	23	I	<b>Reset Input</b> Resets the device; active low signal.
FSC	15	I/O	<b>Frame Synchronization Clock</b> <b>As input:</b> indicates beginning of the frame. FSC must be synchronous with SDI_CLK (Slave Mode). <b>As output:</b> indicates beginning of a new frame (Master Mode).
SDI_TX	17	I	<b>SDI Transmit (from Host)</b> Serial Data Interface (SDI): Transmit data input from Host. <b>Non-multiplex Mode:</b> 16-bit modem data only. <b>Multiplex Mode:</b> 16-bit modem data plus 16-bit control data for every FSC frame.
SDI_RX	16	O	<b>SDI Receive (to Host)</b> Serial Data Interface (SDI): Receive data output to Host; tristate if not active (switchable pull-up). <b>Non-multiplex Mode:</b> 16-bit modem data only. <b>Multiplex Mode:</b> 16-bit modem data plus 16-bit control data for every FSC frame.
SDI_CLK	18	I/O	<b>SDI Clock</b> Serial Data Interface (SDI): Clock for serial data transfer.

Table 2-2 ALIS-D Pin Definitions (cont'd)

Symbol	Pin	Type	Description
FSC2	19	O	<b>Frame Synchronization Clock 2</b> Second FSC to synchronize slave devices. The signal has duration of one SDI_CLK period.
$\overline{\text{INT}}$	14	O	<b>Interrupt</b> Interrupt output pin; open drain, active low signal. Internal 33 k $\Omega$ pull-up resistor.
BM	7	I	<b>Bus Master</b> Determines Master or Slave Mode of the Serial Data Interface. To set Master Mode: at rising edge of $\overline{\text{RESET}}$ signal, set to high and hold. To set Slave Mode: at rising edge of $\overline{\text{RESET}}$ signal, set to low and hold.
SLEEP	6	O	<b>Sleep</b> Indicates that ALIS-D is in the Sleep state.
SCI_CLK/ MODE	11	I	<b>SCI Clock</b> Serial Control Interface: Clock for control communications in <b>Non-multiplex Mode</b> . Also <b>Mode set</b> . To set Multiplex (Non-multiplex) Mode: at rising edge of $\overline{\text{RESET}}$ signal, set to high (low) and hold for at least 10 MCLK cycles.
$\overline{\text{SCI\_CS}}$ / SWAP	10	I	<b>Chip Select/Swap</b> <b>Non-multiplex Mode:</b> SCI: Chip select, active low signal. <b>Multiplex Mode:</b> set during Reset and at rising edge of FSC, determines order of SDI and SCI bits for next FSC frame. Low: first 16 bits for SDI, next 16 bits for SCI; high: reversed.
SCI_IN	13	I	<b>SCI Incoming</b> <b>Non-multiplex Mode:</b> Serial Control Interface (SCI): control information from Host. <b>Multiplex Mode:</b> not used. Tie to high or low if not in use.
SCI_OUT	12	O	<b>SCI Outgoing</b> <b>Non-multiplex Mode:</b> Serial Control Interface (SCI): control information to Host. <b>Multiplex Mode:</b> not used, leave open.

**Table 2-2 ALIS-D Pin Definitions (cont'd)**

<b>Symbol</b>	<b>Pin</b>	<b>Type</b>	<b>Description</b>
CID_T	4	I	<b>CID Tip input</b> Tip input for Caller-ID comparator: must be connected to tip through a capacitor.
CID_R	5	I	<b>CID Ring input</b> Ring input for Caller-ID comparator: must be connected to ring through a capacitor.
BUZZER	9	O	<b>Buzzer</b> Output for line monitoring function: enabled by software setting.
A11	28	O	<b>Digital Isolation Interface</b> to ALIS-A: Must be connected to pin A21 of ALIS-A (see <b>Chapter 3.3.5</b> )
A12	1	O	<b>Digital Isolation Interface</b> to ALIS-A: Must be connected to pin A22 of ALIS-A (see <b>Chapter 3.3.5</b> )
B11	2	I	<b>Digital Isolation Interface</b> to ALIS-A: Must be connected to pin B21 of ALIS-A (see <b>Chapter 3.3.5</b> )
B12	3	I	<b>Digital Isolation Interface</b> to ALIS-A: Must be connected to pin B22 of ALIS-A (see <b>Chapter 3.3.5</b> )
C11	26	O	<b>Digital Isolation Interface</b> to ALIS-A: Must be connected to pin C21 of ALIS-A (see <b>Chapter 3.3.5</b> )
C12	27	O	<b>Digital Isolation Interface</b> to ALIS-A: Must be connected to pin C22 of ALIS-A (see <b>Chapter 3.3.5</b> )
GPO_D	22	O	<b>General Purpose Output</b> Can be used, for example, for hook switch control. Disconnect if not in use.
GPIO_D	8	I/O	<b>General Purpose Input/Output</b> Default: Input. Tie to high or low if not in use.

### 3 Functional Description

The ALIS chipset provides all the major parts of a conventional front-end for modem solutions. This section describes that functionality. Since adaptability to different countries' line characteristics is a particular feature of the ALIS chipset, this section also describes how that adaptation is implemented in a **Digital Filter Structure (DFS)**.

#### 3.1 Functional Overview

The ALIS provides a codec and an electronic Data Access Arrangement (DAA). Advanced features such as ring detection, DTMF and pulse dialing, and Caller-ID are integrated on-chip. Operating states such as Idle and Sleep are implemented to minimize power consumption.

#### 3.2 Block Diagram

Received modem data passes from the Tip/Ring of the telephone interface to the analog front-end ALIS-A, where it is digitized and passed through an digital isolation interface to the ALIS-D. The data proceeds through a sequence of hardware and digital filters and then to the Serial Data Interface (SDI) to the data pump.

Transmitted modem data traverses this path in the reverse direction.

Caller-ID data are also provided by the Tip/Ring, but received at the ALIS-D, in the Caller-ID Functions block. The signal is converted to a 1-bit data stream, passed to the Hardware Filter block for down-sampling, and further passed to the DFS for bandpass filtering and Hilbert transforms, in order to decode it. It is stored in the CID-RAM.

Ring detection is performed in the DFS, based on the analog signal received at the ALIS-A and passed through the ADC and Hardware Filters. This signal is filtered, integrated and compared to a threshold to determine if a potential ring is valid.

Control information from the Host is provided to the ALIS-D through the Serial Control Interface (SCI). This includes both operational commands and programming commands.

General purpose control is provided for both the ALIS-A and ALIS-D. The ALIS-D also provides the SLEEP output signal to indicate that it is in Sleep state, and the BUZZER output signal for line monitoring.

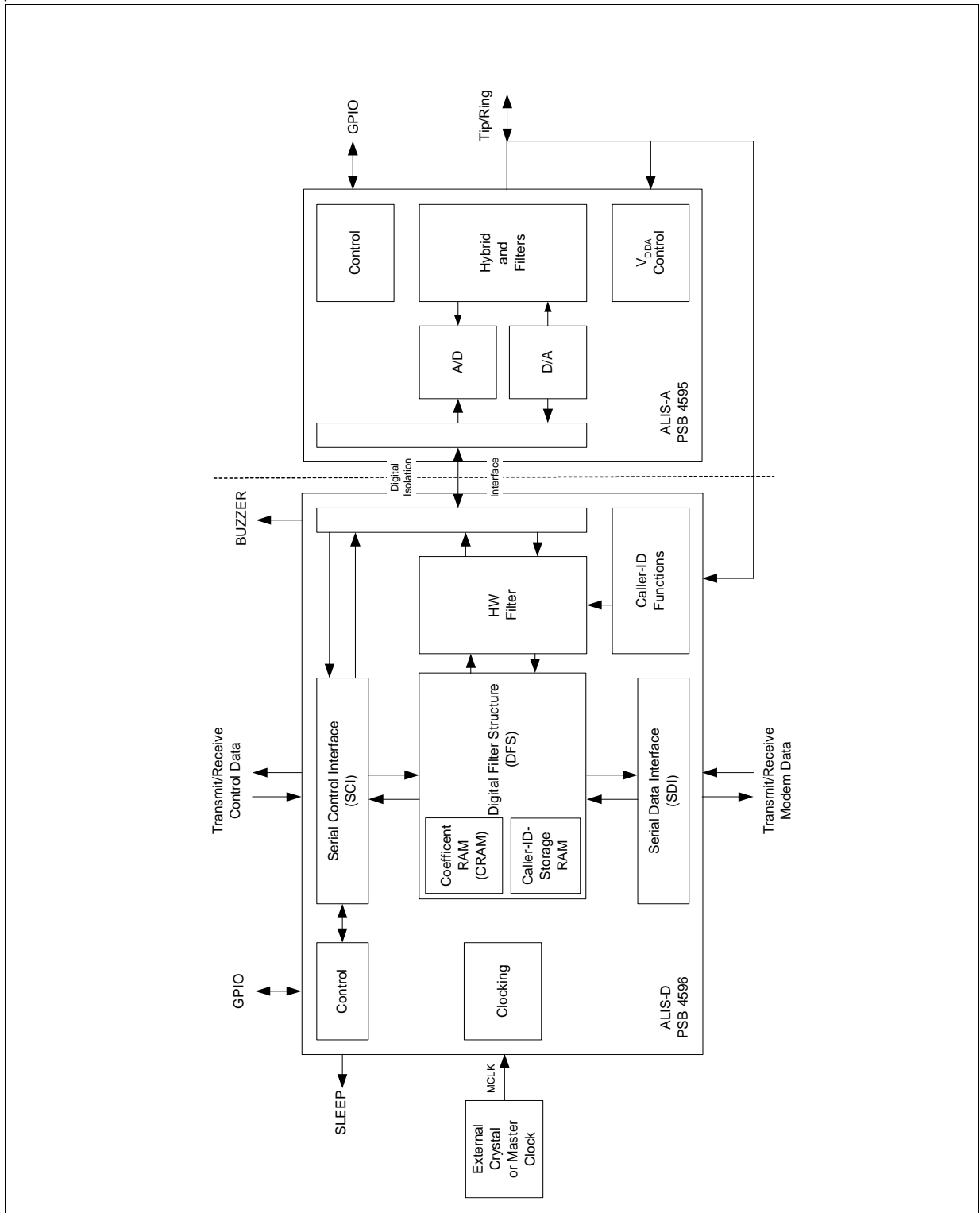


Figure 3-1 ALIS Block Diagram

### 3.3 Functional Blocks

#### 3.3.1 Control: ALIS-A

Provides general purpose input/output. This employs pins GPI\_0\_A, GPI\_1\_A, GPO\_0\_A, and GPO\_1Q\_A.

#### 3.3.2 $V_{DDA}$ Control

Generates the supply voltage for the ALIS-A from the Tip/Ring voltage.

#### 3.3.3 Hybrid Circuit and Filters

The hybrid circuit provides two-wire to four-wire conversion, while analog anti-aliasing pre-filters and smoothing post-filters condition the modem data.

#### 3.3.4 Analog/Digital Conversion

Analog-to-Digital Conversion (ADC) for received data and Digital-to-Analog Conversion (DAC) for transmitted data are provided by high-performance oversampling. This delta-sigma technique converts the analog signal to a digital one-bit data stream.

#### 3.3.5 Digital Isolation Interface

The digital isolation interface is further described in **Chapter 5.1.5**.

#### 3.3.6 Caller-ID Functions

The FSK Caller-ID signal is converted to a 1-bit data stream to reduce power consumption, and then passed to the Hardware Filter block. The Caller-ID interface is further described in **Chapter 5.1.4**.

#### 3.3.7 Hardware Filters

The hardware filters provide interpolation and decimation functions for both modem data and Caller-ID data.

#### 3.3.8 Digital Filter Structure

The Digital Filter Structure (DFS) implements the functions of line impedance matching, bandpass filtering, Hilbert transforms, channel equalization, sampling, ring detection, and Caller-ID storage through Digital Signal Processing (DSP) algorithms. The specific performance of the DFS is matched to a particular country's line characteristics by the values of parameters and coefficients stored in the Coefficient RAM (CRAM) on-chip.

### 3.3.9 Serial Control Interface

The SCI is further described in **Chapter 5.1.1.1**.

### 3.3.10 Serial Data Interface

The SDI is further described in **Chapter 5.1.1.2**.

### 3.3.11 Control: ALIS-D

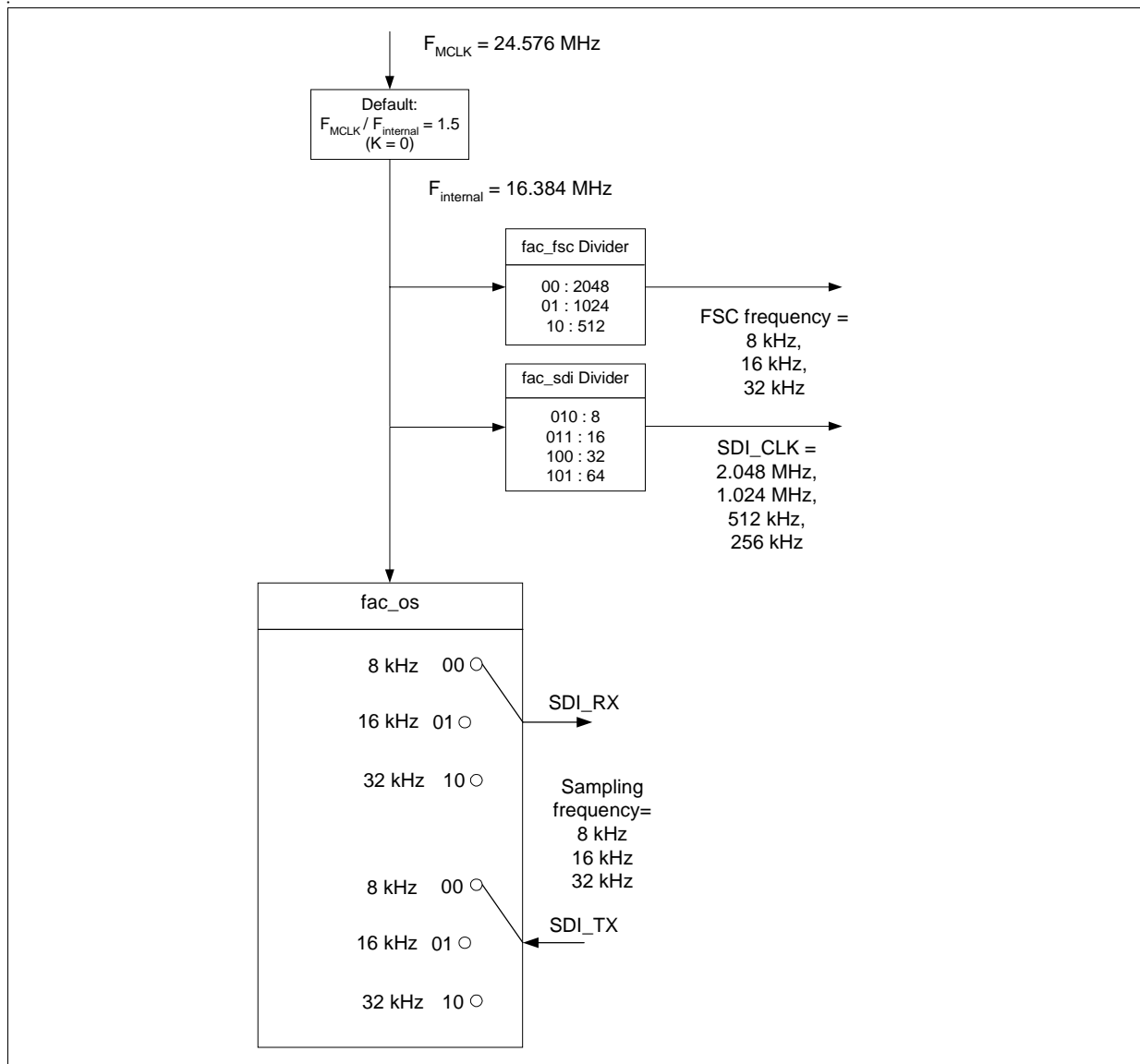
Provides general purpose input/output. This employs pins GPO\_D and GPIO\_D.

### 3.3.12 BUZZER

The output to BUZZER is the one bit digital data stream received from the ALIS-A over the digital isolation interface.



### 3.3.13 Clocking



**Figure 3-2 Clocking of the ALIS in Master Mode**

All operating frequencies of the ALIS are derived from an external source MCLK, an external crystal or master clock. To allow flexibility in selection of external frequency, while enforcing strict integer ratios among the operating frequencies, an internal clock is derived as an adjustable reduction from the external source; and all other rates are derived through reduction of the internal clock by powers of 2.

**Figure 3-2** shows the relationship among these frequencies in Master Mode (see **Chapter 3.4.2**), as well as the options. Four programmable parameters are available: the internal clock parameter  $K$ , the framesync reduction parameter  $fac\_fsc$ , the data clock reduction parameter  $fac\_sdi$ , and the oversampling parameter  $fac\_os$ .

Functional Description

The internal clock frequency  $F_{\text{internal}}$  is reduced from the external clock frequency  $F_{\text{MCLK}}$  by a factor which depends on the parameter K according to the equation:

$$F_{\text{internal}} = \frac{F_{\text{MCLK}}}{1 + \left(\frac{(32768 + K)}{2 \times 32768}\right)} \quad \text{or} \quad K = 65536 \times \left(\frac{F_{\text{MCLK}}}{F_{\text{internal}}} - 1\right) - 32768$$

K is an integer value in the range from -32768 to 32767. The sampling rate for the analog data is obtained by dividing the internal clock frequency by 512, 1024, or 2048.

In Master Mode, the framesync frequency is obtained by dividing the internal clock frequency by 512, 1024, or 2048; and the data clock (SDI\_CLK) frequency is obtained by dividing the internal clock frequency by 8, 16, 32 or 64. In the figure, the reduction factors are exact, but the specific frequencies depend on K and the source frequency.

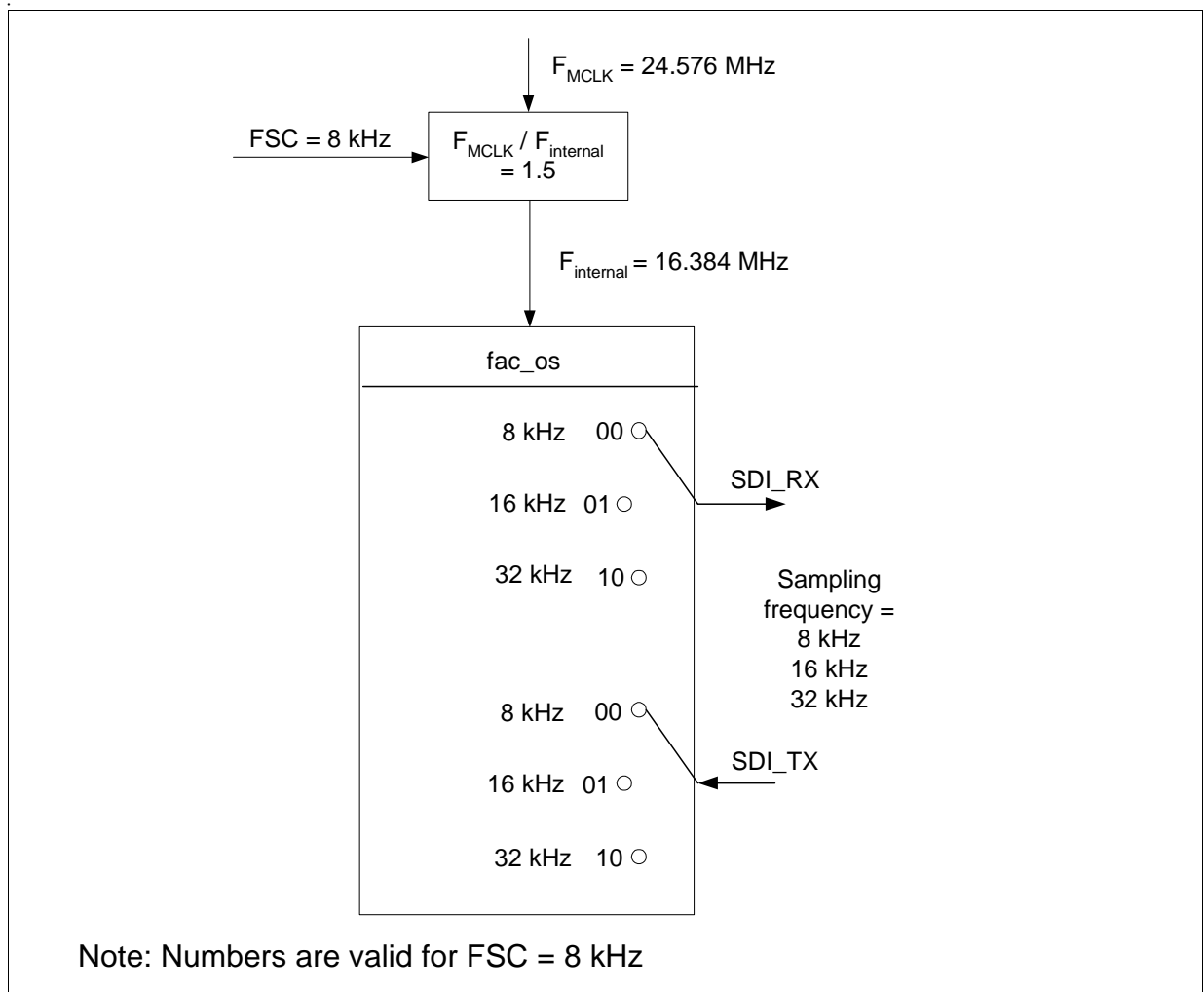


Figure 3-3 Clocking of the ALIS in Slave Mode

In the Slave Mode, the ALIS receives both SDI\_CLK and the framesync frequency from an external device. The internal clock is still controlled by the external source (MCLK) and the K parameter, but in this case the value of K is set by a phase-locked loop synchronized to the externally generated framesync. Other frequencies are still driven by the internal clock. See **Figure 3-3**.

In either Mode, the framesync frequency and the sampling frequency have the same range: if they are set equal, each frame will have one sample. If the sampling frequency exceeds the framesync frequency, multiple samples will be included in each frame. It is important to select fac\_fsc and fac\_os so that the framesync frequency does not exceed the sampling frequency.

Comparison of the framesync and data clock rates shows that the number of SDI\_CLK cycles per frame is the ratio of the division factor determined by fac\_fsc to the division factor determined by fac\_sdi: this is always a multiple of 32. When cascading multiple devices (see **Chapter 5.1.1.5** and **Chapter 5.1.1.7**), the fac\_fsc and fac\_sdi parameters must be set appropriately.

### 3.4 Operating Modes

There are four distinct ways in which the ALIS-D Host interface can be configured. They are characterized by selection of the mode of the Host interface, and by the independent selection of the source of clocking and frame synchronization.

#### 3.4.1 Multiplex and Non-Multiplex Modes

The Host interface can be provided by two different modes. In the Multiplex Mode, the SCI and the SDI are provided over a single set of pins; in the Non-multiplex Mode, the SCI and SDI are provided over separate sets of pins.

#### 3.4.2 Master and Slave Modes

The ALIS-D can operate in two different modes. In the Master Mode, clocking and frame synchronization are generated by the ALIS-D; in the Slave Mode, they are provided by the Host. This has been discussed in **Chapter 3.3.13**.

## 4 Operational Description

### 4.1 Operational Overview

The ALIS is initiated by a Reset, after which it undergoes programming by the Host to determine its configuration.

The ALIS chipset can be set to implement the following features:

- Auto Sleep: The chipset will transition automatically from Idle state to Sleep state after a programmable timeout (see register R4).
- Non-Automatic Call Processing: If Automatic Call Processing is not activated, the chipset will transition from one state to another only under the direct command of the Host.
- Automatic Call Processing: the ALIS will respond to incoming ringing on the Tip/Ring by transitioning among the operating states defined in **Chapter 4.2**. Within the Automatic Call Processing feature, it is possible to set the Caller-ID feature, which will allow automatic storage of the Caller-ID signal; and to instruct the ALIS to issue an interrupt at a programmable number of rings.

### 4.2 Operating States

The following chapter describes the different operating states controlled by STATE register R3.

#### 4.2.1 Idle State

In Idle state, the SCI function is active (Multiplex Mode and None-Multiplex Mode). The Host can read the Caller-ID storage RAM to capture the Caller-ID information, and access the CRAM to program the ALIS-D by loading or reading coefficients. In Idle state, modem data for transmit from the data pump are ignored.

#### 4.2.2 Ringing State

In the Ringing state, the ALIS-D chip is prepared to detect a valid ring. A ringing burst is determined to be valid if it matches the frequency and level appropriate to the country for which the ALIS-D is set.

#### 4.2.3 Caller-ID State

In the Caller-ID state, incoming Caller-ID information will be stored in the Caller-ID storage RAM.

#### 4.2.4 Conversation State

In Conversation state, the SDI is active. The ALIS chipset can receive and transmit modem data, and the tone generators are available. The ALIS synthesizes the DC and AC characteristics of the DAA only in this state.

#### 4.2.5 Pulse Dialing State

In Pulse Dialing state, the Host can perform pulse dialing by switching the bit pdial in register R11.

#### 4.2.6 Sleep State

In Sleep state, power consumption by the ALIS is minimized. All internal clocks are turned off. If the ALIS-D uses an external crystal for the master clock, it is also turned off. If instead, it is receiving an external master clock, this can now be turned off safely. The SLEEP pin indicates high in this state.

The ALIS-D can be awakened from the Sleep state by toggling on the SDI\_TX; or when ringing on the Tip/Ring stimulates the ALIS-A: the external master clock (if present) must be turned on; and the SLEEP pin transits to low. The internal clock is switched on automatically. Alternatively, it can also be Reset using the  $\overline{\text{RESET}}$  pin, as described in Chapter 5.3.

### 4.3 Operational Performance

Telephone line characteristics differ from country to country. However, the table below summarizes what the ALIS can do, as a DAA, in any one country, when loaded with the appropriate set of parameters and coefficients. These coefficient sets are available from Infineon Technologies.

**Table 4-1 DAA Performance Parameters**

Parameter	Symbol	Test Condition	Limit Values			Unit
			min.	typ.	max.	
Frequency Response, Transmit: Low -3 dB corner	$F_{RT}$	High-Pass Filter On			40	Hz
Frequency Response, Transmit: Low -3 dB corner	$F_{RT}$	High-Pass Filter Off			15	Hz
Frequency Response, Transmit: 300 - 3000 Hz	$F_{RT}$		-0.125		0.125	dB
Frequency Response, Transmit: 3400 Hz	$F_{RT}$		0	0.125	0.650	dB

**Operational Description**

**Table 4-1 DAA Performance Parameters (cont'd)**

Parameter	Symbol	Test Condition	Limit Values			Unit
			min.	typ.	max.	
Transmit Full Scale Level: 0 dB gain	$V_{TX}$	between Tip and Ring		3		dBm
Frequency Response, Receive: Low -3 dB corner	$F_{RR}$	High-Pass Filter On			160	Hz
Frequency Response, Receive: Low -3 dB corner	$F_{RR}$	High-Pass Filter Off			28	Hz
Frequency Response, Receive: 300 to 3000 Hz	$F_{RR}$		-0.125		0.125	dB
Frequency Response, Receive: 3400 Hz	$F_{RR}$		0	0.125	0.650	dB
Receive Full Scale Level: 0 dB gain	$V_{RX}$	between Tip and Ring		0		dBm
Total Harmonic Distortion plus Noise: C-weighted	HDN	1 kHz, -10 dBm0	74	77		dB Full Scale
Total Harmonic Distortion plus Noise: linear-weighted	HDN	1 kHz, -10 dBm0	72	75		dBFS
Return Loss: 300 - 3400 Hz			16			dB
Transhybrid Loss: 300 to 3400 Hz	THL		27	35	-	dB
Group Delay, Receive	DRA				340	$\mu$ s
Group Delay, Transmit	DXA				400	$\mu$ s

Operational Description

Figure 4-1 shows the Group Delay Distortion, relative to  $T_{Gmin}$  at 1.5 kHz. This graph applies to the case that the high-pass filter is switched on. If it is off, the distortion will be less, but the exact behavior depends on external components.

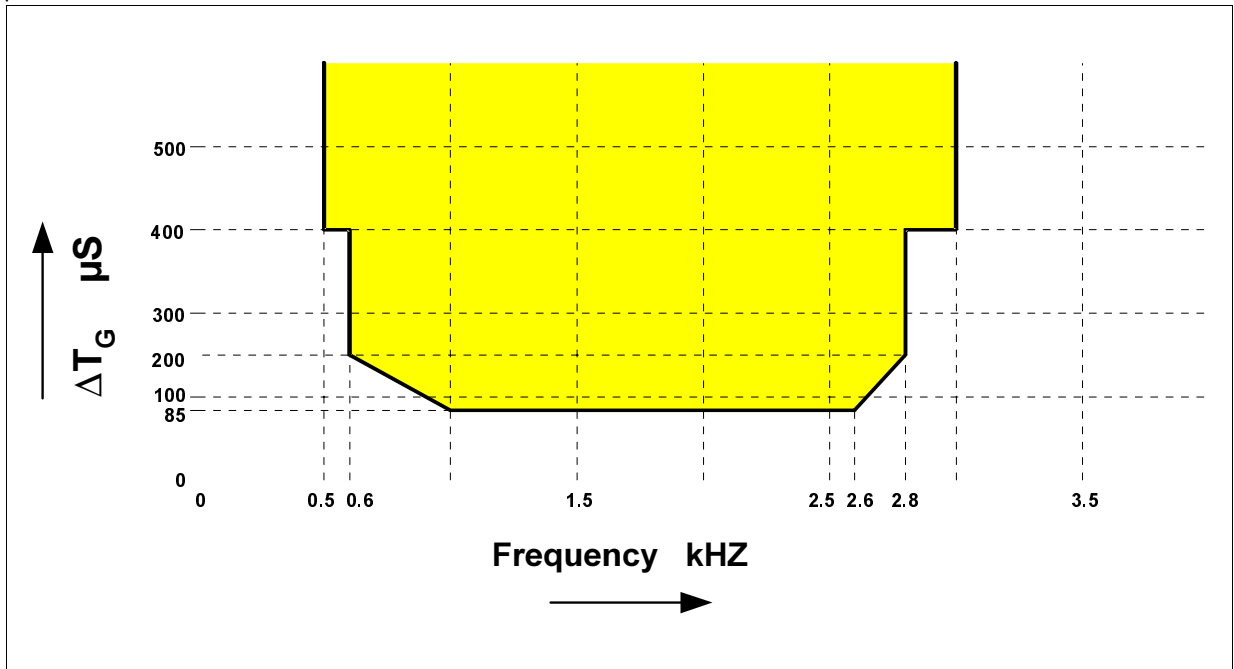


Figure 4-1 Group Delay Distortion, Transmit and Receive (High-Pass Filter On)

Figure 4-2 shows the suppression of the digital output of an out-of-band 0 dBm sine wave applied to the analog input, compared to the digital output of a reference in-band (1 kHz) 0 dBm sine wave.

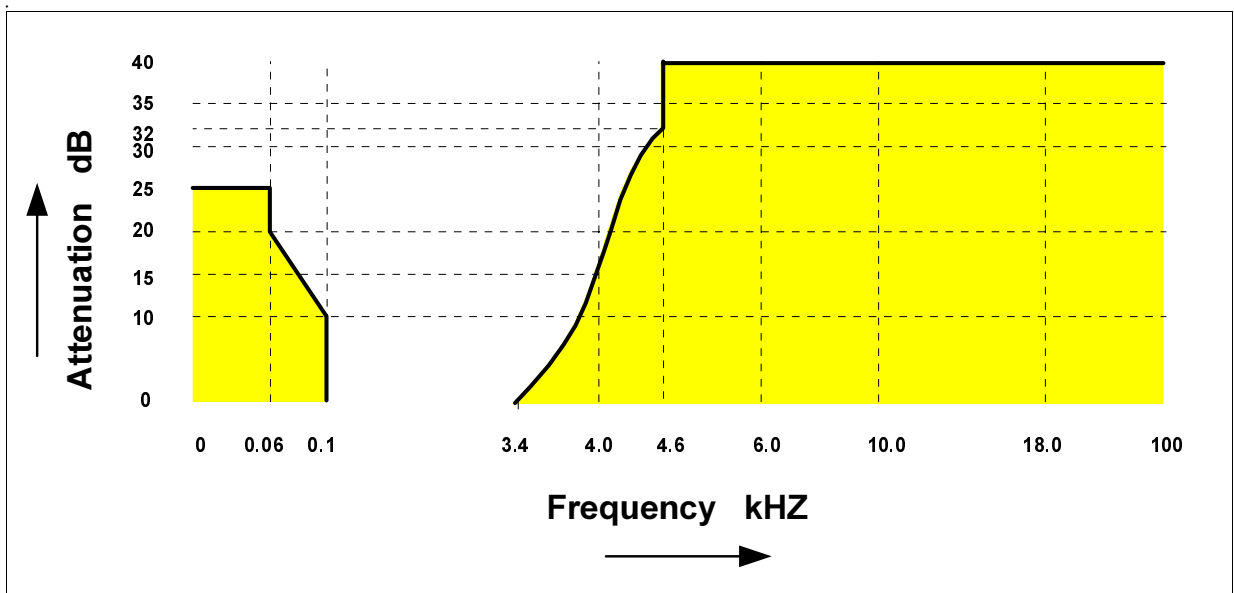
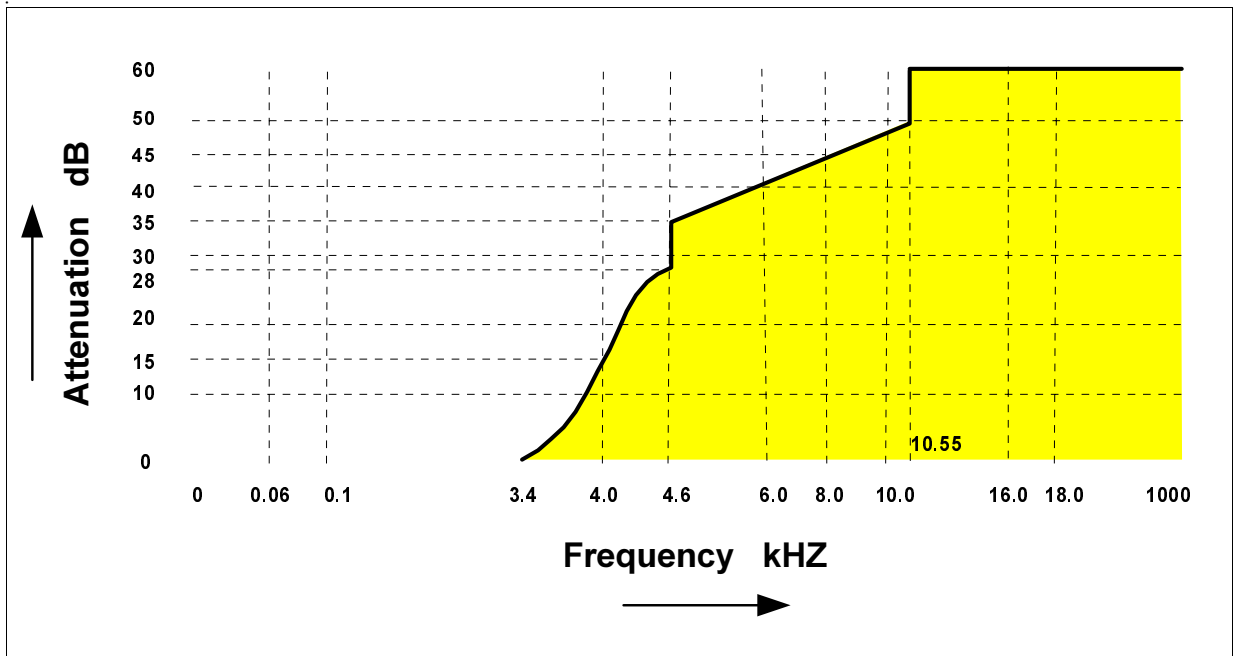


Figure 4-2 Out-of-Band Receive (High-Pass Filter On)



**Figure 4-3 Out-of-Band Transmit**

**Figure 4-3** shows the suppression of the out-of-band analog output of any in-band signal (300 - 3990 Hz), compared to the analog output of a reference in-band (1 kHz) 0 dBm0 sine wave.



## 5 Interface Description

The ALIS has interfaces for data and control from the Host, for access to the telephone network, and for incoming Caller-ID signals. In addition, the ALIS-D must be connected to an external clock or crystal.

### 5.1 Hardware Interface

#### 5.1.1 Host Interface: Control and Data

The Host interface has two principal components: the Serial Control Interface (SCI) and the Serial Data Interface (SDI). The Host uses the SCI to issue operational commands to the ALIS-D and to read from and write to its registers. ALIS-D is also programmed with this interface. The SDI transports modem data between the Host and the ALIS-D.

The SCI and the SDI can use separate pins of the ALIS-D, or they can share pins, using different time slots. We denote the first case as the Non-multiplex Mode of the Host Interface, and the second as the Multiplex Mode.

In this section, we describe the functions and signals of the SCI and SDI, and how they are mapped to the physical pin symbols of the ALIS-D in both Multiplex and Non-multiplex Modes. We also describe how multiple ALIS chipsets can be cascaded.

##### 5.1.1.1 Serial Control Interface

The SCI has the following signals:

**Table 5-1 Mapping of SCI Signals to ALIS-D Pin Symbols**

Serial Control Interface (SCI) Signal	Pin Symbol: Non-multiplex Mode	Pin Symbol: Multiplex Mode
Interrupt: to Host (active low).	$\overline{\text{INT}}$	$\overline{\text{INT}}$
Clocking	SCI_CLK	SDI_CLK
8-bit Commands, 8-bit Write contents: from Host.	SCI_IN	SDI_TX
8-bit Read contents: to Host.	SCI_OUT	SDI_RX
Interface Synchronisation	$\overline{\text{SCI\_CS}}/\text{SWAP}$	FSC

Write bits from the Host are latched on the falling edge of the Clocking, Read bits to the Host are changed on the rising edge of the SCI\_CLK.

### 5.1.1.2 Serial Data Interface

The SDI has the following signals:

**Table 5-2 Mapping of SDI Signals to ALIS-D Pin Symbols**

Serial Data Interface (SDI) Signal	Pin Symbol: Non-multiplex Mode	Pin Symbol: Multiplex Mode
Frame Synchronization	FSC	FSC
Data Clock for Modem	SDI_CLK	SDI_CLK
16-bit Transmit data: from data pump.	SDI_TX	SDI_TX
16-bit Receive data: to data pump.	SDI_RX	SDI_RX

The SDI is a synchronous interface: the FSC pulse identifies the beginning of a frame, Write bits from the Host are latched on the falling edge of the SDI\_CLK, and Read bits to the Host are changed on the rising edge of the SDI\_CLK.

### 5.1.1.3 Master/Slave Modes:

The ALIS-D can be operated either as a master or slave device, controlled by the BM pin.

**Table 5-3 Master/Slave Modes of ALIS-D: SDI Roles**

Symbol	ALIS-D as Master (BM = high)	ALIS-D as Slave (BM = low)
SDI_CLK	Data Clock is generated by ALIS-D.	Data Clock is generated by Host.
FSC	Frame Synchronization is generated by ALIS-D.	Frame Synchronization is generated by Host.

In Master Mode, the ALIS-D begins a data frame with the rising edge of the FSC, which coincides with a rising edge of SDI\_CLK. The next rising edge of SDI\_CLK indicates the start of the first bit for SDI\_RX (Receive data); at the first subsequent falling edge of SDI\_CLK, the first bit for SDI\_TX (Transmit data) is latched. When not active, the SDI\_RX pin is in tristate condition (internal switchable pull-up).

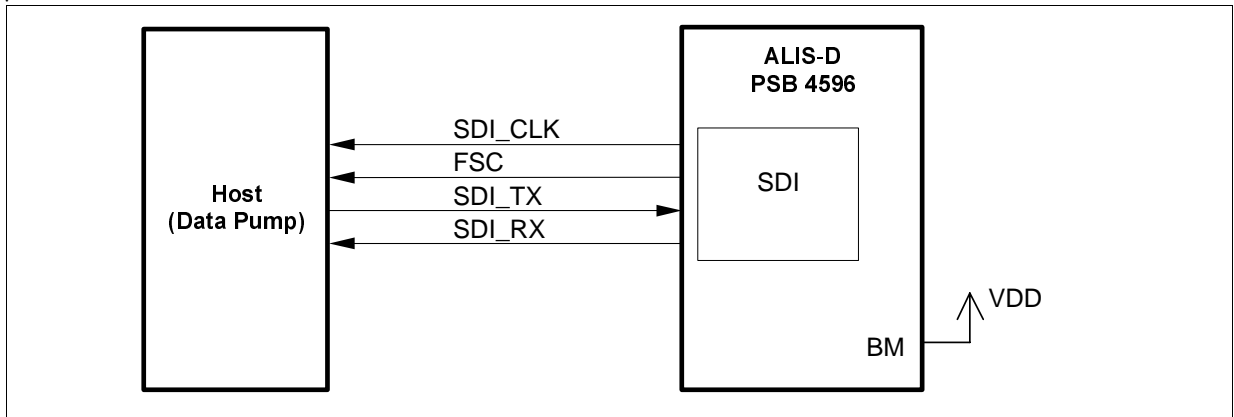


Figure 5-1 SDI in Master Mode

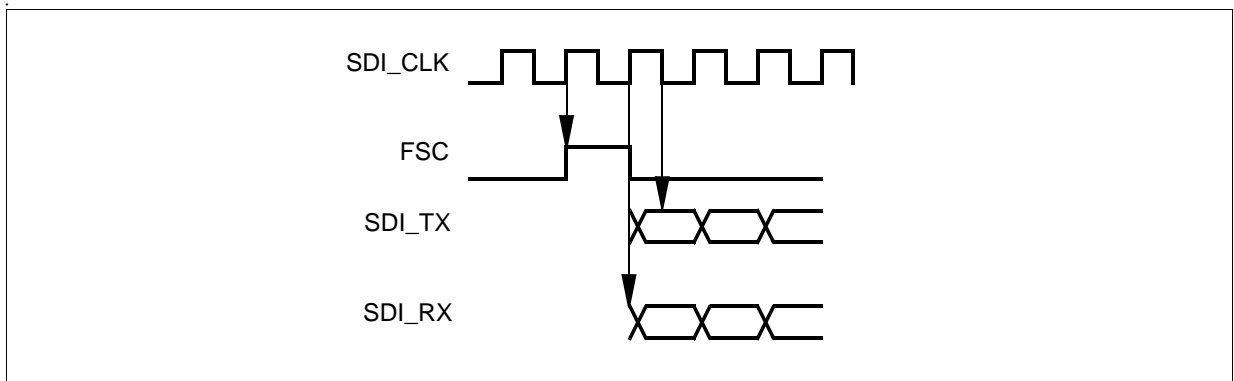


Figure 5-2 SDI Framing in Master Mode

In Slave Mode, it is required that the Host produce the Frame Synchronization synchronously with the Data Clock. The ALIS-D detects the start of a data frame when the FSC is high at the falling edge of SDI\_CLK. The next rising edge of SDI\_CLK indicates the start of the first bit for SDI\_RX (Receive data); at the first subsequent falling edge of SDI\_CLK, the first bit for SDI\_TX (Transmit data) is latched. When not activated, the SDI\_RX pin is in tristate condition (internal switchable pull-up).

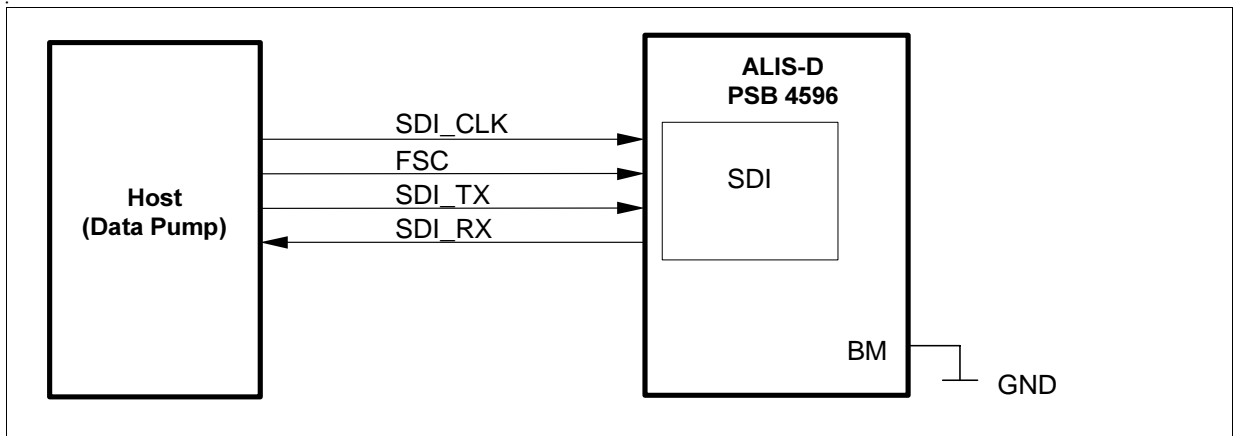


Figure 5-3 SDI in Slave Mode

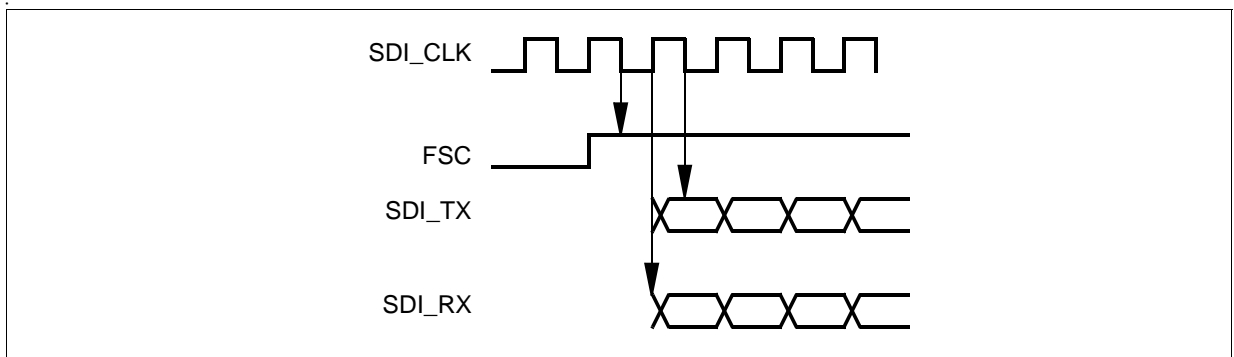


Figure 5-4 SDI Framing in Slave Mode

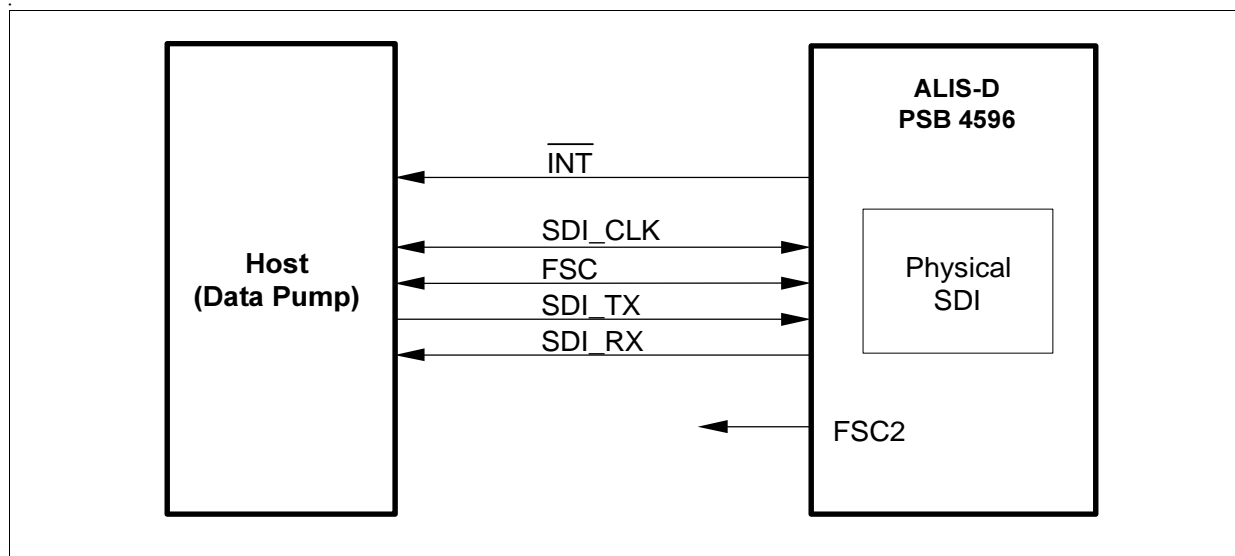
### 5.1.1.4 Multiplex Mode

The Host Interface is set in this mode when the SCI\_CLK/MODE pin of ALIS-D is set to high during Reset.

In Multiplex Mode, five pins are shared by the Serial Data Interface (SDI) and the Serial Control Interface (SCI). The interfaces have different time slots.

**Table 5-4 Multiplex Mode Pins**

Physical Pin Label	SDI Signal	SCI Signal
$\overline{\text{INT}}$	n/a	$\overline{\text{INT}}$
SDI_CLK	SDI_CLK	SCI_CLK
SDI_TX	SDI_TX	SCI_IN
SDI_RX	SDI_RX	SCI_OUT
FSC	FSC	n/a



**Figure 5-5 ALIS-D in Multiplex Mode**

The following figures show the time slots for the SCI and SDI bits. When the  $\overline{\text{SCI\_CS/SWAP}}$  pin is set to low, the SDI is assigned to the first 16 bits after the FSC, and the SCI is assigned to the next 16 bits. When active, the SDI receives and transmits modem data continually. By contrast, the SCI is used only when the Host needs it: during a Write command, the Host uses only the SCI\_IN signal for the command and the content of that command; but during a Read command, the SCI\_IN signal (on the SDI\_TX pin) is used to request the Read (of a register), and the SCI\_OUT signal (on the SDI\_RX pin) is used for the actual contents. If the SCI is not used it is recommended to send zeros in the command slot. **Figure 5-6** and **Figure 5-7** also show a second communication slot for a second device: this will be discussed in **Chapter 5.1.1.5**.

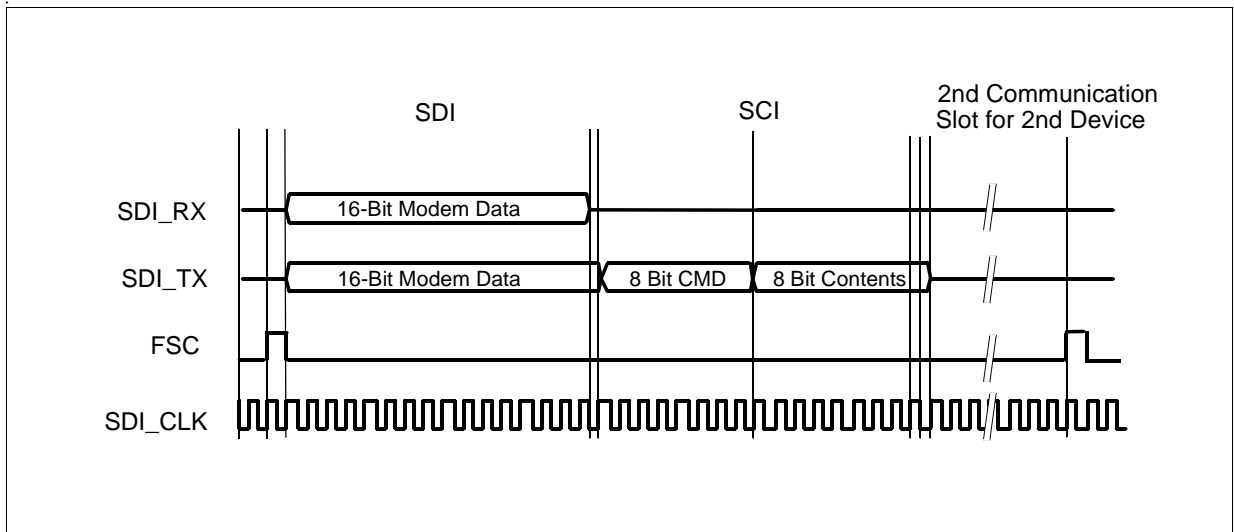


Figure 5-6 Multiplex Mode (SWAP = '0'): Write Access

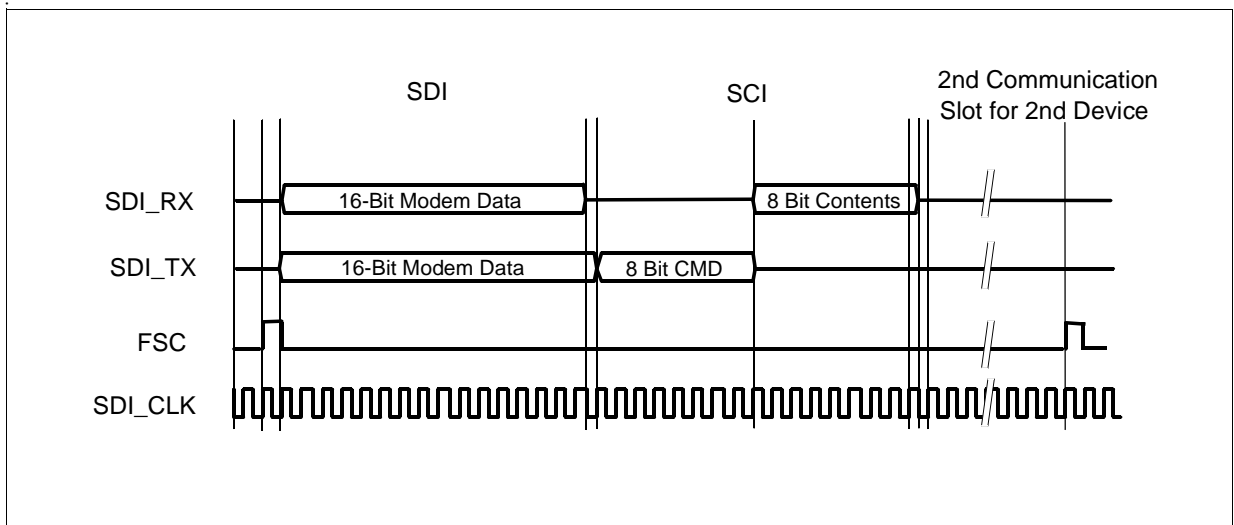
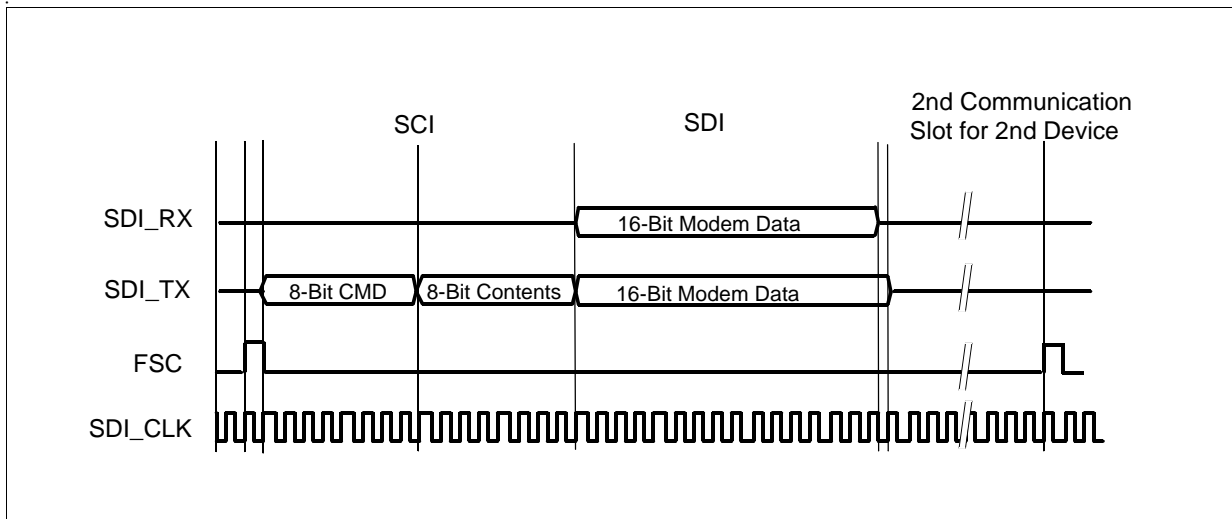


Figure 5-7 Multiplex Mode (SWAP = '0'): Read Access

When the SWAP pin is set to high, the ordering of the SCI and SDI is reversed: the first 16 bits after the FSC are for the SCI, and the next 16 bits are for the SDI (see **Figure 5-8**).



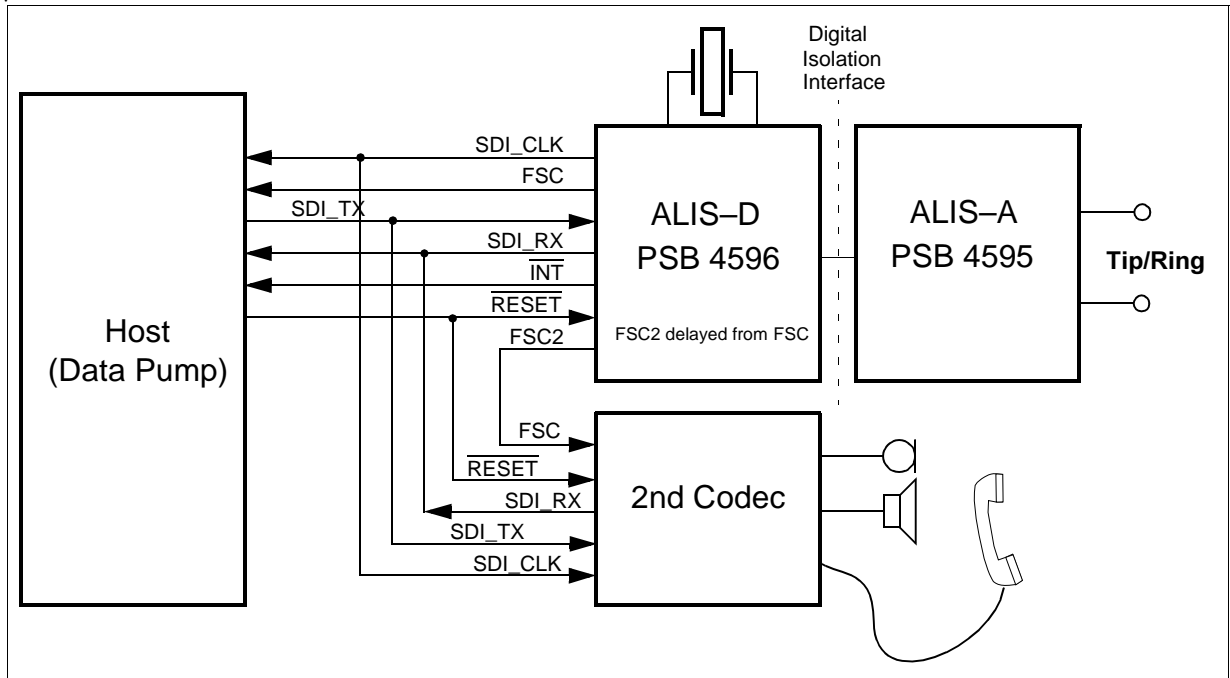
**Figure 5-8 Multiplex Mode (SWAP = '1'): Write Access**

Within the context of the Multiplex Mode, the ALIS-D still can operate as either a Master or a Slave device, as described in **Chapter 5.1.1.2**.

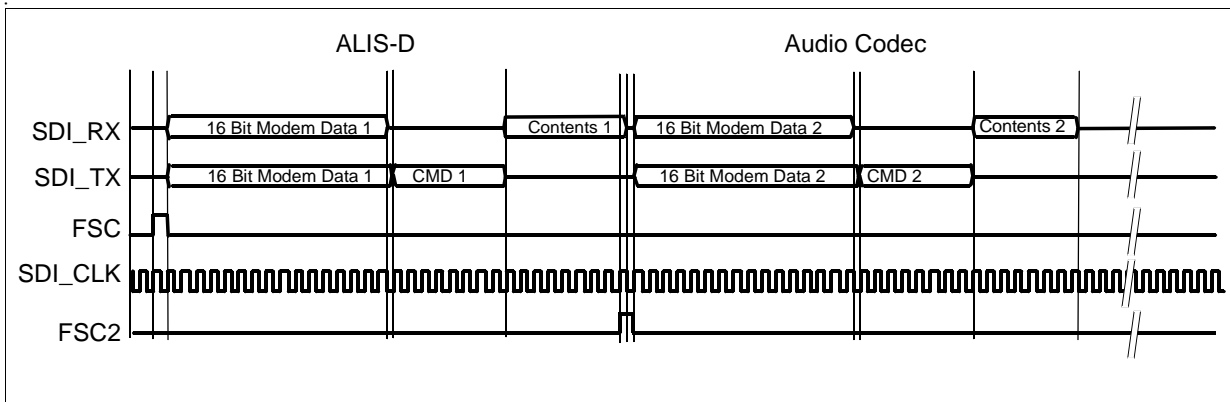
### 5.1.1.5 Multiplex Mode with Cascaded Devices

The ALIS-D in Multiplex Mode can support an additional device, e.g., a codec for a speakerphone application. This device must be configured to receive synchronization from the FSC2 of the ALIS-D. The ALIS-D may be in Master Mode or in Slave Mode.

As shown in **Figure 5-9**, the FSC input of the codec is connected to FSC2 output of the ALIS-D. The FSC2 signal is active high, one SDI\_CLK cycle in duration. The delay between the FSC of the ALIS-D and the FSC2 must be set by programming to allow the codec to use the second communication slot. It can be delayed from 0 to 63 cycles. This second slot is shown in more detail in **Figure 5-10**.



**Figure 5-9 ALIS-D in Multiplex/Master Mode with an Additional Codec**



**Figure 5-10 Framing for an Additional Codec: Read Access**

The role of the second device can also be performed by a second ALIS chipset, with the second ALIS-D in Multiplex/Slave Mode. This is shown in **Figure 5-11** and **Figure 5-12**. Note in **Figure 5-11** that the INT pins can share a common input to the Host, or have separate inputs.



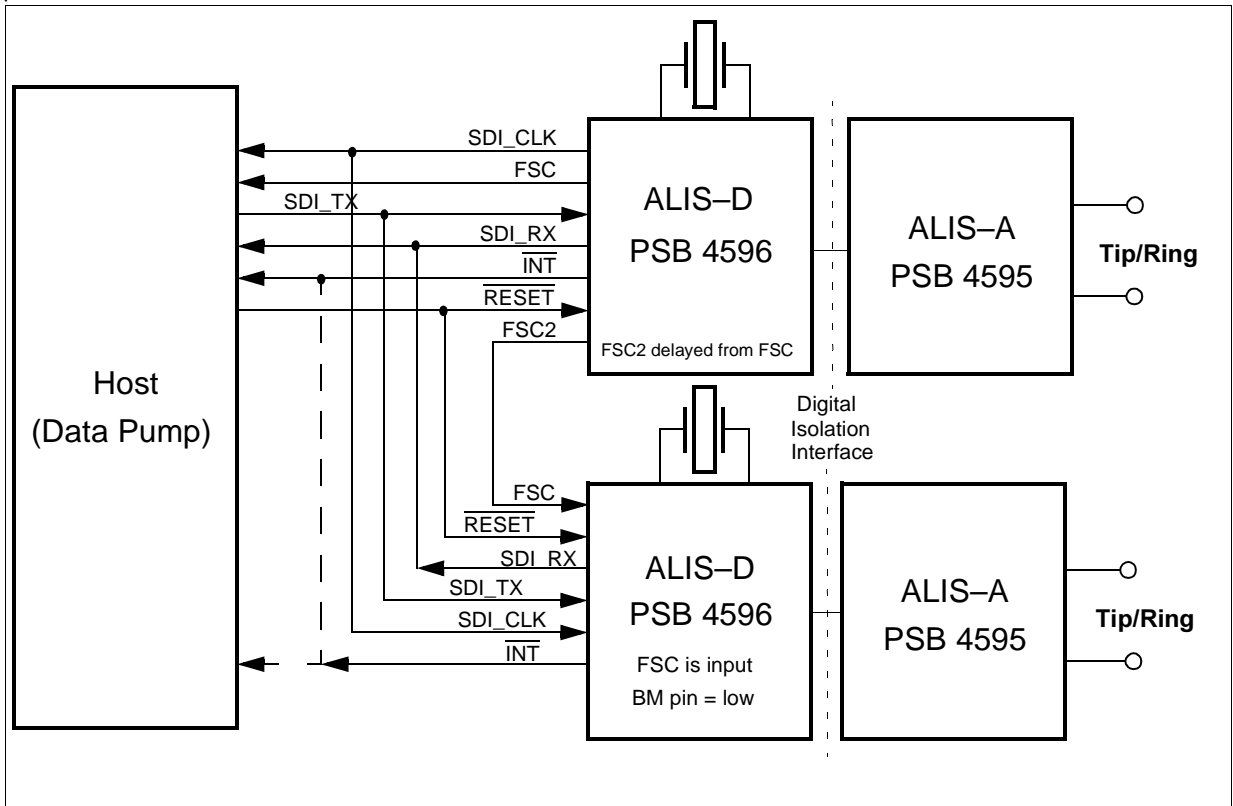


Figure 5-11 Dual-Line Modem: Two ALIS Chipsets

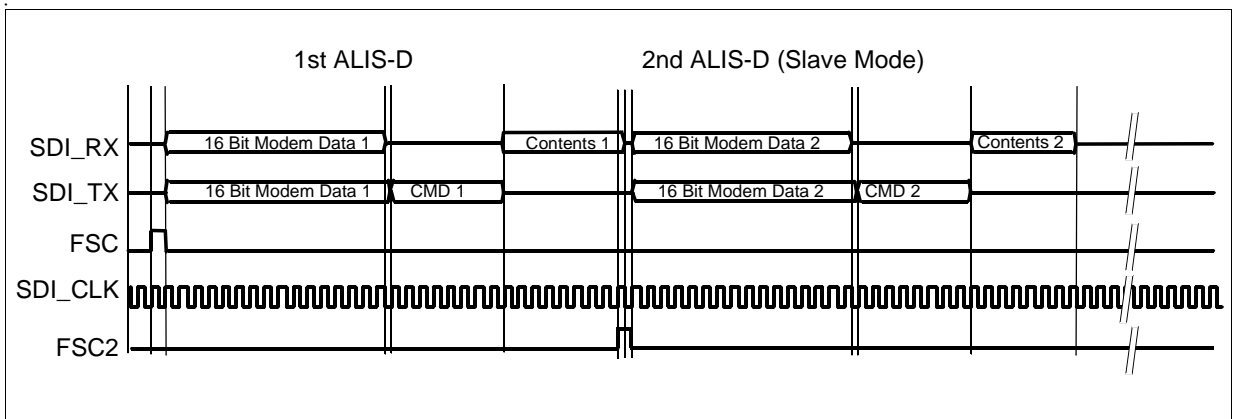


Figure 5-12 Framing for Two ALIS-D Chips: Read Access

It is possible to further cascade more ALIS-Ds “piggy-back”, within the limitation that each receives 32 bits per frame. This is controlled by properly selecting the sub-dividing parameters which determine the SDI clock-rate and the sampling (FSC) rate as shown in **Figure 3-2**.

### 5.1.1.6 Non-multiplex Mode

Figure 5-13 shows the physical layout of the Non-multiplex Mode. The SDI is shown as configured for the ALIS-D acting as a Master device (see Table 5-3).

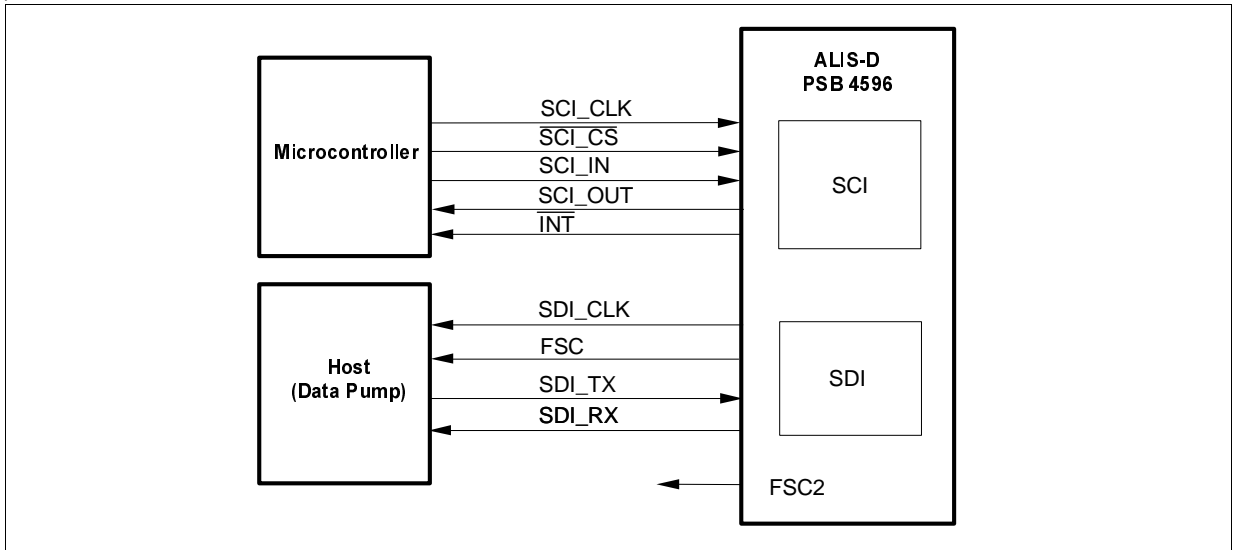


Figure 5-13 ALIS-D in Non-multiplex/Master Mode

In Non-multiplex Mode, the SCI\_CLK is not synchronous: this is illustrated in Figure 5-14 and Figure 5-15, which show the framing for reading and writing to the SCI in this mode.

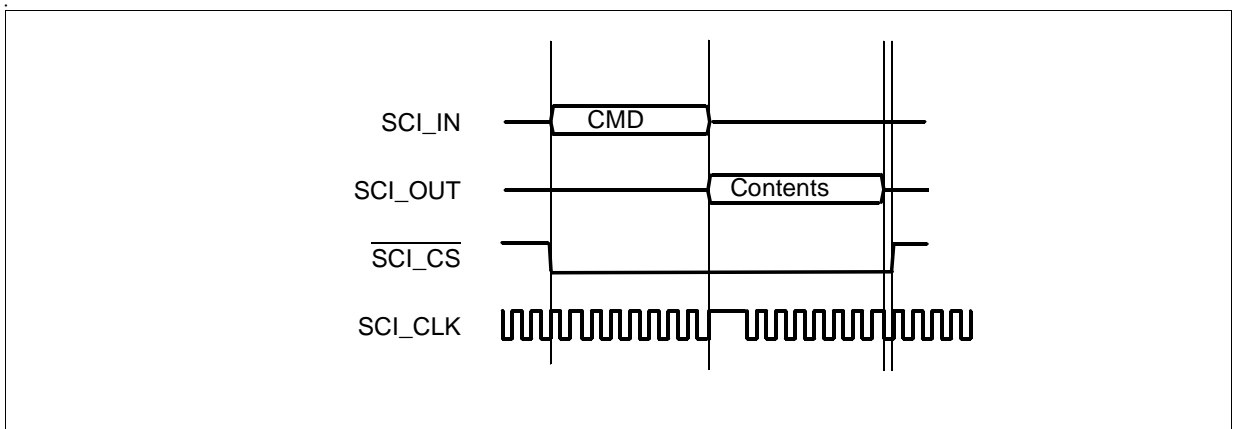
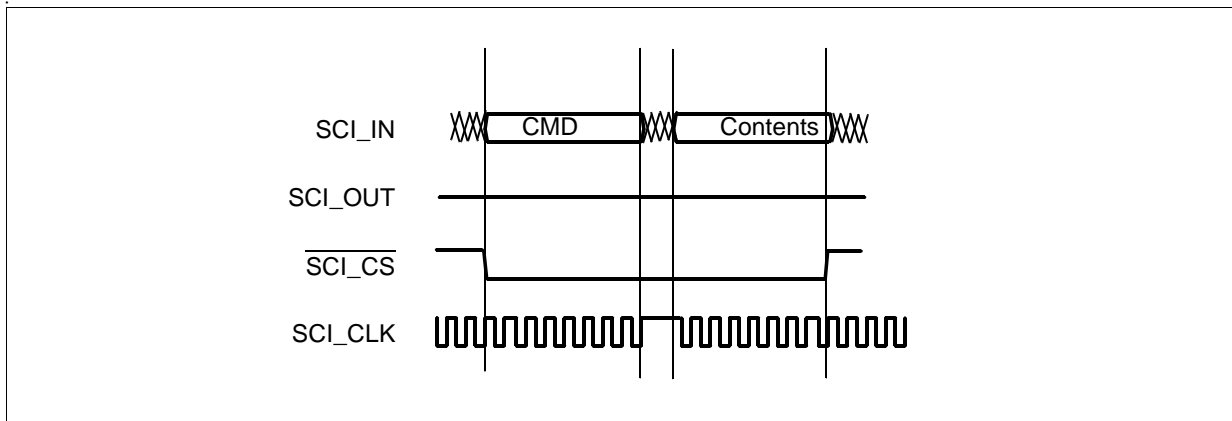


Figure 5-14 Framing for Read Access to SCI in Non-multiplex Mode

During execution of a Read command, the ALIS-D will not accept new commands on SCI\_IN. However, this can be interrupted by setting SCI\_CS high.

Because SCI\_OUT goes to high-impedance (tristate) during the last half-clock-cycle of a Read, it is possible to strap SCI\_OUT together with SCI\_IN to a bi-directional data pin on the Host, without causing bus contention. This can be used to reduce the number of pins to the microprocessor.



**Figure 5-15 Framing for Write Access to SCI in Non-multiplex Mode**

### 5.1.1.7 Multiple ALIS Chipsets in Non-multiplex Mode

In the Non-multiplex Mode, the SCI and the SDI are physically separate, so it is possible to cascade them separately.

**Figure 5-13** shows one ALIS-D interfaced to a Host; however, it would be possible for multiple ALIS-Ds to share all SCI lines except for the SCI\_CS. As long as each chipset has its own chip select pin on the Host, it can be addressed individually.

Similarly, several chipsets could share the SDI lines to the Data Pump. With a layout similar to **Figure 5-11** but in Non-multiplex Mode, and with all ALIS-Ds after the first in Slave Mode, each chipset can be given its own 16-bit time slot. This would look similar to **Figure 5-12**, except that there would be no SCI time slots, so each chipset needs only 16 bits per frame instead of 32.

## 5.1.2 Master Clock

### 5.1.2.1 External Clock

The ALIS-D can be driven by an external clock of frequency between 24 MHz and 33 MHz. This is connected to pin MCLK1; MCLK2 is then left unconnected.

### 5.1.2.2 External Crystal

Alternatively, the ALIS-D can be driven by an external crystal of a fundamental frequency between 24 and 33 MHz. This is connected between pins MCLK1 and MCLK2.

### 5.1.3 Telephone Line Interface

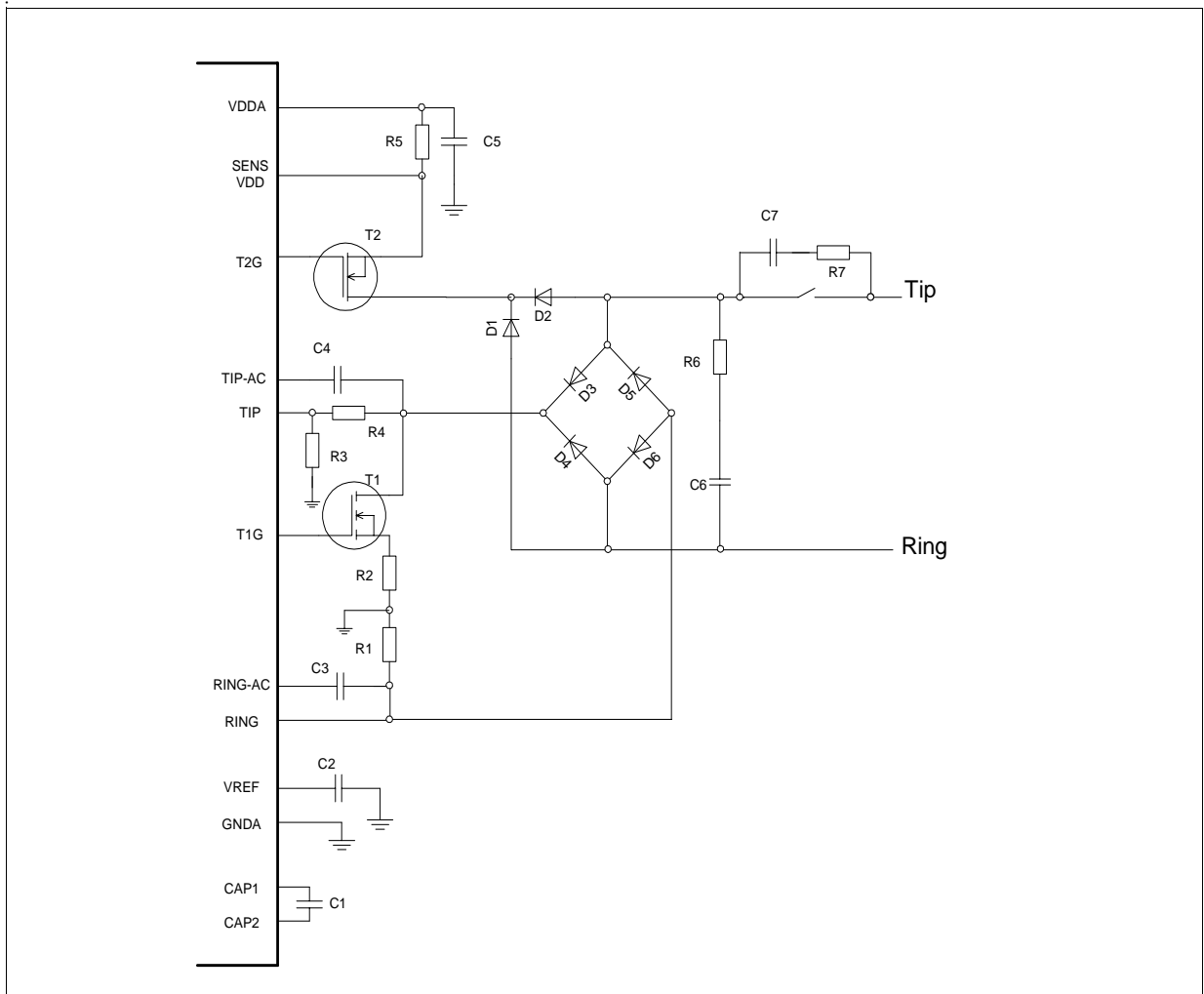


Figure 5-16 Connection of ALIS-A to Telephone Line

Table 5-5 External Components PSB 4595

Transistors	Type/Value	Tolerances	Comments
T1	BSP 88		FET, N channel enhancement type
T2	BSP 129		FET, N channel depletion type
Resistors	Type/Value	Tolerances	Comments
R1	36	1 %	
R2	4.7	5 %	

**Table 5-5 External Components PSB 4595 (cont'd)**

R3	24 k	1 %	
R4	470 k	1 %	
R5	3.6	5 %	
R6	1 k		
R7	240		
<b>Capacitors</b>	Type/Value	Tolerances	Comments
C1	1 $\mu$ / 6 V	10 %	
C2	15 n / 6 V	10 %	
C3	22 n / 250 V	10 %	
C4	22 n / 250 V	10 %	
C5	22 $\mu$ / 6 V	20 %	
C6	0.68 n / 250 V	5 %	
C7	1 $\mu$ / 250V	10 %	
<b>Diodes</b>	Type/Value	Tolerances	Comments
D1	½ BAW101		
D2	½ BAW101		
D3	½ BAW240A		
D4	½ BAW240A		
D5	½ BAW240A		
D6	½ BAW240A		

**Figure 5-16** shows the external components required to connect the ALIS-A to the telephone line. Component values shown are typical. Transistor T1 modulates the loop current and synthesizes the impedance. Transistor T2 regulates the supply voltage. Near Tip, note the relay that serves as hook switch.

### 5.1.3.1 DC Termination

The interface to the Tip/Ring must match different characteristics in different countries. For example, the voltage/current relationship must fit inside a mask defined for that country, as shown in **Figure 5-17**. The voltage/current relationship for the ALIS-A Tip/Ring interface is programmable, so that it can meet different masks when loaded with different coefficient sets. Full coefficient sets will be provided by Infineon Technologies, specific to each country; however, certain specific parameters are made available to allow exploration of the ALIS's flexibility with regard to the mask. The voltage/current relationship is governed by the equation:

$$I(V) = \frac{(V - V_0)}{R} \quad \text{for } (V - V_0) < R \cdot I_{max}$$

and

$$I(V) = I_{max} \quad \text{for } (V - V_0) \geq R \cdot I_{max}$$

In this equation,  $I$  is the line current,  $V$  is the voltage between Tip and Ring, and the following parameters are set by programming:

$R$ , the resistive slope: can be set to 100, 200, 240, or 280  $\Omega$ .

$I_{max}$ , the maximum current: can be set to 50 or 100 mA.

$V_0$  is the sum of the forward voltages of the diodes in the external rectifying bridge (typically  $2 \cdot 0.4$  V for Schottky diodes) plus the parameter  $DCO$ .  $DCO$  can be set to 0, 1.5, 3.5, or 7.2 V.

*Note: The DC termination is enabled only in the Conversation state.*

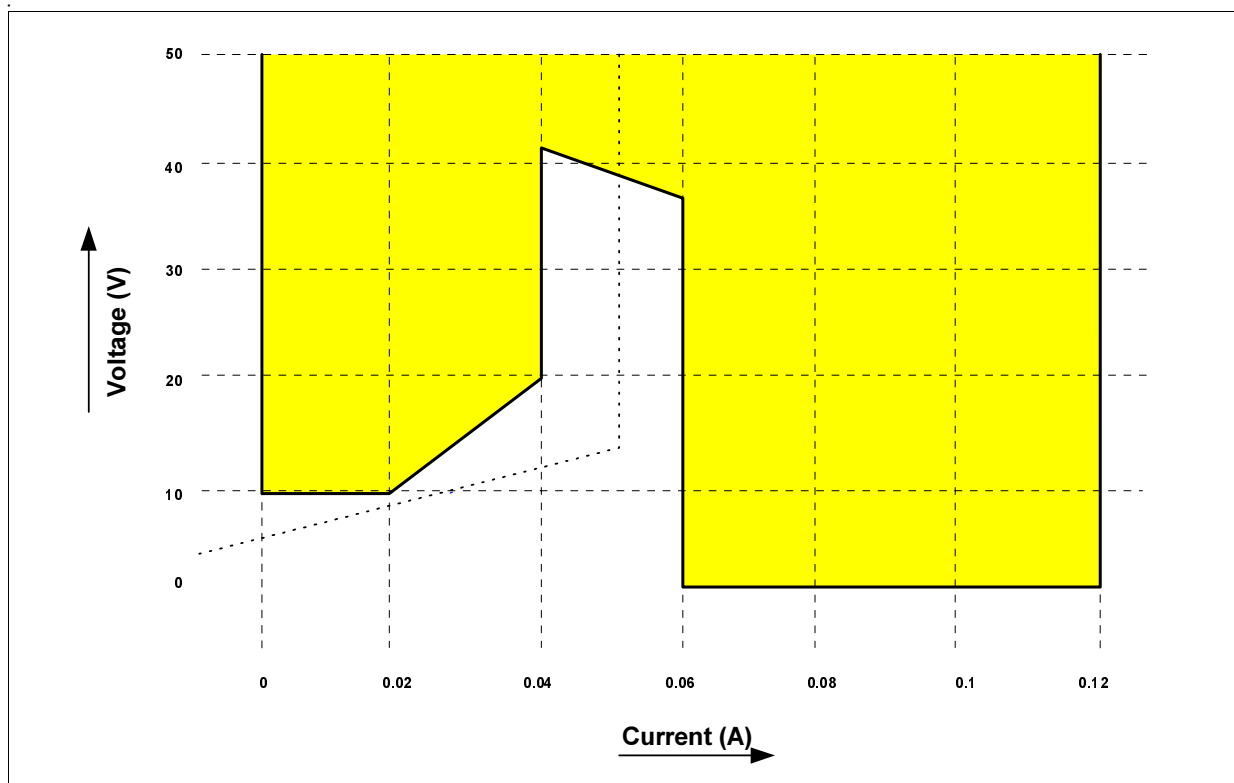


Figure 5-17 Fitting Voltage/Current Relationship into Example Mask

### 5.1.3.2 Pulse Dialing

Pulse dialing is possible by using the Pulse Dialing feature, and is accomplished by having the external transistor T1 short the tip and ring. The duration of and the interval between the pulses is controlled by the Host through the SCI by using the bit pdial in register R11.

### 5.1.3.3 DTMF Dialing

DTMF tones are provided by two internal tone generators of frequency accuracy better than  $\pm 1\%$ . The absolute transmission level is programmable; but, the level of Tone Generator 2 is always 2 to 3 dB greater than that of Tone Generator 1 to realize the required emphasis. Therefore tone generator 2 should be used for the high frequency group of tones.

*Note: The tone generators can also generate in-band sine waves for test purposes.*

### 5.1.3.4 Metering Pulses

Metering pulses up to  $2.5 V_{RMS}$  can be sustained without degradation of performance. To prevent degradation in case of higher voltages, an external metering filter is required.

## 5.1.4 Caller-ID Interface

The ALIS-D is connected to the Tip/Ring through capacitors by the CID\_T and CID\_R pins. The Caller-ID interface complies with the following specifications for Caller-ID: Bellcore TR-NWT-000030 and SR-TSV-002476, Bell 202, and ITU-T V.23.

This service operates by transmitting the Calling Line Identification Presentation (CLIP) from the central office in the silent interval between the first and second rings, using 1200 baud FSK modulation.

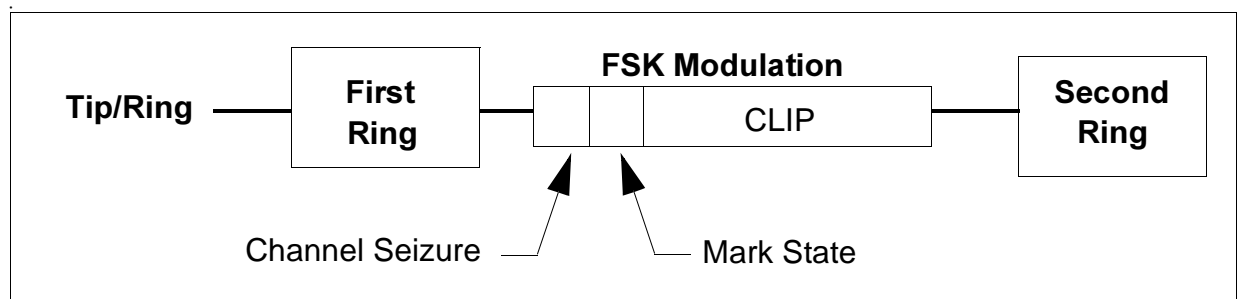
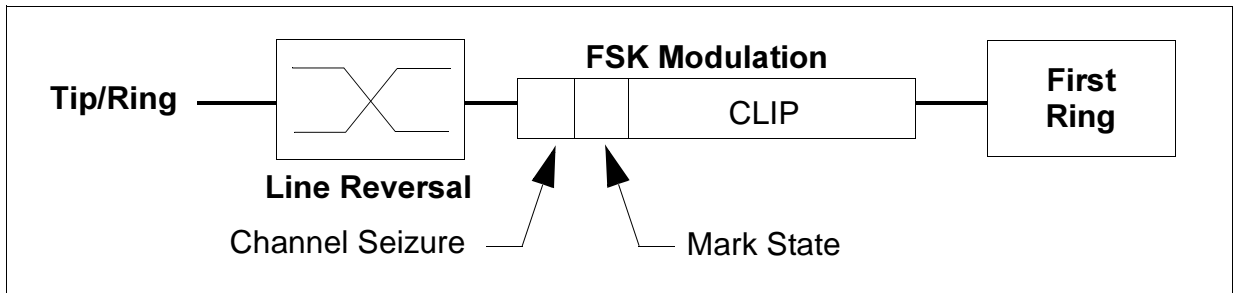


Figure 5-18 Caller-ID Timing

The ALIS-D can be programmed to detect line reversal, the method of initiating Caller-ID employed in the United Kingdom.



**Figure 5-19 Caller ID by Line Reversal**

The ALIS will detect the start of a Caller-ID signal after a MARK sequence (64 or more consecutive '1's), followed by a '0'.

The ALIS will store the signal in the CID-RAM in the registers Index 64/Offset 0 to Index 88/Offset 15 (64 bytes). An interrupt can be generated when the last register is filled. Optionally, it is possible to operate in 2-page mode, in which case an interrupt is also generated when the register Index 72/Offset 15 is filled.

The ALIS-D can store the signal in one of two formats:

1. Parsed according to ITU-T Recommendation V.14, with a START bit ('0'), 8 Caller-ID bytes (LSB first), and up to 10 STOP bits; or
2. Raw form: all bits after the MARK will be stored in order:

**Table 5-6 Storing the Caller ID Signal in CID-RAM**

Index	Offset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Interrupt issued
64	0	cid8	cid7	cid6	cid5	cid4	cid3	cid2	cid1	
...	...	...	...	...	...	...	...	...	...	
72	15	cid256	cid255	cid254	cid253	cid252	cid251	cid250	cid249	i_cid1 (only in 2-page mode)
80	0	cid264	cid263	cid262	cid261	cid260	cid258	cid258	cid257	
...	...	...	...	...	...	...	...	...	...	
88	15	cid512	cid511	cid510	cid509	cid508	cid507	cid506	cid505	i_cid2

*Note: see chapter "Programming" on page 7-78 on how to access these registers.*



### 5.1.5 Digital Isolation Interface

The isolation between ALIS-A and ALIS-D and therefore from the Tip/Ring side to the host/datapump side can be realized in two ways:

#### Capacitive Interface

Isolation is realized by six capacitances. The two “A”, “B” and “C” capacitors must match to within 5 % of the selected value between 10 to 100 pF.

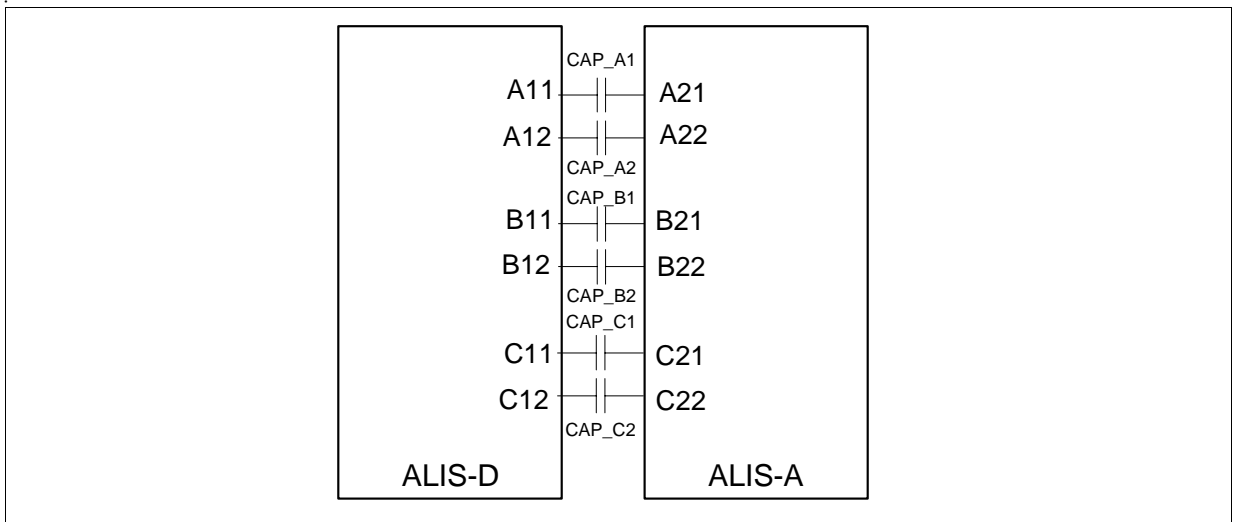


Figure 5-20 Isolation by Capacitive Interface

#### Inductive Interface

Isolation is realized by extra small transformers provided by third party.

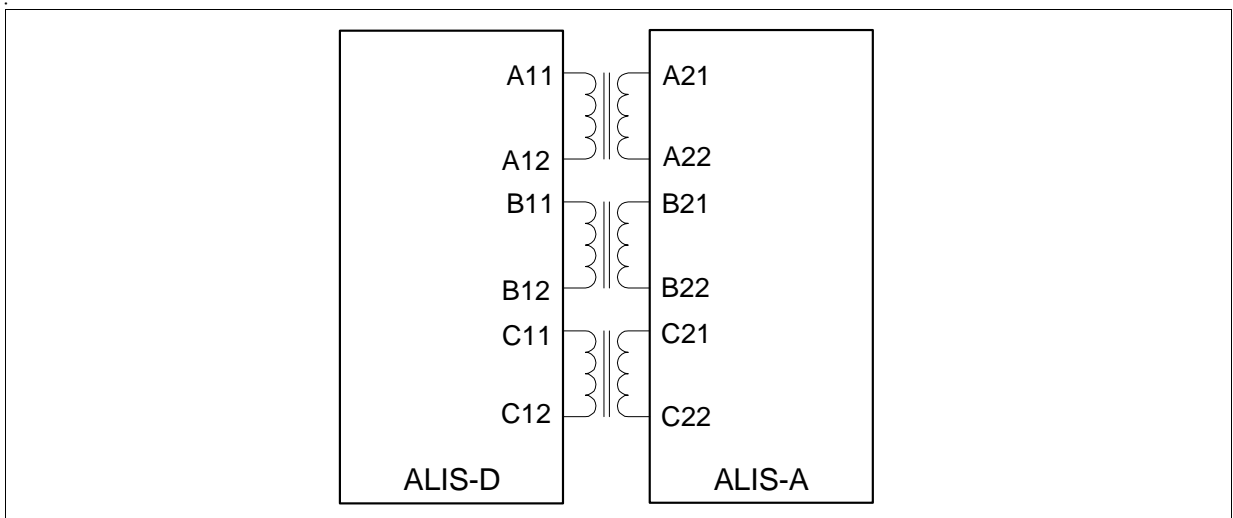


Figure 5-21 Isolation by Inductive Interface

## 5.2 Software Interface

The Host communicates with the ALIS chipset over the Serial Control Interface (SCI). There are three kinds of communication between them:

- Programming of the ALIS-D (this is discussed in **Chapter 7**),
- Operating commands (these control the real-time operation of the ALIS), and
- Interrupts (there are seven specific interrupts that the ALIS-D uses; each can be separately disabled).

All three types of communication entail either reading from or writing to registers in the ALIS-D.

### 5.3 Reset Sequence

The ALIS-D can be Reset by a command from the Host, or by setting the  $\overline{\text{RESET}}$  pin to low, and then releasing it. Over a period of 1300 clock-cycles of MCLK after the rising edge of  $\overline{\text{RESET}}$ , the configuration registers are initialized to their default values: during this period, the ALIS-D undergoes mode selection: the MODE pin sets Multiplex (high) or Non-multiplex (low); the BM pin sets Master (high) or Slave (low).

After that, the ALIS-D must be programmed by the Host to meet specific line conditions. This is done by using the ALIS-D programming commands to set the values of the parameters and coefficients in the Coefficient RAM (CRAM). Complete sets of coefficients appropriate for many countries are available from Infineon Technologies.

After this Reset process, the ALIS-D is in Idle state. From that point on, it will transition to other states in accordance with operating commands from the Host and incoming signals from the Tip/Ring.

## 6 Register Description

The programming and much of the operation of the ALIS chipset is controlled by the values of bits in the registers of the ALIS-D. Some of these bits can be used to adapt the chipset to a specific application; whereas others are reserved for internal use.

The ALIS-D registers are addressed by Index and Offset. Index values are incremented by 8, so the possible Index values are 0, 8, 16,...etc. Offset values are incremented by 1, so the possible Offset values are 0, 1, ... 15 (see "Programming" on page 7-78).

## 6.1 Register Map

**Table 6-1 ALIS-D Registers**

Index & Offset	MSB Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB Bit0	
0	0	index(7)	index(6)	index(5)	index(4)	index(3)	index(2)	index(1)	index(0)
0	1	i_cadence	i_ring	i_cid2	i_cid1	i_vdd	i_gpio_d	i_gpi_1_a	i_gpi_0_a
0	2	en_cadence	en_ring	en_cid2	en_cid1	en_vdd	en_gpio	en_gpi_1_a	en_gpi_0_a
0	3	gpo_d	0	0	0	state(3)	state(2)	state(1)	state(0)
0	4	to_sleep(7)	to_sleep(6)	to_sleep(5)	to_sleep(4)	to_sleep(3)	to_sleep(2)	to_sleep(1)	to_sleep(0)
0	5	n_ring(7)	n_ring(6)	n_ring(5)	n_ring(4)	n_ring(3)	n_ring(2)	n_ring(1)	n_ring(0)
0	6	auto_sleep	auto_ring	sdi_on	osci_on	ring_int	line_rev	cid_v14	sdi_loop
0	7	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
0	8	cad_to(7)	cad_to(6)	cad_to(5)	cad_to(4)	cad_to(3)	cad_to(2)	cad_to(1)	cad_to(0)
0	9	cad_t(7)	cad_t(6)	cad_t(5)	cad_t(4)	cad_t(3)	cad_t(2)	cad_t(1)	cad_t(0)
0	10	ring_cnt(7)	ring_cnt(6)	ring_cnt(5)	ring_cnt(4)	ring_cnt(3)	ring_cnt(2)	ring_cnt(1)	ring_cnt(0)
0	11	0	0	0	0	0	0	0	pdial
0	12	0	0	0	0	0	0	0	valid_ring
0	13	0	0	0	0	s_vdd	gpio_d	gpi_1_a	gpi_0_a
0	14	ver(7)	ver(6)	ver(5)	ver(4)	ver(3)	ver(2)	ver(1)	ver(0)
0	15	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.

Index 8/Offset 0 to Index 56/Offset 15 registers are used by the ALIS-D for internal processes.

8	0	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
...	...	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
56	15	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.

Index 64/Offset 0 to Index 88/Offset 15 registers are used to store the Caller-ID information.

64	0	cid8	cid7	cid6	cid5	cid4	cid4	cid2	cid1
...	...	cid...	cid...	cid...	cid...	cid...	cid...	cid...	cid...
88	15	cid512.	cid511	cid510	cid509	cid508	cid507	cid506	cid505

Index 96/Offset 0 to Index 96/Offset 5 registers are used by the ALIS—D for internal processes.

96	0	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
...	...	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
96	5	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
96	6	k(7)	k(6)	k(5)	k(4)	k(3)	k(2)	k(1)	k(0)
96	7	k(15)	k(14)	k(13)	k(12)	k(11)	k(10)	k(9)	k(8)

Index 96/Offset 8 to Index 104/Offset 2 registers are used by the ALIS—D for coefficients and parameters downloaded during initialization. Some of these bits, as identified, are also intended to allow adaptation for specific applications.

96	8	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
96	9	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
96	10	Res.	Res.	Res.	dco(1)	dco(0)	i_max	r(1)	r(0)

**Table 6-1 ALIS-D Registers (cont'd)**

Index & Offset		MSB Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB Bit0
96	11	Res.	Res.	Res.	gpo_1Q_a	gpo_0_a	Res.	Res.	Res.
96	12	Res.	Res.	Res.	fac_os(1)	fac_os(0)	Res.	Res.	Res.
96	13	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
96	14	Res.	Res.	Res.	en_ptg2	en_ptg1	en_tg2	en_tg1	Res.
96	15	Res.	Res.	Res.	en_cid	Res.	Res.	Res.	Res.
104	0	Res.	Res.	fac_fsc(1)	fac_fsc(0)	Res.	fac_sdi(2)	fac_sdi(1)	fac_sdi(0)
104	1	gpio_d_o	Res.	Res.	osc_off	sw_reset	en_gpio_d_o	Res.	en_buzzer
104	2	en_fsc2	Res.	fsc2del(5)	fsc2del(4)	fsc2del(3)	fsc2del(2)	fsc2del(1)	fsc2del(0)

Index 104/Offset 3 to Index 112/Offset 3 registers are used by the ALIS-D for internal processing.

104	3	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
...	...	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
112	2	en_sci_pu	en_sdi_pu	Res.	Res.	Res.	Res.	Res.	Res.
112	3	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.

Index 128/Offset 0 to Index 184/Offset 15 registers are used to store the coefficients and parameters which adapt the behavior of the ALIS-D. Complete sets of coefficients and parameters are available from Infineon Technologies for each country.

128	0	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
...	...	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
184	15	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.

## 6.2 Detailed Register Descriptions

### Register Description Example:

Index	Offset	Short Name	Long Name	Type	Default Value
-------	--------	------------	-----------	------	---------------

7	6	5	4	3*	2*	1	0
		Res.					

Bits marked with a "\*" are set to 1 by default after reset. For this example, the default value would be 0C<sub>H</sub>.

Reserved bits (like bit 5 in the example) are not allowed to be changed. Read-Modify-Write commands are necessary.

0	0	R0	INDEX	r/w	00 <sub>H</sub>
---	---	----	-------	-----	-----------------

7	6	5	4	3	2	1	0
index(7)	index(6)	index(5)	index(4)	index(3)	index(2)	index(1)	index(0)

**index[7:0]** The ALIS-D registers are addressed by Index and Offset. Index values are incremented by 8, so the possible Index values are 0, 8, 16, ... etc. Offset values are incremented by 1, so the possible Offset values are 0, 1, ... 15. The use of this addressing scheme is described in Chapter 7, Programming.

0	1	R1	INTERRUPTS					r	00 <sub>H</sub>
	7	6	5	4	3	2	1	0	
	i_cadence	i_ring	i_cid2	i_cid1	i_vdd	i_gpio_d	i_gpi_1_a	i_gpi_0_a	

Indicates which interrupt has caused high to low transition on  $\overline{\text{INT}}$  line. All interrupts have time granularity of the FSC, faster events cannot be detected. A Read operation will reset this register to zero and will set the  $\overline{\text{INT}}$  pin to inactive (high).

**i\_cadence** Interrupt based on cadence time out. Two possible causes:

- Valid ring not detected within cadence timeout (defined in register R8) after a valid ring.
- The valid ring not detected within cadence timeout (defined in register R8) after a line reversal/spike.

**i\_ring** Interrupt based on rings; three modes can be selected (see register R6). In each mode, the meaning of the interrupt is different:

- If Automatic Call Processing not selected: A possible ring, as signal on Tip/Ring is higher than  $10 V_{\text{RMS}}$ .
- Automatic Call Processing mode, ring\_int = 1: A valid ring detect, interrupt every ring.
- Automatic Call Processing mode, ring\_int = 0: The programmed number (n\_ring) of valid rings has been detected.

**i\_cid2** Interrupt source: Caller-ID buffer is full or end of CID is detected.

**i\_cid1** Interrupt source: First page of Caller-ID buffer is full or end of CID is detected (only active in 2-page mode).

**i\_vdd** Interrupt source: Status change on power supply indicated by bit s\_vdd in register R13.

**i\_gpio\_d** Interrupt source: Signal change on the pin GPIO\_D on ALIS-D.



**i\_gpi\_1\_a**    Interrupt source: Signal change on the pin GPI\_1\_A on ALIS-A.

**i\_gpi\_0\_a**    Interrupt source: Signal change on the pin GPI\_0\_A on ALIS-A.

0	2	R2	INTERRUPT ENABLE	r/w	00 <sub>H</sub>
---	---	----	------------------	-----	-----------------

7	6	5	4	3	2	1	0
en_cadence	en_ring	en_cid2	en_cid1	en_vdd	en_gpio	en_gpi_1_a	en_gpi_0_a

**en\_cadence** Enable for cadence interrupt (i\_cadence).

en\_cadence = 0 Disabled.

en\_cadence = 1 Enabled.

**en\_ring** Enable for ring interrupt (i\_ring).

en\_ring = 0 Disabled.

en\_ring = 1 Enabled.

**en\_cid2** Enable for interrupt at end of Caller-ID buffer (i\_cid2).

en\_cid2 = 0 Disabled.

en\_cid2 = 1 Enabled.

**en\_cid1** Enable for interrupt for first page of Caller-ID buffer (i\_cid1).

en\_cid1 = 0 Disabled.

en\_cid1 = 1 Enabled, 2-page mode enabled.

**en\_vdd** Enable for i\_vdd.

en\_vdd = 0 Disabled.

en\_vdd = 1 Enabled.

**en\_gpio** Enable for i\_gpio.

en\_gpio = 0 Disabled.

en\_gpio = 1 Enabled.

**en\_gpi\_1\_a** Enable for i\_gpi\_1\_a.  
en\_gpi\_1\_a = 0 Disabled.  
en\_gpi\_1\_a = 1 Enabled.

**en\_gpi\_0\_a** Enable for i\_gpi\_0\_a.  
en\_gpi\_0\_a = 0 Disabled.  
en\_gpi\_o\_a = 1 Enabled.

Register Description

0	3	R3	STATE					r/w	00 <sub>H</sub>
	7	6	5	4	3	2	1	0	
	gpo_d	0	0	0	state(3)	state(2)	state(1)	state(0)	

**gpo\_d** Value of gpo\_d controls pin GPO\_D. It is normally used to control the hook relay.

gpo\_d = 0 Low on GPO\_D.

gpo\_d = 1 High on GPO\_D.

**state[3:0]** Operating states used to control ALIS functionality.

IDLE 0 0 0 0 Idle state.

CIDC 0 0 0 1 Caller-ID state

RCMD 1 0 0 0 Ringing state.

CONV 1 0 0 1 Conversation state.

PULS 1 0 1 0 Pulse Dialing state.

SLEEP 1 1 1 1 Sleep state.

Other values of the variable state[3:0] are reserved.

Register Description

0	4	R4	SLEEP TIMEOUT	r/w	FF <sub>H</sub>
---	---	----	---------------	-----	-----------------

Bit	7*	6*	5*	4*	3*	2*	1*	0*
	to_sleep (7)	to_sleep (6)	to_sleep (5)	to_sleep (4)	to_sleep (3)	to_sleep (2)	to_sleep (1)	to_sleep (0)

**to\_sleep[7:0]** Applicable only for Auto Sleep mode (see register R6): time (in FSC cycles), before device transitions to Sleep state.

0	5	R5	RING NUMBER	r/w	02 <sub>H</sub>
---	---	----	-------------	-----	-----------------

Bit	7	6	5	4	3	2	1*	0
	n_ring (7)	n_ring (6)	n_ring (5)	n_ring (4)	n_ring (3)	n_ring (2)	n_ring (1)	n_ring (0)

**n\_ring[7:0]** Applicable only for Automatic Call Processing mode (see register R6): number of rings before the ring interrupt (i\_ring) will be set.

0	6	R6	AUTO MODES	r/w	02 <sub>H</sub>
---	---	----	------------	-----	-----------------

Bit	7	6	5	4	3	2	1*	0
	auto_sleep	auto_ring	sdi_on	osci_on	ring_int	line_rev	cid_v14	sdi_loop

Sets the operating mode of the chip.

- auto\_sleep** Enables Auto Sleep mode for reduced power consumption.  
 auto\_sleep = 0 ALIS will remain in Idle state indefinitely.  
 auto\_sleep = 1 Sets Auto Sleep mode. Chip will transition automatically from Idle to Sleep state after timeout (register R4), if there is no activity on pin SDI\_TX or on Tip/Ring.
- auto\_ring** Enables the Automatic Call Processing mode.  
 auto\_ring = 0 Automatic Call Processing mode not selected.  
 auto\_ring = 1 ALIS set to Automatic Call Processing mode: The chip will accordingly set the following interrupts, if they are enabled: i\_cid1, i\_cid2 and i\_ring.
- sdi\_on** Enables automatic activation of the SDI.  
 sdi\_on = 0 The SDI is activated only during Conversation state.  
 sdi\_on = 1 The SDI is on except during Sleep state.
- osci\_on** Enables automatic de-activation of the oscillator.  
 osci\_on = 0 During Sleep state, the oscillator is switched off.  
 osci\_on = 1 During Sleep state, the oscillator is active.

- ring\_int**      Applicable only in Automatic Call Processing mode: Enables counting of valid rings.
- ring\_int = 0      Ring interrupt only after the programmed number of rings (n\_ring).
- ring\_int = 1      Every valid ring causes a ring interrupt (i\_ring).
- 
- line\_rev**      Applicable only if Automatic Call Processing is enabled: Enables automatic storing of Caller-ID signal after line reversal.
- line\_rev = 0      No further action after line reversal.
- line\_rev = 1      ALIS automatically starts to store Caller-ID after line reversal.
- 
- cid\_v14**      Enables storing of Caller-ID data in V.14 format.
- cid\_v14 = 0      Chip stores raw bits of the Caller-ID message to the CID-RAM.
- cid\_v14 = 1      Chip stores Caller-ID message to the CID-RAM, according to ITU-T Recommendation V.14.
- 
- sdi\_loop**      Test mode to check the SDI.
- sdi\_loop = 0      Loop back is disabled.
- sdi\_loop = 1      Data from Host are looped back through the SDI with a one-frame delay.

<b>Index 0/Offset 7</b>	<b>COUNTRY-SPECIFIC COEFFICIENTS WILL BE PROVIDED BY INFINEON TECHNOLOGIES.</b>
-------------------------	---

Register Description

0	8	R8	CADENCE TIMEOUT	r/w	7D <sub>H</sub>
---	---	----	-----------------	-----	-----------------

Bit	7	6*	5*	4*	3*	2*	1	0*
	cad_to (7)	cad_to (6)	cad_to (5)	cad_to (4)	cad_to (3)	cad_to (2)	cad_to (1)	cad_to (0)

**cad\_to[7:0]** The cadence timeout: the maximum period between two valid rings. The timeout is  $500 * \text{FSC period} * \text{cad\_to}[7:0]$ . For example, if the FSC frequency is 8000 Hz, the timeout period can be programmed to be a multiple of  $500 * 1/8000 = 62.5$  ms.

0	9	R9	CADENCE TIME	r	00 <sub>H</sub>
---	---	----	--------------	---	-----------------

Bit	7	6	5	4	3	2	1	0
	cad_t(7)	cad_t(6)	cad_t(5)	cad_t(4)	cad_t(3)	cad_t(2)	cad_t(1)	cad_t(0)

**cad\_t[7:0]** Time since last valid ring, measured in units of 500 FSC periods, just as for the cadence timeout (register R8).



**Register Description**

<b>0</b>	<b>10</b>	<b>R10</b>	<b>RING COUNT</b>					<b>r</b>	<b>00<sub>H</sub></b>
----------	-----------	------------	-------------------	--	--	--	--	----------	-----------------------

Bit	7	6	5	4	3	2	1	0
	ring_cnt (7)	ring_cnt (6)	ring_cnt (5)	ring_cnt (4)	ring_cnt (3)	ring_cnt (2)	ring_cnt (1)	ring_cnt (0)

**ring\_cnt[7:0]** Number of valid rings. Reset at the transition from Idle to Ringing state.

<b>0</b>	<b>11</b>	<b>R11</b>	<b>PULSE DIALING</b>					<b>r/w</b>	<b>00<sub>H</sub></b>
----------	-----------	------------	----------------------	--	--	--	--	------------	-----------------------

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	pdial

**pdial** Applicable only in Pulse Dialing state: this bit controls Make and Break for pulse dialing.

pdial = 0            Break

pdial = 1            Make

<b>0</b>	<b>12</b>	<b>R12</b>	<b>RING STATUS</b>					<b>r</b>	<b>00<sub>H</sub></b>
----------	-----------	------------	--------------------	--	--	--	--	----------	-----------------------

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	valid_ ring

**valid\_ring** Indicates if the current ring is valid, as determined by frequency and amplitude. Updated every framesync.

valid\_ring = 0    No ring, or no valid ring.

valid\_ring = 1    Current ring valid.

**Register Description**

<b>0</b>	<b>13</b>	<b>R13</b>	<b>INTERRUPT VALUES</b>					<b>r</b>	<b>00<sub>H</sub></b>
----------	-----------	------------	-------------------------	--	--	--	--	----------	-----------------------

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	s_vdd	gpio_d	gpi_1_a	gpi_0_a

**s\_vdd**      Status of power supply in ALIS-A

s\_vdd = 0      No power.

s\_vdd = 1      Power is supplied and the digital isolation interface is running.

**gpio\_d**      Value of GPIO\_D pin.

gpio\_d = 0      Low on GPIO\_D.

gpio\_d = 1      High on GPIO\_D.

**gpi\_1\_a**      Value of GPI\_1\_A pin.

gpi\_1\_a = 0      Low on GPI\_1\_A.

gpi\_1\_a = 1      High on GPI\_1\_A.

**gpi\_0\_a**      Value of GPI\_0\_A pin.

gpi\_0\_a = 0      Low on GPI\_0\_A.

gpi\_0\_a = 1      High on GPI\_0\_A.

Register Description

0	14	R14	VERSION	r	11 <sub>H</sub>
---	----	-----	---------	---	-----------------

Bit	7	6	5	4	3	2	1	0
	ver(7)	ver(6)	ver(5)	ver(4)	ver(3)	ver(2)	ver(1)	ver(0)

**ver[7:0]** Version of the chip.

Index 0/Offset 15 - Index 56/Offset 15	RESERVED FOR INTERNAL USE, DO NOT MODIFY.
---	---

Index 64/Offset 0 - Index 88/Offset 15	CID-RAM: RESERVED FOR STORING THE CALLER-ID.
---	---

Index 96/Offset 0 - Index 96/Offset 5	RESERVED FOR INTERNAL USE, DO NOT MODIFY.
--	---

96	6	R15	INTERNAL CLOCK PARAMETER	r/w	00 <sub>H</sub>
----	---	-----	--------------------------	-----	-----------------

Bit	7	6	5	4	3	2	1	0
	k(7)	k(6)	k(5)	k(4)	k(3)	k(2)	k(1)	k(0)

96	7	R16	INTERNAL CLOCK PARAMETER	r/w	00 <sub>H</sub>
----	---	-----	--------------------------	-----	-----------------

Bit	7	6	5	4	3	2	1	0
	k(15)	k(14)	k(13)	k(12)	k(11)	k(10)	k(9)	k(8)

**k[15:0]** All frequencies and rates of the chip derive from its internal clock  $F_{\text{internal}}$  (see **Chapter 3.3.13**). This is in turn derived from the external Master Clock  $F_{\text{MCLK}}$  or an external crystal, as shown below. The reduction will be a factor  $F_{\text{MCLK}} / F_{\text{internal}}$  between  $\sim 2$  ( $K = 32767$ ) and 1 ( $K = -32768$ ).

$$\frac{F_{\text{MCLK}}}{F_{\text{internal}}} = 1 + \left( \frac{(32768 + K)}{2 \times 32768} \right) \quad \text{or} \quad K = 65536 \times \left( \frac{F_{\text{MCLK}}}{F_{\text{internal}}} - 1 \right) - 32768$$

K must be programmed in complements of two.

**Table 6-2 Programming Examples for K**

K [Integer]	K [Hex]	$F_{\text{MCLK}}/F_{\text{internal}}$ [1]
-32768	8000	1
...	...	...
-1	FFFF	$\sim 1.5$
0	0000	1.5
...	...	...
32767	7FFF	$\sim 2$

Index 96/Offset 8 - 9	RESERVED FOR INTERNAL USE, DO NOT MODIFY.
-----------------------	---

**Register Description**

<b>96</b>	<b>10</b>	<b>R17</b>	<b>DC Characteristics</b>				<b>r/w</b>	<b>00<sub>H</sub></b>
Bit	7	6	5	4	3	2	1	0
	Res.	Res.	Res.	dco(1)	dco(0)	i_max	r(1)	r(0)

All bits in this register are provided by Infineon Technologies for country-specific application. However, the dco, i\_max, and r bits are also made accessible to allow exploration of the ALIS's flexibility with regard to the DC termination (see **Chapter 5.1.3.1**).

**dco[1:0]**      DC voltage parameter DCO.

00	0 V
01	1.5 V
10	3.5 V
11	7.2 V (in this case the resistive slope R = 70 Ω regardless of bit r[1:0])

**i\_max**      Maximum current I<sub>max</sub>.

0	100 mA
1	50 mA

**r[1:0]**      Resistive slope R.

00	280 Ω
01	240 Ω
10	200 Ω
11	100 Ω

Register Description

96	11	R18	DIGITAL OUTPUTS				r/w	00 <sub>H</sub>
----	----	-----	-----------------	--	--	--	-----	-----------------

Bit	7	6	5	4	3	2	1	0
	Res.	Res.	Res.	gpo_1Q_a	gpo_0_a	Res.	Res.	Res.

**gpo\_1Q\_a** Value of GPO\_1Q\_A pin.  
gpo\_1Q\_a = 0 High on GPO\_1Q\_A.  
gpo\_1Q\_a = 1 Low on GPO\_1Q\_A.

**gpo\_0\_a** Value of GPO\_0\_A pin.  
gpo\_0\_a = 0 Low on GPO\_0\_A.  
gpo\_0\_a = 1 High on GPO\_0\_A.

Register Description

96	12	R19	OVERSAMPLING FACTOR	r/w	00 <sub>H</sub>
----	----	-----	---------------------	-----	-----------------

Bit	7	6	5	4	3	2	1	0
	Res.	Res.	Res.	fac_os (1)	fac_os (0)	Res.	Res.	Res.

**fac\_os[1:0]** The value of fac\_os determines the oversampling factor for the SDI (see **Chapter 3.3.13**): the sampling frequency is determined by:

$$f_{\text{sampling}} = \frac{\text{OversamplingFactor}}{4096} \cdot f_{\text{internal}}$$

- 00 Oversampling factor is 2.
- 01 Oversampling factor is 4.
- 10 Oversampling factor is 8.
- 11 Not allowed.

Index 96/Offset 13	RESERVED FOR INTERNAL USE, DO NOT MODIFY.
--------------------	---

96	14	R20	DTMF				r/w	00 <sub>H</sub>
----	----	-----	------	--	--	--	-----	-----------------

Bit	7	6	5	4	3	2	1	0
	Res.	Res.	Res.	en_ptg2	en_ptg1	en_tg2	en_tg1	Res.

**en\_ptg2** Enables Tone Generator 2 to use downloaded coefficients.  
 en\_ptg2 = 0 Tone Generator 2 produces 1 kHz tone.  
 en\_ptg2 = 1 Tone Generator 2 uses coefficients in CRAM.

**en\_ptg1** Enables Tone Generator 1 to use downloaded coefficients.  
 en\_ptg1 = 0 Tone Generator 1 produces 1 kHz tone.  
 en\_ptg1 = 1 Tone Generator 1 uses coefficients in CRAM.

**en\_tg2** Enables Tone Generator 2  
 en\_tg2 = 0 Tone Generator 2 disabled.  
 en\_tg2 = 1 Tone Generator 2 enabled.

**en\_tg1** Enables Tone Generator 1  
 en\_tg1 = 0 Tone Generator 1 disabled.  
 en\_tg1 = 1 Tone Generator 1 enabled.



Register Description

96	15	R21	ENABLE CID	r/w	00 <sub>H</sub>
----	----	-----	------------	-----	-----------------

Bit	7	6	5	4	3	2	1	0
	Res.	Res.	Res.	en_cid	Res.	Res.	Res.	Res.

**en\_cid** Enables storage of the Caller-ID signal between the first two valid rings, or after line reversal.

en\_cid = 0 Caller-ID disabled.

en\_cid = 1 Caller-ID enabled.

104	0	R22	FRAMESYNC	r/w	42 <sub>H</sub>
-----	---	-----	-----------	-----	-----------------

Bit	7	6*	5	4	3	2	1*	0
	Res.	Res.	fac_fsc (1)	fac_fsc (0)	Res.	fac_sdi (2)	fac_sdi (1)	fac_sdi (0)

**fac\_fsc[1:0]** The value of fac\_fsc controls the framesync frequency (see **Chapter 3.3.13**): it determines the factor by which the frequency of the internal clock is divided to produce the framesync frequency (only in master mode).

$$f_{FSC} = \frac{f_{\text{internal}}}{\text{fscDivider}}$$

00	FSC divider is 2048 (default).
01	FSC divider is 1024.
10	FSC divider is 512.
11	Not allowed.

**fac\_sdi[2:0]** The value of fac\_sdi controls the frequency of the SDI\_CLK (see **Chapter 3.3.13**): it determines the factor by which the frequency of the internal clock is divided to produce the frequency of the SDI\_CLK (only in master mode).

$$f_{SDICLK} = \frac{f_{\text{internal}}}{\text{sdiDivider}}$$

010	SDI_CLK divider is 8 (default).
011	SDI_CLK divider is 16.
100	SDI_CLK divider is 32.
101	SDI_CLK divider is 64.

Other values of the variable fac\_sdi[2:0] are reserved.

104	1	R23	Miscellaneous Control	r/w	00 <sub>H</sub>
-----	---	-----	-----------------------	-----	-----------------

Bit	7	6	5	4	3	2	1	0
	gpio_ d_o	Res.	Res.	osc_off	sw_ reset	en_gpio_ d_o	Res.	en_ buzzer

**gpio\_d\_o** Value for pin GPIO\_D, if enabled as output.

gpio\_d\_o = 0 Low on GPIO\_D.

gpio\_d\_o = 1 High on GPIO\_D.

**osc\_off** Oscillator control

osc\_off = 0 Oscillator on: required when using crystal.

osc\_off = 1 Oscillator off: required when using external clock.

**sw\_reset** Software Reset:

sw\_reset = 0 -

sw\_reset = 1 Causes reset of ALIS. The chip is ready to respond again after 100 μs. This bit is cleared automatically during the reset process.

**en\_gpio\_d\_o**

en\_gpio\_d\_o = 0 GPIO\_D as input.

en\_gpio\_d\_o = 1 GPIO\_D as output.

**en\_buzzer** Buzzer enable.

en\_buzzer = 0 BUZZER pin is set to low.

en\_buzzer = 1 BUZZER pin output is set to data stream after ADC.

Register Description

104	2	R24	FSC2 CONTROL	r/w	00 <sub>H</sub>
-----	---	-----	--------------	-----	-----------------

Bit	7	6	5	4	3	2	1	0
	en_fsc2	Res.	fsc2_ del(5)	fsc2_ del(4)	fsc2_ del(3)	fsc2_ del(2)	fsc2_ del(1)	fsc2_ del(0)

**en\_fsc2** Enables FSC2 as output.  
 en\_fsc2 = 0 FSC2 pin is set permanent low.  
 en\_fsc2 = 1 FSC2 is generated.

**fsc2\_del[5:0]** Delay between FSC and FSC2.  
 fsc2\_del = 000000 delay of one SDI\_CLK cycle  
 fsc2\_del = 000001 delay of two SDI\_CLK cycles  
 ... ..  
 fsc2\_del = 011111 delay of 32 SDI\_CLK cycles  
 fsc2\_del = 111111 delay of 64 SDI\_CLK cycles

Index 104/Offset 3- Index 112/Offset 1	RESERVED FOR INTERNAL USE, DO NOT MODIFY.
---	---

Register Description

112	2	R25	SDI_RX PULL-UP	r/w	23 <sub>H</sub>
-----	---	-----	----------------	-----	-----------------

Bit	7	6	5*	4	3	2	1*	0*
	en_sci_pu	en_sdi_pu	Res.	Res.	Res.	Res.	Res.	Res.

**en\_sci\_pu** Enables internal pull-up for SCI\_OUT pin.

en\_sci\_pu = 0 Pull-up disabled.

en\_sci\_pu = 1 Pull-up enabled.

**en\_sdi\_pu** Enables internal pull-up for SDI\_RX pin.

en\_sdi\_pu = 0 Pull-up disabled.

en\_sdi\_pu = 1 Pull-up enabled.

Index 112/Offset 3 - Index 112/Offset 15	RESERVED FOR INTERNAL USE, DO NOT MODIFY.
---	---

Index 120/Offset 0 - Index 120/Offset 15	RESERVED FOR INTERNAL USE, DO NOT MODIFY.
---	---

Index 128/Offset 0 - Index 184/Offset 15	COEFFICIENT RAM: COUNTRY-SPECIFIC COEFFICIENTS WILL BE PROVIDED BY INFINEON TECHNOLOGIES.
---	---

## 7 Programming

### 7.1 Reset Sequence

The Initialization of the ALIS V3 starts with either a software or a hardware reset:

- Software Reset: The host sets the `sw_reset` bit (bit 3) in register R23 (see page 6-75) to 1. The `sw_reset` bit is automatically cleared to "0" during the reset process.
- Hardware Reset: The `RESET` input pin (pin 23) of ALIS-D has to be set to "low" for at least 500 ns (see **Chapter 8.2** on page 8-90).

Important: It is not sufficient to detach the ALIS V3 from the power supply to initiate a Reset.

Over a period of 1300 clock cycles (= duration of the initialization sequence) of the MCLK, after releasing the `RESET`, the configuration registers are set to their default values and the interface is configured according to the connection of the following pins during the reset phase:

- pin 7 BM ("High" -> Master Mode / "Low" -> Slave Mode) and
- pin 11 `SCI_CLK/MODE` ("High" -> Multiplex Mode / "Low" -> Non multiplex Mode) of the ALIS-D

*Note: If the Multiplex Mode is selected, the input `SCI_CS/SWAP` (pin 10) of the ALIS-D is used to select the order of SDI and SCI bits.*

Following this,

- if in Master Mode:  
The host has to write the value of the internal clock parameter (K), and also the oversampling factor (`fac_os`), FSC dividing factor (`fac_fsc`), and SDI dividing factor (`fac_sdi`), when they are different from the default values (K = 0.5, `fac_os` = 2, `fac_fsc` = 2048 and `fac_sdi` = 8).
- if in Slave Mode:  
K is automatically programmed according to the external sample rate FSC, However the host still has to program the oversampling factor (`fac_os`).

After this Reset process, the configuration of the ALIS V3 is completed by writing all other required bits to the registers (please refer to "Configuration of the ALIS-D" on page 7-80). The ALIS V3 is in the Idle state, and from that point on a transition to other states in accordance with operating commands from the host and incoming signals from the Tip/Ring is possible.

## 7.2 Setup during Reset of the ALIS-D

The following table shows as an example the order of events after resetting ALIS-D with

- Serial Data Interface in Master mode
- Serial Data Interface in Multiplex mode
- First 16 bits SDI and next 16 bits SCI

The order of the steps in this and the following tables is recommended for full functionality:

**Table 7-1 Setup Sequence of the ALIS-D**

Step	Pin (Mode Setting)	Logic State	Description
Reset			
1	23 " $\overline{\text{RESET}}$ " <sup>1)</sup>	pin 23 = low	Initiate Reset of ALIS-D
Master mode			
2	7 "BM" <sup>1)</sup>	pin 7 = high	ALIS-D is set in Master mode
Multiplex mode			
3	11 "SCI_CLK/ MODE" <sup>1)</sup>	pin 11 = high	ALIS-D is set in Multiplex mode
Serial Data Interface			
4	10 " $\overline{\text{SCI\_CS}}$ / SWAP" <sup>1)</sup>	pin 10 = low	First 16 bits for SDI, next 16 bits for SCI
5	23 " $\overline{\text{RESET}}$ " <sup>1)</sup>	pin 23 = high	Release of the Reset after $t_{\text{RESET,min}}$ (t.b.d., about 500 ns)

<sup>1)</sup> see **Table 2-2** on page 2-18

### 7.3 Configuration of the ALIS-D

The following table shows the configuration of ALIS-D with

- Fractional Divider (Parameter K)
- FSC frequency and SDI Clock
- Oversampling Factor

**Table 7-2 Configuration Sequence of the ALIS-D<sup>1)</sup>**

Step	Register	Value <sup>2)</sup> (Example)	Description
Fractional Divider (Parameter K)			
6	R15 (see page 6-68)	00h (default)	Configuration of the Fractional Divider (only in Master mode): Internal Clock = 16.384 MHz
7	R16	00h (default)	
FSC frequency and SDI Clock			
8	R22 (see page 6-73)	XX01X100	FSC = 16 kHz (fac_fsc = 01b) and SDI_CLK = 512 kHz (fac_sdi = 100b)
Oversampling factor			
9	R19 (see page 6-71)	XXX01XXX	Sampling frequency = 16 kHz (fac_os = 01b for oversampling factor = 4)

<sup>1)</sup> valid for MCLK = 24.576 MHz

<sup>2)</sup> X bits are not allowed to be changed (read-modify-write (r/w) operation required).



## 7.4 Determination of the State of the ALIS-D

The following table shows the determination of the State of the ALIS-D with

- Automatic power mode switching
- Detection of Caller-ID
- Ring interrupt after two rings

**Table 7-3 Configuration Sequence of the ALIS-D**

Step	Register	Value <sup>1)</sup>	Description
Automatic Power mode switching			
10	R6 (see page 6-62)	40h	Enables the Automatic Call Processing mode
11	R5 (see page 6-61)	02h	Two rings are programmed before the ring interrupt will be set.
12	R4 (see page 6-61)	0Ah	If Auto Sleep mode is enabled go to sleep after 10 frames.
Ring interrupt			
13	R2 (see page 6-58)	F0h	Enables the interrupts <ul style="list-style-type: none"> <li>– Ring</li> <li>– CID 1, CID 2</li> <li>– Cadence</li> </ul>
CRAM write			
14	Coefficient registers (Index 128 - 184)		CRAM registers are written according to the country specification
Switch DSP flags			
15	R20 (see page 6-72)	XXX1100X	Enables the Tone Generators using CRAM coefficients (en_ptg1 = 1, en_ptg2 = 1, en_tg1 = 0, en_tg2 = 0)
16	R21 (see page 6-73)	XXX1XXXX	Enables Caller-ID (en_cid = 1)

<sup>1)</sup> X bits are not allowed to be changed (read-modify-write (r/w) operation required).

## 7.5 Commands

Programming of ALIS-D consists of writing to or reading from registers of the ALIS-D:

- A **Read** command allows the host to determine the contents of a register in the ALIS-D. It includes the address of the register to be read.
- A **Write** command allows the host to set the contents of a register. It includes the address of the register to be set, and is followed by the data to be written into that register.

Because of the extensive register space required, the address of a register is determined by two parts:

- the 8-bit Index and
- the 4-bit Offset.

A Read or Write command requires either one or two steps, depending on the indexed addressing requirement. If the Index is 0, one step is required. If the Index is not 0, two steps are required.

## 7.5.1 Single-Step Command

If the Index for a register is 0 and the Offset A[3:0] is not 0, Read or Write Commands are executed as single step commands. The data to be written consists of the byte D[7:0].

### 7.5.1.1 Single-Step Write Command

Bit	7	6	5	4	3	2	1	0
	Read/ Write	Index	Offset_ 3	Offset_ 2	Offset_ 1	Offset_ 0	Fixed	Don't Care
	0	0	A3	A2	A1	A0	1	x

Data:

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

In the command byte, the MSB (bit 7) is 0 for **Write**; bit 6 is 0 because the Index is 0 (extended addressing is not needed); the Offset takes 4 bits (bit 5 to bit 2); the fixed bit 1 always has the value 1. The LSB (bit 0) is a don't care bit. Both command and data are transmitted at the SCI\_IN input pin.

### 7.5.1.2 Single-Step Read Command

Bit	7	6	5	4	3	2	1	0
	Read/ Write	Index	Offset_ 3	Offset_ 2	Offset_ 1	Offset_ 0	Fixed	Don't Care
	1	0	A3	A2	A1	A0	1	x

Data:

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

In the command byte, the MSB (bit 7) is 1 for **Read**; bit 6 is 0 because the Index is 0 (extended addressing is not needed); the Offset takes 4 bits (bit 5 to bit 2); the fixed bit 1 always has the value 1. The LSB (bit 0) is a don't care bit.

The Read Command is transmitted at the SCI\_IN input pin; the data of the addressed register are shifted out at the SCI\_OUT output pin.

## 7.5.2 Two-Step Command

If the address of a register requires an Index, **Read** and **Write** commands must be implemented in two steps.

### 7.5.2.1 Two-Step Write Command

#### STEP ONE:

The value of the Index is written to the Index register at address Index 0/Offset 0. In the example below, the value of the Index is represented by the bits J[7:0]:

#### Write Index - First Command:

Bit	7	6	5	4	3	2	1	0
<u>Read/Write</u>	Index	Offset_ 3	Offset_ 2	Offset_ 1	Offset_ 0	Fixed	Don't Care	
0	0	0	0	0	0	1	x	

#### Data (index):

Bit	7	6	5	4	3	2	1	0
	J7	J6	J5	J4	J3	J2	J1	J0

#### STEP TWO:

The data are written to the location of the register, specified by the previously written Index and the Offset represented by the bits A[3:0]:

#### Write Data - Second Command:

Bit	7	6	5	4	3	2	1	0
<u>Read/Write</u>	Index	Offset_ 3	Offset_ 2	Offset_ 1	Offset_ 0	Fixed	Don't Care	
0	1	A3	A2	A1	A0	1	x	

#### Data:

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

In the second command, the index bit (bit 6) is 1, indicating that the Offset A[3:0] is tied to the Index value (which is stored at Index 0/Offset 0) to define the complete address of the register.

### 7.5.2.2 Two-Step Read Command

A **Read** command from a location requiring an Index is also processed in two steps: the first command to write the Index value to address Index 0/Offset 0, and a second command which includes the Offset to read the desired register:

#### STEP ONE:

##### **Write Index - First Command:**

Bit	7	6	5	4	3	2	1	0
<u>Read/</u> <u>Write</u>	Index	Offset_ 3	Offset_ 2	Offset_ 1	Offset_ 0	Fixed	Don't Care	
0	0	0	0	0	0	1	x	

##### **Contents:**

Bit	7	6	5	4	3	2	1	0
	J7	J6	J5	J4	J3	J2	J1	J0

#### STEP TWO:

The second step is reading from the location of the register, specified by the previously written Index and the Offset represented by the bits A[3:0]:

##### **Read Data - Second Command:**

Bit	7	6	5	4	3	2	1	0
<u>Read/</u> <u>Write</u>	Index	Offset_ 3	Offset_ 2	Offset_ 1	Offset_ 0	Fixed	Don't Care	
1	1	A3	A2	A1	A0	1	x	

##### **Contents:**

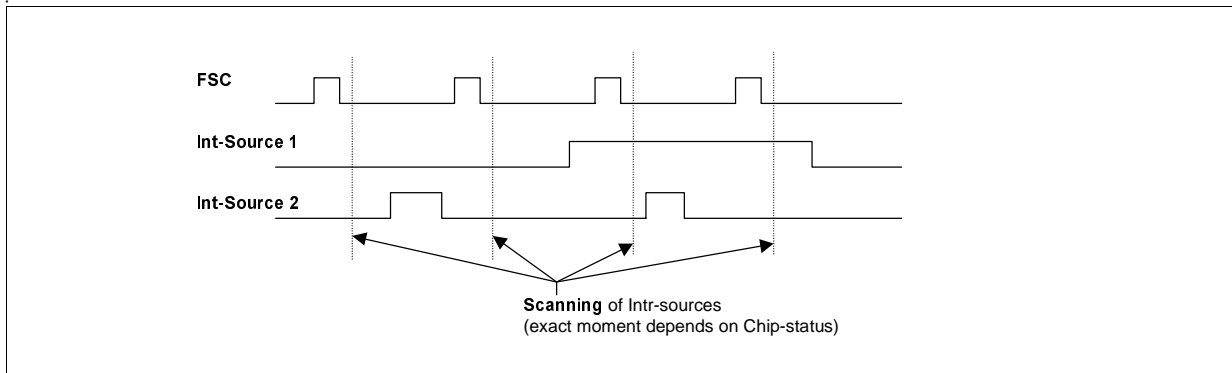
Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

Both commands are transmitted at the SCI\_IN input pin; the contents of the addressed register are shifted out at the SCI\_OUT output pin.

## 7.6 Interrupt Handling

The interrupt handling in ALIS V3 is realized by the ALIS firmware. The interrupt sources are sampled once every frame. An interrupt source has to be stable for a minimum of one frame period in order to be detected.

In the following example the change of interrupt source 1 is detected. Interrupt source 2 is ignored because its duration is less than a frame hence it is not detected.



**Figure 7-1 Scanning of an Interrupt**

The following table shows the interrupt register (software register) which consists of four static and four dynamic interrupts (for further description of this register see 'R1' on page 6-56).

**Table 7-4 Interrupt Register R1**

Dynamic Interrupts				Static Interrupts			
7	6	5	4	3	2	1	0
i_ca- dence	i_ring	i_cid2	i_cid1	i_vdd	i_gpio _d	i_gpi_ 1_a	i_gpi_ 0_a

### 7.6.1 Static Interrupts

Any change of a static interrupt source longer than two frame periods generates an interrupt. Every detected signal change is indicated by '1' in the corresponding bit in the interrupt register R1.

The static interrupts in the interrupt register are reset automatically by reading register R1 from the host.

The actual value of the static interrupt sources is available in R13 (see page 6-66). The firmware copies the status of the static interrupt sources to register R13 every frame.

**Table 7-5 Static Interrupts**

<b>Interrupt</b>	<b>Bit in Register R1</b>	<b>Description</b>
i_gpi_0_a	Bit 0	Signal pin 18 "GPI_0_A" at ALIS-A
i_gpi_1_a	Bit 1	Signal pin 17 "GPI_1_A" at ALIS-A
i_gpio_d	Bit 2	Signal pin 8 "GPIO_D" at ALIS-D
i_vdd	Bit 3	Indicates that the ALIS-A is power supplied, and the digital isolation interface is running

The interrupts i\_gpi\_0\_a, i\_gpi\_1\_a and i\_vdd are transferred via the Digital Isolation Interface to the ALIS-D. They are stored in R13 (see page 6-66) (= interrupt source).

## 7.6.2 Dynamic Interrupts

An event generates an interrupt. Every detected event is indicated by '1' in the corresponding bit in the interrupt register (for further description of this register see 'R1' on page 6-56). The bits in this register are cleared automatically by reading the interrupt register from the host.

The interrupt sources of the dynamic interrupts are cleared automatically.

**Table 7-6 Dynamic Interrupts**

Interrupt	Bit in Register R1	Description
i_cid1	Bit 4	First page of the Caller ID buffer is full or end of CID is detected (2 page mode)
i_cid2	Bit 5	a) Caller ID buffer is full or end of CID is detected (1 page mode). b) Second page of Caller ID buffer is full or end of CID is detected (2 page mode).
i_ring	Bit 6	Interrupt bases on rings; three modes can be selected (refer to 'R6' on page 6-62): <ul style="list-style-type: none"> <li>• if auto_ring='1' then <ul style="list-style-type: none"> <li>– Detection of a valid ring (ring_int='1' in 'R6' on page 6-62)</li> <li>– Detection of the programmed number (n_ring, see 'R5' on page 6-61) of valid rings (ring_int='0' in 'R6' on page 6-62)</li> </ul> </li> <li>• if auto_ring='0' then detection of a signal on Tip/Ring (higher than 10 Vrms).</li> </ul>
i_cadence	Bit 7	Interrupt bases on cadence time out. The timeout can be programmed via 'R8' (see page 6-64). Possible causes: Valid ring not detected within cadence timeout after a valid ring Valid ring not detected within cadence timeout after line reversal/spike.



### 7.6.3 Interrupt Handling for the Host

The host can program the interrupt enable register (see 'R2' on page 6-58) to enable the interrupts with '1' in the corresponding bits.

The pin 14  $\overline{\text{INT}}$  of the ALIS-D indicates an interrupt with "low".

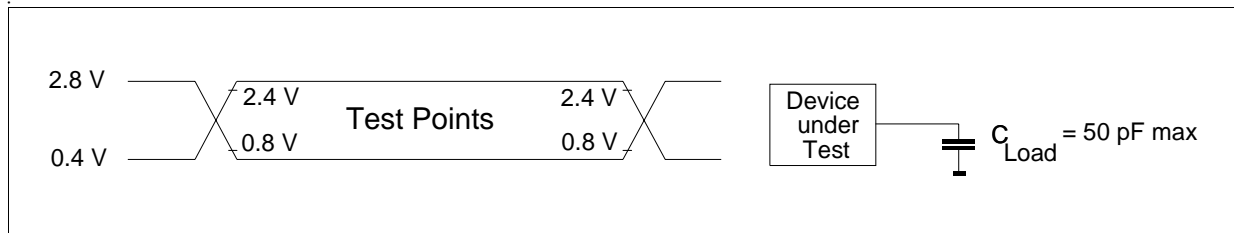
The host has to read the interrupt register (see 'R1' on page 6-56) to get the information about the source of the interrupt. After reading the interrupt register it is cleared automatically and the pin  $\overline{\text{INT}}$  is set to "high".

If a static interrupt source causes an interrupt, the host can read the interrupt values register ('R13' on page 6-66) to get the actual value of the corresponding static interrupt source.

If all interrupts are disabled, the host still can poll the interrupt register to detect a signal change for a static interrupt source or an event for a dynamic interrupt source.

## 8 Timing Diagrams

### 8.1 Input/Output Waveform for AC Tests



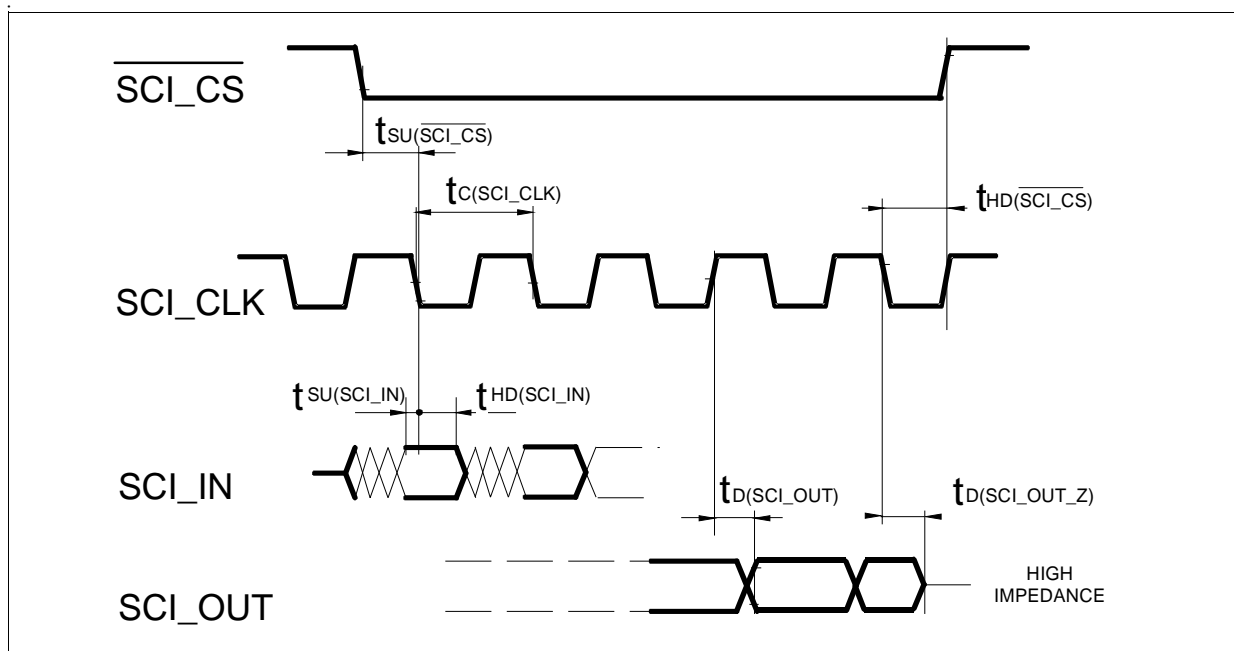
**Figure 8-1** Waveform for AC Tests

During AC-Testing, the inputs are driven at a low level of 0.4 V and a high level of 2.8 V. The timing tests are made at 0.8 V and 2.4 V respectively.

### 8.2 Reset Timing

To Reset the ALIS, pulses applied to the  $\overline{\text{RESET}}$  pin must be less than 0.8 V and longer than  $t_{\text{RESET,min}}$  (t.b.d., about 500 ns). Pulses shorter than  $t_{\text{RESET,ignore}}$  (t.b.d., about 100 ns) are ignored.

### 8.3 Serial Control Interface Timing



**Figure 8-2** Serial Control Interface Timing

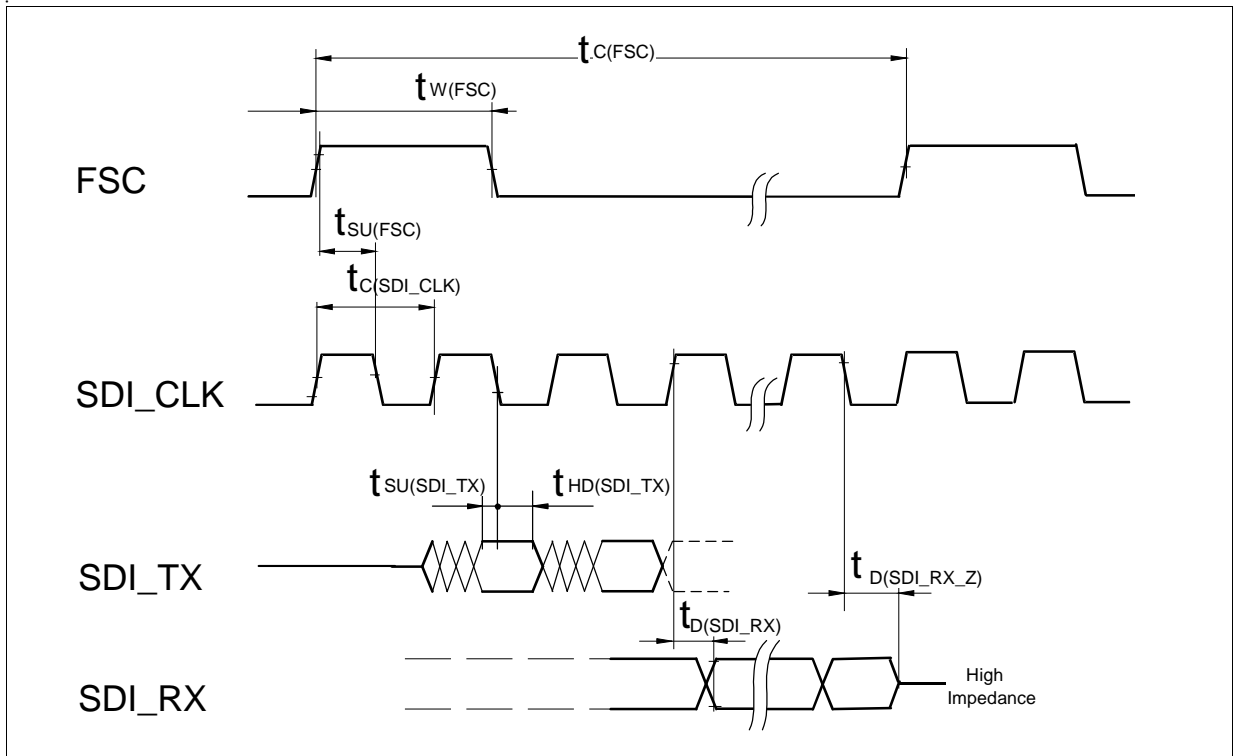
**Table 8-1 Serial Control Interface Timing Characteristics**

*SCI\_CLK need not have constant frequency. These values apply for  $V_{DD} = 3.3 V \pm 5\%$ , and ambient temperature in the range 0 - 70°C.*

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
SCI Clock-Cycle Time	$t_{C(SCI\_CLK)}$	488		-	ns
SCI Clock Duty Cycle		t.b.d.	50	t.b.d.	%
SCI frequency		-	-	2048	kHz
Setup Time: SCI_CS $\downarrow$ until next SCI_CLK $\downarrow$	$t_{SU(SCI\_CS)}$	t.b.d.	t.b.d.	t.b.d.	ns
Hold Time: last SCI_CLK $\downarrow$ until SCI_CS $\uparrow$	$t_{HD(SCI\_CS)}$	120			ns
Setup Time: SCI_IN valid before SCI_CLK $\downarrow$	$t_{SU(SCI\_IN)}$	60			ns
Hold Time: last SCI_CLK $\downarrow$ until SCI_IN invalid	$t_{HD(SCI\_IN)}$	120			ns
Delay Time: SCI_CLK $\uparrow$ until SCI_OUT valid	$t_{D(SCI\_OUT)}$			100	ns
Delay Time: last SCI_CLK $\downarrow$ until SCI_OUT_Z (when SCI_OUT goes to tristate)	$t_{D(SCI\_OUT\_Z)}$	13		40	ns

*Note: Switchable SCI\_OUT internal pull-up resistor: 660 k $\Omega$*

### 8.4 Serial Data Interface Timing



**Figure 8-3 Serial Data Interface Timing**

*Note: SDI\_RX goes to tristate on last bit of 16 transferred bits in a FSC frame.*

**Table 8-2 Serial Data Interface Timing Characteristics**

These values apply for  $V_{DD} = 3.3 V \pm 5\%$ , and ambient temperature in the range 0 - 70°C.

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
SDI Clock-Cycle Time	$t_{C(SDI\_CLK)}$	488		-	ns
SDI Clock Duty Cycle		45	50	55	%
SDI Clock frequency		256	-	2048	kHz
Frame Synchronization Clock (FSC)- Cycle Time	$t_{C(FSC)}$	31	125	139	μs
FSC frequency		7.2	8	32	kHz
FSC Pulse Width (required as input, in Slave Mode)	$t_{W(FSC)}$	$t_{C(SDI\_CLK)}$			
FSC Pulse Width (produced as output, in Master Mode)	$t_{W(FSC)}$		$t_{C(SDI\_CLK)}$		
Setup Time: SDI_TX valid before SDI_CLK↓	$t_{SU(SDI\_TX)}$	t.b.d.			ns
Hold Time: last SDI_CLK↓ until SDI_TX invalid	$t_{HD(SDI\_TX)}$	t.b.d.			ns
Delay Time: SDI_CLK↑ until SDI_RX valid	$t_{D(SDI\_RX)}$			t.b.d.	ns
Delay Time: last SDI_CLK↑ until FSC↑	$t_{D(FSC)}$		0	t.b.d.	ns
Setup Time: FSC↑ until next SDI_CLK↓	$t_{SU(FSC)}$	t.b.d.	0.5* $t_{C(SDI\_CLK)}$		ns
Delay Time: last SDI_CLK↓ until SDI_RX_Z (when SDI_RX goes to tristate)	$t_{D(SDI\_RX\_Z)}$	13		40	ns

The frame synchronization clock-cycle time is  $1/f_{FSC}$ , where  $f_{FSC}$  is the sampling rate. In turn,  $f_{FSC}$  is controlled by the parameter `fac_fsc`. See **Chapter 3.3.13**.

*Note: Switchable SDI\_RX internal pull-up resistor: 660 kΩ*

## 9 Electrical Characteristics

### 9.1 Recommended Operating Conditions

Table 9-1 Recommended Operating Conditions

Parameter	Symbol	Conditions			Unit
		min.	typ.	max.	
Digital Supply Voltage ALIS-D	$V_{DD}$	3.14	3.3	3.46	V
Analog Supply Voltage ALIS-A	$V_{DDA}$		4.25		V
Ambient Temperature under bias	$T_A$	0		70	°C
Operating Frequency	$f_{MCLK}$	24	24.576	33	MHz
Clock Duty Cycle		45	50	55	%
Signal Rise and Fall Time	$t_r, t_f$			20	ns

*Note: Extended operation outside the recommended limits may degrade performance and affect reliability.*

## 9.2 Extreme Absolute Range

Ratings in the following table, **Table 9-2**, apply to both ALIS-A and ALIS-D.

**Table 9-2 Extreme Absolute Range**

Parameter	Symbol	Range		Unit
		min.	max.	
Digital Supply Voltage	$V_{DD}$	-0.3	4.5	V
Analog Supply Voltage	$V_{DDA}$	-0.3	7.0	V
Analog Input Voltage	$V_{in}$	-0.3	$V_{DDA} + 0.3$	V
Digital Input Voltages	$VD_{in}$	-0.3	5.5	V
DC Output Current	$I_{out}$	-5	5	mA
Storage Temperature	$T_{ST}$	-60	125	°C
Ambient Temperature under bias	$T_A$	0	70	°C
Maximum Power Dissipation	$PD_{max}$		1	W

*Note: Stresses above those listed may cause permanent damage to the device. Extended operation at the absolute maximum levels may affect device reliability.*

### 9.3 DC Characteristics

#### 9.3.1 ALIS-A DC Characteristics

Table 9-3 DC Characteristics of the ALIS-A

These values apply for  $V_{DDA} = 4.25$  V, and ambient temperature in the range 0 - 70°C.

Parameter	Symbol	Conditions	Spec. Limits			Unit
			min.	typ.	max.	
<b><math>V_{DDA}</math> Supply Current</b>						
– in Ringing state (AC current during ringing burst, due to synthesized ringer impedance)	$I_{DDA1}$	$V_{ring} = 60$ Vdc + 90 Vrms $f_{ring} = 25 - 50$ Hz		2.5	3	mA
– in Conversation state (DC current, due to synthesized DC characteristics)	$I_{DDA2}$			7	10	mA
– in Pulse Dialing break state	$I_{DDA3}$	$V_{TIP/RING} = 60$ Vdc			500	$\mu$ A
<b>General Purpose Inputs and Outputs</b>						
Low-level Input Voltage: - at pins: Test, GPI_0_A, and GPI_1_A	$V_{IL}$				0.8	V
High-level Input Voltage: - at pins: Test, GPI_0_A, and GPI_1_A	$V_{IH}$		2.0			V
Low-level Output Voltage: - at pins: GPO_0_A, and GPO_1Q_A	$V_{OL}$	$I_{OL} = 5$ mA			0.5	V
High-level Output Voltage: - at pins: GPO_0_A, and GPO_1Q_A	$V_{OH}$	$I_{OH} = -5$ mA	3.25			V
Input Current Low	$I_{IL}$	$V_{IL} = GNDA$			$\pm 1$	$\mu$ A
Input Current High	$I_{IH}$	$V_{IH} = V_{DDA}$			$\pm 1$	$\mu$ A



**Electrical Characteristics**

**Table 9-3 DC Characteristics of the ALIS-A (cont'd)**

*These values apply for  $V_{DDA} = 4.25\text{ V}$ , and ambient temperature in the range  $0 - 70^{\circ}\text{C}$ .*

Parameter	Symbol	Conditions	Spec. Limits			Unit
			min.	typ.	max.	
<b>Input DC Resistance (on Tip/Ring)</b>						
– in Idle state	$R_{IN}$	Hook switch must be open, so infinite input resistance	5			$\text{M}\Omega$
– in Conversation state	$R_{IN}$	See <b>Chapter 5.1.3.1</b>				W
– in Pulse Dialing state	$R_{IN}$	During the “make” period			200	W
<b>Power-Up time</b>	$t_{PU}$				100	ms

### 9.3.2 ALIS-D DC Characteristics

**Table 9-4 DC Characteristics of the ALIS-D**

*These characteristics apply when  $V_{DD} = 3.3\text{ V} \pm 5\%$ , and for ambient temperature in the range  $0 - 70\text{ }^{\circ}\text{C}$ . All digital inputs are 5V tolerant.*

Parameter	Symbol	Conditions	Spec. Limits			Unit
			min.	typ.	max.	
<b>Supply Current:</b>		$V_{DD} = 3.3\text{ V}$ , no load				
– in Sleep state	$I_{DD0}$			< 10	50	$\mu\text{A}$
– in Idle state	$I_{DD1}$	$f_{MCLK} = 24\text{ MHz}$		3.5	10	mA
– in Ringing state	$I_{DD2}$	$f_{MCLK} = 24\text{ MHz}$		8	15	mA
– in Caller-ID state	$I_{DD3}$	$f_{MCLK} = 24\text{ MHz}$		8	15	mA
– in Conversation state	$I_{DD4}$	$f_{MCLK} = 24\text{ MHz}$		13	25	mA
– in Pulse Dialing state	$I_{DD5}$	$f_{MCLK} = 24\text{ MHz}$		8	15	mA
<b>Low-level Input Voltage:</b>						
– at CMOS Inputs: SCI_CLK, SCI_CS, SCI_IN, SDI_CLK, SDI_TX, MODE, FSC	$V_{IL1}$				0.8	V
– at CMOS Input: $\overline{\text{RESET}}$	$V_{IL3}$				0.8	V
– at clock Input: MCLK1	$V_{IL2}$				0.5	V
<b>High-level Input Voltage:</b>						
– at CMOS Inputs: SCI_CLK, SCI_CS, SCI_IN, SDI_CLK, SDI_TX, MODE, FSC	$V_{IH1}$		2.0		5.5	V
– at CMOS Input: $\overline{\text{RESET}}$	$V_{IH2}$		2.0		5.5	V
– at clock Input: MCLK1	$V_{IH3}$		2.0		5.5	V
<b>Low-level Output Voltage:</b>						
– at pins: SCI_OUT, $\overline{\text{INT}}$ , SDI_RX, FSC	$V_{OL}$	$I_{OL} = 5\text{ mA}$			0.5	V

Electrical Characteristics

**Table 9-4 DC Characteristics of the ALIS-D (cont'd)**

These characteristics apply when  $V_{DD} = 3.3\text{ V} \pm 5\%$ , and for ambient temperature in the range 0 - 70 °C. All digital inputs are 5V tolerant.

Parameter	Symbol	Conditions	Spec. Limits			Unit
			min.	typ.	max.	
<b>High-level Output Voltage:</b>						
- at pins: SCI_OUT, SDI_RX, FSC	$V_{OH}$	$I_{OH} = -5\text{ mA}$	$V_{DD} - 0.5$			V
<b>Input Current Low:</b>						
- at CMOS inputs: SCI_CLK, GPIO_D, SCI_CS, SCI_IN, SDI_CLK, SDI_TX, MODE, FSC, RESET	$I_{IL}$	$V_{IL} = \text{GND}$			$\pm 1$	$\mu\text{A}$
<b>Input Current High:</b>						
- at CMOS Inputs: SCI_CLK, GPIO_D, SCI_CS, SCI_IN, SDI_CLK, SDI_TX, MODE, FSC, RESET.	$I_{IH}$	$V_{IH} = V_{DD}$			$\pm 1$	$\mu\text{A}$
<b>Tristate Current Low:</b>						
Tristates, Bidirectionals: SCI_OUT, FSC, $\overline{\text{INT}}^{1)}$	$I_{OZL}$	$V_{IL} = \text{GND}$			$\pm 1$	$\mu\text{A}$
<b>Tristate Current High:</b>						
Tristates, Bidirectionals: SCI_OUT, FSC	$I_{OZH}$	$V_{IH} = V_{DD}$			$\pm 1$	$\mu\text{A}$

<sup>1)</sup> 33 k $\Omega$  internal pull-up resistor not taken into consideration.

Note: For load currents see "DC Output Current" in **Table 9-2**.

## 9.4 AC Characteristics

These characteristics apply under the following test conditions:

- Ambient temperature in the range 0 - 70 °C.
- $V_{DD} = 3.3 \text{ V} \pm 5\%$ .
- Line impedance  $Z_L = 600 \Omega \pm 0.1\%$ .
- The frequency of the test signal is 1004 Hz.
- $V_{DDA}$  is programmed to 4.25 V.
- The analog voltage level is defined as 0 dBm = 0.775 V<sub>rms</sub> when loaded at 600 Ω.
- The digital voltage level is defined such that 0 dBm0 = -3 dB below Full Scale.
- The ALIS-D gain parameters are set such that AGX = 0 dB = AGR, and an analog signal of 0 dBm corresponds to a digital signal of 0 dBm0.

**Table 9-5 AC Characteristics**

<b>Power Supply Rejection Ratio</b>		<b>Ripple: 0 - 150 kHz; 70 mVrms</b>				
Either Supply/Direction	PSRR	300 Hz - 3.4 kHz	40			dB
Either Supply/Direction	PSRR	3.4 - 150 kHz	25			dB
<b>Ring Threshold</b>	$V_{RThresh}$	$V_{DDA} = 4.25 \text{ V}$			10	Vrms

### 9.4.1 Absolute Gain Error

**Table 9-6 Absolute Gain Error**

<b>Direction</b>	<b>Symbol</b>	<b>Test Condition</b>	<b>Ambient Temperature</b>	<b>Limit Values</b>			<b>Unit</b>
				<b>min.</b>	<b>typ.</b>	<b>max</b>	
Receive	AE_R	-10 dBm analog input	25 °C	-1	± 0.5	+1	dB
Receive	AE_R	-10 dBm analog input	0 - 70 °C	-1.2	± 0.7	+1.2	dB
Transmit	AE_X	-10 dBm0 digital input	25 °C	-1	± 0.5	+1	dB
Transmit	AE_X	-10 dBm0 digital input	0 - 70 °C	-1.2	± 0.7	+1.2	dB

### 9.4.2 Gain Tracking

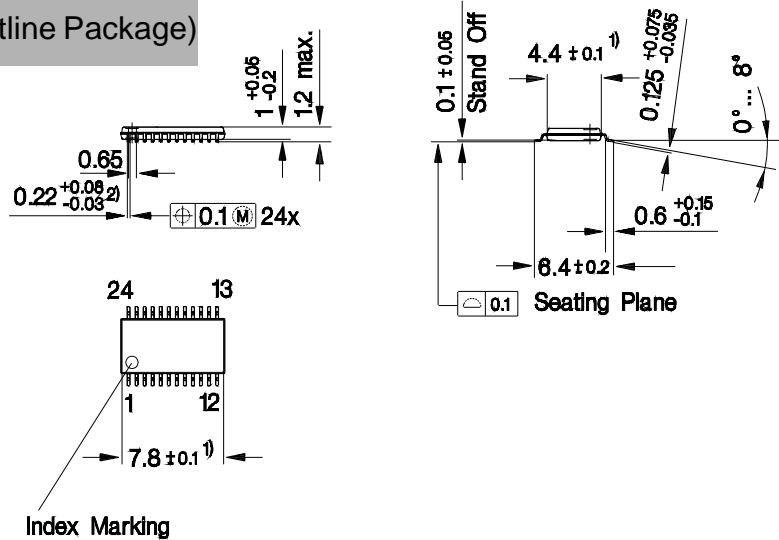
Table 9-7 Gain Tracking

Direction	Symbol	Test Condition	Limit Values			Unit
			min.	typ.	max.	
Receive	GT_R	0 to -10 dBm analog input	-0.15	± 0.01	0.15	dB
Receive	GT_R	-10 to -40 dBm analog input	-0.15	± 0.01	0.15	dB
Receive	GT_R	-40 to -50 dBm analog input	-0.3	± 0.07	0.3	dB
Transmit	GT_X	0 to -10 dBm0 digital input	-0.5	± 0.05	0.5	dB
Transmit	GT_X	-10 to -40 dBm0 digital input	-0.1	± 0.07	0.1	dB
Transmit	GT_X	-40 to -50 dBm0 digital input	-0.5	± 0.3	0.5	dB

## 10 Package Outlines

### P-TSSOP24 PSB 4595

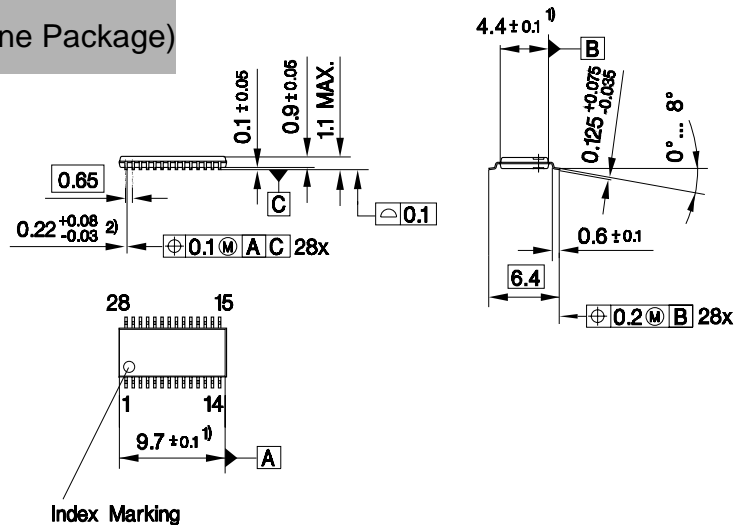
(Plastic Thin Shrink Small Outline Package)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion of 0.08 max. per side

### P-TSSOP28 PSB 4596

(Plastic Thin Shrink Small Outline Package)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion of 0.08 max. per side

### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

## 11 Appendix

### Glossary

AC	Alternating <b>C</b> urrent
ADC	Analog-to- <b>D</b> igital <b>C</b> onversion
ALIS	Analog <b>L</b> ine <b>I</b> nterface <b>S</b> olution, PSB 4595 and PSB 4596
CRAM	<b>C</b> oefficient <b>R</b> AM (Random Access Memory)
DAA	<b>D</b> ata <b>A</b> ccess <b>A</b> rrangement
DAC	<b>D</b> igital-to- <b>A</b> nalog <b>C</b> onversion
DC	<b>D</b> irect <b>C</b> urrent
DFS	<b>D</b> igital <b>F</b> ilter <b>S</b> tructure
DSP	<b>D</b> igital <b>S</b> ignal <b>P</b> rocessing
DTMF	<b>D</b> ual <b>T</b> one <b>M</b> ulti- <b>F</b> requency
FCC	<b>F</b> ederal <b>C</b> ommunications <b>C</b> ommission
ISDN	<b>I</b> ntegrated <b>S</b> ervices <b>D</b> igital <b>N</b> etwork
ITU	<b>I</b> nternational <b>T</b> elecommunication <b>U</b> nion
ITU-T	<b>I</b> nternational <b>T</b> elecommunication <b>U</b> nion - <b>T</b> SB (Telecommunications Standardization Bureau)
SCI	<b>S</b> erial <b>C</b> ontrol <b>I</b> nterface
SDI	<b>S</b> erial <b>D</b> ata <b>I</b> nterface
USB	<b>U</b> niversal <b>S</b> erial <b>B</b> us

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