MV78200

Discovery™ Innovation Series CPU Family

Hardware Specifications

MV-S104671-U0, Rev. C
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Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.x

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PRODUCT OVERVIEW

Building upon the Marvell® high-performance Sheeva™ CPU core, the MV78200 is part of the Discovery™ Innovation series CPU family.

The MV78200 is optimally designed for a broad range of applications ranging from sophisticated routers, switches, and wireless-base stations to high-volume storage and laser printer applications.

The MV78200 incorporates two fully ARMv5TE-compliant dual-issue CPU cores, with a double-precision, IEEE compliant Floating-point Unit (FPU), and 512 KB of L2 cache.

Its innovative crossbar architecture, advanced communications peripherals, and performance-tuned interfaces, make it a perfect, high-performance solution for embedded applications such as:

- Printers
- Core and edge routers
- Cellular base stations
- Ethernet switch management
- Storage arrays
- Network Attached Storage (NAS) devices

■ **The MV78200 Includes**

- Two high performance Sheeva™ dual issue CPUs with IEEE compliant FPU support
- 512 KB L2 cache per CPU
- High bandwidth DDR II memory interface (32/64-bit DDR2–800 MHz data rate with an 8-bit ECC option)
- 8/16/32-bit device bus with up to five chip selects, and with NAND and NOR Flash support
- Two x4 wide PCI Express ports with integrated PHY; each one can also act as four x1 ports
- Four Gigabit Ethernet MAC controllers
- Three USB 2.0 ports with integrated PHYs
- Two SATA 2.0 ports with integrated 3 Gbps SATA II PHY
- Security Cryptographic engine
- Four 16550 compatible UARTs
- Two channels SLIC/Codec TDM interface
- Four IDMA engines
- Integrated Storage Accelerator engine (two XOR DMA or iSCSI CRC engines)
- Timers
- Interrupt controller

■ **Sheeva™ Dual-Issue CPU with FPU support**

- Up to 1 GHz
- Super-scalar, dual-issue CPU
- Single-precision and double-precision FPU support
- 32-bit and 16-bit RISC architecture
- Compliant with v5TE architecture, published in the *ARM Architect Reference Manual*, Second Edition
- Supports 32-bit instruction set for performance and flexibility
- Supports 16-bit Thumb instruction set for code density
- Supports DSP instructions to boost performance for signal processing applications
- Includes MMU to support virtual memory features
- MPU can be used instead of MMU
- 32-KB I-Cache and 32-KB D-Cache, parity protected
- 512-KB unified L2 cache, ECC protected
- 64-bit internal data bus
- Variable pipeline stages—six to nine stages
- Out-of-order execution for increased performance
- In-order retire via Reordering Buffer (ROB)
- Branch Prediction Unit
- Supports JTAG/ARM-compatible ICE
- Supports both Big and Little Endian modes

■ **DDR2 SDRAM controller**

- Up to 400 MHz clock frequency (DDR2–800 MHz data rate)
- DDR SDRAM with a clock ratio of 1:N and 2:N (up to 1:5) between the DDR SDRAM and the Sheeva™ core, respectively
- SSTL 1.8V I/Os
- Auto-calibration of I/Os output impedance
- Supports four DRAM banks
- Supports all DDR devices, densities up to 2 Gb
- Up to 4 GB address space

- Supports all DIMMs configurations (registered and un-buffered, x8 or x16 DRAM devices)
- Supports 2T mode to enable high-frequency operation, even under heavy load configuration
- Supports DRAM bank interleaving
- Supports up to 32 open pages
- Supports up to 128-byte burst per single memory access

■ **Device Bus controller**
- 32-bit multiplexed address/data bus
- Supports different types of standard memory devices such as Flash, ROM, and SRAM
- Supports NAND Flash
- Five chip selects with programmable timing
- Optional external wait-state support
- 8-, 16-, or 32-bit width device support
- Up to 128-byte burst per single device bus access
- Support for boot ROMs

■ **Two PCI Express interfaces (x4)**
- PCI Express Base 1.1 compliant
- Integrated low-power SERDES PHY, based on proven Marvell SERDES technology
- Can be configured as an Endpoint or as Root Complex
- x1/x4 link width, 2.5 GHz signalling
- Lane polarity reversal support
- Maximum payload size of 128 bytes
- Single Virtual Channel (VC-0)
- Replay buffer support
- Extended PCI Express configuration space
- Advanced Error Reporting (AER) support
- Power management: L0s and SW L1 support
- Interrupt emulation message support
- Error message support

■ **Configurable PCI Express x4 or Quad x1 port**
- Each one of the PCI-Express ports can be configured to act as four independent x1 ports; this is useful for interfacing multiple off-the-shelf PCI-Express devices.
- Each of the x1 ports is PCI Express Base 1.1 compliant, has its own register file, and supports the full feature set as the x4 port.

■ **PCI Express Master specific features**
- Host to PCI Express bridge—translates CPU cycles to PCI Express Memory or configuration cycles
- Supports DMA bursts between memory and PCI-Express
- Supports up to four outstanding read transactions
- Maximum read request of up to 128 bytes
- Maximum write request of up to 128 bytes

■ **PCI Express Target specific features**
- Supports reception of up to four read requests
- Maximum read request of up to 4 KB
- Maximum write request of up to 128 bytes
- Supports PCI Express access to all of the device's internal registers

■ **Four Gigabit Ethernet MACs**
- Support 10/100/1000 Mbps
- Full wire speed receive and transmit of short packets
- GMII/MII interface when using a single port
- RGMII interface when using Port0 and Port1
- Priority queueing on receive based on DA, VLAN-Tag, IP-TOS
- Also supports queuing based on Marvell DSA Tag
- Layer2/3/4 frame encapsulation detection
- Supports long frames (up to 9K) on both receive and transmit
- Hardware TCP/IP checksum on receive and transmit

■ **Three USB 2.0 ports**
- Each port can act as USB host or peripheral
- USB 2.0 compliant
- Integrated USB 2.0 PHY
- EHCI compatible as a host
- As a host, supports direct connection to all peripheral types (LS, FS, HS)
- As a peripheral, connects to all host types (HS, FS) and hubs
- Up to six independent endpoints supporting control, interrupt, bulk, and isochronous data transfers
- Dedicated DMA for data movement between memory and port

■ **Integrates Two Marvell 3 Gbps SATA PHYs**
- Compliant with SATA II Phase 1 specifications
  - Supports SATA II Native Command Queuing (NCQ), up to 128 outstanding commands per port
  - First party DMA (FPDMA) full support
  - Backwards compatible with SATA I devices
- Supports SATA II Phase 2 advanced features
  - 3 Gbps SATA II speed
  - Port Multiplier (PM)—Performs FIS-Based Switching as defined in SATA working group PM definition
  - Port Selector (PS)—Issues the protocol-based OOB sequence to select the active host port
- Supports device 48-bit addressing
- Supports ATA Tag Command Queuing

- **SATA II Host controller**
  - Two SATA 2.0 ports
  - Enhanced-DMA [EDMA] for the SATA ports
  - Automatic command execution without host intervention
  - Command queuing support, for up to 128 outstanding commands
  - Separate SATA request/response queues
  - 64-bit addressing support for descriptors and data buffers in system memory
  - Read ahead
  - Advanced interrupt coalescing
  - Target mode operation—Two Marvell® devices can be attached through the SATA ports, enabling data communication between the MV78200 and another Marvell SATA device
  - Advanced drive diagnostics via the ATA SMART command
- **Cryptographic engine**
  - Hardware implementation on encryption and authentication engines to boost packet processing speed
  - Dedicated DMA to feed the hardware engines with data from the internal SRAM memory or from the DDR memory
  - Implements AES, DES, and 3DES encryption algorithms
  - Implements SHA1 and MD5 authentication algorithms
- **Four UART interfaces**
  - 16550 UART compatible
  - Each port has two pins for transmit and receive operations, and two pins for modem control functions
  - One channel also supports DMA
- **Time Division Multiplexing (TDM) Interface**
  - Generic interface to standard SLIC/Codec devices
  - Compatible with standard PCM highway formats
  - TDM protocol support for two channels, up to 128 time slots
  - SPI interface for codec registers read/write access
  - Integrated DMA to transfer voice data to/from memory buffer
- **Four Channel Independent DMA controller**
  - Chaining via linked-lists of descriptors
  - Moves data from any interface to any interface
  - DMA trigger by software or external hardware
  - Supports increment or hold on both Source and Destination Address
- **Two XOR DMAs**
  - Useful for RAID application
  - Supports XOR operation on up to eight source blocks
  - Supports also iSCSI CRC-32 calculation
- **Interrupt controller**
  Maskable interrupts to CPU core
  (and PCI Express in the case of PCI Express Endpoint)
- **Eight General Purpose 32-bit Timer/Counters**
- **SPI port**
  - General purpose SPI interface
  - Also support boot from SPI ROM
- **Two TWSI interfaces**
  General purpose TWSI master/slave
- **24 Multi-Purpose pins dedicated for peripheral functions and General Purpose I/O**
  - Each pin can be configured independently
  - GPIO inputs can be used to register interrupts from external devices, and to generate maskable interrupts
- **Clock Generation**
  - Supports internal generation of CPU core clock, DRAM clock, core clock, GbE clock, USB clock, and SATA clock from a single 25 MHz reference clock
  - Also supports spread spectrum reference clock
- **Power Down support**
  - Supports CPU Wait for Interrupt mode (shut down CPU core clock)
  - Selectable gating of clock trees of different interfaces
  - Supports DRAM self-refresh
  - Supports PCI-Express, USB, and SATA PHYs shut down
- **27 x 27 mm FCBGA package, 1mm ball pitch**

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Preface

About this Document

The *MV78200 Hardware Specifications* provides a features list, overview, pin description, ball map, and electrical specifications for the MV78200 device. This datasheet also includes information on configuration settings and physical specifications.

It is intended to be the basic source of information for designers of new systems.

In this document, the MV78200 is often referred to as “the device”.

Related Documentation

The following documents contain additional information related to the MV78200:

- *MV76100, MV78100, and MV78200 Functional Specification* (Doc. No. MV-S800598-U0)
- *MV76100, MV78100, and MV78200 Design Guide* (Doc. No. MV-S301291-00)[1]
- *TB-235: Differences Between the MV76100, MV78100, and MV78200 Revisions A0 and A1* (Doc. No. MV-S105821-00)[1]

See the Marvell® Extranet website for the latest product documentation.

1. This document is a Marvell proprietary confidential document requiring an NDA and can be downloaded from the Marvell Extranet.

Document Conventions

The following conventions are used in this document:

Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals #	An n letter at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated by angle brackets. Example: <RegInit> Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format. Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use. A lowercase <n> in angle brackets in a register indicates that there are multiple registers with this name. Example: Multicast Configuration Register<n>
Reset Values	Reset values have the following meanings: 0 = Bit clear 1 = Bit set
Abbreviations	Gb: gigabit GB: gigabyte Kb: kilobit KB: kilobyte Mb: megabit MB: megabyte
Numbering Conventions	Unless otherwise indicated, all numbers in this document are decimal (base 10). An 0x prefix indicates a hexadecimal number. An 0b prefix indicates a binary number.

1 Overview

The MV78200 device is part of the Discovery™ Innovation series CPU family. It provides a single-chip, high-performance, cost-effective solution for different types of applications, such as printers, routers, web switches, storage applications, and wireless infrastructure.

The MV78200 integrates two dual-issue, ARMv5 compatible CPUs, with integrated double-precision FPU, and 512 KB of L2 cache, for each of the cores. The MV78200 supports the following interfaces:

- 32-bit/64-bit DDR2 SDRAM interface with an additional 8-bit ECC option
- 8/16/32-bit device bus interface
- Two PCI Express x4 interfaces; each one can also act as four x1 interfaces
- Three USB 2.0 ports
- Two SATA II ports
- Four Gigabit Ethernet MACs

Additionally, the MV78200 integrates:

- A cryptographic hardware accelerator
- Two XOR DMA engines
- Four IDMA engines
- Four 16550 compatible UARTs; one interface can support DMA-based transmit
- A two channel SLIC/Codec TDM interface
- SPI port
- Two TWSI ports
- Eight general purpose timers/counters
- A watchdog timer
- An interrupt controller

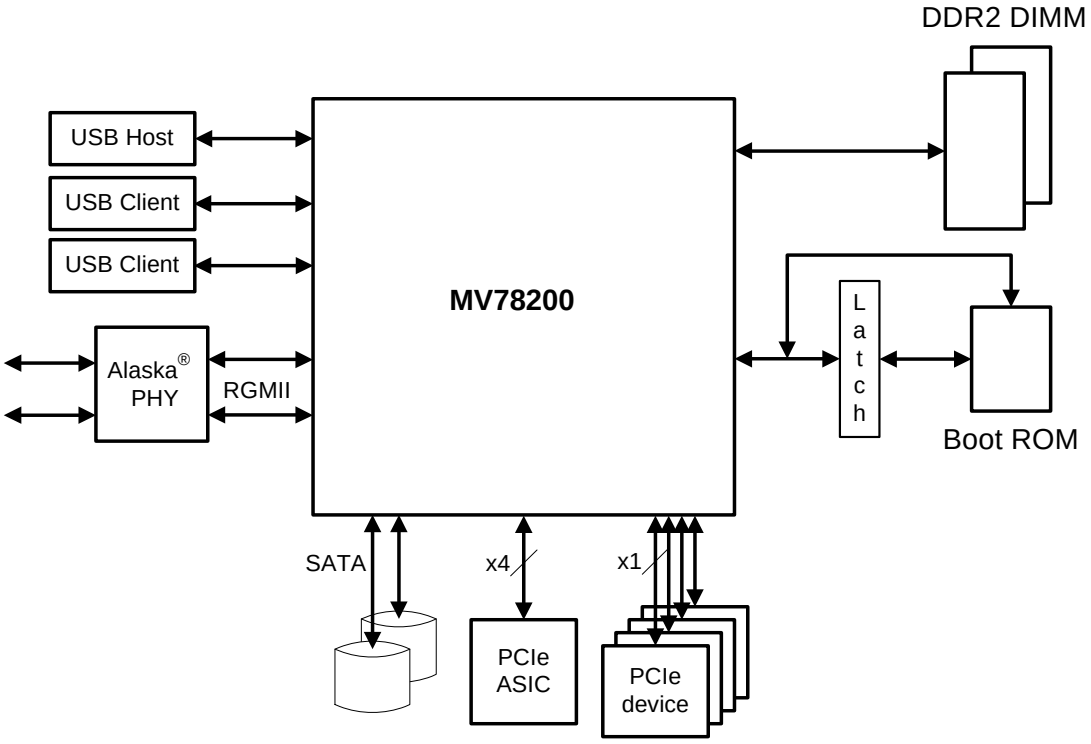
The MV78200 architecture is based on an Mbus fabric connecting all of the units. Each unit is connected to the Mbus via a full duplex 64-bit data path.

The Mbus architecture enables concurrency of transactions between multiple units, resulting in high accumulative throughput. It also supports split transactions with out-of-order completion.

For low latency CPU-to-DRAM access, the MV78200 also implements a dedicated point-to-point, 128-bit full duplex data path, between the ARM compliant CPU core and the DRAM controller. The CPU Bus Interface Unit (BIU) and DRAM controller complex run synchronously. This implementation guarantees minimum CPU-to-DRAM latency, which is critical in embedded applications.

A typical application is shown in Figure 1.

Figure 1: MV78200 Application Example

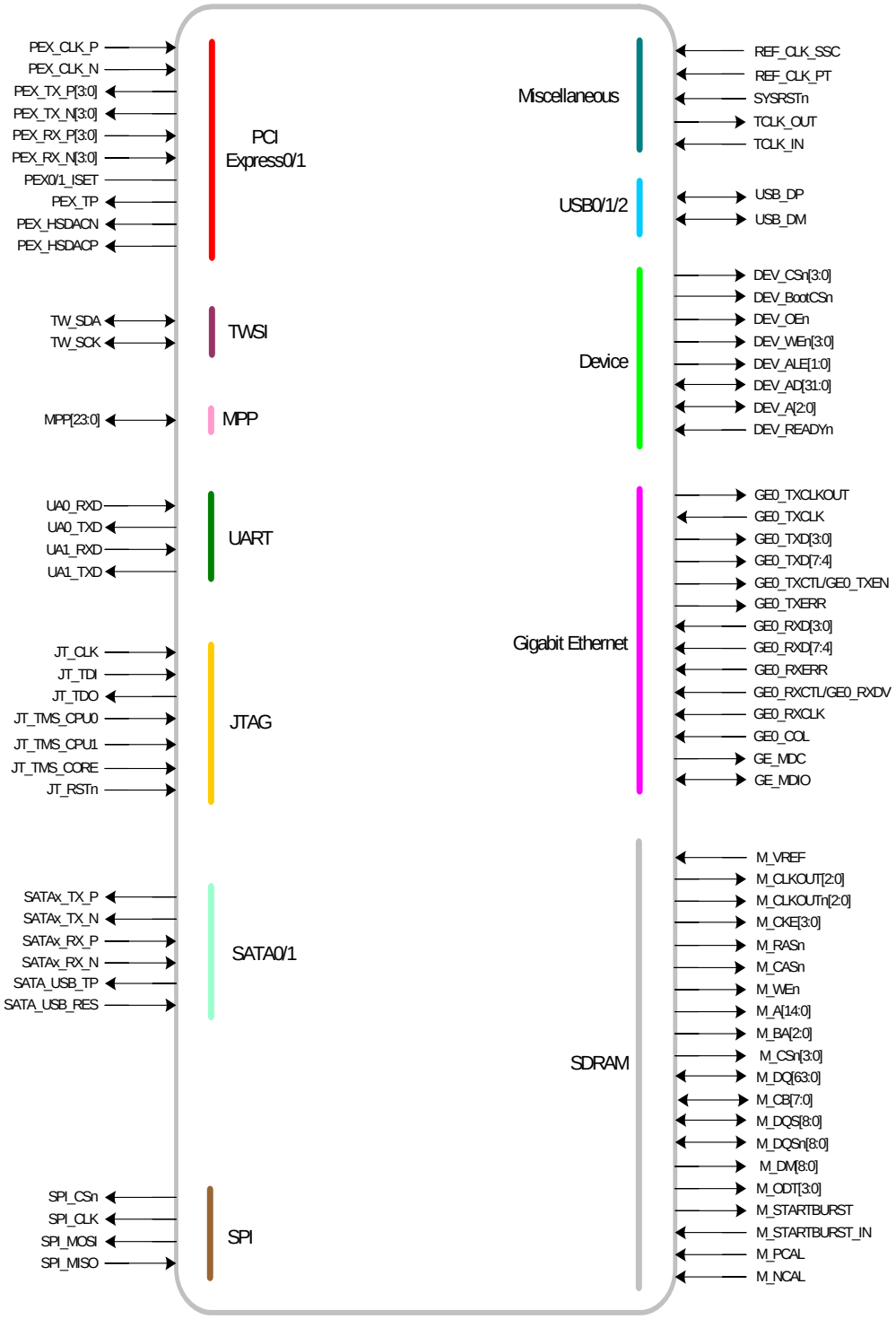


2 Pin Information

This section provides the pin logic diagram for MV78200 and a detailed description of the pin assignments and their functionality.

2.1 Pin Logic

Figure 2: MV78200 Interface Pin Logic Diagram



2.2 Pin Descriptions

This section details all the pins for the different interfaces providing a functional description of each pin and pin attributes.

Table 1 lists the conventions used to identify I/O or O type pins.

Table 1: Pin Functions and Assignments Table Key

Term	Definition
<n>	Represents port number
Analog	Analog Driver/Receiver or Power Supply
Calib	Calibration pad type
CML	Common Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
DDR	Double Data Rate
GND	Ground Supply
HCSL	High-speed Current Steering Logic
I	Input
I/O	Input/Output
O	Output
o/d	Open Drain pin The pin allows multiple drivers simultaneously (wire-OR connection). A pull-up is required to sustain the inactive value.
Power	VDD Power Supply
SDR	Single Data Rate
SSTL	Stub Series Terminated Logic for 1.8V
t/s	Tri-State pin
TS	Tri-State Value
XXXn	n - Suffix represents an Active Low Signal

Table 2: Interface Pin Prefixes

Interface	Prefix
DDR SDRAM	M_
PCI Express	PEX_
Gigabit Ethernet	GE_
USB 2.0	USB_
TWSI	TWSI_
SPI	SPI_

Table 2: Interface Pin Prefixes (Continued)

Interface	Prefix
UART	UA_
Device Bus	DEV_
MPP	N/A
JTAG	JT_
Misc	N/A
SATA	SATA_
TDM	TDM_

2.2.1 Power Supply Pins

Table 3 provides the voltage levels for the various interface pins. These also include the analog power supplies for the PLLs or PHYS.

Table 3: Power Supply Pins

Pin Name	Pin Type	Description
VDD_CPU0 VDD_CPU1	Power	1.1V CPU voltage
VDD	Power	1.0V core voltage
VDD_GE	Power	1.8V or 3.3V I/O supply voltage for the Ethernet interface (for the exact reset configuration, refer to Section 7.4, Pins Sample Configuration)
VDD_M	Power	1.8V I/O supply voltage for the DRAM interface
VDDO_A	Power	3.3V I/O supply voltage for the TWSI1, SPI, JTAG interfaces
VDDO_B	Power	1.8V or 3.3V I/O supply voltage for Device Bus[31:16], TWSI0 (for the exact reset configuration, refer to Section 7.4, Pins Sample Configuration)
VDDO_C	Power	1.8V or 3.3V I/O supply voltage for the Device Bus[15:0], Device Bus controls, MPP[23:12], UART, and system signals: • REF_CLK_SSC • REF_CLK_PT • SYSRSTn • TCLK_OUT • TCLK_IN (For the exact reset configuration, refer to Section 7.4, Pins Sample Configuration.)
VDDO_D	Power	1.8V or 3.3V I/O supply voltage for MPP[11:0] (for the exact reset configuration, refer to Section 7.4, Pins Sample Configuration)
VSS	GND	
PLL_AVDD	Power	PCLK PLL quiet power supply 1.8V **NOTE:** Implement the PLL filter as described in the *MV76100, MV78100, and MV78200 Design Guide*.
PLL_AVSS	GND	PCLK PLL quiet VSS **NOTE:** Implement the PLL filter as described in the *MV76100, MV78100, and MV78200 Design Guide*.
IREF_AVDD	Power	SATA and USB PHYs current source voltage filtered 1.8V **NOTE:** Implement the PLL filter as described in the *MV76100, MV78100, and MV78200 Design Guide*.
M_VREF	Power	SSTL Reference Voltage Reference voltage for SSTL interface, typically VDD_M/2. **Note**: See the *MV76100, MV78100, and MV78200 Design Guide* for the VREF recommended topology.
PEX0_AVDD PEX1_AVDD	Power	PCI Express PHY quiet power supply 1.8V. **NOTE:** See the *MV76100, MV78100, and MV78200 Design Guide* for power supply filtering recommendations.

Table 3: Power Supply Pins

Pin Name	Pin Type	Description
USB0_AVDD USB1_AVDD USB2_AVDD	Power	USB 2.0 PHY quiet 3.3V power supply. **NOTE:** See the *MV76100, MV78100, and MV78200 Design Guide* for power supply filtering recommendation.
SATA0_AVDD SATA1_AVDD	Power	SATA quiet 2.5V power supply **NOTE:** See *MV76100, MV78100, and MV78200 Design Guide* for power supply filtering recommendation.

2.2.2 Miscellaneous Pin Assignment

The Miscellaneous signal list contains clocks, reset, and PLL related signals.

Table 4: Miscellaneous Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
REF_CLK_SSC	I	CMOS	VDDO_C	25 MHz reference clock input for TCLK PLL and PCLK (CPU core, Mbus-L, and SDRAM clock) PLL. Supports a SSC source clock. **NOTE:** REF_CLK_SSC voltage swing is according to VDDO_C.
REF_CLK_PT	I	CMOS	VDDO_C	25 MHz reference clock input for USB 2.0 PHY, GbE interface, and SATA PHY. Must be a pure tone clock. **NOTES:** • If the SSC clock is not required, REF_CLK_PT can be configured via reset strapping to also drive the PCLK and TCLK PLLs. In this configuration, tie REF_CLK_SSC to VSS. • REF_CLK_PT voltage swing is according to VDDO_C.
SYSRSTn	I	CMOS	VDDO_C	System Reset Main reset signal of the device. Used to reset all units to their initial state. **NOTE:** For reset timing, see in the *MV76100, MV78100, and MV78200 Design Guide*.
SYSRST_OUTn	O	CMOS	See descrpition	Open Drain Reset Output Reset request from the device to the board reset logic. The power rail in use is determined by the MPP pin used for SYSRST_OUTn: • VDDO_B (DEV_AD[21], DEV_AD[24], DEV_AD[29], DEV_AD[30], DEV_AD[31]) • VDDO_C (MPP[13])
TCLK_OUT	O	CMOS	VDDO_C	TCLK PLL Output. **NOTES:** • TCLK_OUT pin can be configured to drive a clock running at 1:N of TCLK rate, rather than TCLK PLL output. • If using an external TCLK_IN core clock input rather than the internally generated TCLK, leave TCLK_OUT not connected. TCLK_OUT voltage swing is according to VDDO_C.
TCLK_IN	I	CMOS	VDDO_C	Core Clock Input (150 MHz–200 MHz). An alternative to the internally generated TCLK. De-skewed inside the chip to 0 skew between the input to the internal clock tree. Useful for high speed synchronous interface operation. **NOTES:** • If using the internally generated TCLK, connect TCLK_IN to VSS. • The TCLK_IN voltage swing is according to VDDO_C.
THERMAL_A THERMAL_C	I	Analog		Temperature diode anode/cathode THERMAL_A and THERMAL_C provide connectivity to the on-chip temperature diode that can be used to determine the die junction temperature. **NOTE:** When unused can be left unconnected.

Table 4: Miscellaneous Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
SATA_USB_TP	O	Analog		SATA and USB test point **NOTE:** Can be left unconnected.
SATA_USB_RES	I	Analog		Pull-down resistor for the SATA and USB reference current. 6.04 kilohm pull-down to VSS with resistor accuracy of 1%.

2.2.3 DDR SDRAM Interface Pin Assignments

Table 5: DDR SDRAM Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
M_CLKOUT[2:0] M_CLKOUTn[2:0]	O	SSTL	VDD_M	Three pairs of DRAM differential clocks. When not using all clock pairs use one of the following strapping configurations and register setting for the unused pair/s: • Leave the unused pair unconnected. In addition, for the unused pair, set <Clk1Drv> bit[12] or <Clk2Drv> bit[13] to 1 (driven normally), in the DDR Controller Control (Low) (Offset: 0x1404). • Connect the unused pair to pull down. In addition, for the unused pair, set <Clk1Drv> bit[12] or <Clk2Drv> bit[13] to 0 (high-z). **NOTE:** M_CLKOUT[0] and M_CLKOUTn[0] cannot be disabled and is always driven.
M_CKE[3:0]	O	SSTL	VDD_M	Driven by the MV78200 device high to enable DRAM clock. Driven low when setting the DRAM in self refresh mode. **NOTES:** • All four CKE pins are driven together (no separate self refresh per each DRAM bank). • When unused can be left unconnected.
M_RASn	O	SSTL	VDD_M	SDRAM Row Address Select Asserted to indicate an active ROW address driven on the SDRAM address lines.
M_CASn	O	SSTL	VDD_M	SDRAM Column Address Select Asserted to indicate an active column address driven on the SDRAM address lines.
M_WEn	O	SSTL	VDD_M	SDRAM Write Enable Asserted to indicate a write command to the SDRAM.
M_A[14:0]	O	SSTL	VDD_M	SDRAM Address Driven during RASn and CASn cycles to generate, together with the bank address bits, the SDRAM address.
M_BA[2:0]	O	SSTL	VDD_M	Driven by the MV78200 device during M_RASn and M_CASn cycles to select one of the eight DRAM virtual banks. **NOTE:** If an SDRAM device does not support the BA[2] pin, leave the M_BA[2] unconnected.
M_CSn[3:0]	O	SSTL	VDD_M	SDRAM Chip Selects Asserted to select a specific SDRAM bank. **NOTE:** When unused can be left unconnected.
M_DQ[63:0]	t/s I/O	SSTL	VDD_M	SDRAM Data Bus Driven during write to SDRAM. Driven by SDRAM during reads. **NOTE:** When configured to 32-bit mode, M_DQ[63:32] can be left unconnected.

Table 5: DDR SDRAM Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
M_CB[7:0]	t/s I/O	SSTL	VDD_M	DRAM ECC Driven by the MV78200 during write to SDRAM. Driven by SDRAM during reads. **NOTE:** When ECC is unused, leave M_CB[7:0] unconnected.
M_DQS[8:0], M_DQSn[8:0]	t/s I/O	SSTL	VDD_M	SDRAM Data Strobe Driven by the MV78200 during write to SDRAM. Driven by SDRAM during reads. **NOTES:** • When ECC is unused, leave M_DQS[8] unconnected. • When configured to 32-bit mode, M_DQS[7:4] and M_DQSn[7:4] can be left unconnected.
M_DM[8:0]	O	SSTL	VDD_M	SDRAM Data Mask Asserted by the MV78200 to select the specific bytes out of the 72-bit data/ECC to be written to the SDRAM. **NOTES:** • When ECC is unused, leave M_DM[8]/M_DQSn[8] unconnected. • When configured to 32-bit mode, M_DM[7:4] can be left unconnected.
M_ODT[3:0]	O	SSTL	VDD_M	SDRAM On Die Termination Control Driven by the MV78200 device high to connect DRAM on die termination, and low to disconnect the DRAM termination. **NOTES:** • For the recommended setting, refer to the *MV76100, MV78100, and MV78200 Design Guide*. • When unused can be left unconnected.
M_STARTBURST	O	SSTL	VDD_M	MV78200 indication of starting a burst. **NOTE:** For the exact length calculation for routing and termination requirements, see the *MV76100, MV78100, and MV78200 Design Guide*.
M_START BURST_IN	I	SSTL	VDD_M	M_STARTBURST signal routed back to MV78200. Used as a reference signal for the incoming read data driven by the SDRAM. **NOTE:** For the exact length calculation for routing and termination requirements, see the *MV76100, MV78100, and MV78200 Design Guide*.
M_BB	I	CMOS	VDDO_C	SDRAM battery backup trigger **NOTE:** This signal is multiplexed on the MPP pins, see Section 6, Pin Multiplexing, on page 48.
M_PCAL	I	Calib		DRAM interface signals P channel output driver calibration. Connect to VSS through a 35–70 Ω resistor. **NOTE:** See the *MV76100, MV78100, and MV78200 Design Guide* for the recommended values of the calibration resistors.

Table 5: DDR SDRAM Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
M_NCAL	I	Calib		DRAM interface signals N channel output driver calibration. Connect to VDD_M through a 35–70 Ω resistor.. **NOTE:** See the *MV76100, MV78100, and MV78200 Design Guide* for the recommended values of the calibration resistors.

2.2.4 Device Bus Interface Pin Assignments

Note

If using a 16-bit Device Bus, DEV_AD[23:16] and DEV_WEn[3:2] can be used for pins multiplexing (as MPP pins). If using an 8-bit Device Bus also DEV_AD[15:9] and DEV_WEn[1] can be used for pins multiplexing (see Section 6, Pin Multiplexing, on page 48 for more details).

NAND Flash interface signals are multiplexed on the Device Bus interface and on MPP pins. Refer to the NAND Flash section in the *MV76100, MV78100, and MV78200 Functional Specifications* for more information.

Table 6: Device Bus Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
DEV_CSn[3:0]	O	CMOS	VDDO_C	Device Bus Chip Select corresponds to Bank [3:0]. **NOTE:** These pins have internal pullup resistors.
DEV_BootCSn	O	CMOS	VDDO_C	Device Bus Boot Chip Select corresponds to Boot Bank. **NOTE:** This pin has an integrated pullup resistor.
DEV_OEn/ DEV_A[15]	O	CMOS	VDDO_C	Device Bus Output Enable **NOTE:** This pin has an integrated pullup resistor.
				Used as DEV_A[15] (device address bus) during first ALE cycle (DEV_ALE[1]).
DEV_WEn[3:0]/ DEV_A[16]	O	CMOS	VDDO_C	Device Bus Byte Write Enable (bit per byte) **NOTE:** These pins have integrated pullup/pulldown resistors. See details in Table 28, Reset Configuration, on page 56.
				DEV_WEn[0] is used as DEV_A[16] (device address bus) during first ALE cycle (DEV_ALE[1]).
DEV_ALE[1:0]	O	CMOS	VDDO_C	Device Bus Address Latch Enable **NOTE:** These pins have integrated pullup/pulldown resistors. See details in Table 28, Reset Configuration, on page 56.
DEV_AD[7:0]/ DEV_A[13:6]/ DEV_A[26:19]	t/s I/O	CMOS	VDDO_C	Used as DEV_AD[7:0] (device data bus) during the data phase. Driven by MV78200 on write access, and by the device on read access. **NOTE:** These pins have integrated pullup/pulldown resistors. See details in Table 28, Reset Configuration, on page 56.
				Used as DEV_A[13:6] (device address bus) during first ALE cycle (DEV_ALE[1]).
				Used as DEV_A[26:19] (device address bus) during second ALE cycle (DEV_ALE[0]).

Table 6: Device Bus Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
DEV_AD[15:8]/ DEV_A[14]/ DEV_A[15])	t/s I/O	CMOS	VDDO_C	Used as DEV_AD[15:8] (device data bus) during the data phase. Driven by MV78200 on write access, and by the device on read access. **NOTE:** These pins have integrated pullup/pulldown resistors. See details in Table 28, Reset Configuration, on page 56.
				DEV_AD[8] is used as DEV_A[14] (device address bus) during first ALE cycle (DEV_ALE[1]).
				DEV_AD[8] is used as DEV_A[15] (device address bus) during second ALE cycle (DEV_ALE[0]).
DEV_AD[31:16]	t/s I/O	CMOS	VDDO_B	Used as DEV_AD[31:16] (device data bus) during the data phase. Driven by MV78200 on write access, and by the device on read access. **NOTE:** When using Device Bus as a 8/16b interface, DEV_AD[23:16] can be used for other functions. See Section 6, Pin Multiplexing. These pins have integrated pullup/pulldown resistors. See details in Table 28, Reset Configuration, on page 56.
DEV_A[2:0]/ DEV_A[5:3]/ DEV_A[18:16]	t/s I/O	CMOS	VDDO_C	Device Bus Address Bus Used as DEV_A[2:0] during the data phase. DEV_A[2:0] is not latched, but connected directly to the device. It is an incrementing address in case of burst access. **NOTE:** These pins have integrated pullup/pulldown resistors. See details in Table 28, Reset Configuration, on page 56.
				Device Bus Address Used as DEV_A[5:3] during the first ALE cycle (DEV_ALE[1]).
				Device Bus address Used as DEV_A[18:16] during the second ALE cycle (DEV_ALE[0]).
DEV_READYn	I	CMOS	VDDO_C	Device READY Used as cycle extender when interfacing a slow device. **NOTE:** When inactive during a device access, access is extended until DEV_READYn assertion. This pin has an integrated pulldown resistor.
DEV_BURSTn/ DEV_LASTn	O	CMOS	VDDO_C	Device Burst/Device Last

2.2.5 PCI Express Interface Pin Assignments

Table 7: PCI Express Port 0/1 Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
Port0				
PEX0_CLK_P PEX0_CLK_N	I	HCSL	PEX0_AVDD	PCI Express Port0 Reference Clock Input 100 MHz, differential pair
PEX0_TX<n>_P[1] PEX0_TX<n>_N	O	CML	PEX0_AVDD	Port0 Transmit Lane 0/1/2/3 Differential pair of PCI Express transmit data
PEX0_RX<n>_P PEX0_RX<n>_N	I	CML	PEX0_AVDD	Port0 Receive Lane 0/1/2/3 Differential pair of PCI Express receive data
PEX0_ISET		Analog		Reference Current 4.99 kilohm pull-down to VSS with resistor accuracy of 1%.
Port1				
PEX1_CLK_P PEX1_CLK_N	I	HCSL	PEX1_AVDD	PCI Express Port1 Reference Clock Input 100 MHz, differential pair
PEX1_TX<n>_P[1] PEX1_TX<n>_N	O	CML	PEX1_AVDD	Port1 Transmit Lane 0/1/2/3 Differential pair of PCI Express transmit data
PEX1_RX<n>_P PEX1_RX<n>_N	I	CML	PEX1_AVDD	Port1 Receive Lane 0/1/2/3 Differential pair of PCI Express receive data
PEX1_ISET		Analog		Reference Current 4.99 kilohm pull-down to VSS with resistor accuracy of 1%.

1. This port contains four lanes. It can be configured to x4 or to Quad x1. For details on this port's configuration, see Table 28, Reset Configuration, on page 56.

Table 8: PCI Express Common Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
PEX_TP	O	Analog		Analog Test Point Test point signals should be left unconnected
PEX_HSDACP PEX_HSDACN	O	CML		High Speed DAC **NOTE:** See the *MV76100, MV78100, and MV78200 Design Guide* for the recommended connectivity.

2.2.6 Gigabit Ethernet Port Interface Pin Assignments

Note

Some GbE interface pins are connected to the VDD_GE power rail and some pins are connected to the VDDO_D power rail.

Table 9: Gigabit Ethernet Port Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
GE0_TXCLKOUT	t/s O	CMOS	VDD_GE	RGMII Transmit Clock RGMII transmit reference output clock for GE0_TXD[3:0] and GE0_TXCTL Provides 125 MHz, 25 MHz or 2.5 MHz clock. Not used in MII mode.
				GMII Transmit Clock Provides the timing reference for the transfer of the GE0_TXEN, GE0_TXERR, and GE0_TXD[7:0] signals. This clock operates at 125 MHz.
GE0_TXCLK	I	CMOS	VDD_GE	MII Transmit Clock MII transmit reference clock from PHY. Provides the timing reference for the transmission of the GE0_TXEN, GE0_TXERR, and GE0_TXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.
GE0_TXD[3:0]	t/s O	CMOS	VDD_GE	RGMII Transmit Data Contains the transmit data nibble outputs that run at double data rate with bits [3:0] presented on the rising edge of GE0_TXCLKOUT and bits [7:4] presented on the falling edge. **NOTE:** These pins have integrated pullup/pulldown resistors. See details in Table 28, Reset Configuration, on page 56.
				MII Transmit Data Contains the transmit data nibble outputs that are synchronous to the GE0_TXCLK input.
				GMII Transmit Data Contains the transmit data nibble outputs that are synchronized to GE0_TXCLKOUT.
GE0_TXD[7:4]	t/s O	CMOS	VDDO_D	GMII Transmit Data Contains the transmit data nibble outputs that are synchronized to GE0_TXCLKOUT. **NOTE:** Multiplexed on MPP.

Table 9: Gigabit Ethernet Port Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
GE0_TXCTL/ GE0_TXEN	t/s O	CMOS	VDD_GE	RGMII Transmit Control Transmit control synchronous to the GE0_TXCLKOUT output rising/falling edge. GE0_TXCTL is presented on the rising edge of GE0_TXCLKOUT. A logical derivative of GE0_TXEN and GE0_TxER is presented on the falling edge of GE0_TXCLKOUT. **NOTE:** Internally pulled down to 0x0.
				MII Transmit Enable Indicates that the packet is being transmitted to the PHY. It Is synchronous to GE0_TXCLK.
				GMII Transmit Enable Indicates that the packet is being transmitted to the PHY. It Is synchronous to GE0_TXCLKOUT.
GE0_TXERR	t/s O	CMOS	VDDO_D	MII Transmit Error It is synchronous to GE0_TXCLK. **NOTE:** Multiplexed on MPP.
				GMII Transmit Error It Is synchronous to GE0_TXCLKOUT. **NOTE:** Multiplexed on MPP.
GE0_CRS	I	CMOS	VDDO_D	MII Carrier Sense Indicates that the receive medium is non-idle. In half-duplex mode, GE0_CRS is also asserted during transmission. GE0_CRS is not synchronous to any clock. **NOTE:** Multiplexed on MPP.
				GMII Carrier Sense **NOTE:** Multiplexed on MPP.
GE0_RXD[3:0]	I	CMOS	VDD_GE	RGMII Receive Data Contains the receive data nibble inputs that are synchronous to GE0_RXCLK input rising/falling edge.
				MII Receive Data Contains the receive data nibble inputs that are synchronous to GE0_RXCLK input.
				GMII Receive Data Contains the receive data nibble inputs that are synchronous to GE0_RXCLK input.
GE0_RXD[7:4]	I	CMOS	VDDO_D	GMII Receive Data Contains the receive data nibble inputs that are synchronous to GE0_RXCLK input. **NOTE:** Multiplexed on MPP.

Table 9: Gigabit Ethernet Port Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
GE0_RXERR	I	CMOS	VDDO_D	MII Receive Error Indicates that an error symbol, a false carrier, or a carrier extension symbol is detected on the cable. It is synchronous to GE0_RXCLK input. **NOTE:** Multiplexed on MPP.
				GMII Receive Error It is synchronous to GE0_RXCLK input. **NOTE:** Multiplexed on MPP.
GE0_RXCTL/ GE0_RXDV	I	CMOS	VDD_GE	RGMII Receive Control GE0_RXCTL is presented on the rising edge of GE0_RXCLK. A logical derivative of GE0_RXDV and GE0_RXERR is presented on the falling edge of RXCLK.
				MII Receive Data Valid Indicates that valid data is present on the GE0_RXD lines. It is synchronous to GE0_RXCLK.
				GMII Receive Data Valid It is synchronous to GE0_RXCLK input.
GE0_RXCLK	I	CMOS	VDD_GE	RGMII Receive Clock The receive clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock derived from the received data stream.
				MII Receive Clock Provides the timing reference for the reception of the GE0_RXDV, GE0_RXERR, and GE0_RXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.
				GMII Receive Clock Provides the timing reference for the reception of the GE0_RXDV, GE0_RXERR, and GE0_RXD[7:0] signals. This clock operates at 125 MHz.
GE0_COL	I	CMOS	VDDO_D	MII Collision Detect Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode. GE0_COL is not synchronous to any clock. **NOTE:** If not using the MII interface, this pin must be left unconnected. Multiplexed on MPP.
GE_MDC	t/s O	CMOS	VDD_GE	Management Data Clock MDC is derived from TCLK divided by 128. Provides the timing reference for the transfer of the MDIO signal.
GE_MDIO	t/s I/O	CMOS	VDD_GE	Management Data In/Out Used to transfer control information and status between PHY devices and the GbE controller. **NOTE:** A 2 kilohm pullup resistor is required.

Note GE0_TXD[7:4], GE0_RXD[7:4], GE0_TXERR, GE0_RXERR, GE0_CRS, and GE0_COL are multiplexed on MPP pins. Also, GbE ports 1 and 2 are multiplexed on MPP pins. GbE port 3 is multiplexed on the Device bus pins. See Section 6, Pin Multiplexing, on page 48.

2.2.7 USB 2.0 Port Interface Pin Assignments

Table 10: USB 2.0 Ports 0/1/2 Interface Pin Assignments

Pin Name	I/O / Pin Type		Power Rails	Description
Where <n> represents USB Port0, Port1, or Port2.				
USB<n>_DP USB<n>_DM	I/O	CML	USB0/1/2 _AVDD	USB 2.0 Port0/1/2 data+ and data- pair

2.2.8 SATA II Port Interface Pin Assignments

Table 11: SATA II Port 0/1 Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rails	Description
Port0				
SATA0_TX_P SATA0_TX_N	O	CML	SATA0_ AVDD	Transmit data: Differential analog output of SATA II Port0
SATA0_RX_P SATA0_RX_N	I	CML	SATA0_ AVDD	Receive data: Differential analog input of SATA II Port0
SATA0_ PRESENTn	O	CMOS	VDDO_C	When this signal is asserted there is an active link between the SATA II port and the external device (disk). **NOTE:** This signal is multiplexed on the MPP pins, see Section 6, Pin Multiplexing, on page 48.
SATA0_ACTn	O	CMOS	VDDO_C	When this signal is asserted, there is an active and used link between the SATA II port and the external device (disk). **NOTE:** This signal is multiplexed on the MPP pins, see Section 6, Pin Multiplexing, on page 48.
Port1				
SATA1_TX_P SATA1_TX_N	O	CML	SATA1_ AVDD	Transmit data: Differential analog output of SATA II Port1
SATA1_RX_P SATA1_RX_P	I	CML	SATA1_ AVDD	Receive data: Differential analog input of SATA II Port1
SATA1_ PRESENTn	O	CMOS	VDDO_C	When this signal is asserted there is an active link between the SATA II port and the external device (disk). **NOTE:** This signal is multiplexed on the MPP pins, see Section 6, Pin Multiplexing, on page 48.
SATA1_ACTn	O	CMOS	VDDO_C	When this signal is asserted, there is an active and used link between the SATA II port and the external device (disk). **NOTE:** This signal is multiplexed on the MPP pins, see Section 6, Pin Multiplexing, on page 48.

2.2.9 TWSI Interface Pin Assignment

Table 12: TWSI Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rails	Description
TWSI0_SDA	o/d I/O	CMOS	VDDO_B	TWSI port0 SDA Address or write data driven by the TWSI master or read response data driven by the TWSI slave. **NOTE:** Requires a pullup resistor to VDDO_B.
TWSI0_SCK	o/d I/O	CMOS	VDDO_B	TWSI port0 Serial Clock Serves as output when acting as an TWSI master. Serves as input when acting as an TWSI slave. **NOTE:** Requires a pullup resistor to VDDO_B.
TWSI1_SDA	o/d I/O	CMOS	VDDO_A	TWSI port1 SDA Address or write data driven by the TWSI master or read response data driven by the TWSI slave. **NOTE:** Requires a pull-up 4.7 kΩ resistor to VDDO_A.
TWSI1_SCK	o/d I/O	CMOS	VDDO_A	TWSI port1 Serial Clock Serves as output when acting as an TWSI master. Serves as input when acting as an TWSI slave. **NOTE:** Requires a pull-up 4.7 kΩ resistor to VDDO_A.

2.2.10 SPI Interface Pin Assignment

Table 13: SPI Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rails	Description
SPI_CSn	O	CMOS	VDDO_A	SPI chip select
SPI_CLK	O	CMOS	VDDO_A	SPI clock
SPI_MOSI	O	CMOS	VDDO_A	SPI data output
SPI_MISO	I	CMOS	VDDO_A	SPI data input

2.2.11 UART Interface Pin Assignment

Table 14: UART 0/1/2/3 Interfaces Pin Assignments

Pin Name	I/O	Pin Type	Power Rails	Description
UA0_RXD UA1_RXD	I	CMOS	VDDO_C	UART0/1 RX Data
UA0_TXD UA1_TXD	O	CMOS	VDDO_C	UART0/1 TX Data
UA0_CTSn UA1_CTSn	I	CMOS	VDDO_C	UART0/1 Clear To Send **NOTE:** Multiplexed on MPP.
UA0_RTSn UA1_RTSn	O	CMOS	VDDO_C	UART0/1 Request To Send **NOTE:** Multiplexed on MPP.
UA2_RXD UA3_RXD	I	CMOS	VDDO_C or VDDO_B	UART2/3 RX Data **NOTE:** Multiplexed on MPP.
UA2_TXD UA3_TXD	O	CMOS	VDDO_C or VDDO_B	UART2/3 TX Data **NOTE:** Multiplexed on MPP.
UA2_CTSn UA3_CTSn	I	CMOS	VDDO_C or VDDO_B	UART2/3 Clear To Send **NOTE:** Multiplexed on MPP.
UA2_RTSn UA3_RTSn	O	CMOS	VDDO_C or VDDO_B	UART2/3 Request To Send **NOTE:** Multiplexed on MPP.

Note

For the UART pins that are multiplexed, see Section 6, Pin Multiplexing, on page 48 for details.

2.2.12 TDM Interface Pin Assignment

Note According to the pin multiplexing setting (see Table 26, MPP Function Summary, on page 49), the power rails for the TDM pins can be VDDO_B or VDDO_C.

Table 15: TDM Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rails	Description
TDM_INTn	I	CMOS	VDDO_B or VDDO_C	Interrupt input from the SLIC device **NOTE:** Multiplexed on MPP.
TDM_RSTn	O	CMOS	VDDO_B or VDDO_C	SLIC reset input Driven by the MV78200. **NOTE:** Multiplexed on MPP.
TDM_PCLK	I/O	CMOS	VDDO_B or VDDO_C	PCM audio bit clock Driven by the MV78200 if configured as PCLK master. Input to MV78200 (driven by the SLIC device) if configured as PCLK slave. **NOTE:** Multiplexed on MPP.
TDM_FSYNC	I/O	CMOS	VDDO_B or VDDO_C	Frame Sync signal Driven by the MV78200 if configured as FSYNC master. Input to MV78200 (driven by the SLIC device) if configured as FSYNC slave. **NOTE:** Multiplexed on MPP.
TDM_DRX	I	CMOS	VDDO_B or VDDO_C	PCM audio input data **NOTE:** Multiplexed on MPP.
TDM_DTX	O	CMOS	VDDO_B or VDDO_C	PCM audio output data **NOTE:** Multiplexed on MPP.
TDM0_RXQ TDM1_RXQ	O	CMOS	VDDO_B or VDDO_C	TDM channel0/1 Rx qualifier Driven by MV78200 to the SLIC device. Useful when interfacing with a SLIC device that does not support time slot multiplexing (indicates the exact time slot in which the SLIC device should drive PCM data on TDM_DRX). **NOTE:** Multiplexed on MPP.
TDM0_TXQ TDM1_TXQ	O	CMOS	VDDO_B or VDDO_C	TDM channel0/1 Tx qualifier Driven by MV78200 to the SLIC device. Useful when interfacing with a SLIC device that does not support time slot multiplexing (indicates the exact time slot in which the SLIC device should sample PCM data on TDM_DTX). **NOTE:** Multiplexed on MPP.

Table 15: TDM Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rails	Description
TDM0_SCSn TDM1_SCSn	O	CMOS	VDDO_B or VDDO_C	SPI chip select0/1 Driven by MV78200 to the SLIC device. Useful when the MV78200 interfaces two SLIC devices and uses two SPI chip select signals (one to each SLIC device) rather than chaining of the devices. **NOTE:** Multiplexed on MPP.
TDM_SCLK	O	CMOS	VDDO_B or VDDO_C	SPI clock Driven by the MV78200 to the SLIC device. **NOTE:** Multiplexed on MPP.
TDM_SMOSI	O	CMOS	VDDO_B or VDDO_C	SPI write data Driven by the MV78200 to the SLIC device. **NOTE:** Multiplexed on MPP.
TDM_SMISO	I	CMOS	VDDO_B or VDDO_C	SPI read data Driven by the SLIC device to the MV78200 **NOTE:** Multiplexed on MPP.

Note

The SLIC device has a dedicated SPI interface for SLIC registers access. This is not the MV78200 SPI interface listed in Section 2.2.10, SPI Interface Pin Assignment, on page 36.

2.2.13 MPP Interface Pin Assignment

Table 16: MPP Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rails	Description
MPP[11:0]	t/s I/O	CMOS	VDDO_D	Multi Purpose Pin Various functionalities **NOTE:** These pins have internal pullup resistors.
MPP[23:12]	t/s I/O	CMOS	VDDO_C	Multi Purpose Pin Various functionalities **NOTE:** These pins have internal pullup resistors.

2.2.14 JTAG Interface Pin Assignment

Table 17: JTAG Pin Assignments

Pin Name	I/O	Pin Type	Power Rails	Description
JT_CLK	I	CMOS	VDDO_A	JTAG Clock Clock input for the JTAG controller. **NOTE:** This pin is internally pulled down to 0.
JT_RSTn	I	CMOS	VDDO_A	JTAG Reset When asserted, resets the JTAG controller. **NOTE:** This pin is internally pulled down to 0.[1]
JT_TMS_CPU0 JT_TMS_CPU1	I	CMOS	VDDO_A	CPU0/1 JTAG Mode Select Controls CPU0 JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TMS_CORE	I	CMOS	VDDO_A	Core JTAG Mode Select Controls the Core JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TDO	O	CMOS	VDDO_A	JTAG Data Out Driven on the falling edge of JT_CLK.
JT_TDI	I	CMOS	VDDO_A	JTAG Data In JTAG serial data input. Sampled with the JT_CLK rising edge. **NOTE:** This pin is internally pulled up to 1.

1. If this pull-down conflicts with other devices, the JTAG tool must not use this signal. This signal is not mandatory for the JTAG interface, since the TAP (Test Access Port) can be reset by driving the JT_TMS signal HIGH for 5 JT_CLK cycles. If JT_RSTn is not used it should be connected to reset signal. Otherwise the internal pull down will keep the TAP controller in reset.

3 Unused Interface Strapping

Table 18 lists the signal strapping for systems in which some of the MV78200 interfaces are unused, not connected.

Table 18: Unused Interface Strapping

Unused Interface	Strapping
Ethernet RGMII	If not using Port0, use a 1–4.7 kilohm pull down for the following signals: GE0_TXCLK, GE0_RXCLK, GE0_RXD[3:0], GE0_RXDV
Ethernet SMI	GE_MDIO must be 2 kilohm pulled up.
TWSI	TWSI0_SCK and TWSI0_SDA must be pulled up through a 1–4.7 kilohm resistor to VDDO_B. TWSI1_SCK and TWSI1_SDA must be pulled up through a 1–4.7 kilohm resistor to VDDO_A.
Device	VDDO_B and VDDO_C power balls must be connected to 3.3V or to 1.8V according to the corresponding reset strap setting.
USB	Discard the power filter. Leave USBx_AVDD connected to 3.3V. All other signals can be left unconnected.
PCI Express 0	Configure it to x4 reset_sampling Dev_AD[3] = 0. Discard the analog power filters. Connect PEX1_AVDD to VDD (1V), to save power suppliers. Pull down the PEX0_CLK_N signal through a 50 kilohm resistor to GND. Pull up the PEX0_CLK_P signal through a 16 kilohom resistor to VDD. All other signals can be left unconnected.
PCI Express 1	Configure it to X4 reset sampling DEV_AD[4] = 0. Discard the analog power filters. Connect PEX1_AVDD to VDD (1V),, to save power suppliers. Pull down the PEX1_CLK_N signal through a 50 kilohm resistor to GND. Pull up the PEX1_CLK_P signal through a 16 kilohm to VDD. All other signals can be left unconnected.
SATA	Discard the analog power filters and connect it to VDD (1V) Connect the SATA_USB_RES to 6.04 kilohm resistor to pull down. All other signals can be left unconnected.

4 MV78200 Pin Map and Pin List

Note The attached pin maps and pin lists are PRELIMINARY and SUBJECT TO CHANGE.

The MV78200 pin list is provided as an Excel file attachment.

To open the attached Excel pin list file, double-click the pin icon below:

MV78200 Pinout

Note File attachments are only supported by Adobe Reader 6.0 and above.
To download the latest version of free Adobe Reader go to http://www.adobe.com.

5 Clocking

5.1 Clock Domains

The MV78200 device has multiple clock domains:

- Sheeva™ PCLK0, PCLK1: Sheeva™ CPUs clocks—up to 1 GHz
- HCLK: The Sheeva™ CPU bus (MbusL) clock. Also used as the DRAM interface clock—up to 400 MHz
- TCLK: The MV78200 core clock, also used as the reference clock for the MV78200 device bus. Runs at 166 MHz or 200 MHz.
- PCI-Express clock: Runs at 250 MHz
- GbE ports clock: 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps operation
- SATA clock: Runs at 150 Mhz
- USB clock: Runs at 480 MHz
- UART clock. Up to TCLK frequency divided by 16
- SPI clock: Up to 50 MHz
- TWSI clock: Up to 100 kHz

The supported PCLK to HCLK clock ratios are 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, and 5 determined via reset strapping. Table 19 summarizes the possible frequencies.

Table 19: HCLK and PCLK0 Frequencies

HCLK/Ratio	1	1.5	2	2.5	3	3.5	4	4.5	5
200	NA	NA	400	500	600	700	800	900	1000
250	NA	NA	500	625	750	875	1000	NA	NA
267	NA	400	533	667	800	933	NA	NA	NA
300	NA	450	600	750	900	NA	NA	NA	NA
333	NA	500	667	833	1000	N/A	N/A	NA	NA
400	400	600	800	1000	NA	NA	NA	NA	NA

Table 20: CPU1 Frequencies for HCLK = 200 MHz

CPU0	CPU1
400	400, 500, 600, 800, 1000
500	500, 1000
600	400, 600, 800

Table 20: CPU1 Frequencies for HCLK = 200 MHz (Continued)

CPU0	CPU1
700	700
800	400,600, 800
900	900
1000	400, 500, 1000

Table 21: CPU1 Frequencies for HCLK = 250 MHz

CPU0	CPU1
500	500, 750, 1000
625	625
750	375, 500, 750
875	875
1000	500, 1000

Table 22: CPU1 Frequencies for HCLK = 267 MHz

CPU0	CPU1
400	400
533	533
667	667
800	400, 800
933	933

Table 23: CPU1 Frequencies for HCLK = 300 MHz

CPU0	CPU1
450	450, 600, 900
600	450, 600, 900
750	750
900	450, 600, 900

Table 24: CPU1 Frequencies for HCLK = 333 MHz

CPU0	CPU1
500	500, 667, 1000
667	500, 667, 1000
833	833
1000	500, 667, 1000

Table 25: CPU1 Frequencies for HCLK = 400 MHz

CPU0	CPU1
400	400, 600, 800
600	400, 600, 800
800	400, 600, 800
1000	1000

5.2 PLLs and Clock Pins

The MV78200 has the following on-chip PLLs:

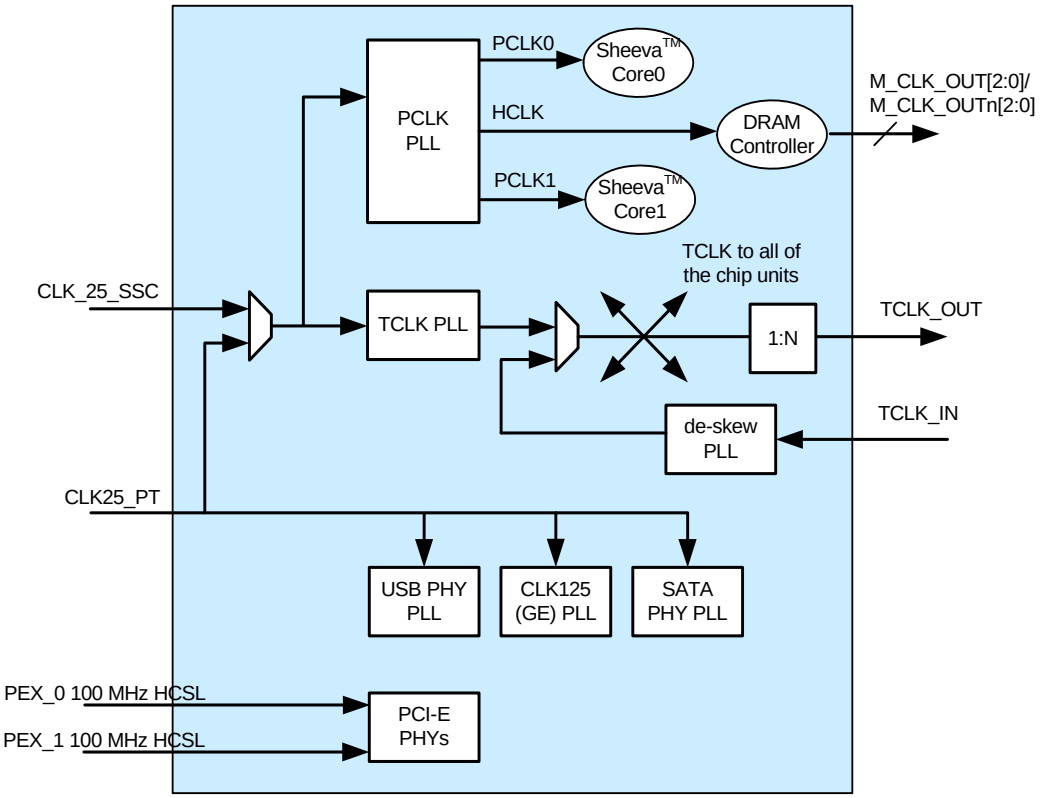
- PCLK PLL—Generates PCLK/1 (Sheeva™ core clocks) and HCLK (Sheeva™ bus and SDRAM I/F clock)
- TCLK PLL—Generates the internal core frequency
- GE_CLK125 PLL—Generates 125 MHz reference clock for the GbE MAC
- PCI Express PHY PLL
- USB PHY PLL
- SATA PHY PLL

Note

The different MV78200 PLLs require dedicated quiet power supplies (AVDD/AVSS). See the *MV76100, MV78100, and MV78200 Design Guide* for a detailed description of these power supplies and required power filtering.

The MV78200 clocking scheme is shown in Figure 3.

Figure 3: MV78200 Clocks



The MV78200 supports generation of PCLK, HCLK, and TCLK from a 25 MHz input clock CLK25_SSC. This clock can be generated by a spread spectrum clock generator (SSCG) under the following restrictions:

- Spread does not exceed -0.5% of the maximum frequency.
- The modulation frequency does not exceed 33 KHz.

The PLLs using this clock source track the spread characteristics of the input clock (meaning TCLK, PCLK, HCLK, and M_CLK_OUT also become spread spectrum clocks).

There is a single PCLK PLL that generates PCLK0 (CPU0 clock), PCLK1 (CPU1 clock) and HCLK (CPU bus clock which is also DRAM clock). All three clocks are synchronous to each other (edge aligned), resulting in low latency CPU to DRAM path (no synchronization required).

The CPU L2 cache clock (named XPCLK) runs relative to the CPU PCLK, with the ratio determined by the reset configuration.

The CPU can be placed in "wait for interrupt" mode. In this mode, most of the PCLK clock tree is turned off (only wake-up logic is kept alive).

The TCLK clock tree can be generated from one of two sources:

- TCLK PLL (selectable 166 MHz or 200 MHz operation)
- From external TCLK_IN input. In this mode, clock input is de-skewed to have zero skew to the external clock input. This mode is useful when using the chip device bus as a high speed synchronous interface (better AC timing)

The MV78200 drives TCLK clock tree output on TCLK_OUT pin. The device can also configured to drive a divided (1:N) TCLK on TCLK_OUT pin.

The TCLK clock tree to each of the MV78200 units can be gated via register. This is useful for power saving modes, when most of the chip interfaces are not in use. See the Power Saving section in the Functional Specification for further details.

A second 25 MHz input clock, CLK25_PT, is used as a reference clock for the USB PHY PLL, for the CLK125 PLL, and for the SATA PHY PLL. This clock must be pure tone.

Note

- If the SSC clock is not required, CLK25_PT can be configured via reset strapping to also drive the PCLK and TCLK PLLs, as shown in Figure 3, MV78200 Clocks, on page 46. If using this configuration, tie CLK25_SSC to VSS via a pull down resistor.
- The MV78200 SATA PHY generates an SSC signal on its output (TX_P/TX_N) and tolerates an SSC signal on its input (RX_P/RX_N), as defined in the SATA specification.

The PCI Express PHY receives a 100 MHz reference clock. It generates two clocks:

- A 250 MHz PCLK used by the PCI Express unit (transaction layer, link layer, and PHY MAC layer)
- A 2.5 GHz clock for the PHY analog part.

The PCI Express PLL also tolerates a spread spectrum reference clock, as defined by the PCI Express specification:

- Spread of -0.5% of the maximum frequency
- The modulation frequency does not exceed 33 kHz

6 Pin Multiplexing

6.1 MPP Multiplexing

The MV78200 device contains 24 Multi Purpose Pins (MPP). When using the device bus as a 16-bit interface, DEV_AD[31:16] and DEV_WEn[3:2] are also used for pins multiplexing, resulting in a total of 42 pins. When using 8-bit device bus, DEV_AD[15:9] and DEV_WEn[1] are also used for pins multiplexing, resulting in total of 50 pins.

Each pin can be assigned to a different functionality through the MPP Control register.

- GPIO: General Purpose In/Out Port, 32 GPIOs available—see the General Purpose I/O Port section in the *MV76100, MV78100, and MV78200 Functional Specification.*
- GE0_TXD[7:4], GE0_RXD[7:4], GE0_TXER, GE0_RXER, GE0_CRS, GE0_COL: GbE port0 Signals when configured to MII or GMII interface—see the Gigabit Ethernet Controller section in the *MV76100, MV78100, and MV78200 Functional Specification*.
- GEx_TXD[3:0], GEx_RXD[3:0], GEx_TXCLKOUT, GEx_TXCTL, GEx_RXCLK, GEx_RXCTL: GbE ports 1–3 pins.
- M_BB: SDRAM battery backup trigger—see the DRAM Self Refresh section in the *MV76100, MV78100, and MV78200 Functional Specification*.
- UAx_RXD, UAx_TXD, UAx_CTSn, UAx_RTSn - UART pins.
-
- SATAn_ACTn/SATAn_PRESENTn: SATA active and SATA present indications—see the SATA section in the *MV76100, MV78100, and MV78200 Functional Specification*.
- DEV_NFWEn[3:0], DEV_NFREn[3:0]: NAND Flash additional signals—see the Device Bus section in the *MV76100, MV78100, and MV78200 Functional Specification*.
- TDM_INTn, TDM_RSTn, TDM_PCLK, TDM_FSYNC, TDM_DRX, TDM_DTX, TDM_SCSn, TDM_SCLK, TDM_SMOSI, TDM_SMISO: TDM (voice) interface signals—see the TDM section in the *MV76100, MV78100, and MV78200 Functional Specification.*
- SYSRST_OUTn - open drain reset output—See Section 7, System Power Up and Reset Settings, on page 53.

Table 26 shows each MPP pins' functionality as determined by the MPP Multiplex registers, refer to the Pins Multiplexing Interface Registers section in the *MV76100, MV78100, and MV78200 Functional Specification* for more information. The coloring scheme demonstrates the different power segments (yellow = VDDO_B, sky blue = VDDO_C, green = VDDO_D). Note that MPP[23:12] share the same power segment (VDDO_C) as DEV_AD[15:0], all device bus control signals, UART0 and UART1 signals, and system signals (see pin list for more details).

Note

Empty fields in Table 26 indicate non-functional settings.

Table 26: MPP Function Summary

MPP Pin	0x0	0x1	0x2	0x3	0x4	0x5	0x6
MPP[0]	GPIO[0] (in/out)	GE0_COL (in)	GE1_TXCLKOUT (out)				
MPP[1]	GPIO[1] (in/out)	GE0_RXERR (in)	GE1_TXCTL (out)				
MPP[2]	GPIO[2] (in/out)	GE0_CRS (in)	GE1_RXCTL (in)				
MPP[3]	GPIO[3] (in/out)	GE0_TXERR (out)	GE1_RXCLK (in)				
MPP[4]	GPIO[4] (in/out)	GE0_TXD[4] (out)	GE1_TXD[0] (out)				
MPP[5]	GPIO[5] (in/out)	GE0_TXD[5] (out)	GE1_TXD[1] (out)				
MPP[6]	GPIO[6] (in/out)	GE0_TXD[6] (out)	GE1_TXD[2] (out)				
MPP[7]	GPIO[7] (in/out)	GE0_TXD[7] (out)	GE1_TXD[3] (out)				
MPP[8]	GPIO[8] (in/out)	GE0_RXD[4] (in)	GE1_RXD[0] (in)				
MPP[9]	GPIO[9] (in/out)	GE0_RXD[5] (in)	GE1_RXD[1] (in)				
MPP[10]	GPIO[10] (in/out)	GE0_RXD[6] (in)	GE1_RXD[2] (in)				
MPP[11]	GPIO[11] (in/out)	GE0_RXD[7] (in)	GE1_RXD[3] (in)				
MPP[12]	GPIO[12] (in/out)		GE2_TXCLKOUT (out)	M_BB (in)	UA0_CTSn (in)	NAND Flash REn[0] (out)	TDM0_SCSn (out)
MPP[13]	GPIO[13] (in/out)		GE2_TXCTL (out)	SYSRST_OUTn (out)	UA0_RTSn (out)	NAND Flash WEn[0] (out)	TDM_SCLK (out)

Table 26: MPP Function Summary (Continued)

MPP Pin	0x0	0x1	0x2	0x3	0x4	0x5	0x6
MPP[14]	GPIO[14] (in/out)		GE2_RXCTL (in)	SATA1_ACTn (out)	UA1_CTSn (in)	NAND Flash REn[1] (out)	TDM_SMOSI (out)
MPP[15]	GPIO[15] (in/out)		GE2_RXCLK (in)	SATA0_ACTn (out)	UA1_RTSn (out)	NAND Flash WEn[1] (out)	TDM_SMISO (in)
MPP[16]	GPIO[16] (in/out)		GE2_TXD[0] (out)	SATA1_PRESENTn (out)	UA2_TXD (out)	NAND Flash REn[3] (out)	TDM_INTn (in)
MPP[17]	GPIO[17] (in/out)		GE2_TXD[1] (out)	SATA0_PRESENTn (out)	UA2_RXD [in)	NAND Flash WEn[3] (out)	TDM_RSTn (out)
MPP[18]	GPIO[18] (in/out)		GE2_TXD[2] (out)		UA0_CTSn (in)	BOOT NAND Flash REn (out)	
MPP[19]	GPIO[19] (in/out)		GE2_TXD[3] (out)		UA0_RTSn (out)	BOOT NAND Flash WEn (out)	
MPP[20]	GPIO[20] (in/out)		GE2_RXD[0] (in)		UA1_CTSn (in)		TDM_PCLK (in/out)
MPP[21]	GPIO[21] (in/out)		GE2_RXD[1] (in)		UA1_RTSn (out)		TDM_FSYNC (in/out)
MPP[22]	GPIO[22] (in/out)		GE2_RXD[2] (in)		UA3_TXD (out)	NAND Flash REn[2] (out)	TDM_DRX (in)
MPP[23]	GPIO[23] (in/out)		GE2_RXD[3] (in)		UA3_RXD (in)	NAND Flash WEn[2] (out)	TDM_DTX (out)
DEV_AD[16]	GPIO[24] (in/out)		GE3_TXCLKOUT (out)		UA2_TXD (out)		TDM_INTn (in)
DEV_AD[17]	GPIO[25] (in/out)		GE3_TXCTL (out)		UA2_RXD (in)		TDM_RSTn (out)
DEV_AD[18]	GPIO[26] (in/out)		GE3_RXCTL (in)		UA2_CTSn (in)		TDM_PCLK (in/out)

Table 26: MPP Function Summary (Continued)

MPP Pin	0x0	0x1	0x2	0x3	0x4	0x5	0x6
DEV_ AD[19]	GPIO[27] (in/out)		GE3_RXCLK (in)		UA2_RTSn (out)		TDM_ FSYNC (in/out)
DEV_ AD[20]	GPIO[28] (in/out)		GE3_TXD[0] (out)		UA3_TXD (out)		TDM_ DRX (in)
DEV_ AD[21]	GPIO[29] (in/out)		GE3_TXD[1] (out)		UA3_RXD (in)	SYSRST_ OUTn (out)	TDM_ DTX (out)
DEV_ AD[22]	GPIO[30] (in/out)		GE3_TXD[2] (out)		UA3_CTSn (in)		
DEV_ AD[23]	GPIO[31] (in/out)		GE3_TXD[3] (out)		UA3_RTSn (out)		TDM1_ SCSn (out)
DEV_ AD[24]		GPIO[0] (in/out)	GE3_RXD[0] (in)		UA3_TXD (out)	SYSRST_ OUTn (out)	TDM0_ RXQ (out)
DEV_ AD[25]		GPIO[1] (in/out)	GE3_RXD[1] (in)		UA3_RXD (in)		TDM0_ TXQ (out)
DEV_ AD[26]		GPIO[2] (in/out)	GE3_RXD[2] (in)		UA2_TXD (out)		TDM1_ RXQ (out)
DEV_ AD[27]		GPIO[3] (in/out)	GE3_RXD[3] (in)		UA2_RXD (in)		TDM1_ TXQ (out)
DEV_ AD[28]		GPIO[4] (in/out)	UA0_CTSn (in)		UA2_TXD (out)		TDM0_ SCSn (out)
DEV_ AD[29]		GPIO[5] (in/out)	UA0_RTSn (out)		UA2_RXD (in)	SYSRST_ OUTn (out)	TDM_ SCLK (out)
DEV_ AD[30]		GPIO[6] (in/out)	UA1_CTSn (in)		UA3_TXD (out)	SYSRST_ OUTn (out)	TDM_ SMOSI (out)
DEV_ AD[31]		GPIO[7] (in/out)	UA1_RTSn (out)		UA3_RXD (in)	SYSRST_ OUTn (out)	TDM_ SMISO (in)
DEV_ AD[9]		GPIO[17] (in/out)					TDM_ INTn (in)

Table 26: MPP Function Summary (Continued)

MPP Pin	0x0	0x1	0x2	0x3	0x4	0x5	0x6
DEV_ AD[10]		GPIO[18] (in/out)					TDM_ RSTn (out)
DEV_ AD[11]		GPIO[19] (in/out)					TDM_ PCLK (in/out)
DEV_ AD[12]		GPIO[20] (in/out)					TDM_ FSYNC (in/out)
DEV_ AD[13]		GPIO[21] (in/out)					TDM_ DRX (in)
DEV_ AD[14]		GPIO[22] (in/out)		SATA0_ACT n (out)			TDM_ DTX (out)
DEV_ AD[15]		GPIO[23] (in/out)					TDM1_ SCSn (out)
DEV_ WEn[1]		GPIO[16] (in/out)					
DEV_ WEn[2]		GPIO[8] (in/out)		SATA1_ACT n (out)			
DEV_ WEn[3]		GPIO[9] (in/out)		SATA0_ACT n (out)	M_BB (in)		

Note

Depending on the pin's configured functionality, each pin can act as an output or input pin. MPP[23:0] and DEV_AD[23:16] wake up as GPIO. All other pins wake up as non-functional inputs pads (0x0 Column), with one exception. If the chip is configured at reset to boot from CE Care NAND Flash, MPP[19:18] wake up as BOOT NAND Flash output signals.

The muxing options on DEV_AD[31:16] and DEV_WEn[3:2] only apply if all five device chip selects are configured as 8- or 16-bit wide. Muxing options on DEV_AD[15:9] and DEV_WEn[1] only apply if all five device chip selects are configured as 8-bit wide. Where device bus pins multiplexing applies, these pins wake up as input (no drive).

7 System Power Up and Reset Settings

This section provides information about the MV78200 power-up sequence and configuration at reset.

7.1 Power Up/Down Sequence Requirements

7.1.1 Power Up Sequence Requirements

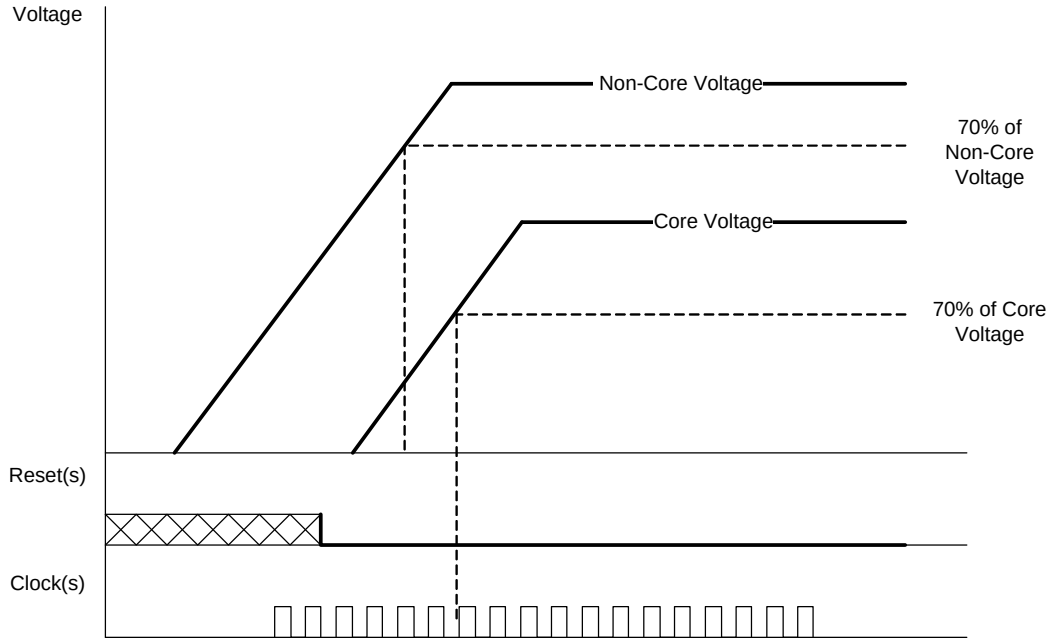
These guidelines must be applied to meet the MV78200 device power-up requirements:

- The Non-Core voltages (I/O and Analog) as listed in Table 27 must reach 70% of their voltage level before the Core voltages reach 70% of their voltage level.
  The order of the power up sequence between the Non-Core voltages is unimportant so long as the Non-Core voltages power up before the Core voltages reach 70% of their voltage level (shown in Figure 4).
- The reset signal(s) must be asserted before the Core voltages reach 70% of their voltage level (shown in Figure 4).
- The reference clock(s) inputs must toggle with their respective voltage levels before the Core Voltages reach 70% of their voltage level (shown in Figure 4).

Table 27: I/O and Core Voltages

Non-Core Voltages		Core Voltages
I/O Voltages	**Analog Power Supplies**	
VDD_GE VDD_M VDDO_A VDDO_B VDDO_C VDDO_D	PLL_AVDD PEX0_AVDD PEX1_AVDD USB0_AVDD, USB1_AVDD, USB2_AVDD SATA0_AVDD, SATA1_AVDD	VDD VDD_CPU0, VDD_CPU1

Figure 4: Power Up Sequence Example



Note

- It is the designer's responsibility to verify that the power sequencing requirements of other components are also met.
- Although the non-core voltages can be powered up any time before the core voltages, allow a reasonable time limitation (for example, 100 ms) between the **first** non-core voltage power-up and the **last** core voltage power-up.

7.1.2 Power Down Sequence Requirements

There are no special requirements for the core supply to go down first, or for reset assertion when powering down.

Note

Although there is no limitation for power-down sequence between non-core and core voltages, allow a reasonable time limitation (for example, 100 ms) between the **first** and **last** voltage power-down.

7.2 Hardware Reset

The MV78200 has one reset input pin — SYSRSTn. When asserted, the entire chip is placed in its initial state. All outputs are placed in high-z.

The following output pins are still active during SYSRSTn assertion:

- TCLK_OUT
- GE0_TXCLKOUT
- M_CLKOUT[2:0], M_CLKOUTn[2:0]
- M_CKE[3:0]
- M_ODT[3:0]
- M_STARTBURST
- SATAx_TX_P
- SATAx_TX_N
- PEXx_TX_N
- PEXx_TX_P
- USBx_DM
- USBx_DP

The MV78200 has an optional SYSRST_OUTn open drain output signal, multiplexed on MPP pins, that is used as a reset request from the MV78200 to the board reset logic. This signal is set when one of the following maskable events occurs:

- Received hot reset indication from the PCI Express port 0.0 link (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the Reset register section of the *MV78200 User Manual*). In this case, SYSRST_OUTn is asserted for duration of ~300 TCLK cycles.
- PCI Express port 0.0 link failure (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the Reset register section of the *MV78200 User Manual*). In this case, SYSRST_OUTn is asserted for duration of ~300 TCLK cycles .
- Watchdog timer expiration and bit <WDRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the Reset register section of the *MV78200 User Manual*).
- Bit <SystemSoftRst> is set to 1 in System Soft Reset Register and bit <SoftRstOutEn> is set to 1 in RSTOUTn Mask Register.

Note

Reset must be active for a minimum length of 100ms. Core power, I/O power, and analog power must be stable (VDD +/- 5%) during that time and onward.

7.3 PCI Express Reset

As a Root Complex, the MV78200 can generate a Hot Reset to the PCI Express port. Upon CPU setting the PCI Express Control register's <conf_mstr_hot_reset> bit, the PCI Express unit sends a Hot Reset indication to the Endpoint (see the PCI Express Interface section in the *MV76100, MV78100, and MV78200 Functional Specification*).

When the MV78200 works as an Endpoint, and a Hot Reset packet is received:

- A maskable interrupt is asserted
- If the PCI Express Debug Control register's <conf_dis_hot_rst_reg_rst> is cleared, the MV78200 also resets the PCI Express register file to its default values.
- The MV78200 triggers an internal reset, if not masked by PCI Express Debug Control register's <conf_msk_hot_reset> bit.

Link failure is detected if the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state). When Link failure is detected:

- A maskable interrupt is asserted
- If the PCI Express Debug Control register's <conf_dis_link_fail_reg_rst> is cleared, the MV78200 also resets the PCI Express register file to its default values.
- The MV78200 triggers an internal reset, if not masked by PCI Express Debug Control register's <conf_msk_link_fail> bit.

Whether initiated by a Hot Reset or link failure, this internal reset indication can be routed to SYSRST_OUTn output as explained in Section 7.2, Hardware Reset, on page 55. The external reset logic can assert SYSRSTn in response and reset the entire chip.

Note Only PEX0 port (or PEX0.0 port in Quad x1 configuration) can act as PCI Express endpoint, and only this port can generate the PCI Express internal reset indication.

7.4 Pins Sample Configuration

The following pins are sampled during SYSRSTn de-assertion. Internal pull up/down resistors set the default mode. External pull up/down resistors are required to change the default mode of operation. These signals must remain pulled up or down until SYSRSTn de-assertion (zero Hold time in respect to SYSRSTn de-assertion).

Note If external logic is used instead of pull up and pull down resistors, the logic must drive all of the signals to the desired values during SYSRSTn assertion. To prevent bus contention on these pins, the external logic must float the bus no later than the third TCLK cycle after SYSRSTn de-assertion. Refer to the *MV76100, MV78100, and MV78200 Design Guide* for additional information.

All reset sampled values are registered in Reset Sample (Low) and Reset Sample (High) registers (see the Device Interface Registers in the *MV76100, MV78100, and MV78200 Functional Specification*). This is useful for board debug purposes.

Multiple functionality applies to DEV_AD[31:9] and DEV_WEn[3:1], as described in Section 6, Pin Multiplexing, on page 48. If an external device is driving any of these signals, make sure to keep this external device in reset state (prevent it from driving) or use glue logic to disconnect it from the MV78200 as long as the MV78200 SYSRSTn input is asserted.

Table 28: Reset Configuration

Pin	Power Rail	Configuration Function
DEV_AD[0]	VDDO_C	Reserved
		This signal must be sampled as 0 at reset de-assertion. **NOTES:** • Internally pulled down to 0x0. • The board design should support future pull up/pull down requirements on this pin. Setting recommendations will be published following silicon samples.

Table 28: Reset Configuration (Continued)

Pin	Power Rail	Configuration Function
DEV_AD[1]	VDDO_C	Reserved
		This signal must be sampled as 0 at reset de-assertion. **NOTES:** • Internally pulled down to 0x0. • The board design should support future pull up/pull down requirements on this pin. Setting recommendations will be published following silicon samples.
DEV_AD[2]	VDDO_C	PCI Express Port0 mode select
		0 = Endpoint 1 = Root Complex **NOTES:** • Internally pulled up to 0x1. • When PCI Express port0 is configured to Quad x 1 (DEV_AD[3]=1), this bit controls Port 0.0 only.
DEV_AD[3]	VDDO_C	PCI Express Port0 configuration
		0 = x4 1 = Quad x1 **NOTE:** Internally pulled down to 0x0.
DEV_AD[4]	VDDO_C	PCI Express Port1 configuration
		0 = x4 1 = Quad x1 **NOTE:** Internally pulled up to 0x1.
DEV_AD[7:5]	VDDO_C	HCLK Frequency select
		0x0 = Reserved 0x1 = 200 MHz 0x2 = 267 MHz 0x3 = 333 MHz 0x4 = 400 MHz 0x5 = 250 MHz 0x6 = 300 MHz 0x7 = Reserved **NOTE:** Internally pulled to 0x2.
DEV_AD[11:8]	VDDO_C	PCLK0 to HCLK ratio
		0x0 = 1 0x1 = 1.5 0x2 = 2 0x3 = 2.5 0x4 = 3 0x5 = 3.5 0x6 = 4 0x7 = 4.5 0x8 = 5 0xB–0xF = Reserved **NOTE:** Internally pulled to 0x4.

Table 28: Reset Configuration (Continued)

Pin	Power Rail	Configuration Function
DEV_AD[13:12]	VDDO_C	PCLK0 to CPU0 L2 ratio
		0x0 = 1 0x1 = 2 0x2 = 3 0x3 = Reserved **NOTE:** Internally pulled to 0x1.
DEV_AD[17:14]	[15:14] VDDO_C [17:16] VDDO_B	PCLK1 to HCLK ratio
		0x0 = 1 0x1 = 1.5 0x2 = 2 0x3 = 2.5 0x4 = 3 0x5 = 3.5 0x6 = 4 0x7 = 4.5 0x8 = 5 0x9 = 5.5 0xA = 6 0xB–0xF = Reserved **NOTE:** Internally pulled to 0x4.
DEV_AD[19:18]	VDDO_B	PCLK1 to CPU1 L2 ratio
		0x0 = 1 0x1 = 2 0x2 = 3 0x3 = Reserved **NOTE:** Internally pulled to 0x1.
DEV_AD[20]	VDDO_B	CPU1 Enable
		This signal must be sampled as 0 at reset de-assertion. 0 = Disable 1 = Enable **NOTE:** Internally pulled down to 0x0.
DEV_AD[22:21]	VDDO_B	DEV_BootCEn Device Width
		0x0 = 8 bits 0x1 = 16 bits 0x2 = 32 bits 0x3 = Reserved **NOTE:** Internally pulled down to 0x0.

Table 28: Reset Configuration (Continued)

Pin	Power Rail	Configuration Function
DEV_AD[24:23]	VDDO_B	Boot DeviceType Selection
		0x0 = Boot from device bus 0x1 = Boot from SPI 0x2 = Boot from CE don't care NAND Flash 0x3 = Boot from CE care NAND Flash If DEV_AD[24:23] is set to 0x3, MPP[19:18] pins wake up as NAND Flash outputs. **NOTE:** Internally pulled down to 0x0.
DEV_AD[26:25]	VDDO_B	NAND Flash Initialization Sequence
		Selects if NAND Flash initialization sequence is performed. Required for NAND Flash devices that do not support preload feature. Only relevant if DEV_AD[24] is set to 1 (boot from NAND Flash). 0x0 = No initialization 0x1 = Init sequence enabled, 3 address cycles 0x2 = Init sequence enabled, 4 address cycles 0x3 = Init sequence enabled, 5 address cycles **NOTE:** Internally pulled down to 0x0.
DEV_AD[27]	VDDO_B	Big Endian/Little Endian mode
		0 = Little Endian 1 = Big Endian **NOTE:** Internally pulled down to 0x0.
DEV_AD[28]	VDDO_B	CLK25 Select
		0 = Both CLK25_PT and CLK25_SSC are used. 1 = Only CLK25_PT is used. **NOTE:** Internally pulled up to 0x1.
DEV_AD[29]	VDDO_B	DRAM Interface Width
		0 = 64/72-bits 1 = 32/40-bits **NOTE:** Internally pulled to 0x0.
DEV_AD[30]	VDDO_B	NAND Flash Initialization Command
		Selects whether to append command 0x30 to the address cycles of the NAND Flash initialization sequence or not. Relevant only when using the NAND Flash initialization sequence (DEV_AD[26:25] != 0x0). 0 = Do not append command 0x30. 1 = Append command 0x30. **NOTE:** Internally pulled to 0x0.
DEV_AD[31]	VDDO_B	VDDO_C Voltage Select
		0 = 1.8V 1 = 3.3V **NOTE:** Internally pulled up to 0x1.

Table 28: Reset Configuration (Continued)

Pin	Power Rail	Configuration Function
DEV_ALE[0]	VDDO_C	VDDO_B Voltage Select
		0 = 1.8V 1 = 3.3V **NOTE:** Internally pulled up to 0x1.
DEV_ALE[1]	VDDO_C	VDDO_D Voltage Select
		0 = 1.8V 1 = 3.3V **NOTE:** Internally pulled up to 0x1.
DEV_WEn[0]	VDDO_C	VDD_GE Voltage Select
		0 = 1.8V 1 = 3.3V **NOTE:** Internally pulled down to 0x0.
DEV_WEn[1]	VDDO_C	DEV_WEn and DEV_OEn multiplexing option for A[16:15] bits
		Defines if OE and WE are latched at first ALE cycle as A[15] and A[16]. This fact influences the OEn and WEn signal as follows: 0 = A[16:15] bits are not multiplexed on OE and WE signals. **NOTE:** Whenever CS is inactive OE and WE are inactive. 1 = A[16:15] bits are multiplexed on OE and WE signals **NOTE:** Whenever CS is inactive and ALE[1:0] are high, OE and WE are inactive. **NOTE:** Internally pulled down to 0x0.
DEV_WEn[2]	VDDO_C	Reserved
		This signal must be sampled as 0 at reset de-assertion. **NOTE:** Internally pulled down to 0x0.
DEV_WEn[3]	VDDO_C	Reserved
		This signal must be sampled as 0 at reset de-assertion. **NOTE:** Internally pulled down to 0x0.
DEV_A[0]	VDDO_C	TCLK Mode Select
		0 = TCLK is driven from TCLK_IN input (De-skew mode) 1 = TCLK generated internally by TCLK PLL **NOTE:** Internally pulled up to 0x1.

Table 28: Reset Configuration (Continued)

Pin	Power Rail	Configuration Function
DEV_A[2:1]	VDDO_C	TCLK frequency select/TCLK De-skew PLL Tune
		If DEV_A[0] is set to 1 - DEV_A[2:1] functions as TCLK frequency select: 0x0 = 166 MHz 0x1 = 200 MHz 0x2, 0x3 = Reserved If DEV_A[0] is set to 0, DEV_A[2:1] functions as TCLK de-skew PLL Tune. A setting recommendation will be released after chip silicon testing. When using TCLK_IN input Board design should support future pull up/pull down requirement on these pins. A final setting recommendation will be published following silicon samples. **NOTE:** Internally pulled to 0x1.
GE0_TXD[0]	VDD_GE	TCLK De-skewer PLL Frequency Band Select
		Functions as TCLK De-Skewer PLL Frequency band select. Relevant for De-skew mode only (DEV_A[0] is set to 0) . 0 = 166 MHz 1 = 200 MHz **NOTE:** Internally pulled down to 0x0.
GE0_TXD[1]	VDD_GE	Reserved
		This signal must be sampled as 1 at reset de-assertion. **NOTE:** Internally pulled up to 0x1.
GE0_TXD[3:2]	VDD_GE	DEV_ALE Mode Select
		Defines DEV_ALE[1:0] behaviour in respect to address driven by device bus controller (address setup and hold time in respect to DEV_ALE falling edge). Useful for device bus topologies in which DEV_AD bus is heavily loaded. 0x0 = Address is driven for two TCLK cycles. ALE toggles after one TCLK cycle. 0x1 = Address is driven for three TCLK cycles. ALE toggles after two TCLK cycles. 0x2 = Address is driven for four TCLK cycles. ALE toggles after three TCLK cycles. 0x3 = Reserved **NOTE:** Internally pulled down to 0x0.
GE0_TXCTL	VDD_GE	Reserved
		This signal must be sampled as 0 at reset de-assertion. **NOTE:** Internally pulled down to 0x0.

Note Even if using a 8/16-bit device, the reset sampling on the upper device bus is still used.

7.5 Power Up and Boot Sequence

The MV78200 requires that SYSRSTn remain asserted for at least 1 ms after power and clocks are stable. The following procedure describes the boot sequence starting with the reset assertion:

1. While SYSRSTn is asserted, the PCLK, TCLK, and CLK125 PLLS are locked. SYSRSTn assertion should be at least 1 ms.
2. Upon SYSRSTn de-assertion, the pad drive auto-calibration process starts. It takes 512 TCLK cycles.
3. In parallel, TCLK de-skew PLL locks when working in de-skew mode.
4. If configured to boot from NAND Flash which does not support preload operation, the MV78200 also performs a NAND Flash boot init sequence.

Upon completing the above sequence, the CPU reset is deasserted, and CPU starts executing boot code from DEV_BOOTCSn (whether it is a NOR Flash or a NAND Flash or from SPI Flash).

As part of the CPU boot code, the CPU typically performs the following:

- Change the chip default address map if required, and configure PCI-Express address map.
- Configure device bus timing parameters according to devices attached to device bus.
- Configures the proper DRAM controller parameters, and then triggers DRAM initialization (set DRAM Initialization Control register's <InitEn> bit [0] to 1).
- If using DRAM ECC, also initializes DRAM content. Initializes proper ECC to the entire DRAM space.
- Set the <PEXEn> bits in the CPU Control and Status register to wake up the PCI Express link.

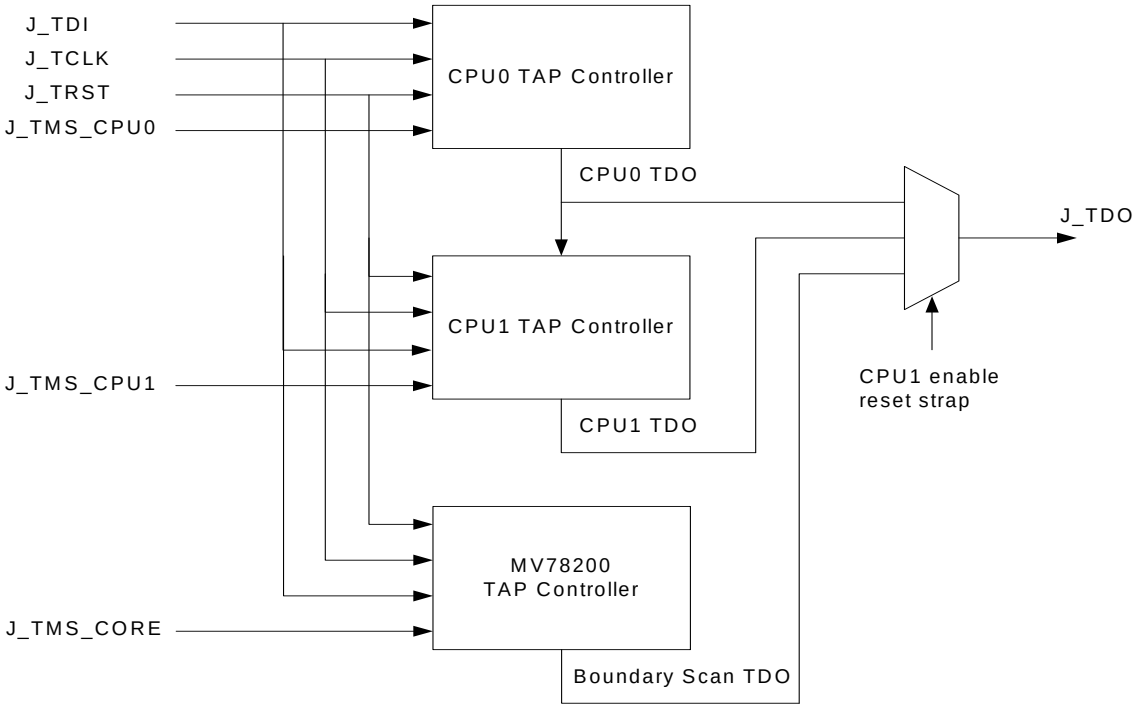
For Dual CPU operation, CPU0 must also change the default address map of CPU1, specifiaclly the boot window.

8 JTAG Interface

The MV78200 JTAG interface is used for chip boundary scan as well as for CPU cores debugger.

TAP controllers implementation is described in the diagram below.

Figure 5: MV78200 TAP Controller



The MV78200 supports the following test modes:

- Boundary scan: In this mode, keep J_TMS_CPU high; this will reset the CPUs TAP controllers and mux the boundary scan TDO signal on the J_TDO pin.
- CPU debugger: In this mode, keep J_TMS_CORE high; this will reset the MV78200 TAP controller and mux the CPU TDO signal on the J_TDO pin.

The two CPU core TAP controllers are chained (CPU0_TDO is connected to CPU1_TDI; CPU1_TDO is driven on J_TDO pin). In case the chip is configured at reset to single CPU (DevAD[20] sampled low), the two CPUs TAP controllers are not chained, and CPU0_TDO is connected to J_TDO pin.

9 Electrical Specifications (Preliminary)

Note The numbers specified in this section are PRELIMINARY and SUBJECT TO CHANGE.

9.1 Absolute Maximum Ratings

Table 29: Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDD	-0.5	1.32	V	Core voltage
IREF_AVDD	-0.5	2.2	V	SATA and USB PHYs current source voltage filtered 1.8V
VDD_CPU0 VDD_CPU1	-0.5	1.32	V	CPU core voltage (Relevant for both VDD_CPU0 and VDD_CPU1)
PLL_AVDD	-0.5	2.2	V	Analog supply for the internal PLL
VDD_GE	-0.5	4.0	V	I/O voltage for: RGMII/GMII/MII/SMI interfaces
VDD_M	-0.5	2.2	V	I/O voltage for: SDRAM DDR2 interface
M_VREF	-0.5	1.1	V	Reference voltage for: SDRAM DDR2 interface
VDDO_A	-0.5	4.0	V	I/O voltage for: TWSI1, JTAG, and SPI interfaces
VDDO_B, VDDO_C, VDDO_D	-0.5	4.0	V	I/O voltage for: Device Bus, TWSI0, UART interfaces, MPP, REF_CLK_SSC, REF_CLK_PT, and SYSRSTn
PEX0_AVDD, PEX1_AVDD	-0.5	2.2	V	Voltage for: PCI Express interface
USB0_AVDD, USB1_AVDD, USB2_AVDD	-0.5	4.0	V	I/O voltage for: USB interface
SATA0_AVDD, SATA1_AVDD	-0.5	3.0	V	I/O voltage for: SATA interface
TC	-40	125	° C	Case temperature

Table 29: Absolute Maximum Ratings (Continued)

Parameter	Min	Max	Units	Comments
TSTG	-40	125	° C	Storage temperature

Caution

- Exposure to conditions at or beyond the maximum rating can damage the device.
- Operation beyond the recommended operating conditions (Table 30) is neither recommended nor guaranteed.

Note

Before designing a system, it is recommended that you read application note AN-63: *Thermal Management for Marvell Technology Products*. This application note presents basic concepts of thermal management for Integrated Circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

9.2 Recommended Operating Conditions

Table 30: Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
VDD	0.95	1.0	1.05	V	Core voltage
IREF_AVDD	1.7	1.8	1.9	V	SATA and USB PHYs current source voltage filtered 1.8V
VDD_CPU0 VDD_CPU1	1.05	1.1	1.15	V	CPU core voltage
PLL_AVDD	1.7	1.8	1.9	V	Analog supply for the internal PLL
VDD_GE	1.7	1.8	1.9	V	I/O voltage for: RGMII/SMI 1.8V interfaces **NOTE:** VDD_GE can be set to either 1.8V or 3.3V according to Section 7.2, Hardware Reset, on page 55.
	3.15	3.3	3.45	V	I/O voltage for: RGMII/GMII/MII/SMI 3.3V interfaces
VDD_M	1.7	1.8	1.9	V	I/O voltage for: SDRAM DDR2 interface
M_VREF	0.49*VDD_M	0.5*VDD_M	0.51*VDD_M	V	Reference voltage for: SDRAM DDR2 interface
VDDO_A	3.15	3.3	3.45	V	I/O voltage for: TWSI1, JTAG, and SPI interfaces
VDDO_B, VDDO_C, VDDO_D	1.7	1.8	1.9	V	I/O voltage for: Device Bus, TWSI0, UART interfaces, and MPP **NOTE:** VDDO_B, VDDO_C, and VDDO_D can be set to either 1.8V or 3.3V according to Section 7.2, Hardware Reset, on page 55.
	3.15	3.3	3.45	V	
PEX0_AVDD, PEX1_AVDD	1.7	1.8	1.9	V	Voltage for: PCI Express interface
USB0_AVDD, USB1_AVDD, USB2_AVDD	3.15	3.3	3.45	V	I/O voltage for: USB interface
SATA0_AVDD, SATA1_AVDD	2.375	2.5	2.625	V	Voltage for: SATA interface
TJ	0		105	° C	Junction Temperature

Caution Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

9.3 Thermal Power Dissipation (Preliminary)

Table 31: Thermal Power Dissipation

Interface	Symbol	Test Conditions	Typ	Units
Core	P_{VDD}		1200	mW
Embedded CPU (Relevant for both VDD_CPU0 and VDD_CPU1)	P_{VDD_CPU}	Two CPUs, 1 GHz, VDD_CPU=1.1V	4200	mW
RGMII 1.8V interface	P_{VDD_GE}	One Port, VDD_GE=1.8V	90	mW
DDR2 DIMM interface (72-bit) ODT	P_{VDD_M}	M_CLK=333 MHz	1675	mW
Miscellaneous (Device Bus interface, TWSI, JTAG, MPP, SPI, UART)	P_{MISC}		300	mW
PCI Express interface	P_{PEX}	For one PCI Express interface in x4 mode	400	mW
USB interface	P_{USB}	For one USB port	70	mW
SATA interface	P_{SATA}	For one SATA port	180	mW

Notes:

1. The values are for nominal voltage.
2. Trace load is 5 pF unless otherwise specified.
3. Power in mW is calculated using the typical recommended VDDIO specification for each power rail.

9.4 Current Consumption (Preliminary)

Table 32: Current Consumption

Interface	Symbol	Test Conditions	Max	Units
Core	I_{VDD}		1500	mA
Embedded CPU (Relevant for both VDD_CPU0 and VDD_CPU1)	I_{VDD_CPU}	Two CPUs, 1 GHz, VDD_CPU=1.1V	4400	mA
RGMII 1.8V interface	I_{VDD_GE}	One Port, VDD_GE=1.8V	50	mA
DDR2 DIMM interface (72-bit) ODT	I_{VDD_M}	M_CLK=333 MHz	1200	mA
Miscellaneous (Device Bus interface, TWSI, JTAG, MPP, SPI, UART)	I_{MISC}		90	mA
PCI Express interface	I_{PEX}	For one PCI Express interface in x4 mode	220	mA
USB interface	I_{USB}	For one USB port	25	mA
SATA interface	I_{SATA}	For one SATA port	75	mA

Notes:

1. Trace load is 5 pF unless otherwise specified.
2. Current in mA is calculated using maximum recommended VDDIO specification for each power rail.
3. All output clocks toggling at their specified rate.
4. Maximum drawn current from the power supply.

9.5 DC Electrical Specifications

Note See the Pin Description Section for internal pullup/pulldown,

9.5.1 General 3.3V (CMOS) DC Electrical Specifications

Table 33 is relevant for the following interfaces that only operate at 3.3V:

- SPI
- JTAG

Table 33 is also relevant if the following interfaces are configured to operate at 3.3V, according to Section 7.2, Hardware Reset, on page 55.

- Device Bus
- MPP
- RGMII
- GMII
- MII
- SMI
- TDM
- SYSRSTn
- UART
- REF_CLK_PT
- TCLK_OUT
- TCLK_IN

Table 33: General 3.3V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.5.2 General 1.8V (CMOS) DC Electrical Specifications

Table 33 is relevant if the following interfaces are configured to operate at 1.8V, according to Section 7.2, Hardware Reset, on page 55.

- Device Bus
- MPP
- GMII
- MII
- RGMII
- SMI
- TDM
- SYSRSTn
- UART
- REF_CLK_PT
- REF_CLK_SSC
- TCLK_OUT
- TCLK_IN

Table 34: General 1.8V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.35*VDDIO	V	-
Input high level	VIH		0.65*VDDIO		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.45	V	-
Output high level	VOH	IOH = -2 mA	VDDIO-0.45		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.5.3 SDRAM DDR2 Interface DC Electrical Specifications

Table 35: SDRAM DDR2 Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL	-	-0.3		VREF - 0.125	V	-
Input high level	VIH	-	VREF + 0.125		VDDIO + 0.3	V	-
Output low level	VOL	IOL = 13.4 mA			0.28	V	-
Output high level	VOH	IOH = -13.4 mA	1.42			V	-
Rtt effective impedance value	RTT	See note 2	120	150	180	ohm	1 , 2
			60	75	90	ohm	1 , 2
			40	50	60	ohm	1 , 2
Deviation of VM with respect to VDDQ/2	dVm	See note 3	-6		6	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply VREF +/- 0.25 to input pin separately, then measure current I(*VREF* +0.25) and I(*VREF* - 0.25) respectively.

$$RTT = \frac{0.5}{I_{(VREF+0.25)} - I_{(VREF-0.25)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1\right) \times 100\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.

9.5.4 Two-Wire Serial Interface (TWSI) 3.3V DC Electrical Specifications

Table 36: TWSI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 3 mA	-		0.4	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6 AC Electrical Specifications

See Section 9.7, Differential Interface Electrical Characteristics, on page 108 for differential interface specifications.

9.6.1 Reference Clock and Reset AC Timing Specifications

Table 37: Reference Clock and Reset AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
Core Reference Clock					
Frequency	$F_{REF\_CLK\_SSC}$ $F_{REF\_CLK\_PT}$	25 - 100 ppm	25 + 100 ppm	MHz	
Clock duty cycle	$DC_{REF\_CLK\_SSC}$ $DC_{REF\_CLK\_PT}$	40	60	%	
Slew rate	$SR_{REF\_CLK\_SSC}$ $SR_{REF\_CLK\_PT}$	0.7		V/ns	1
Pk-Pk jitter	$JR_{REF\_CLK\_SSC}$ $JR_{REF\_CLK\_PT}$		200	ps	
Core Reference Clock Spread Spectrum Requirements					
Modulation Frequency	$Fmod_{REF\_CLK\_SSC}$	0	33	kHz	2
Modulation Index	$Fspread_{REF\_CLK\_SSC}$	-0.5	0	%	2
Ethernet Reference Clock					
Frequency in MII-MAC mode	F_{GE0_TXCLK}	2.5 - 100 ppm	25 + 100 ppm	MHz	
	F_{GE0_RXCLK}				
MII clock duty cycle	DC_{GE0_TXCLK}	35	65	%	
	DC_{GE0_RXCLK}				
Slew rate	SR_{GE0_TXCLK}	0.7		V/ns	1
	SR_{GE0_RXCLK}				
SMI Master Mode Reference Clock					
SMI output MDC clock	F_{GE_MDC}	TCLK/128		MHz	
TWSI Master Mode Reference Clock					
SCK output clock	F_{TWSI0_SCK}, F_{TWSI1_SCK}	TCLK/1600		kHz	
SPI Output Clock					
SPI output clock	F_{SPI_SCK}	TCLK/30	TCLK/4	MHz	6
SPI output clock (Integrated with the TDM interface)	F_{TDM_SCLK}	TCLK/254	TCLK/10	MHz	7

Table 37: Reference Clock and Reset AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
TCLK_OUT Reference Clock					5
Frequency	F_{TCLK_OUT}		166	MHz	
Clock duty cycle	DC_{TCLK_OUT}	40	60	%	3
TCLK_IN Reference Clock					
Frequency	F_{TCLK_IN}	150	200	MHz	4
Clock duty cycle	DC_{TCLK_IN}	40	60	%	
Slew rate	SR_{TCLK_IN}	0.7		V/ns	1
Pk-Pk jitter	JR_{TCLK_IN}		200	ps	
Reset Specifications					
Refer to Section 7, System Power Up and Reset Settings.					

Notes:

1. Slew rate is defined from 20% to 80% of the reference clock signal.
2. Defined on linear sweep or “Hershey’s Kiss” (US Patent 5,631,920) modulations.
3. The load is CL = 15 pF.
4. See Table 28, Reset Configuration, on page 56 for more details.
5. Relevant only when working in source synchronous device bus mode.
6. For additional information regarding configuring this clock, see the Serial Memory Interface Control Register in the *MV76100, MV78100, and MV78200 Functional Specification*.
7. For additional information regarding configuring this clock, see the TDM Interface section in the *MV76100, MV78100, and MV78200 Functional Specifications*.

Figure 6: TCLK_Out Reference Clock Test Circuit

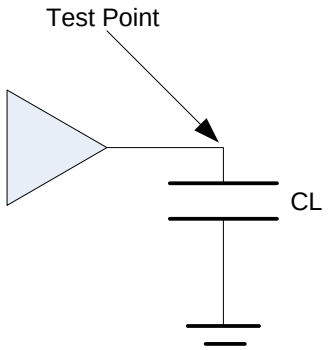
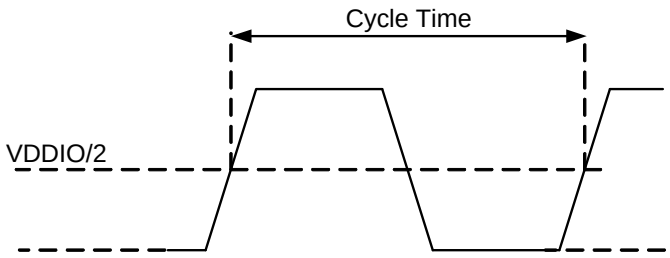


Figure 7: TCLK_Out AC Timing Diagram



9.6.2 Reduced Gigabit Media Independent Interface (RGMII) AC Timing

9.6.2.1 RGMII AC Timing Table

Table 38: RGMII AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	125.0		MHz	-
Data to Clock output skew	TskewT	-0.50	0.50	ns	2
Data to Clock input skew	TskewR	1.00	2.60	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

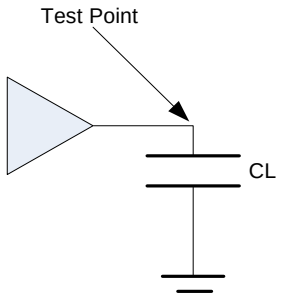
General comment: tCK = 1/fCK.

General comment: If the PHY does not support internal-delay mode, the PC board design requires routing clocks so that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.
For 10/100 Mbps RGMII, the Max value is unspecified.

1. For RGMII at 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns, respectively.
2. For all signals, the load is CL = 5 pF.

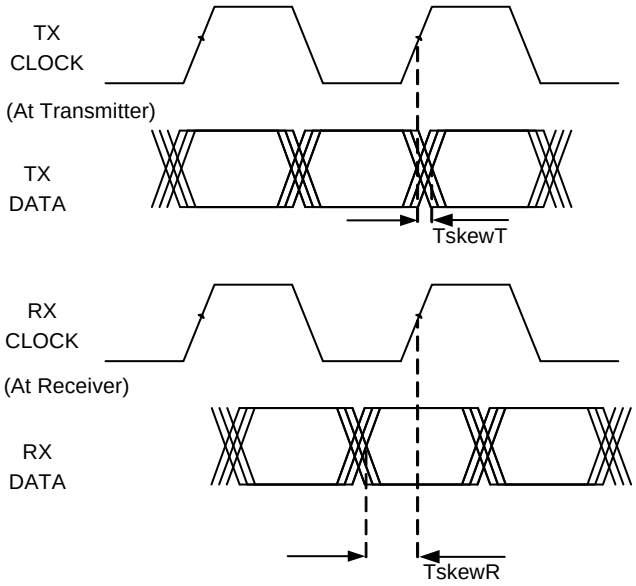
9.6.2.2 RGMII Test Circuit

Figure 8: RGMII Test Circuit



9.6.2.3 RGMII AC Timing Diagram

Figure 9: RGMII AC Timing Diagram



9.6.3 Media Independent Interface (MII) AC Timing

9.6.3.1 MII AC Timing Table

Table 39: MII AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data input setup relative to RX_CLK rising edge	tSU	8.0	-	ns	-
Data input hold relative to RX_CLK rising edge	tHD	8.0	-	ns	-
Data output delay relative to MII_TX_CLK rising edge	tOV	0.0	20.0	ns	1

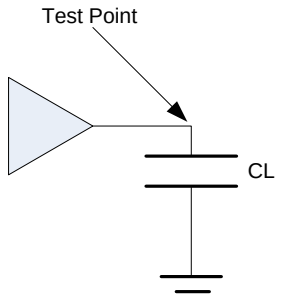
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

9.6.3.2 MII Test Circuit

Figure 10: MII Test Circuit



9.6.3.3 MII AC Timing Diagrams

Figure 11: MII Output Delay AC Timing Diagram

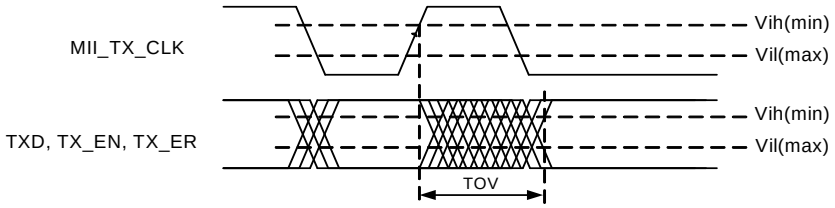
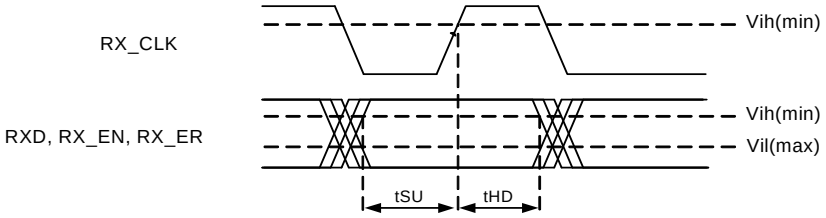


Figure 12: MII Input AC Timing Diagram



9.6.4 Gigabit Media Independent Interface (GMII) AC Timing

9.6.4.1 GMII AC Timing Table

Table 40: GMII AC Timing Table

Description	Symbol	125 MHz		Units	Notes
		Min	Max		
GTX_CLK cycle time	tCK	7.5	8.5	ns	-
RX_CLK cycle time	tCKrx	7.5	-	ns	-
GTX_CLK and RX_CLK high level width	tHIGH	2.5	-	ns	1
GTX_CLK and RX_CLK low level width	tLOW	2.5	-	ns	1
GTX_CLK and RX_CLK rise time	tR	-	1.0	ns	1, 2
GTX_CLK and RX_CLK fall time	tF	-	1.0	ns	1, 2
Data input setup time relative to RX_CLK rising edge	tSETUP	2.0	-	ns	-
Data input hold time relative to RX_CLK rising edge	tHOLD	0.0	-	ns	-
Data output valid before GTX_CLK rising edge	tOVB	2.5	-	ns	1
Data output valid after GTX_CLK rising edge	tOVA	0.5	-	ns	1

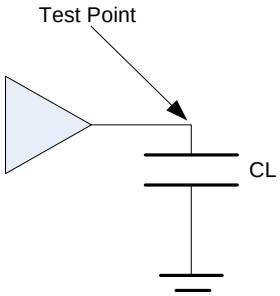
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

9.6.4.2 GMII Test Circuit

Figure 13: GMII Test Circuit



9.6.4.3 GMII AC Timing Diagrams

Figure 14: GMII Output AC Timing Diagram

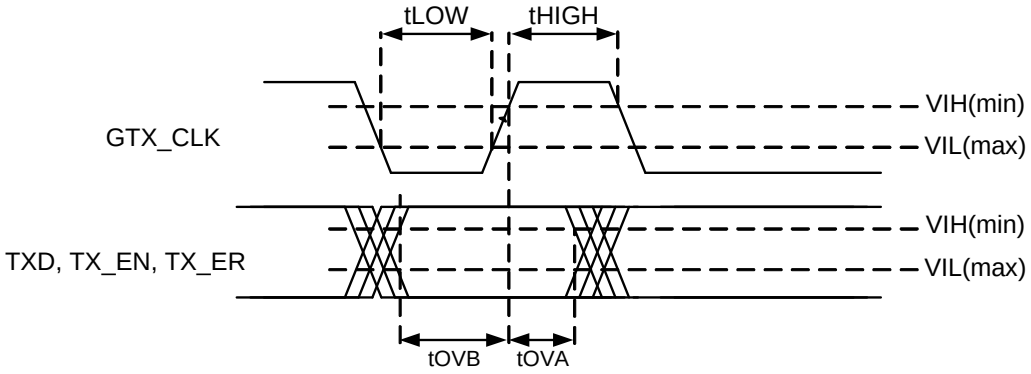
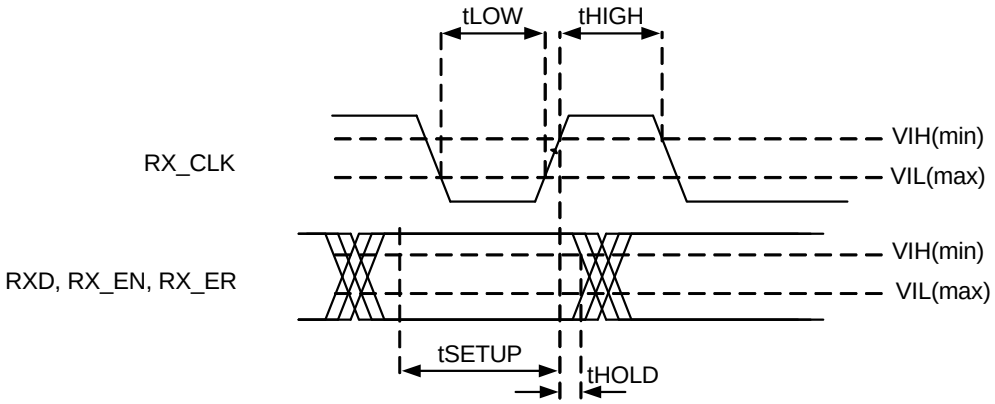


Figure 15: GMII Input AC Timing Diagram



9.6.5 Serial Management Interface (SMI) AC Timing

9.6.5.1 SMI Master Mode AC Timing Table

Table 41: SMI Master Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
MDC clock frequency	fCK	See note 2		MHz	2
MDC clock duty cycle	tDC	0.4	0.6	tCK	-
MDIO input setup time relative to MDC rise time	tSU	40.0	-	ns	-
MDIO input hold time relative to MDC rise time	tHO	0.0	-	ns	-
MDIO output valid before MDC rise time	tOVB	15.0	-	ns	1
MDIO output valid after MDC rise time	tOVA	15.0	-	ns	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For MDC signal, the load is CL = 390 pF, and for MDIO signal, the load is CL = 470 pF.

2. See "Reference Clocks" table for more details.

9.6.5.2 SMI Master Mode Test Circuit

Figure 16: MDIO Master Mode Test Circuit

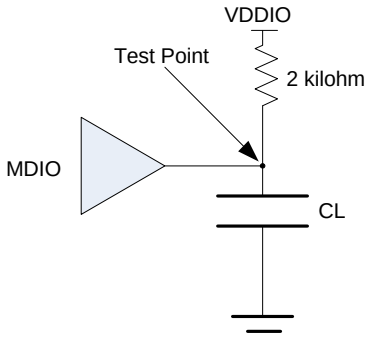
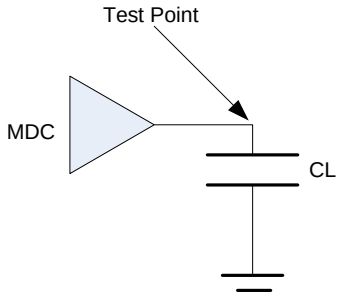


Figure 17: MDC Master Mode Test Circuit



9.6.5.3 SMI Master Mode AC Timing Diagrams

Figure 18: SMI Master Mode Output AC Timing Diagram

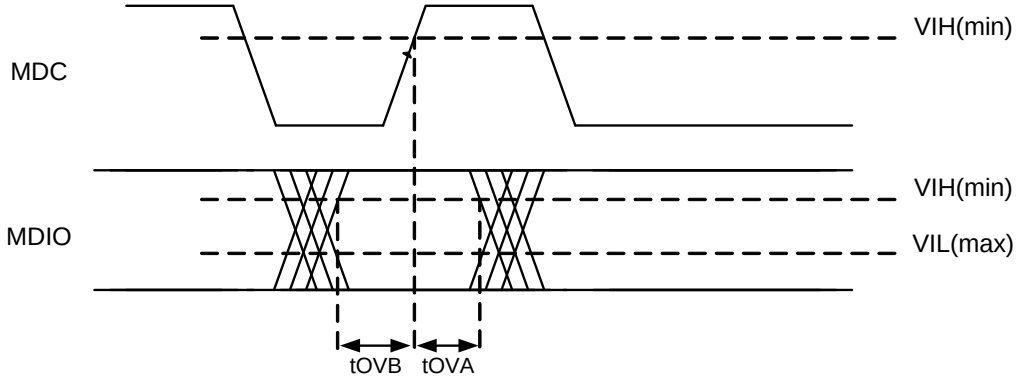
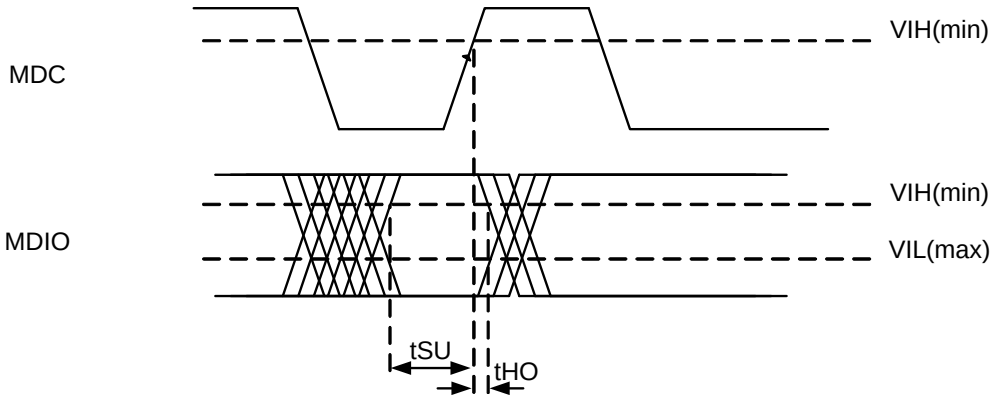


Figure 19: SMI Master Mode Input AC Timing Diagram



9.6.6 SDRAM DDR2 Interface AC Timing

9.6.6.1 SDRAM DDR2 400 MHz Interface AC Timing Table

Table 42: SDRAM DDR2 400 MHz Interface AC Timing Table

Description	Symbol	400 MHz @ 1.8V		Units	Notes
		Min	Max		
Clock frequency	fCK	400.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	0.38	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.38	-	ns	-
DQ and DM output pulse width	tDIPW	0.35	-	tCK(avg)	-
DQS output high pulse width	tDQSH	0.35	-	tCK(avg)	-
DQS output low pulse width	tDQSL	0.35	-	tCK(avg)	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK(avg)	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK(avg)	1
CLK-CLKn rising edge to DQS output rising edge	tDQSS	-0.11	0.11	tCK(avg)	-
DQS write preamble	tWPRE	0.35	-	tCK(avg)	-
DQS write postamble	tWPST	0.41	-	tCK(avg)	-
CLK-CLKn high-level width	tCH	0.48	0.52	tCK(avg)	1, 2, 3
CLK-CLKn low-level width	tCL	0.48	0.52	tCK(avg)	1, 2, 4
DQ input setup time relative to DQS in transition	tDSI	-0.40	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	0.60	-	ns	-
Address and control output pulse width	tIPW	0.67	-	tCK(avg)	-

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate measured from Vref +/-125 mV).

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

General comment: For Address and Control output timing parameters, refer to the Address Timing table.

General comment: tCK = 1/fCK.

General comment: For all signals, the load is CL = 14 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. Refer to SDRAM DDR2 clock specifications table for more information.
3. tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.
4. tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

Table 43: SDRAM DDR2 400 MHz Interface Address and Control Timing Table

Description	Symbol	400 MHz @ 1.8V		Units	Notes
		Min	Max		
Address and Control invalid output time before CLK-CLkn rising edge	tAOIB	-	0.20	ns	1, 3
Address and Control invalid output time after CLK-CLKn rising edge	tAOIA	-	0.40	ns	1, 3
Address and Control valid output time before CLK-CLkn rising edge	tAOVB	0.95	-	ns	1, 2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	0.95	-	ns	1, 2
Address and Control valid output time before CLK-CLkn rising edge	tAOVB	1.50	-	ns	1, 4
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	0.45	-	ns	1, 4

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: For all signals, the load is CL = 14 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. This timing value is defined when Address and Control signals are output on CLK-CLKn falling edge.
   For more information, see register settings.
3. This timing value is defined when Address and Control signals are output on CLK-CLKn rising edge
   (1T and 2T configurations). For more information, see register settings.
4. This timing value is defined when Address and Control signals are output ¼ cycle after CLK-CLKn rising edge.

9.6.6.2 SDRAM DDR2 400 MHz Clock Specifications

Table 44: SDRAM DDR2 400 MHz Clock Specifications

Description	Symbol	Min	Max	Units	Notes
Clock period jitter	tJIT(per)	-100	100	ps	1
Clock perior jitter during DLL locking period	tJIT(per,lck)	-80	80	ps	2
Cycle to cycle clock period jitter	tJIT(cc)	-200	200	ps	3
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-160	160	ps	4
Cumulative error across 2 cycles	tERR(2per)	-150	150	ps	5
Cumulative error across 3 cycles	tERR(3per)	-175	175	ps	5
Cumulative error across 4 cycles	tERR(4per)	-200	200	ps	5
Cumulative error across 5 cycles	tERR(5per)	-200	200	ps	5
Cumulative error across n cycles, n=6...10, inclusive	tERR(6-10per)	-300	300	ps	5
Cumulative error across n cycles, n=11…50, inclusive	tERR(11-50per)	-450	450	ps	5
Duty cycle jitter	tJIT(duty)	-100	100	ps	6
Absolute clock period	tCK(abs)	See note 7		ps	7
Absolute clock high pulse width	tCH(abs)	See note 8		ps	8
Absolute clock low pulse width	tCL(abs)	See note 9		ps	9

Notes:

General comment: All timing values are defined on CLK / CLKn crossing point, unless otherwise specified.

1. tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).
   tJIT(per) = Min/max of {tCKi- tCK(avg) where i=1 to 200}.
   tJIT(per) defines the single period jitter when the DLL is already locked.
2. tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
3. tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of |tCKi+1 – tCKi|.
   tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
4. tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
5. tERR(nper) is defined as the cumulative error across multiple consecutive cycles from tCK(avg).
   Refer to JEDEC Standard No. 79-2 (DDR2 SDRAM Specification) for more information.
6. tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of
   any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).
   tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)} where,
   tJIT(CH) = {tCHi- tCH(avg) where i=1 to 200}; tJIT(CL) = {tCLi- tCL(avg) where i=1 to 200}.
7. tCK(abs),min = tCK(avg),min + tJIT(per),min; tCK(abs),max = tCK(avg),max + tJIT(per),max.
8. tCH(abs),min = tCH(avg),min x tCK(avg),min + tJIT(duty),min; tCH(abs),max = tCH(avg),max x tCK(avg),max + tJIT(duty),max.
9. tCL(abs),min = tCL(avg),min x tCK(avg),min + tJIT(duty),min; tCL(abs),max = tCL(avg),max x tCK(avg),max + tJIT(duty),max.

9.6.6.3 SDRAM DDR2 333 MHz Interface AC Timing Table

Table 45: SDRAM DDR2 333 MHz Interface AC Timing Table

Description	Symbol	333 MHz @ 1.8V		Units	Notes
		Min	Max		
Clock frequency	fCK	333.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	0.45	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.45	-	ns	-
DQ and DM output pulse width	tDIPW	0.35	-	tCK(avg)	-
DQS output high pulse width	tDQSH	0.35	-	tCK(avg)	-
DQS output low pulse width	tDQSL	0.35	-	tCK(avg)	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK(avg)	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK(avg)	1
CLK-CLKn rising edge to DQS output rising edge	tDQSS	-0.11	0.11	tCK(avg)	-
DQS write preamble	tWPRE	0.35	-	tCK(avg)	-
DQS write postamble	tWPST	0.41	-	tCK(avg)	-
CLK-CLKn high-level width	tCH	0.48	0.52	tCK(avg)	1, 2, 3
CLK-CLKn low-level width	tCL	0.48	0.52	tCK(avg)	1, 2, 4
DQ input setup time relative to DQS in transition	tDSI	-0.50	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	0.75	-	ns	-
Address and control output pulse width	tIPW	0.67	-	tCK(avg)	-

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate measured from Vref +/-125 mV).

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

General comment: For Address and Control output timing parameters, refer to the Address Timing table.

General comment: tCK = 1/fCK.

General comment: For all signals, the load is CL = 14 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. Refer to SDRAM DDR2 clock specifications table for more information.
3. tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.
4. tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

Table 46: SDRAM DDR2 333 MHz Interface Address and Control Timing Table

Description	Symbol	333 MHz @ 1.8V		Units	Notes
		Min	Max		
Address and Control invalid output time before CLK-CLkn rising edge	tAOIB	-	0.28	ns	1, 3
Address and Control invalid output time after CLK-CLKn rising edge	tAOIA	-	0.28	ns	1, 3
Address and Control valid output time before CLK-CLkn rising edge	tAOVB	1.00	-	ns	1, 2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	1.00	-	ns	1, 2

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: For all signals, the load is CL = 14 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. This timing value is defined when Address and Control signals are output on CLK-CLKn falling edge. For more information, see register settings.
3. This timing value is defined when Address and Control signals are output on CLK-CLKn rising edge (1T and 2T configurations). For more information, see register settings.

9.6.6.4 SDRAM DDR2 333 MHz Clock Specifications

Table 47: SDRAM DDR2 333 MHz Clock Specifications

Description	Symbol	Min	Max	Units	Notes
Clock period jitter	tJIT(per)	-125	125	ps	1
Clock perior jitter during DLL locking period	tJIT(per,lck)	-100	100	ps	2
Cycle to cycle clock period jitter	tJIT(cc)	-250	250	ps	3
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-200	200	ps	4
Cumulative error across 2 cycles	tERR(2per)	-175	175	ps	5
Cumulative error across 3 cycles	tERR(3per)	-225	225	ps	5
Cumulative error across 4 cycles	tERR(4per)	-250	250	ps	5
Cumulative error across 5 cycles	tERR(5per)	-250	250	ps	5
Cumulative error across n cycles, n=6...10, inclusive	tERR(6-10per)	-350	350	ps	5
Cumulative error across n cycles, n=11…50, inclusive	tERR(11-50per)	-450	450	ps	5
Duty cycle jitter	tJIT(duty)	-125	125	ps	6
Absolute clock period	tCK(abs)	See note 7		ps	7
Absolute clock high pulse width	tCH(abs)	See note 8		ps	8
Absolute clock low pulse width	tCL(abs)	See note 9		ps	9

Notes:

General comment: All timing values are defined on CLK / CLKn crossing point, unless otherwise specified.

1. tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).
   tJIT(per) = Min/max of {tCKi- tCK(avg) where i=1 to 200}.
   tJIT(per) defines the single period jitter when the DLL is already locked.
2. tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
3. tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of |tCKi+1 – tCKi|.
   tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
4. tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
5. tERR(nper) is defined as the cumulative error across multiple consecutive cycles from tCK(avg).
   Refer to JEDEC Standard No. 79-2 (DDR2 SDRAM Specification) for more information.
6. tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of
   any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).
   tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)} where,
   tJIT(CH) = {tCHi- tCH(avg) where i=1 to 200}; tJIT(CL) = {tCLi- tCL(avg) where i=1 to 200}.
7. tCK(abs),min = tCK(avg),min + tJIT(per),min; tCK(abs),max = tCK(avg),max + tJIT(per),max.
8. tCH(abs),min = tCH(avg),min x tCK(avg),min + tJIT(duty),min; tCH(abs),max = tCH(avg),max x tCK(avg),max + tJIT(duty),max.
9. tCL(abs),min = tCL(avg),min x tCK(avg),min + tJIT(duty),min; tCL(abs),max = tCL(avg),max x tCK(avg),max + tJIT(duty),max.

9.6.6.5 SDRAM DDR2 266 MHz Interface AC Timing Table

Table 48: SDRAM DDR2 266 MHz Interface AC Timing Table

Description	Symbol	266 MHz @ 1.8V		Units	Notes
		Min	Max		
Clock frequency	fCK	266.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	0.42	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.42	-	ns	-
DQ and DM output pulse width	tDIPW	0.35	-	tCK	-
DQS output high pulse width	tDQSH	0.35	-	tCK	-
DQS output low pulse width	tDQSL	0.35	-	tCK	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK	1
CLK-CLKn rising edge to DQS output rising edge	tDQSS	-0.11	0.11	tCK	-
DQS write preamble	tWPRE	0.35	-	tCK	-
DQS write postamble	tWPST	0.41	-	tCK	-
CLK-CLKn high-level width	tCH	0.45	0.55	tCK	1
CLK-CLKn low-level width	tCL	0.45	0.55	tCK	1
DQ input setup time relative to DQS in transition	tDSI	-0.50	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	1.20	-	ns	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	2.90	-	ns	1, 2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	0.30	-	ns	1, 2
Address and control output pulse width	tIPW	0.67	-	tCK	-

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate measured from Vref +/-125 mV).

General comment: tCK = 1/fCK.

General comment: For all signals, the load is CL = 16 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. This timing value is defined when Address and Control signals are output ¼tCK after CLK-CLKn rising edge.

   For more information, see register settings.

9.6.6.6 SDRAM DDR2 200 MHz Interface AC Timing Table

Table 49: SDRAM DDR2 200 MHz Interface AC Timing Table

Description	Symbol	200 MHz @ 1.8V		Units	Notes
		Min	Max		
Clock frequency	fCK	200.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	0.50	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.50	-	ns	-
DQ and DM output pulse width	tDIPW	0.35	-	tCK	-
DQS output high pulse width	tDQSH	0.35	-	tCK	-
DQS output low pulse width	tDQSL	0.35	-	tCK	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK	1
CLK-CLKn rising edge to DQS output rising edge	tDQSS	-0.11	0.11	tCK	-
DQS write preamble	tWPRE	0.35	-	tCK	-
DQS write postamble	tWPST	0.41	-	tCK	-
CLK-CLKn high-level width	tCH	0.45	0.55	tCK	1
CLK-CLKn low-level width	tCL	0.45	0.55	tCK	1
DQ input setup time relative to DQS in transition	tDSI	-0.55	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	1.50	-	ns	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	2.25	-	ns	1, 2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	0.80	-	ns	1, 2
Address and control output pulse width	tIPW	0.67	-	tCK	-

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate measured from Vref +/-125 mV).

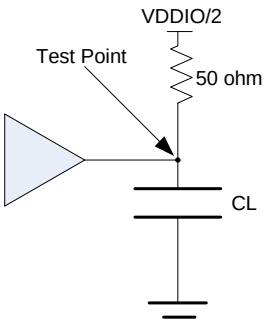
General comment: tCK = 1/fCK.

General comment: For all signals, the load is CL = 16 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. This timing value is defined when Address and Control signals are output ¼tCK after CLK-CLKn rising edge.
   For more information, see register settings.

9.6.6.7 SDRAM DDR2 Interface Test Circuit

Figure 20: SDRAM DDR2 Interface Test Circuit



9.6.6.8 SDRAM DDR2 Interface AC Timing Diagrams

Figure 21: SDRAM DDR2 Interface Write AC Timing Diagram

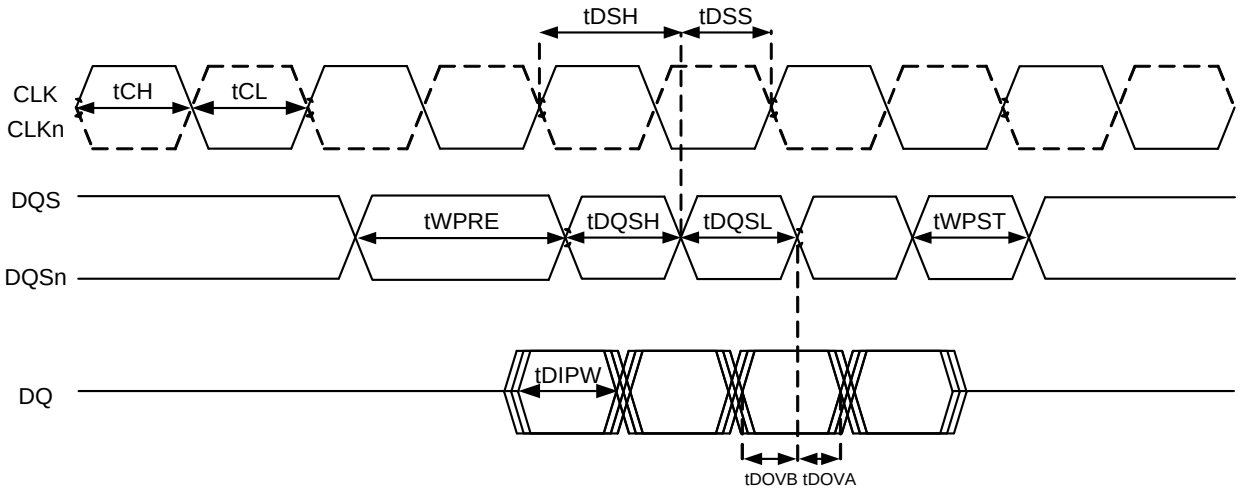


Figure 22: SDRAM DDR2 Interface Address and Control AC Timing Diagram

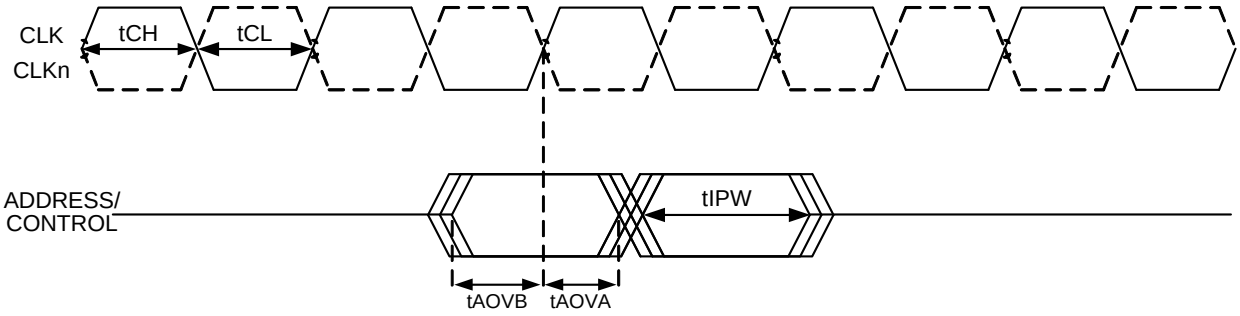
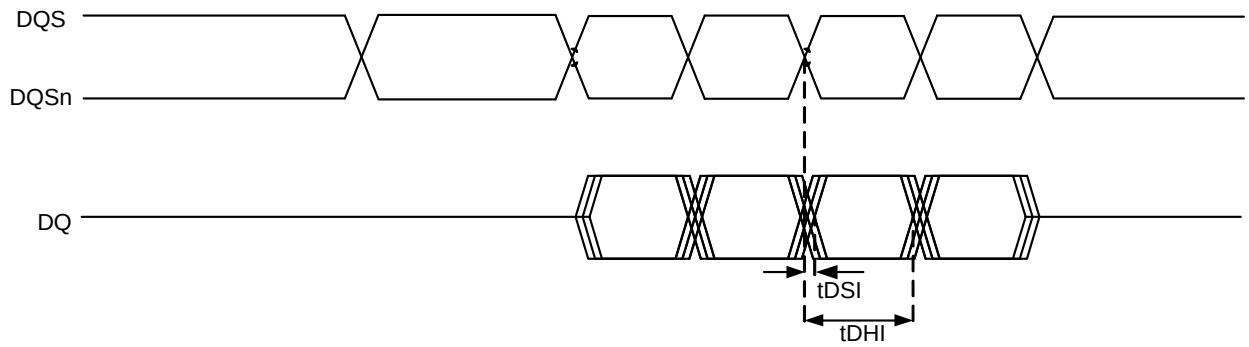


Figure 23: SDRAM DDR2 Interface Read AC Timing Diagram



9.6.7 Serial Peripheral Interface (SPI) AC Timing

9.6.7.1 SPI (Master Mode) AC Timing Table

Table 50: SPI (Master Mode) AC Timing Table

Description	Symbol	SPI		Units	Notes
		Min	Max		
SCLK clock frequency	fCK	See Note 3		MHz	3
SCLK high time	tCH	0.46	-	tCK	1
SCLK low time	tCL	0.46	-	tCK	1
SCLK slew rate	tSR	0.5	-	V/ns	1
Data out valid relative to SCLK falling edge	tDOV	-2.5	2.5	ns	1
CS active before SCLK rising edge	tCSB	8.0	-	ns	1
CS not active after SCLK rising edge	tCSA	8.0	-	ns	1
Data in setup time relative to SCLK rising edge	tSU	0.2	-	tCK	2
Data in hold time relative to SCLK rising edge	tHD	5.0	-	ns	2

Notes:

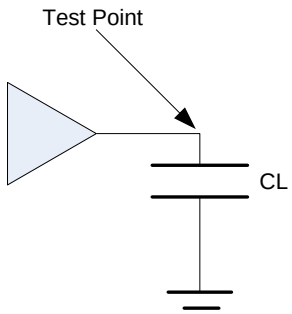
General comment: All values were measured from 0.3*vddio to 0.7*vddio, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. Defined from vddio/2 to vddio/2.
3. See "Reference Clocks" table for more details.

9.6.7.2 SPI (Master Mode) Test Circuit

Figure 24: SPI (Master Mode) Test Circuit



9.6.7.3 SPI (Master Mode) Timing Diagrams

Figure 25: SPI (Master Mode) Normal Output AC Timing Diagram

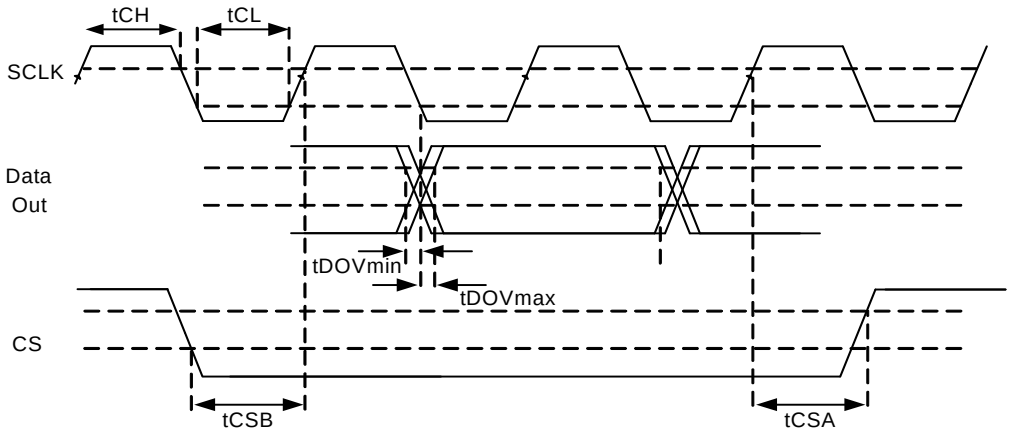


Figure 26: SPI (Master Mode) Normal Input AC Timing Diagram

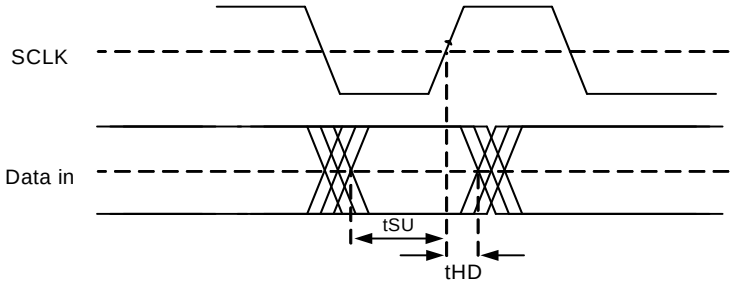


Figure 27: SPI (Master Mode) Opposite Output AC Timing Diagram

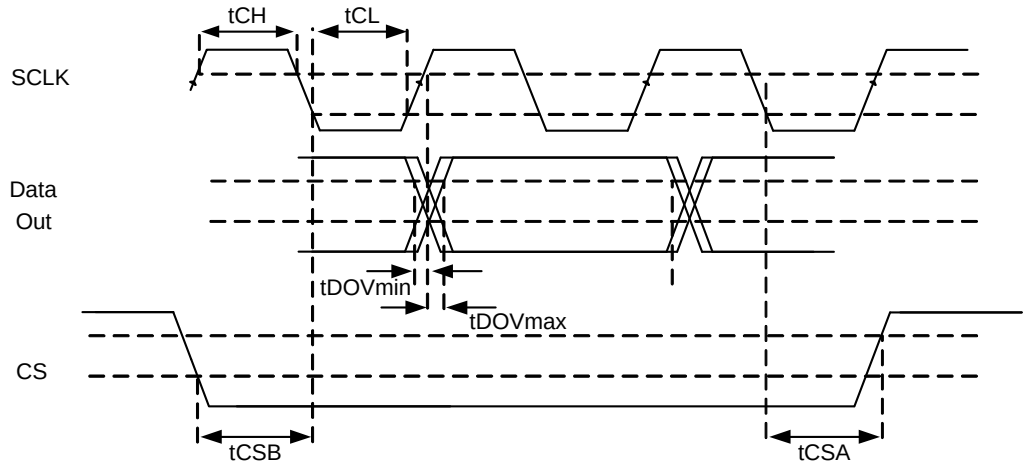
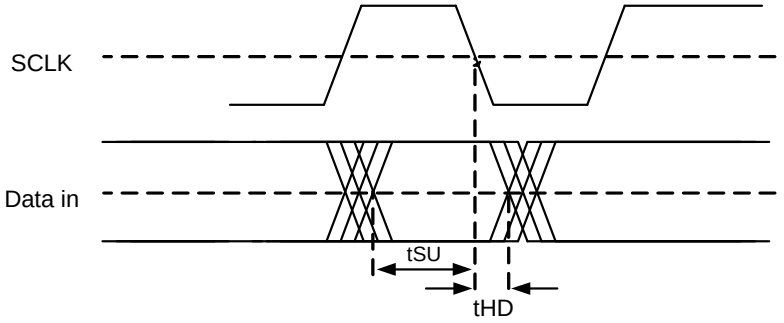


Figure 28: SPI (Master Mode) Opposite Input AC Timing Diagram



9.6.8 Two-Wire Serial Interface (TWSI) AC Timing

9.6.8.1 TWSI AC Timing Table

Table 51: TWSI Master AC Timing Table

Description	Symbol	Min	Max	Units	Notes
SCK clock frequency	fCK	See note 1		kHz	1
SCK minimum low level width	tLOW	0.47	-	tCK	2
SCK minimum high level width	tHIGH	0.40	-	tCK	2
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	2, 3
SDA and SCK fall time	tf	-	300.0	ns	2, 3
SDA output delay relative to SCK falling edge	tOV	0.0	0.4	tCK	2

Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. See "Reference Clocks" table for more details.
2. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
3. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

Table 52: TWSI Slave AC Timing Table

Description	Symbol	100 kHz (Max)		Units	Notes
		Min	Max		
SCK minimum low level width	tLOW	4.7	-	us	1
SCK minimum high level width	tHIGH	4.0	-	us	1
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	1, 2
SDA and SCK fall time	tf	-	300.0	ns	1, 2
SDA output delay relative to SCK falling edge	tOV	0.0	4.0	us	1

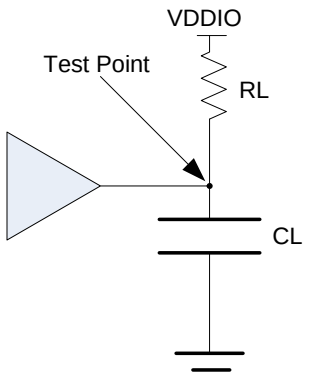
Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

9.6.8.2 TWSI Test Circuit

Figure 29: TWSI Test Circuit



9.6.8.3 TWSI AC Timing Diagrams

Figure 30: TWSI Output Delay AC Timing Diagram

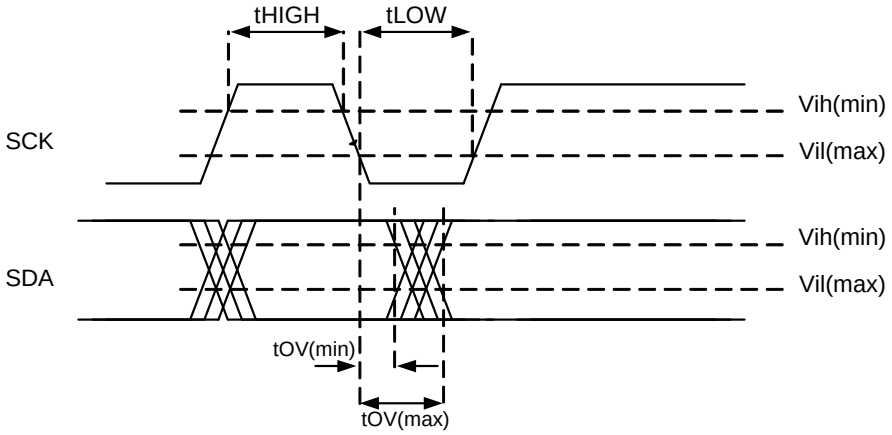
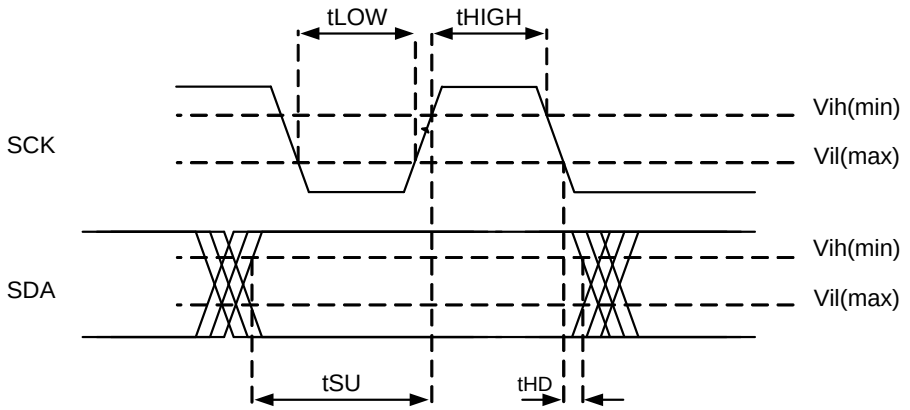


Figure 31: TWSI Input AC Timing Diagram



9.6.9 Device Bus Interface AC Timing

9.6.9.1 Device Bus Interface AC Timing Table

Table 53: Device Bus Interface AC Timing Table (when using TCLK_OUT as the reference clock)

Description	Symbol	Min	Max	Units	Notes
Data/READYn input setup relative to clock rising edge	tSU	3.0	-	ns	-
Data/READYn input hold relative to clock rising edge	tHD	1.0	-	ns	-
Address/Data output delay relative to clock rising edge	tOV	0.8	3.5	ns	1
Address output valid before ALE signal falling edge	tAOAB	7.5	-	ns	1 , 2
Address output valid after ALE signal falling edge	tAOAA	3.5	-	ns	1 , 2

Notes:

General comment: All timing values are for interfacing synchronous devices.

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 10 pF.
2. The AD bus is normally loaded with high capacitance. Make sure to work according to HW design guidelines or simulations in order to meet the latch AC timing requirements.

Table 54: Device Bus Interface AC Timing Table (when using TCLK_IN as the reference clock)

Description	Symbol	Min	Max	Units	Notes
Data/READYn input setup relative to clock rising edge	tSU	1.5	-	ns	-
Data/READYn input hold relative to clock rising edge	tHD	0.5	-	ns	-
Address/Data output delay relative to clock rising edge	tOV	1.5	3.0	ns	1
Address output valid before ALE signal falling edge	tAOAB	5.2	-	ns	1 , 2
Address output valid after ALE signal falling edge	tAOAA	2.8	-	ns	1 , 2

Notes:

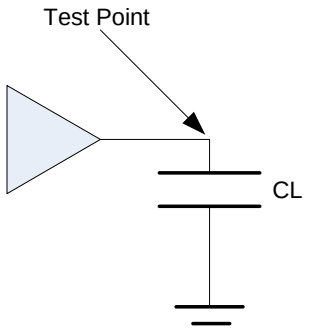
General comment: All timing values are for interfacing synchronous devices.

General comment: All values are defined on VDDIO/2.2, unless otherwise specified.

1. For all signals, the load is CL = 5 pF.
2. The AD bus is normally loaded with high capacitance. Make sure to work according to HW design guide lines or simulations in order to meet the latch AC timing requirements.

9.6.9.2 Device Bus Interface Test Circuit

Figure 32: Device Bus Interface Test Circuit



9.6.9.3 Device Bus Interface AC Timing Diagram

Figure 33: Device Bus Interface Output Delay AC Timing Diagram

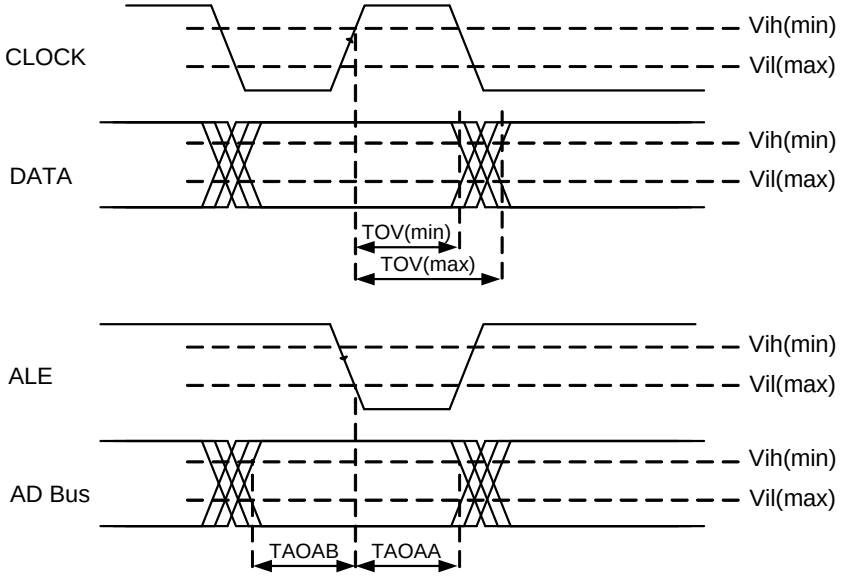
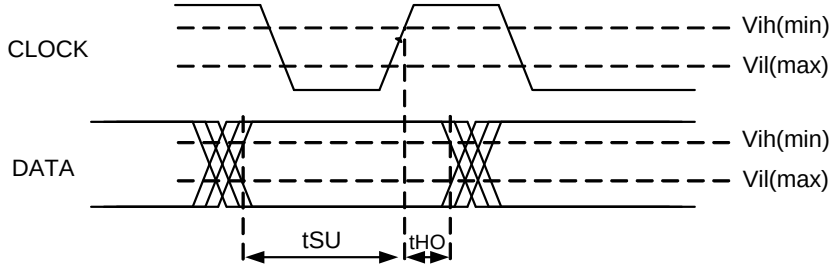


Figure 34: Device Bus Interface Input AC Timing Diagram



9.6.10 JTAG Interface AC Timing

9.6.10.1 JTAG Interface AC Timing Table

Table 55: JTAG Interface 30 MHz AC Timing Table

Description	Symbol	30 MHz		Units	Notes
		Min	Max		
JTClk frequency	fCK	30.0		MHz	-
JTClk minimum pulse width	Tpw	0.45	0.55	tCK	-
JTClk rise/fall slew rate	Sr/Sf	0.50	-	V/ns	2
JTRSTn active time	Trst	1.0	-	ms	-
TMS, TDI input setup relative to JTClk rising edge	Tsetup	6.67	-	ns	-
TMS, TDI input hold relative to JTClk rising edge	Thold	13.0	-	ns	-
JTClk falling edge to TDO output delay	Tprop	1.0	8.33	ns	1

Notes:

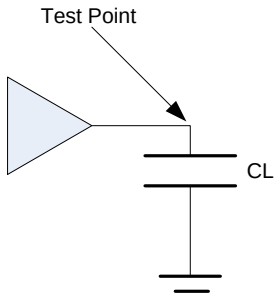
General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 10 pF.
2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.

9.6.10.2 JTAG Interface Test Circuit

Figure 35: JTAG Interface Test Circuit



9.6.10.3 JTAG Interface AC Timing Diagrams

Figure 36: JTAG Interface Output Delay AC Timing Diagram

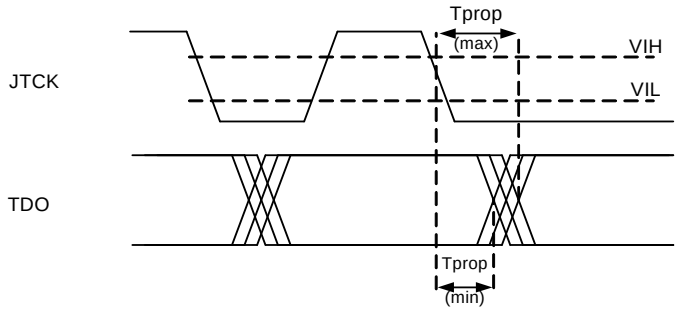
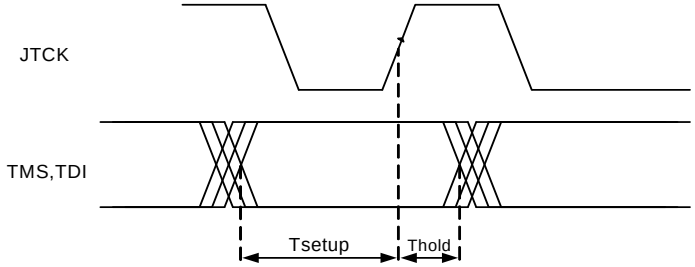


Figure 37: JTAG Interface Input AC Timing Diagram



9.6.11 Time Division Multiplexing (TDM) Interface AC Timing

9.6.11.1 TDM Interface AC Timing Table

Table 56: TDM Interface AC Timing Table

Description	Symbol	16.384 MHz		Units	Notes
		Min	Max		
PCLK cycle time	1/tC	0.256	16.384	MHz	1, 3
PCLK duty cycle	tDTY	0.4	0.6	tC	1
PCLK rise/fall time	tR/tF	-	3.0	ns	1, 2, 8
DTX and FSYNC valid after PCLK rising edge	tD	0.0	10.0	ns	1, 4, 6
DRX and FSYNC setup time relative to PCLK falling edge	tSU	5.0	-	ns	5, 7
DRX and FSYNC hold time relative to PCLK falling edge	tHD	5.0	-	ns	5, 7

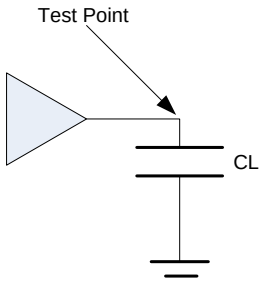
Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

1. For all signals, the load is CL = 20 pF.
2. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
3. PCLK can be configured to 0.256, 0.512, 0.768, 1.024, 1.536, 2.048, 4.096, 8.192, 16.384 MHz frequencies only.
4. This parameter is relevant to FSYNC signal in master-mode only.
5. This parameter is relevant to FSYNC signal in slave-mode only.
6. In negative-mode, the DTX signal is relative to PCLK falling edge.
7. In negative-mode, the DRX signal is relative to PCLK rising edge.
8. This parameter is relevant when the PCLK pin is output.

9.6.11.2 TDM Interface Test Circuit

Figure 38: TDM Interface Test Circuit



9.6.11.3 TDM Interface Timing Diagrams

Figure 39: TDM Interface Output Delay AC Timing Diagram

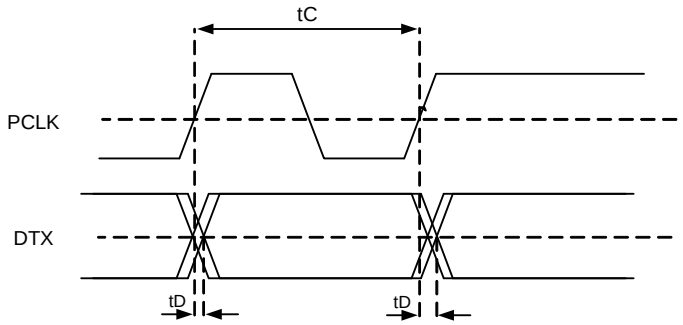
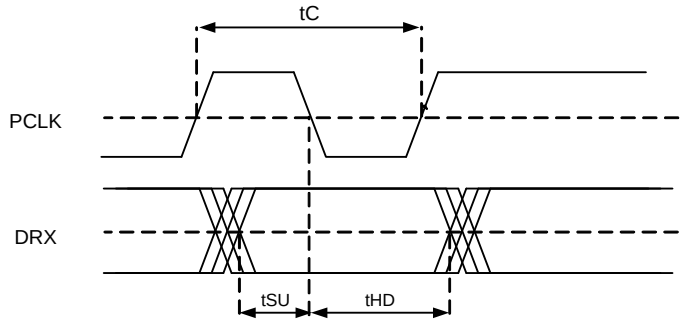


Figure 40: TDM Interface Input Delay AC Timing Diagram



9.7 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the following differential interfaces:

- PCI Express (PCIe) Interface Electrical Characteristics
- SATA Interface Electrical Characteristics
- USB Interface Electrical Characteristics

9.7.1 Differential Interface Reference Clock Characteristics

9.7.1.1 PCI Express Interface Differential Reference Clock Characteristics

Table 58

Note The reference clock characteristics in Table 58 is relevant for the PEX0_CLK_P, PEX0_CLK_N, PEX1_CLK_P, PEX1_CLK_N pins.

Table 57: PCI Express Interface Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	100.0		MHz	-
Clock duty cycle	DCrefclk	0.4	0.6	tCK	-
Differential rising/falling slew rate	SRrefclk	0.6	4.0	V/nS	3
Differential high voltage	VIHrefclk	150.0	-	mV	-
Differential low voltage	VILrefclk	-	-150.0	mV	-
Absolute crossing point voltage	Vcross	250.0	550.0	mV	1
Variation of Vcross over all rising clock edges	Vcrs_dlta	-	140.0	mV	1
Average differential clock period accuracy	Tperavg	-300.0	2800.0	ppm	-
Absolute differential clock period	Tperabs	9.8	10.2	nS	2
Differential clock cycle-to-cycle jitter	Tccjit	-	150.0	pS	-

Notes:

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 1.1, March 2005, section 2.1.3 for more information.

1. Defined on a single-ended signal.
2. Including jitter and spread spectrum.
3. Defined from -150 mV to +150 mV on the differential waveform.

PCI Express Interface Spread Spectrum Requirements

Table 58: PCI Express Interface Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	0.0	33.0	kHz	1
Fspread	-0.5	0.0	%	1

Notes:
1. Defined on linear sweep or “Hershey’s Kiss” (US Patent 5,631,920) modulations.

9.7.2 PCI Express (PCIe) Interface Electrical Characteristics

9.7.2.1 PCI Express Interface Driver and Receiver Characteristics

Table 59: PCI Express Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	2.5		Gbps	-
Unit interval	UI	400.0		ps	-
Baud rate tolerance	Bppm	-300.0	300.0	ppm	2
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.75	-	UI	-
Differential return loss	TRLdiff	10.0	-	dB	1
Common mode return loss	TRLcm	6.0	-	dB	1
DC differential TX impedance	ZTXdiff	80.0	120.0	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.175	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss	RRLdiff	10.0	-	dB	1
Common mode return loss	RRLcm	6.0	-	dB	1
DC differential RX impedance	ZRXdiff	80.0	120.0	Ohm	-
DC common input impedance	ZRXcm	40.0	60.0	Ohm	-

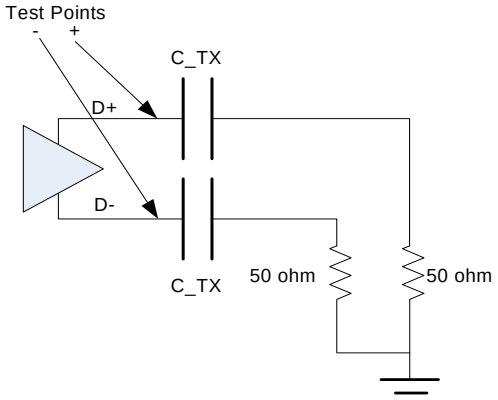
Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.1, March, 2005.

1. Defined from 50 MHz to 1.25 GHz.
2. Does not account for SSC dictated variations.

9.7.2.2 PCI Express Interface Test Circuit

Figure 41: PCI Express Interface Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

9.7.3 SATA Interface Electrical Characteristics

9.7.3.1 SATA I Interface Gen1 Mode Driver and Receiver Characteristics

Table 60: SATA I Interface Gen1i Mode Driver and Receiver Characteristicss

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	1.5		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	666.67		ps	-
Driver Parameters					
Differential impedance	Zdifftx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLOD	14.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLOD	8.0	-	dB	-
Differential return loss (300 MHz-1.2 GHz)	RLOD	6.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLOD	3.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	1.0	-	dB	-
Output differential voltage	Vdifftx	400.0	600.0	mV	2
Total jitter at connector data-data, 5UI	TJ5	-	0.355	UI	1
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.175	UI	-
Total jitter at connector data-data, 250UI	TJ250	-	0.470	UI	1
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.220	UI	-
Receiver Parameters					
Differential impedance	Zdiffrx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLID	18.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLID	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	10.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	8.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	3.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	1.0	-	dB	-
Input differential voltage	Vdiffrx	325.0	600.0	mV	-
Total jitter at connector data-data, 5UI	TJ5	-	0.430	UI	1
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.250	UI	-
Total jitter at connector data-data, 250UI	TJ250	-	0.600	UI	1
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.350	UI	-

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Total jitter is defined as TJ = (14 * RJσ) + DJ where Rjσ is random jitter.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See functional register description for more details.

Table 61: SATA I Interface Gen1m Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	1.5		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	666.67		ps	-
Driver Parameters					
Differential impedance	Zdifftx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLOD	14.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLOD	8.0	-	dB	-
Differential return loss (300 MHz-1.2 GHz)	RLOD	6.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLOD	3.0	-	dB	-
Output differential voltage	Vdifftx	400.0	600.0	mV	2
Total jitter at connector data-data, 5UI	TJ5	-	0.355	UI	1
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.175	UI	-
Total jitter at connector data-data, 250UI	TJ250	-	0.470	UI	1
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.220	UI	-
Receiver Parameters					
Differential impedance	Zdiffrx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLID	18.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLID	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	10.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	8.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	3.0	-	dB	-
Input differential voltage	Vdiffrx	240.0	600.0	mV	-
Total jitter at connector data-data, 5UI	TJ5	-	0.430	UI	1
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.250	UI	-
Total jitter at connector data-data, 250UI	TJ250	-	0.600	UI	1
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.350	UI	-

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Total jitter is defined as TJ = (14 * RJσ) + DJ where Rjσ is random jitter.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See functional register description for more details.

9.7.3.2 SATA II Interface Gen2 Mode Driver and Receiver Characteristics

Table 62: SATA II Interface Gen2i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.0		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	333.33		ps	-
Driver Parameters					
Output differential voltage	Vdifftx	400.0	700.0	mV	1 , 2
Differential return loss (150 MHz-300 MHz)	RLOD	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLOD	8.0	-	dB	-
Differential return loss (600 MHz-2.4 GHz)	RLOD	6.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLOD	1.0	-	dB	-
Total jitter at connector clock-data	TJ10	-	0.30	UI	3
Deterministic jitter at connector clock-data	DJ10	-	0.17	UI	3
Total jitter at connector clock-data	TJ500	-	0.37	UI	4
Deterministic jitter at connector clock-data	DJ500	-	0.19	UI	4
Receiver Parameters					
Input differential voltage	Vdiffrx	275.0	750.0	mV	5
Differential return loss (150 MHz-300 MHz)	RLID	18.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	14.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	10.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	8.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLID	1.0	-	dB	-
Total jitter at connector clock-data	TJ10	-	0.46	UI	3
Deterministic jitter at connector clock-data	DJ10	-	0.35	UI	3
Total jitter at connector clock-data	TJ500	-	0.60	UI	4
Deterministic jitter at connector clock-data	DJ500	-	0.42	UI	4

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See functional register description for more details.
3. Defined for BR/10.
4. Defined for BR/500.
5. 0.5 UI is the point where the signal meets the minimum level.

Table 63: SATA II Interface Gen2m Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.0		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	333.33		ps	-
Driver Parameters					
Output differential voltage	Vdifftx	400.0	700.0	mV	1 , 2
Differential return loss (150 MHz-300 MHz)	RLOD	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLOD	8.0	-	dB	-
Differential return loss (600 MHz-2.4 GHz)	RLOD	6.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	3.0	-	dB	-
Total jitter at connector clock-data	TJ10	-	0.30	UI	3
Deterministic jitter at connector clock-data	DJ10	-	0.17	UI	3
Total jitter at connector clock-data	TJ500	-	0.37	UI	4
Deterministic jitter at connector clock-data	DJ500	-	0.19	UI	4
Receiver Parameters					
Input differential voltage	Vdiffrx	240.0	750.0	mV	5
Differential return loss (150 MHz-300 MHz)	RLID	18.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	14.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	10.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	8.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	3.0	-	dB	-
Total jitter at connector clock-data	TJ10	-	0.46	UI	3
Deterministic jitter at connector clock-data	DJ10	-	0.35	UI	3
Total jitter at connector clock-data	TJ500	-	0.60	UI	4
Deterministic jitter at connector clock-data	DJ500	-	0.42	UI	4

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See functional register description for more details.
3. Defined for BR/10.
4. Defined for BR/500.
5. 0.5 UI is the point where the signal meets the minimum level.

9.7.4 USB Interface Electrical Characteristics

9.7.4.1 USB Driver and Receiver Characteristics

Table 64: USB Low Speed Driver and Receiver Characteristics

Description	Symbol	Low Speed		Units	Notes
		Min	Max		
Baud Rate	BR	1.5		Mbps	-
Baud rate tolerance	Bppm	-15000.0	15000.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	3
Data fall time	TLR	75.0	300.0	ns	3, 4
Data rise time	TLF	75.0	300.0	ns	3, 4
Rise and fall time matching	TLRFM	80.0	125.0	%	-
Source jitter total: to next transition	TUDJ1	-95.0	95.0	ns	5
Source jitter total: for paired transitions	TUDJ2	-150.0	150.0	ns	5
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. See "Data Signal Rise and Fall Time" waveform.
4. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
5. Including frequency tolerance. Timing difference between the differential data signals.

   Defined at crossover point of differential data signals.

Table 65: USB Full Speed Driver and Receiver Characteristics

Description	Symbol	Full Speed		Units	Notes
		Min	Max		
Baud Rate	BR	12.0		Mbps	-
Baud rate tolerance	Bppm	-2500.0	2500.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	4
Output rise time	TFR	4.0	20.0	ns	3, 4
Output fall time	TFL	4.0	20.0	ns	3, 4
Source jitter total: to next transition	TDJ1	-3.5	3.5	ns	5, 6
Source jitter total: for paired transitions	TDJ2	-4.0	4.0	ns	5, 6
Source jitter for differential transition to SE0 transition	TFDEOP	-2.0	5.0	ns	6
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-
Receiver jitter : to next transition	tJR1	-18.5	18.5	ns	6
Receiver jitter: for paired transitions	tJR2	-9.0	9.0	ns	6

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1.. Defined with 1.425 kilohm pull-up resistor to 3.6V.

2.. Defined with 14.25 kilohm pull-down resistor to ground.

3. Defined from 10% to 90% for rise time and 90% to 10% for fall time.

4. See "Data Signal Rise and Fall Time" waveform.

5. Including frequency tolerance. Timing difference between the differential data signals.

6. Defined at crossover point of differential data signals.

Table 66: USB High Speed Driver and Receiver Characteristics

Description	Symbol	High Speed		Units	Notes
		Min	Max		
Baud Rate	BR	480.0		Mbps	-
Baud rate tolerance	Bppm	-500.0	500.0	ppm	-
Driver Parameters					
Data signaling high	VHSOH	360.0	440.0	mV	-
Data signaling low	VHSOL	-10.0	10.0	mV	-
Data rise time	THSR	500.0	-	ps	1
Data fall time	THSF	500.0	-	ps	1
Data source jitter		See note 2			2
Receiver Parameters					
Differential input signaling levels		See note 3			3
Data signaling common mode voltage range	VHSCM	-50.0	500.0	mV	-
Receiver jitter tolerance		See note 3			3

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
2. Source jitter specified by the "TX eye diagram pattern template" figure.
3. Receiver jitter specified by the "RX eye diagram pattern template" figure.

9.7.4.2 USB Interface Driver Waveforms

Figure 42: Low/Full Speed Data Signal Rise and Fall Time

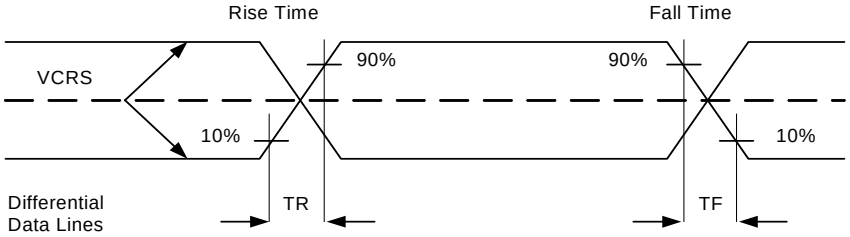


Figure 43: High Speed TX Eye Diagram Pattern Template

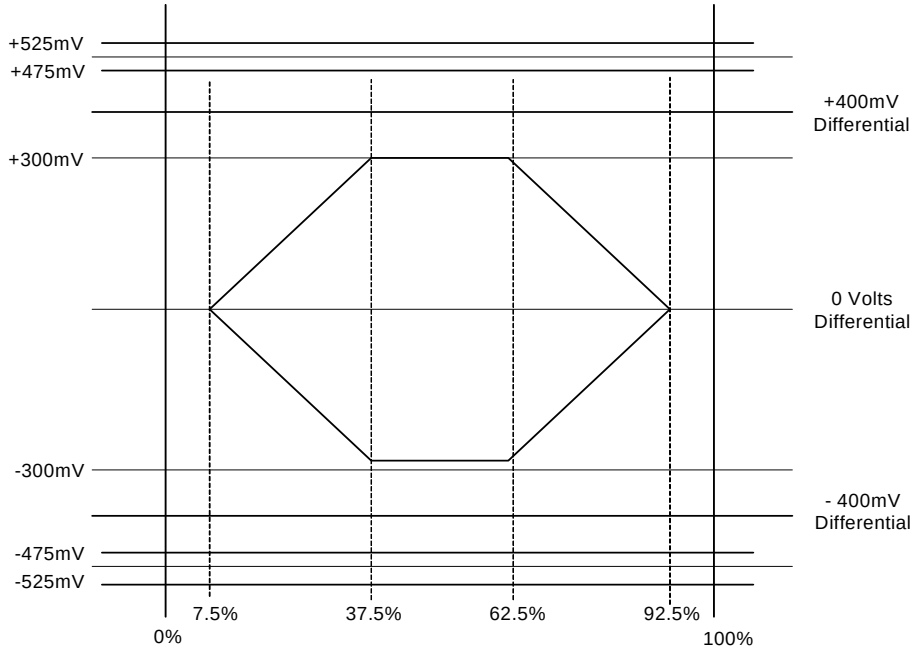
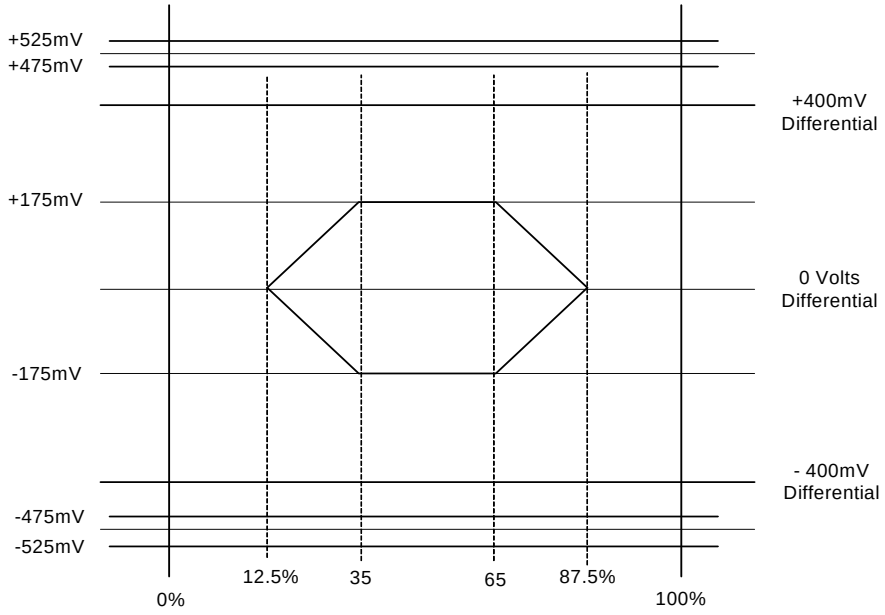


Figure 44: High Speed RX Eye Diagram Pattern Template



10 Thermal Data (Preliminary)

Table 67 provides the package thermal data for the MV78200. This data is derived from simulations that were run according to the JEDEC standard.

Note The thermal parameters are preliminary and subject to change.

The documents listed below provide a basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell® products. Before designing a system it is recommended to refer to these documents:

- Application Note, *AN-63 Thermal Management for Selected Marvell® Products* (Doc. No. MV-S300281-00)
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations*(Doc. No. MV-S700019-00)

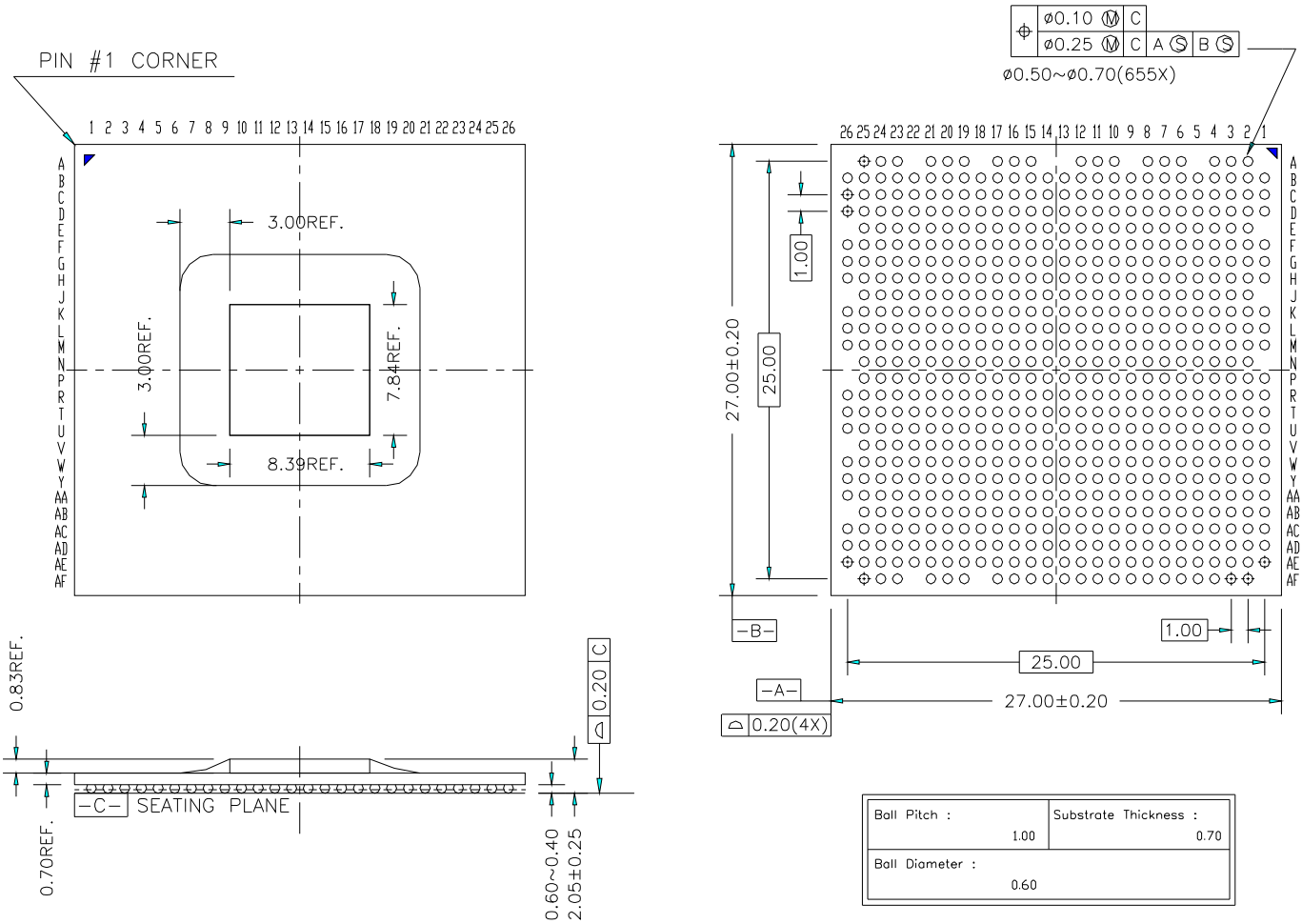
Table 67: Thermal Data for the MV78200 in FCBGA Package

Symbol	Definition	Airflow Value (C/W)		
		0[m/s]	1[m/s]	2[m/s]
θ_{JA}	Thermal resistance: junction to ambient	16.7	15.2	14.4
ψ_{JT}	Thermal characterization parameter: junction to top center	0.3	0.3	0.3
ψ_{JB}	Thermal characterization parameter: junction to board	9.8	9.5	9.4
θ_{JC}	Thermal resistance: junction to case (not air-flow dependent)	0.2		
θ_{JB}	Thermal resistance: junction to board (not air-flow dependent)	14.0		

11 Package Mechanical Dimensions

The MV78200 uses a 655-pin 27 mm x 27 mm FCBGA package with 1 mm pitch.

Figure 45: 655 Pin FCBGA Package and Dimensions



12 Part Order Numbering/Package Marking

Figure 46 is an example of the part order numbering scheme for the MV78200. Refer to Marvell® Field Application Engineers (FAEs) or representatives for further information on die revisions when ordering parts.

Figure 46: Sample Part Number

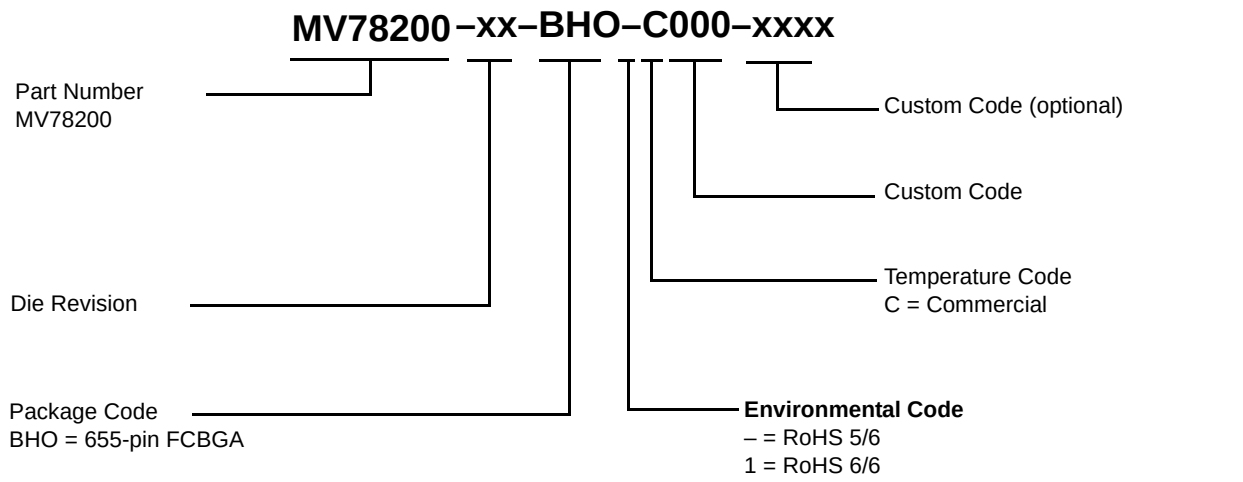
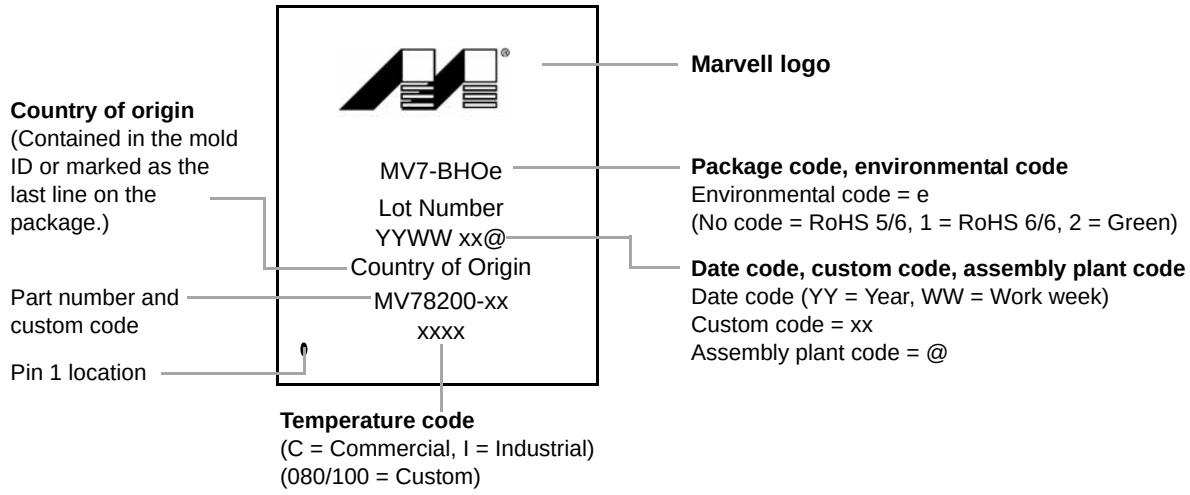


Table 68: MV78200 Part Order Options

Package Type	Part Order Number
655-pin FCBGA	MV78200-A0- BHO-C080 (800 MHz; RoHS 5/6 compliant package)
655-pin FCBGA	MV78200-A0- BHO1C080 (800 MHz; RoHS 6/6 compliant package)
655-pin FCBGA	MV78200-A0- BHO-C100 (1 GHz; RoHS 5/6 compliant package)
655-pin FCBGA	MV78200-A0- BHO1C100 (1 GHz; RoHS 6/6 compliant package)

Figure 47 shows a sample Commercial package marking and pin 1 location for the MV78200.

Figure 47: MV78200 Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate.

13 Revision History

Table 69: Revision History

Document Type	Revision	Date
Release	C	December 6, 2008

Product Overview
- Changed the name of the Feroceon® CPU to Sheeva™.

Section 2, Pin Information:
- Updated the IREF_AVDD signal description Table 3, Power Supply Pins, on page 21.
- Added the SYSRST_OUTn pin to Table 4, Miscellaneous Pin Assignments, on page 23. This signal is multiplexed on the MPP pins.
- Added the M_BB pin to Table 5, DDR SDRAM Interface Pin Assignments, on page 25. The SDRAM battery backup signal trigger is multiplexed on the MPP pins.
- Changed the value to from 5 kilohm to 4.99 kilohm for PEXn_ISET in Table 7, PCI Express Port 0/1 Interface Pin Assignments, on page 30.
- Added a note that some GbE interface pins are connected to the VDD_GE power rail and some pins are connected to the VDDO_D power rail Table 9, Gigabit Ethernet Port Interface Pin Assignments, on page 31.
- Added the SATA0/1_PRESENTn and SATA0/1_ACTn pins to Table 11, SATA II Port 0/1 Interface Pin Assignments, on page 35. These signals are multiplexed on the MPP pins.
- Added SATA0_AVDD and SATA1_AVDD as the power rail for the SATA pins in Table 11.

Section 3, Unused Interface Strapping:
- Updated pull up and pull down resistor values in Table 18, Unused Interface Strapping, on page 41.

Section 7, System Power Up and Reset Settings, on page 53.
- Added power rail information to Table 28, Reset Configuration, on page 56.
- Added 0x2 setting for DEV_AD[13:12] and DEV_AD[19:18].
- Corrected the configuration settings for DEV_AD[30] (NAND Flash Initialization Command) in Table 28 .

Section 9, Electrical Specifications (Preliminary)
- Updated the IREF_VDD to minimum -0.5V to maximum 2.2V in Table 29, Absolute Maximum Ratings, on page 64.
- Revised the IREF_VDD values and VDDO_A/B/C/D minimum and maximum values in the Table 30, Recommended Operating Conditions, on page 66.
- Changed the embedded CPU typical power dissipation to 4200 mW in Table 31, Thermal Power Dissipation, on page 68.

Section 9.6.6, SDRAM DDR2 Interface AC Timing
- Revised Table 43, SDRAM DDR2 400 MHz Interface Address and Control Timing Table, on page 86.
- Added Table 49, SDRAM DDR2 200 MHz Interface AC Timing Table, on page 92.

Section 9.6.7, Serial Peripheral Interface (SPI) AC Timing
- Added AC timing information for this interface.

Section 9.6.9, Device Bus Interface AC Timing
- Changed the minimum values for tAOAB from 5.0 ns to 7.5 ns and tAOAA from 5.0 ns to 3.5 ns in Table 53, Device Bus Interface AC Timing Table (when using TCLK_OUT as the reference clock), on page 101.

Section 9.7, Differential Interface Electrical Characteristics
- Added note that the spread spectrum requirements are defined on a linear sweep or a Hershey's kiss modulation in Table 58, PCI Express Interface Spread Spectrum Requirements, on page 109.

Table 69: Revision History (Continued)

Document Type	Revision	Date
Section 9.7.3, SATA Interface Electrical Characteristics • Added Table 61, SATA I Interface Gen1m Mode Driver and Receiver Characteristics, on page 113 and Table 63, SATA II Interface Gen2m Mode Driver and Receiver Characteristics, on page 115. Section 10, Thermal Data (Preliminary), on page 120. • Updated thermal data. Section 11, Package Mechanical Dimensions, on page 121. • Updated Figure 45, "655 Pin FCBGA Package and Dimensions in Section 11, Package Mechanical Dimensions, on page 121. The capacitors have been removed from the figure.		
Release	B	June 2, 2008
Product Overview • Suppports 40-bit/72-bit DDR2 SDRAM interface • Integrates four 16550-compatible UART ports; also supports DMA based transmit • Integrates a two-channel SLIC/Codec TDM interface • Feroceon® core supports 32-Kbyte I-Cache and 32-Kbyte D-Cache, parity protected • PCI Express port is PCI Express Base 1.1 compliant Section 2, Pin Information: • Updated the IREF_AVDD signal description in Table 3, Power Supply Pins, on page 21. • Added thermal diode pins THERMAL_A/C and TCLK_IN note in TCLK_OUT pin in Table 4, Miscellaneous Pin Assignments, on page 23. • Added pullups on MPP pins • Added M_CLKOUT[2:0] and M_CLKOUTn[2:0] in Table 5, DDR SDRAM Interface Pin Assignments, on page 25 • Revised Table 6, Device Bus Interface Pin Assignments, on page 28 • Updated Table 7, p. 30 added Table 8, PCI Express Common Pin Assignments, on page 30 • Added a note that some GbE interface pins are connected to the VDD_GE power rail and some pins are connected to the VDDO_D power rail in Table 9, Gigabit Ethernet Port Interface Pin Assignments, on page 31. • Added S0_AVDD and S1_AVDD as the power rail for the SATA pins in Table 11, SATA II Port 0/1 Interface Pin Assignments, on page 35 • Changed SPI pins names in Table 13, SPI Interface Pin Assignments, on page 36. • Updated TDM interface signals in Table 15, TDM Interface Pin Assignments, on page 38. • Added power pins to Table 10, USB 2.0 Ports 0/1/2 Interface Pin Assignments, on page 35 and Table 15, TDM Interface Pin Assignments, on page 38 • Changed TWSI1 from VDDO_B to VDDO_A in Table 12, TWSI Interface Pin Assignments, on page 36 Section 4, MV78100 Pin Map and Pin List • Pinout list and map are embedded as an attachment. • Updates are recorded in the pinout Revision History. Section 5, Clocking • Added TCLK:N feature • Updated Figure 3, MV78200 Clocks, on page 46 Section 6, Pin Multiplexing • Updated Note on page 52. • Changed column 0x0 so that device does not wake up in default with multiple pins have same functionality (e.g. multiple pins assigned as GPIO[0]). • Updated UART1 muxing. • Replaced some UA2 and UA3 flow control signals, with UA2 and UA3 data signals (column 0x3) in order to have four UARTs even with three or four GbE ports. • Removed UA1_TXD and UA1_RXD from multiplexing table. • Added UA0 and UA1 CTS/RTS options on DEV_AD[31:28] (to allow for configuring four RGMII ports and still have RGMII signals). • Fixed GPIO muxing. • Updated locations of SYSRST_OUTn. • Removed SYSRST_OUTn from Dev_AD[15] and Dev_WEn[2], and put it on Dev_AD[21,24,29,30,31].		

Table 69: Revision History (Continued)

Document Type	Revision	Date
Section 7, System Power Up and Reset Settings • Added Section 7.1, Power Up/Down Sequence Requirements, on page 53. • Updated Note on page 56. • Added new NF reset strap. • Added DEV_ALE modes strap. • Added more clocking operating points. Section 9, Electrical Specifications (Preliminary) • Updated Section 9.3, Thermal Power Dissipation (Preliminary), on page 68. • Updated Section 9.4, Current Consumption (Preliminary), on page 69. Section 9.6.1, Reference Clock and Reset AC Timing Specifications, on page 74 • Added parameters for an SPI output clock, integrated with the TDM interface. Section 9.6.6, SDRAM DDR2 Interface AC Timing • Replaced 64-bit 333 MHz Interface Timing and Clock Specification tables with 64-bit 400 MHz tables. • Added: • Table 43, SDRAM DDR2 400 MHz Interface Address and Control Timing Table, on page 86 • Table 45, SDRAM DDR2 333 MHz Interface AC Timing Table, on page 88 • Table 47, SDRAM DDR2 333 MHz Clock Specifications, on page 90 • Table 46, SDRAM DDR2 333 MHz Interface Address and Control Timing Table, on page 89 • Table 48, SDRAM DDR2 266 MHz Interface AC Timing Table, on page 91 • Updated Figure 21, SDRAM DDR2 Interface Write AC Timing Diagram, on page 93. • Updated Figure 23, SDRAM DDR2 Interface Read AC Timing Diagram, on page 94. Section 9.6.8, Two-Wire Serial Interface (TWSI) AC Timing • Updated TWSI output waveform Figure 30, TWSI Output Delay AC Timing Diagram, on page 99. Section 9.6.10, JTAG Interface AC Timing, on page 104. • Updated section. Section 9.6.11, Time Division Multiplexing (TDM) Interface AC Timing, on page 106. • Added section. Section 9.7, Differential Interface Electrical Characteristics • Updated Table 57, PCI Express Interface Differential Reference Clock Characteristics, on page 108 to reflect both input and output modes. Section 9.7.3, SATA Interface Electrical Characteristics • In Table 60, SATA I Interface Gen1i Mode Driver and Receiver Characteristicss, on page 112, return loss parameters (TX and RX) were added according to updated standard. Section 10, Thermal Data (Preliminary), on page 120 • Updated section. Section 11, Package Mechanical Dimensions, on page 121 • Updated Figure 45, “655 Pin FCBGA Package and Dimensions. The capacitors have been removed from the figure. Section 12, Part Order Numbering/Package Marking, on page 122 • Updated section.		
Initial Release	A	October 9, 2007

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