Configuration Devices for SRAM-Based LUT Devices

December 2002, ver. 12.2 Data Sheet

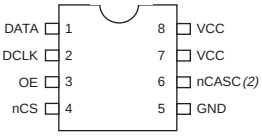
Features

- Serial device family for configuring APEX™ II, APEX 20K (including APEX 20K, APEX 20KC, and APEX 20KE), Mercury™, ACEX® 1K, and FLEX® (FLEX 6000, FLEX 10KE, and FLEX 10KA) devices
- Easy-to-use 4-pin interface to APEX II, APEX 20K, Mercury, ACEX, and FLEX devices
- Low current during configuration and near-zero standby current
- 5.0-V and 3.3-V operation
- Software design support with the Altera® Quartus® II and MAX+PLUS® II development systems for Windows-based PCs as well as Sun SPARCstation, and HP 9000 Series 700/800
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from Data I/O, BP Microsystems, and other manufacturers
- Available in compact plastic packages (see Figures 1 and 2)
  - 8-pin plastic dual in-line package (PDIP)
  - 20-pin plastic J-lead chip carrier (PLCC) package
  - 32-pin plastic thin quad flat pack (TQFP) package
  - 100-pin plastic thin quad flat pack (TQPF) package
  - 88-pin Ultra FineLine BGA™ package
- EPC2 device has reprogrammable Flash configuration memory
  - 5.0-V and 3.3-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface
  - Built-in JTAG boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1
  - ISP circuitry is compatible with IEEE Std. 1532 for EPC2 configuration device
  - Supports programming through Serial Vector Format Files (**.svf**), Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**), Jam STAPL Byte-Code Files (**.jbc**), and the MAX+PLUS II software via the MasterBlaster™, ByteBlasterMV™, or BitBlaster™ download cable
  - `nINIT_CONF` pin allows a JTAG instruction to initiate device configuration
  - Can be programmed with Programmer Object Files (**.pof**) for EPC1 and EPC1441 devices
  - Available in 20-pin PLCC and 32-pin TQFP packages

- EPC4, EPC8, and EPC16 configuration devices have reprogrammable Flash configuration memory with density up to 16,000,000 or 32,000,000 bits with compression feature in these devices.

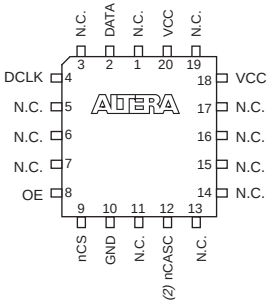
For detailed information on configuration devices, refer to the *Enhanced Configuration Devices (EPC4, EPC8, & EPC16) Data Sheet*.

Figure 1. EPC1, EPC1441, EPC1213, EPC1064, & EPC1064V Package Pin-Out Diagrams *Note (1)*



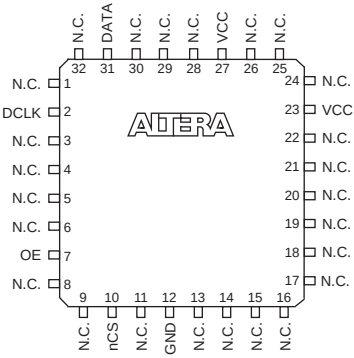
8-Pin PDIP

EPC1
EPC1441
EPC1213
EPC1064
EPC1064V



20-Pin PLCC

EPC1
EPC1441
EPC1213
EPC1064
EPC1064V



32-Pin TQFP

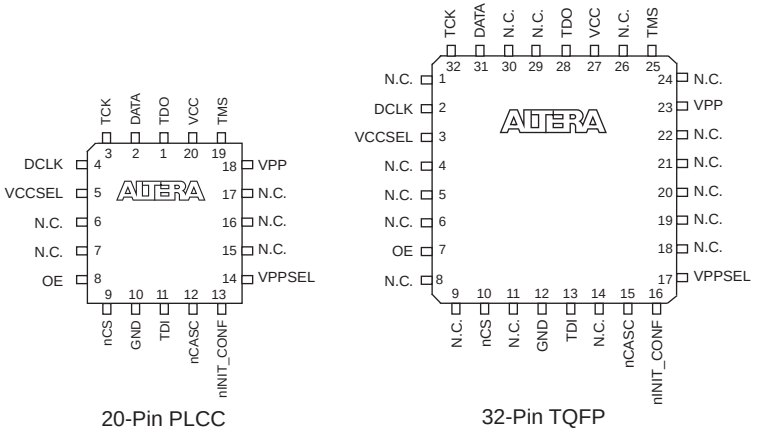
EPC1441
EPC1064
EPC1064V

Notes to Figure 1:

(1) EPC1, EPC1441, EPC1213, and EPC1064 devices are one-time programmable devices. ISP programming is not available in these devices because they do not have JTAG pins.

(2) The nCASC pin is available on EPC1 and EPC1213 devices. On the EPC1064, EPC1064V, and EPC1441 devices, it is a reserved pin and should not be connected.

Figure 2. EPC2 Package Pin-Out Diagrams



Functional Description

With SRAM-based devices, configuration data must be reloaded each time the system initializes, or when new configuration data is needed. Altera configuration devices store configuration data for SRAM-based APEX II, APEX 20K, Mercury, ACEX, and FLEX devices. Table 1 lists Altera configuration devices.

Table 1. Configuration Devices

Device	Description
EPC16	16,000,000 × 1 bit with 3.3-V operation
EPC8	8,000,000 × 1 bit with 3.3-V operation
EPC4	4,000,000 × 1-bit device with 3.3-V operation
EPC2	1,695,680 × 1-bit device with 5.0-V or 3.3-V operation
EPC1 *(1)*	1,046,496 × 1-bit device with 5.0-V or 3.3-V operation
EPC1441 *(1)*	440,800 × 1-bit device with 5.0-V or 3.3-V operation
EPC1213 *(1)*	212,942 × 1-bit device with 5.0-V operation
EPC1064 *(1)*	65,536 × 1-bit device with 5.0-V operation
EPC1064V	65,536 × 1-bit device with 3.3-V operation

Note to Table 1:

(1) These devices are one-time programable.

Table 2 lists the configuration device used with each APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX device.

Table 2. Configuration Devices Used for Each APEX II, APEX 20K, Mercury, ACEX & FLEX Device (Part 1 of 2)

Family	Device	Data Size (Bits)	EPC1064 EPC1064V	EPC1213	EPC1441	EPC1	EPC2	EPC4	EPC8	EPC16
APEX II (1.5 V)	EP2A15	4,714,000					3		1	1
	EP2A25	6,276,000					4		1	1
	EP2A40	9,612,000					6		1	1
	EP2A70	17,390,000					11			1
Mercury (1.8 V)	EP1M120	1,297,000					1	1	1	1
	EP1M350	4,383,000					3		1	1
APEX 20KC (1.8 V)	EP20K200C	1,964,000					2	1	1	1
	EP20K400C	3,901,000					3	1	1	1
	EP20K600C	5,564,000					4		1	1
	EP20K1000C	8,938,000					6		1	1
APEX 20KE (1.8 V)	EP20K30E	347,000			1	1	1	1	1	1
	EP20K60E	641,000				1	1	1	1	1
	EP20K100E	1,009,000				1	1	1	1	1
	EP20K160E	1,523,000					1	1	1	1
	EP20K200E	1,964,000					2	1	1	1
	EP20K300E	2,733,000					2	1	1	1
	EP20K400E	3,901,000					3	1	1	1
	EP20K600E	5,564,000					4		1	1
	EP20K1000E	8,938,000					6		1	1
	EP20K1500E	12,011,000					8		1	1
APEX 20K (2.5 V)	EP20K100	985,000				1	1	1	1	1
	EP20K200	1,950,000					2	1	1	1
	EP20K400	3,878,000					3	1	1	1
ACEX 1K (2.5 V)	EP1K10	178,000		1	1	1	1	1	1	1
	EP1K30	470,000				1	1	1	1	1
	EP1K50	785,000				1	1	1	1	1
	EP1K100	1,337,000					1	1	1	1

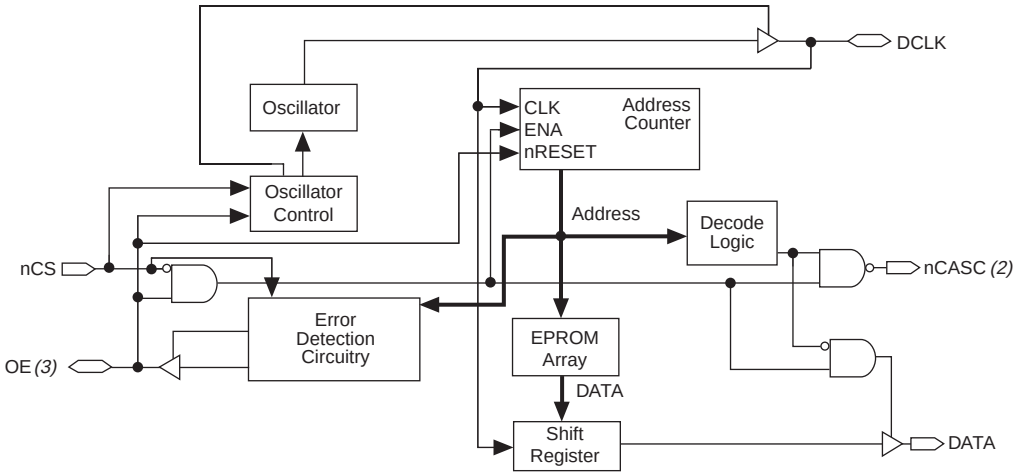
Table 2. Configuration Devices Used for Each APEX II, APEX 20K, Mercury, ACEX & FLEX Device (Part 2 of 2)

Family	Device	Data Size (Bits)	EPC1064 EPC1064V	EPC1213	EPC1441	EPC1	EPC2	EPC4	EPC8	EPC16
FLEX 10KE (2.5 V)	EPF10K30E	470,000				1	1	1	1	1
	EPF10K50E	785,000				1	1	1	1	1
	EPF10K50S	785,000				1	1	1	1	1
	EPF10K100B	1,2000,000					1	1	1	1
	EPF10K100E	1,336,000					1	1	1	1
	EPF10K130E	1,840,000					2	1	1	1
	EPF10K200E	2,757,000					2	1	1	1
	EPF10K200S	2,757,000					2	1	1	1
FLEX 10KA (3.3 V)	EPF10K10A	120,000		1	1	1	1	1	1	1
	EPF10K30A	402,000			1	1	1	1	1	1
	EPF10K50V	621,000			1	1	1	1	1	1
	EPF10K100A	1,200,000				1	1	1	1	1
	EPF10K130V	1,582,000				1	1	1	1	1
	EPF10K250A	3,292,000					2	1	1	1
FLEX 10K (5.0 V)	EPF10K10	118,000		1	1	1	1	1	1	1
	EPF10K20	231,000			1	1	1	1	1	1
	EPF10K30	376,000			1	1	1	1	1	1
	EPF10K40	498,000				1	1	1	1	1
	EPF10K50	621,000				1	1	1	1	1
	EPF10K70	893,000				1	1	1	1	1
	EPF10K100	1,200,000					1	1	1	1
FLEX 6000/A (3.3 V)	EPF6010A	260,000			1	1				
	EPF6016 (5.0 V) / EPF6016A	260,000			1	1				
	EPF6024A	398,000			1	1				
FLEX 8000A (5.0 V)	EPF8282A / EPF8282AV (3.3 V)	40,000	1	1	1	1				
	EPF8452A	64,000	1	1	1	1				
	EPF8636A	96,000		1	1	1				
	EPF8820A	128,000		1	1	1				
	EPF81188A	192,000		1	1	1				
	EPF1500A	250,000			1	1				

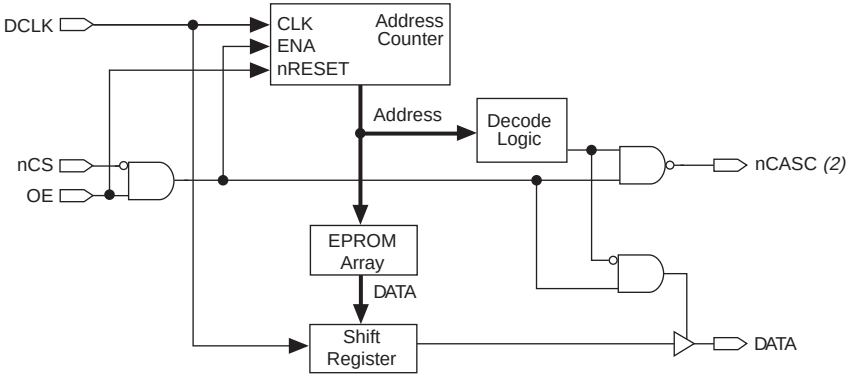
Figure 3 shows the configuration device block diagram.

Figure 3. Configuration Device Block Diagram

PLD (except FLEX 8000) Configuration Using an EPC2, EPC1, or EPC1441 *(1)*



FLEX 8000 Device Configuration Using an EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V



Notes to Figure 3:

(1) Do not use EPC2 devices to configure FLEX 6000 devices.

(2) The EPC1441, EPC1064, and EPC1064V devices do not support data cascading. The EPC2, EPC1, and EPC1213 devices support data cascading.

(3) The OE pin is a bidirectional open-drain pin.

Device Configuration

The control signals for configuration devices—nCS, OE, and DCLK—interface directly with APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX device control signals. All APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX devices can be configured by a configuration device without requiring an external intelligent controller.

The configuration device's OE and nCS pins control the tri-state buffer on the DATA output pin, and enable the address counter (and the oscillator in EPC4, EPC 8, EPC16, EPC2, EPC1, and EPC1441 devices). When OE is driven low, the configuration device resets the address counter and tri-states its DATA pin. The nCS pin controls the output of the configuration device. If nCS is held high after the OE reset pulse, the counter is disabled and the DATA output pin is tri-stated. When nCS is driven low, the counter and DATA output pin are enabled. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of nCS.

The EPC4, EPC8, EPC16, EPC2, EPC1, and EPC1441 devices determine the operation mode and whether the APEX 20K, Mercury, ACEX 1K, FLEX 10K, FLEX 8000, or FLEX 6000 protocols should be used when OE is driven high.

When the configuration device has driven out all of its data and has driven nCASC low, the device tri-states the DATA pin to avoid contention with other configuration devices.

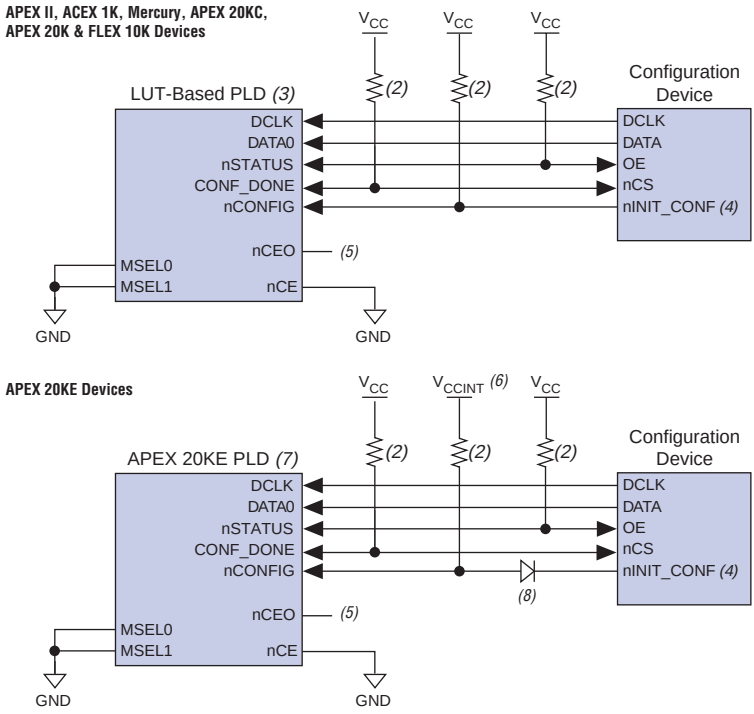
The EPC2 device allows the user to initiate configuration of the PLD via an additional pin, nINIT_CONF, that can be tied to the nCONFIG pin of the PLD(s) to be configured. A JTAG instruction causes the EPC4, EPC8, EPC16, and EPC2 device to drive nINIT_CONF low, which in turn pulls nCONFIG low. The EPC4, EPC8, EPC16, and EPC2 device then drives nINIT_CONF high to start configuration. When the JTAG state machine exits this state, nINIT_CONF releases nCONFIG and configuration is initiated.

An EPC4, EPC8, EPC16, and EPC2 device can be programmed with a POF generated for an EPC1 or EPC1441 device, however, an EPC2 device cannot configure FLEX 6000 or FLEX 8000 devices. An EPC1 device can be programmed using a POF generated for an EPC1441 device.

APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K & FLEX 6000 Device Configuration

APEX 20K, Mercury, ACEX 1K, and FLEX devices can be configured with EPC4, EPC8, EPC16, EPC2, EPC1, or EPC1441 devices. FLEX 6000 devices can be configured with EPC1 or EPC1441 devices. APEX II devices can be configured with EPC2, EPC4, EPC8, and EPC16 devices. The EPC4, EPC8, EPC16, EPC2, EPC1, or EPC1441 device stores configuration data in its EPROM array and serially clocks data out with an internal oscillator. The OE, nCS, and DCLK pins supply the control signals for the address counter and the output tri-state buffer. The configuration device sends a serial bitstream of configuration data to its DATA pin, which is routed to the DATA0 or DATA input pin on the LUT-based PLD device. Figure 4 shows an LUT-based PLD configured with a single EPC2, EPC1, or EPC1441 device.

Figure 4. ACEX 1K, APEX 20K, APEX II, FLEX 10K, FLEX 6000, or Mercury Device Configured with an EPC2, EPC1, or EPC1441 Configuration Device *Note (1)*



Notes to Figure 4:

(1) Do not use EPC2 devices to configure FLEX 6000 devices.

(2) The pull-up resistor should be connected to the same supply voltage as the configuration device. All pull-up resistors are 1 kΩ. APEX 20KE pull up resistors are 10 kΩ. The `OE`, `nCS`, and `nINIT_CONF` pins on EPC2, EPC4, EPC8, and EPC16 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The Quartus II software uses the internal pull-up resistors by default. To turn off the internal pull-up resistors, check the *Disable nCS and OE pull-ups on configuration device* option when generating programming files.

(3) The diagram shows an APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX device, which has `MSEL0` and `MSEL1` tied to ground. For FLEX 6000 devices, `MSEL` is tied to ground, and the `DATA0` pin is named `DATA`. EPC4, EPC8, EPC16, and EPC2 configuration devices cannot be used with FLEX 6000 devices. All other connections are the same for APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX devices.

(4) The `nINIT_CONF` pin is only available on EPC2, EPC4, EPC8, and EPC16 devices and has an internal pull up of 1 kΩ that is always active. If `nINIT_CONF` is not available or not used, `nCONFIG` must be pulled to V_{CC} either directly or through a 1-kΩ resistor.

(5) The `nCEO` pin is left unconnected.

(6) To ensure successful configuration between APEX 20KE and configuration devices in all possible power-up sequences, pull up `nCONFIG` to V_{CCINT}.

(7) This diagram is for APEX 20KE devices only.

(8) To isolate the 1.8-V and 3.3-V power supplies when configuration APEX 20KE devices, add a diode between the APEX 20KE device's `nCONFIG` pin and the configuration device's `nINIT_CONF` pin. Select a diode with a threshold voltage (V_T) less than or equal to 0.7 V. The diode will make the `nINIT_CONF` pin an open-drain pin; the pin will only be able to drive low or tri-state.

Table 3 describes EPC2, EPC1, and EPC1441 pin functions during APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX device configuration. For information on EPC4, EPC8, and EPC16 devices, refer to *Enhanced Configuration Devices (EPC4, EPC8, & EPC16) Data Sheet*.

Table 3. EPC2, EPC1, & EPC1441 Pin Functions During APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K & FLEX 6000 Configuration (Part 1 of 3) *Notes (1), (2)*

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP *(3)*	20-Pin PLCC	32-Pin TQFP *(4)*		
DATA	1	2	31	Output	Serial data output. The DATA pin is tri-stated before configuration when the nCS pin is high, and after the configuration device finishes sending its configuration data. This operation is independent of the device's position in the cascade chain.
DCLK	2	4	2	I/O	DCLK is a clock output when configuring with a single configuration device or when the configuration device is the first device in a configuration device chain. DCLK is a clock input for subsequent configuration devices in a configuration device chain. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device. When configuring with the first EPC2 or EPC1 device in a configuration device chain or with a single EPC1441 device, the DCLK pin drives low after configuration is complete or when OE is low.
OE *(5)*	3	8	7	Open-Drain I/O	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count. If this pin is low (reset) during configuration, the internal oscillator becomes inactive and DCLK drives low. See "Error Detection Circuitry" on page 23.
nCS *(5)*	4	9	10	Input	Chip select input (active low). A low input allows DCLK to increment the address counter and enables DATA to drive out. If the EPC1 or EPC2 is reset with nCS low, the device initializes as the first device in a configuration chain. If the EPC1 or EPC2 device is reset with nCS high, the device initializes as the subsequent device in the chain.

Table 3. EPC2, EPC1, & EPC1441 Pin Functions During APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K & FLEX 6000 Configuration (Part 2 of 3) *Notes (1), (2)*

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP *(3)*	20-Pin PLCC	32-Pin TQFP *(4)*		
nCASC *(6)*	6	12	15	Output	Cascade select output (active low). This output goes low when the address counter has reached its maximum value. In a chain of EPC1 or EPC2 devices, the nCASC pin of one device is connected to the nCS pin of the next device, which permits DCLK to clock data from the next EPC1 or EPC2 device in the chain.
nINIT_CONF *(5)*, *(7)*	–	13	16	Open-Drain Output	Allows the INIT_CONF JTAG instruction to initiate configuration. This pin is connected to the nCONFIG pin of the LUT device to initiate configuration from the EPC2 via a JTAG instruction. If multiple EPC2 devices are used to configure an ACEX, APEX, FLEX or Mercury device, only the first EPC2 has its nINIT_CONF pin tied to the device's nCONFIG pin.
TDI *(7)*	–	11	13	Input	JTAG data input pin. Connect this pin to V_{CC} if the JTAG circuitry is not used.
TDO *(7)*	–	1	28	Output	JTAG data output pin. Do not connect this pin if the JTAG circuitry is not used.
TMS *(7)*	–	19	25	Input	JTAG mode select pin. Connect this pin to V_{CC} if the JTAG circuitry is not used.
TCK *(7)*	–	3	32	Input	JTAG clock pin. Connect this pin to ground if the JTAG circuitry is not used.
VCCSEL *(7)*	–	5	3	Input	Mode select for V_{CC} supply. VCCSEL must be connected to ground if the device uses a 5.0-V power supply (i.e., V_{CC} = 5.0 V). VCCSEL must be connected to V_{CC} if the device uses a 3.3-V power supply (i.e., V_{CC} = 3.3 V).
VPPSEL *(7)*	–	14	17	Input	Mode select for VPP. VPPSEL must be connected to ground if VPP uses a 5.0-V power supply (i.e., VPP = 5.0 V). VPPSEL must be connected to V_{CC} if VPP uses a 3.3-V power supply (i.e, VPP = 3.3 V).
VPP *(7)*	–	18	23	Power	Programming power pin. For the EPC2 device, this pin is normally tied to V_{CC}. If the EPC2 V_{CC} is 3.3 V, VPP can be tied to 5.0 V to improve in-system programming times. For EPC1 and EPC1441 devices, VPP must be tied to V_{CC}.

Table 3. EPC2, EPC1, & EPC1441 Pin Functions During APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K & FLEX 6000 Configuration (Part 3 of 3) *Notes (1), (2)*

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP *(3)*	20-Pin PLCC	32-Pin TQFP *(4)*		
VCC	7, 8	20	27	Power	Power pin.
GND	5	10	12	Ground	Ground pin. A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.

***Notes to** Table 3:*

(1) Do not use EPC2 devices to configure FLEX 6000 devices.
(2) Pin-out information for EPC8 and EPC16 configuration devices, please refer to each respective data sheet.
(3) This package is available for EPC1 and EPC1441 devices only.
(4) This package is available for EPC2 and EPC1441 devices only.
(5) The OE, nCS, and nINIT_CONF pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins.
(6) The EPC1441 device does not support data cascading. EPC2 and EPC1 devices support data cascading.
(7) This pin applies to the EPC2 device only.

APEX II, APEX 20K, Merucry, ACEX 1K, FLEX 10K & FLEX 6000 Device Configuration with Multiple EPC2 or EPC1 Configuration Devices

When configuration data for APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX devices exceeds the capacity of a single EPC2 or EPC1 configuration device, multiple EPC2 or EPC1 devices can be cascaded together. If multiple EPC2 or EPC1 devices are required, the nCASC and nCS pins provide handshaking between the devices.

EPC8 and EPC16 configuration devices cannot be cascaded together. The EPC1441 device does not support data cascading.

When configuring APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX 10K devices with cascaded EPC2 or EPC1 devices, the position of the EPC2 or EPC1 device in the chain determines its operation. Similarly, when configuring FLEX 6000 devices with cascaded EPC1 devices, the position of the EPC1 device in the chain determines its operation. When the first or master device in a configuration device chain is powered-up or reset and the nCS pin is driven low, the master device controls configuration. The master device supplies all clock pulses to one or more LUT-based PLDs and to any subsequent slave devices during configuration. The master EPC2 or EPC1 device also provides the first stream of data to the LUT-based PLD during multi-device configuration. After the master EPC2 or EPC1 device finishes sending configuration data, the master EPC2 or EPC1 device drives its nCASC pin low, which drives the nCS pin of the first slave EPC2 or EPC1 device low. This action causes the slave EPC2 or EPC1 device to send configuration data to the LUT-based PLDs.

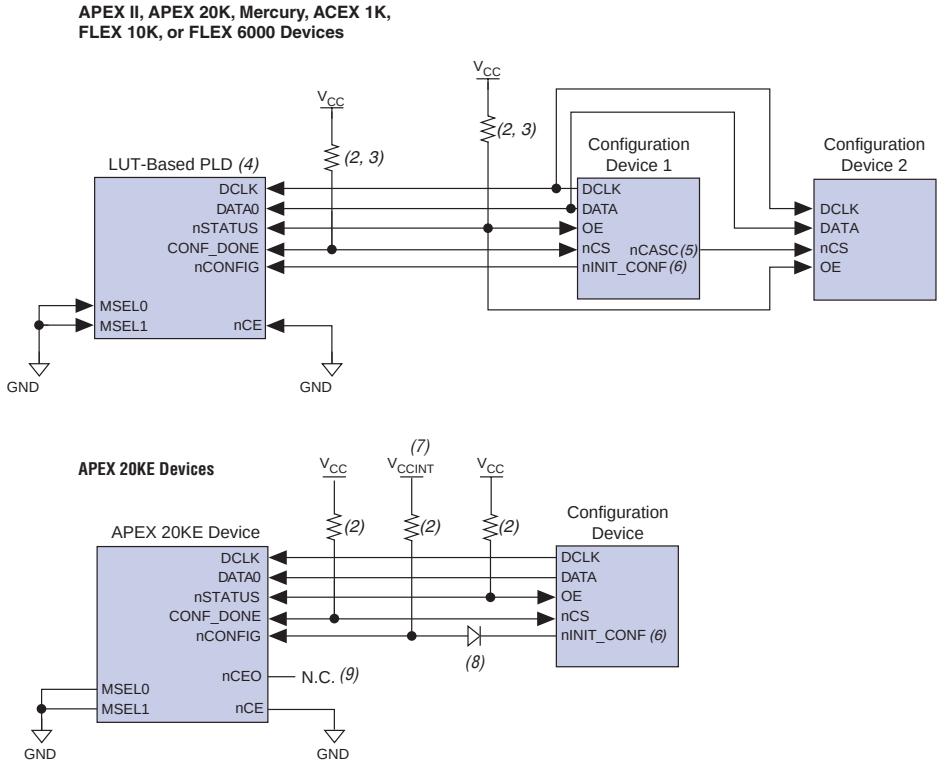
The master EPC2 or EPC1 device clocks all subsequent slave devices until configuration is complete. Once all configuration data is transferred and the nCS pin on the master EPC2 or EPC1 device is driven high by the LUT-based PLD's CONF_DONE pin, the master EPC2 or EPC1 device clocks 16 additional cycles to initialize the LUT-based PLD(s). The master EPC2 or EPC1 device then goes into zero-power (idle) state. If nCS on the master EPC2 or EPC1 device is driven high before all configuration data is transferred, or if nCS is not driven high after all configuration data is transferred, the master EPC2 or EPC1 device drives the APEX 20K, Mercury, ACEX 1K, and FLEX device's nSTATUS pin low, indicating a configuration error.

Configuration automatically restarts if the project is compiled with the *Auto-Restart Configuration on Frame Error* option turned on in the MAX+PLUS II software's **Global Project Device Options** dialog box (Assign menu).

Figure 5 shows an APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 device configured with two EPC2 or EPC1 devices. Additional EPC2 or EPC1 devices can be added by connecting nCASC to nCS of the subsequent slave EPC2 or EPC1 device in the chain and connecting DCLK, DATA, and OE in parallel.

A mixture of APEX 20K, Mercury, ACEX 1K, FLEX 10K, and FLEX 6000 devices can be configured in the same chain. A mixture of FLEX 10K, FLEX 10KA, FLEX 10KE, and 5.0-V and 3.3-V FLEX 6000 devices can be configured in the same chain. See "Configuration Chain with Multiple Voltage Levels" on page 25.

Figure 5. APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 Device Configured with Two EPC2 or EPC1 Configuration Devices *Note (1)*



Notes to** Figure 5**:

(1) Do not use EPC2 devices to configure FLEX 6000 devices.

(2) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(3) All pull-up resistors are 1 kΩ (APEX 20KE pull-resistors are 10 kΩ). The `OE` and `nCS` pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins.

(4) The diagram shows an APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX device, which has `MSEL0` and `MSEL1` tied to ground. For FLEX 6000 devices, `MSEL` is tied to ground, and the `DATA0` pin is named `DATA`. EPC8, EPC16, and EPC2 devices cannot be used with FLEX 6000 devices. All other connections are the same for FLEX 6000 devices. The Quartus II software uses the internal pull-up resistors by default. To turn off the internal pull-up resistors, check the *Disable nCS and OE pull-ups on configuration device* option when generating programming files.

(5) EPC4, EPC8, and EPC16 devices cannot be cascaded.

(6) The `nINIT_CONF` pin is only available on EPC2 devices and has an internal pull up of 1 kΩ that is always active. If `nINIT_CONF` is not available or not used, `nCONFIG` must be pulled to V_{CC} either directly or through a 1-kΩ resistor.

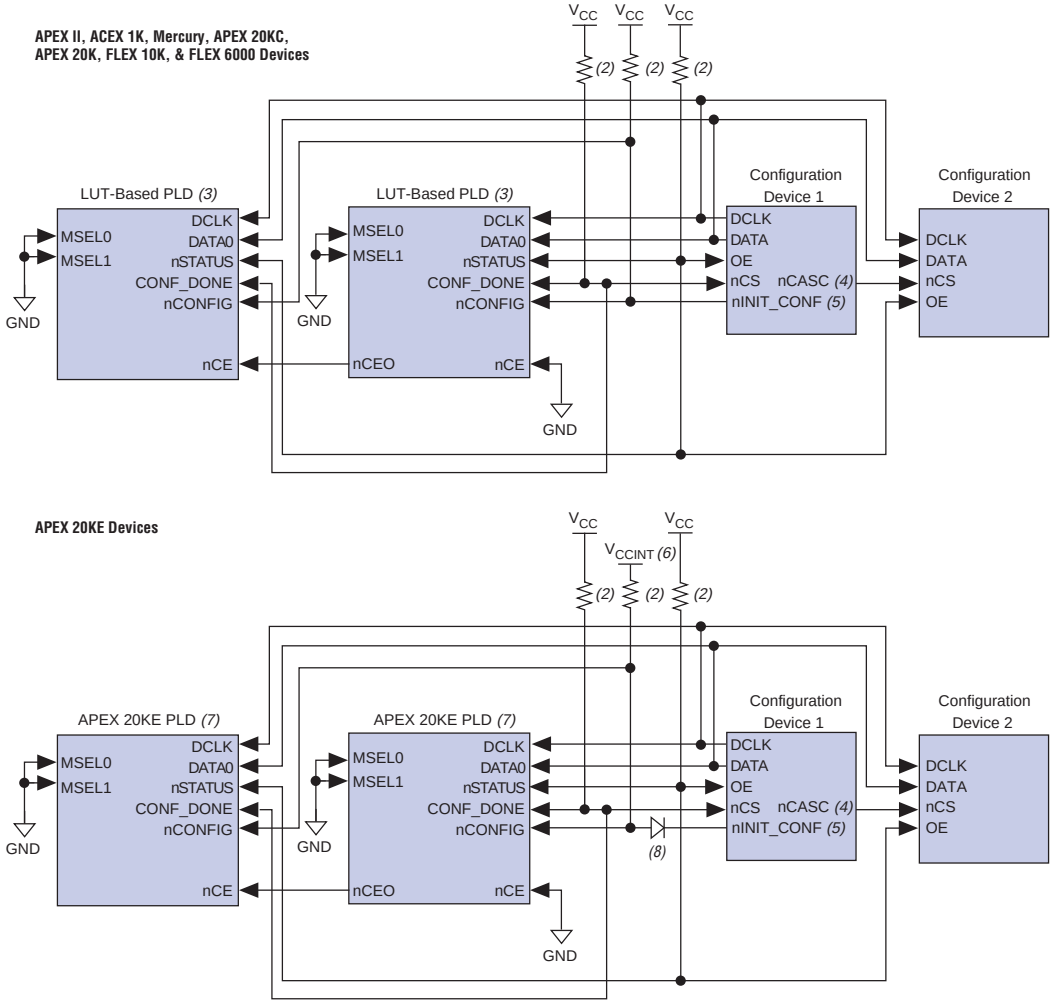
(7) To ensure successful configuration between APEX 20KE and configuration devices in all possible power-up sequences, pull up `nCONFIG` to V_{CCINT}.

(8) To isolate the 1.8-V and 3.3-V power supplies when configuring APEX 20KE devices, add a diode between the APEX 20KE device's `nCONFIG` pin and the configuration device's `nINIT_CONF` pin. Select a diode with a threshold voltage (V_T) less than or equal to 0.7 V. The diode will make the nINIT_CONF pin an open-drain pin; the pin will only be able to drive low or tri-state.

(9) The `nCEO` pin is left unconnected.

Figure 6 shows two APEX II, APEX 20K, Mercury, ACEX 1K, and FLEX devices configured with two EPC2 or EPC1 devices.

Figure 6. Two ACEX 1K, APEX 20K, APEX II, FLEX 10K, FLEX 6000, or Mercury Devices Configured with Two EPC2 or EPC1 Configuration Devices *Note (1)*



Notes to Figure 6:

(1) Do not use EPC2 devices to configure FLEX 6000 devices.

(2) The pull-up resistor should be connected to the same supply voltage as the configuration device. All pull-up resistors are 1 kΩ (APEX 20KE pull-resistors are 10 kΩ). The OE and nCS pins on EPC2 devices have internal, user-configurable 1-kΩ pull-up resistors. If internal pull-up resistors are used, external pull-up resistors should not be used on these pins. The Quartus II software uses the internal pull-up resistors by default. To turn off the internal pull-up resistors, check the *Disable nCS and OE pull-ups on configuration device* option when generating programming files.

(3) The diagram shows an APEX II, APEX 20K, Mercury, ACEX 1K, or FLEX 10K device, which has MSEL0 and MSEL1 tied to ground. For FLEX 6000 devices, MSEL is tied to ground, and the DATA0 pin is named DATA. EPC2 cannot be used with FLEX 6000 devices. All other connections are the same for FLEX 6000 devices.

(4) EPC4, EPC8, and EPC16 devices cannot be cascaded.

(5) The nINIT_CONF pin is only available on EPC2 devices and has an internal pull up of 1 kΩ that is always active. If nINIT_CONF is not available or not used, nCONFIG must be pulled to V_{CC} either directly or through a 1-kΩ resistor.

(6) To ensure successful configuration between APEX 20KE and configuration devices in all possible power-up sequences, pull up nCONFIG to V_{CCINT}.

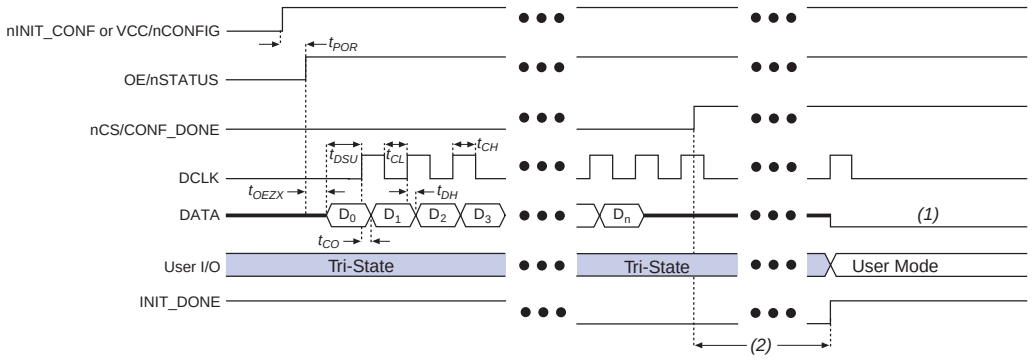
(7) This diagram is for APEX 20KE devices only.

(8) To isolate the 1.8-V and 3.3-V power supplies when configuration APEX 20KE devices, add a diode between the APEX 20KE device's nCONFIG pin and the configuration device's nINIT_CONF pin. Select a diode with a threshold voltage (V_T) less than or queal to 0.7 V. The diode will make the nINIT_CONF pin an open-drain pin; the pin will only be able to drive low or tri-state.

For more information on APEX 20K, ACEX 1K, FLEX 10K, or FLEX 6000 device configuration, see *Application Note 116 (Configuring ACEX 1K, APEX 20K, FLEX 10K & FLEX 6000 Devices)*.

Figure 7 shows the timing waveform for the configuration device scheme.

Figure 7. Configuration Device Scheme Timing Waveform



Notes to Figure 7:

(1) The configuration devivce will drive DATA low after configuration.

(2) APEX II and APEX 20K devices (except EP2A70 devices) enter user mode 40 clock cycles after CONF_DONE goes high. EP2A70 devices enter user mode 72 clock cycles after CONF_DONE goes high. FLEX 10K and FLEX 6000 devices enter user mode 10 clock cycles after CONF_DONE goes high. Mercury devices enter user mode 136 clock cycles after CONF_DONE goes high.

Table 4 defines the APEX 20K, FLEX 10K, and FLEX 6000 timing parameters when using EPC2 devices at 3.3 V.

Table 4. APEX 20K, FLEX 10K & FLEX 6000 Timing Parameters using EPC2 Devices at 3.3 V *Note (1)*

Symbol	Parameter	Min	Max	Units
t_{POR}	POR delay *(2)*		200	ms
t_{OEZX}	OE high to DATA output enabled		80	ns
t_{CH}	DCLK high time	40	100	ns
t_{CL}	DCLK low time	40	100	ns
t_{DSU}	Data setup time before rising edge on DCLK	30		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CO}	DCLK to DATA out		30	ns
t_{OEW}	OE low pulse width to guarantee counter reset	100		ns
f_{CLK}	DCLK frequency	5	12.5	MHz

***Notes to** Table 4:*

(1) For more information regarding EPC4, EPC8, or EPC16 configuration device timing parameters, see the *Enhanced Configuration Device (EPC4, EPC8 & EPC16) Data Sheet*.

(2) The configuration device imposes a POR delay upon initial power-up to allow the voltage supply to stabilize. Subsequent reconfigurations do not incur this delay.

Table 5 defines the APEX 20K, FLEX 10K, and FLEX 6000 timing parameters when using EPC1 and EPC1441 devices at 3.3 V.

Table 5. APEX 20K, FLEX 10K & FLEX 6000 Timing Parameters using EPC1 & EPC1441 Devices at 3.3 V *Note (1)*

Symbol	Parameter	Min	Max	Units
t_{POR}	POR delay *(2)*		200	ms
t_{OEZX}	OE high to DATA output enabled		80	ns
t_{CH}	DCLK high time	50	250	ns
t_{CL}	DCLK low time	50	250	ns
t_{DSU}	Data setup time before rising edge on DCLK	30		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CO}	DCLK to DATA out		30	ns
t_{OEW}	OE low pulse width to guarantee counter reset	100		ns
f_{CLK}	DCLK frequency	2	10	MHz

Notes to** Table 5**:

(1) For more information regarding EPC4, EPC8, or EPC16 configuration device timing parameters, see the *Enhanced Configuration Device (EPC4, EPC8 & EPC16) Data Sheet*.

(2) The configuration device imposes a POR delay upon initial power-up to allow the voltage supply to stabilize. Subsequent reconfigurations do not incur this delay.

Table 6 defines the APEX 20K, FLEX 10K, and FLEX 6000 timing parameters when using EPC2, EPC1, and EPC1441 devices at 5.0 V.

Table 6. APEX 20K, FLEX 10K & FLEX 6000 Timing Parameters using EPC2, EPC1 & EPC1441 Devices at 5.0 V *Notes (1), (2)*

Symbol	Parameter	Min	Max	Units
t_{POR}	POR delay *(3)*		200	ms
t_{OEZX}	OE high to DATA output enabled		50	ns
t_{CH}	DCLK high time	30	75	ns
t_{CL}	DCLK low time	30	75	ns
t_{DSU}	Data setup time before rising edge on DCLK	30		ns
t_{DH}	Data hold time after rising edge on DCLK	0		ns
t_{CO}	DCLK to DATA out		30	ns
t_{OEW}	OE low pulse width to guarantee counter reset	100		ns
f_{CLK}	DCLK frequency	6.7	16.7	MHz

Notes to** Table 6**:

(1) Do not use EPC16, EPC8, EPC4, or EPC2 devices to configure FLEX 6000 devices.
(2) For more information regarding EPC4, EPC8, or EPC16 configuration device timing parameters, see the *Enhanced Configuration Device (EPC4, EPC8 & EPC16) Data Sheet*.
(3) The configuration device imposes a POR delay upon initial power-up to allow the voltage supply to stabilize. Subsequent reconfigurations do not incur this delay.

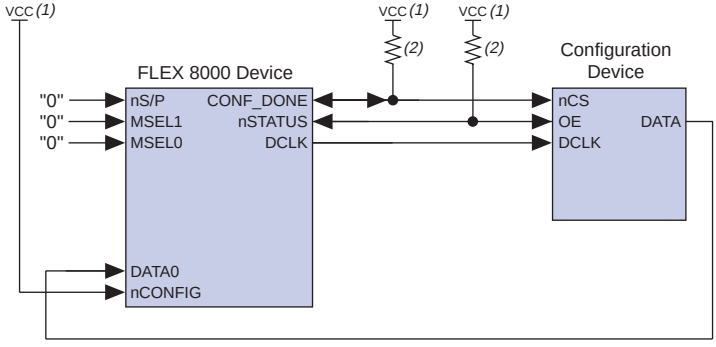
FLEX 8000 Device Configuration

FLEX 8000 devices differ from ACEX 1K, APEX 20K, APEX II, FLEX 10K, and FLEX 6000 devices in that they have internal oscillators that can provide a DCLK signal to the configuration device. The configuration device sends configuration data out as a serial bitstream on the DATA output pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The EPC1, EPC1441, EPC1213, EPC1064, and EPC1064V configuration devices support this type of configuration.

EPC1 and EPC1441 devices can replace the EPC1213, EPC1064, and EPC1064V configuration devices. The EPC1 or EPC1441 device automatically emulates the EPC1213, EPC1064, or EPC1064V when it is programmed with the appropriate POF. When the EPC1 or EPC1441 device is programmed with an EPC1213, EPC1064, or EPC1064V POF, the FLEX 8000 device drives the EPC1 or EPC1441 device's OE pin high and clocks the EPC1 or EPC1441 device. One EPC1 device can store more configuration data than the EPC1064, EPC1064V, EPC1213, or EPC1441 device. Therefore, designers can use one type of configuration device for all FLEX devices. In addition, a single EPC1 or EPC1441 device can configure any FLEX 8000 device.

For multi-device configuration of FLEX 8000 devices, the nCASC and nCS pins provide handshaking between multiple configuration devices, allowing several cascaded EPC1 or EPC1213 devices to serially configure multiple FLEX 8000 devices. The EPC1441, EPC1064, and EPC1064V do not support data cascading. Figure 8 shows a FLEX 8000 device configured with a single EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V configuration device.

Figure 8. FLEX 8000 Device Configured with an EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V Configuration Device



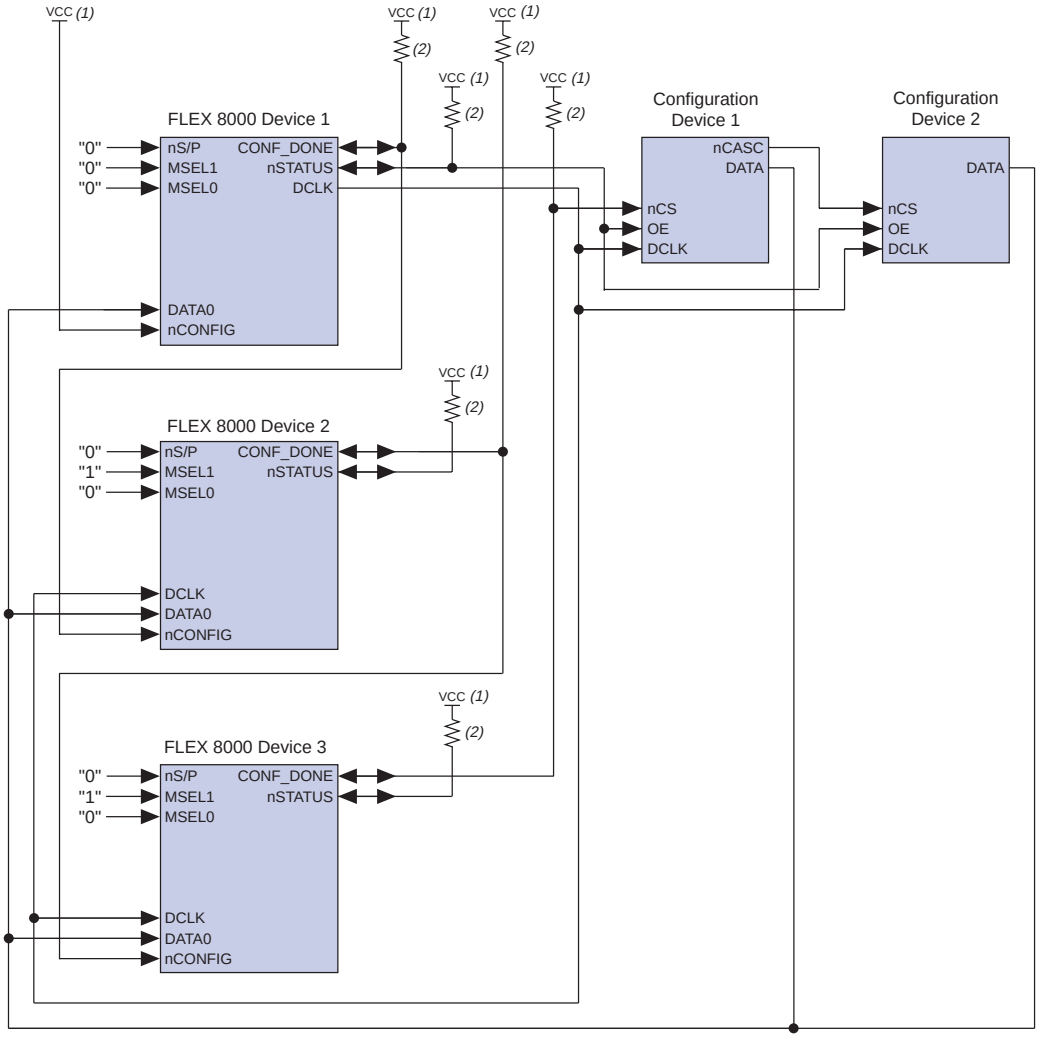
Notes to Figure 8:

(1) The pull-up resistor should be connected to the same supply voltage as the configuration device.

(2) All pull-up resistors are 1 kΩ.

Figure 9 shows three FLEX 8000 devices configured with two EPC1 or EPC1213 configuration devices.

Figure 9. FLEX 8000 Multi-Device Configuration with Two EPC1 or EPC1213 Configuration Devices



Notes to** Figure 9**:

(1) The pull-resistor should be connected to the same supply voltage as the confiuration device.

(2) All pull-up resistors are 1 kΩ.

Table 7 describes the pin functions of all configuration devices during FLEX 8000 device configuration.

Table 7. Configuration Device Pin Functions During FLEX 8000 Device Configuration

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP *(1)*	20-Pin PLCC	32-Pin TQFP *(2)*		
DATA	1	2	31	Output	Serial data output. The DATA pin is tri-stated before configuration when the nCS pin is high and after the configuration device finishes sending its configuration data. This operation is independent of the device's position in the cascade chain.
DCLK	2	4	2	Input	DCLK is a clock input when using EPC1, EPC1213, EPC1064, and EPC1064V configuration devices. Rising edges on DCLK increment the internal address counter and present the next bit of data to the DATA pin. The counter is incremented only if the OE input is held high, the nCS input is held low, and all configuration data has not been transferred to the target device.
OE	3	8	7	Open-Drain I/O	Output enable (active high) and reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS *(3)*	4	9	10	Input	Chip-select input (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC	6	12	15	Output	Cascade-select output (active low). This output goes low when the address counter has reached its maximum value. The nCASC output is usually connected to the nCS input of the next device in a configuration chain, so the next DCLK clocks data out of the next device.
VCC	7, 8	20	27	Power	Power pin.
GND	5	10	12	Ground	Ground pin. A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.

Notes: to *Table 7*

(1) This package is available for EPC1, EPC1441, EPC1213, EPC1064, and EPC1064V devices only.
(2) This package is available for EPC1441, EPC1064, and EPC1064V devices only.
(3) The EPC1441, EPC1064, and EPC1064V devices do not support data cascading. The EPC1 and EPC1213 devices support data cascading for FLEX 8000 devices.

For more information on FLEX 8000 device configuration, see the following documents:

- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

Power & Operation

This section describes Power-On Reset (POR) delay, error detection, and 3.3-V and 5.0-V operation of Altera configuration devices.

Power-On Reset

During initial power-up, a POR delay occurs to permit voltage levels to stabilize. When configuring an APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 device with an EPC4, EPC8, EPC16, EPC2, EPC1, or EPC1441 device, the POR delay occurs inside the configuration device, and the POR delay is a maximum of 200 ms. When configuring a FLEX 8000 device with an EPC1213, EPC1064, or EPC1064V device, the POR delay occurs inside the FLEX 8000 device, and the POR delay is typically 100 ms, with a maximum of 200 ms.

Error Detection Circuitry

The EPC4, EPC8, EPC16, EPC2, EPC1, and EPC1441 configuration devices have built-in error detection circuitry for configuring APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 devices only.

Built-in error-detection circuitry uses the nCS pin of the configuration device, which monitors the CONF_DONE pin on the APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 device. An error condition occurs if the CONF_DONE pin does not go high after all the configuration data has been sent, or if the CONF_DONE pin goes high before the configuration device has completed sending configuration data. When an error condition occurs, the configuration device drives its OE pin low, which drives the APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 device's nSTATUS pin low, indicating an error. After an error, configuration automatically restarts if the *Auto-Restart Configuration on Frame Error* option is turned on in the **Global Project Device Options** dialog box (Assign menu) in the MAX+PLUS II software. For APEX 20K, APEX II, and Mercury devices, the Quartus II software provides a similar option.

In addition, if the APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 device detects a cyclic redundancy code (CRC) error in the received data, it may also flag the error by driving nSTATUS low. This low signal on nSTATUS resets the configuration device, allowing reconfiguration. CRC checking is performed when configuring all APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 devices.

3.3-V or 5.0-V Operation

EPC2, EPC1, and EPC1441 devices can configure 5.0-V, 3.3-V, or 2.5-V devices. For each configuration device, an option must be set for 5.0-V or 3.3-V operation (EPC4, EPC8, and EPC16 devices are 3.3 V). For EPC1 and EPC1441 configuration devices, the *Use Low-Voltage Configuration EPROM* option in the **Global Project Device Options** dialog box (Assign menu) in the MAX+PLUS II software sets this parameter. (For APEX 20K, APEX II, and Mercury devices, the Quartus II software provides a similar option.) For EPC2 devices, this option is set externally by the VCCSEL pin. In addition, the EPC2 device has an externally controlled option, set by the VPPSEL pin, to adjust the programming voltage to 5.0 V or 3.3 V.

The functions of the VCCSEL and VPPSEL pins are described below.

- VCCSEL pin—For EPC2 configuration devices, 5.0-V or 3.3-V operation is controlled by the VCCSEL option pin. The device functions in 5.0-V mode when VCCSEL is connected to GND; the device functions in 3.3-V mode when VCCSEL is connected to V_{CC}.
- VPPSEL pin—The EPC2 VPP programming power pin is normally tied to V_{CC}. For EPC2 devices operating with a 3.3-V supply, it is possible to improve EPC2 in-system programming times by providing VPP with a 5.0-V supply. For all other devices, VPP must be tied to V_{CC}. The EPC2 device's VPPSEL pin must be set in accordance with the EPC2 VPP pin. If the VPP pin is supplied by a 5.0-V supply, VPPSEL must be connected to GND; if the VPP pin is supplied by a 3.3-V power supply, VPPSEL must be connected to V_{CC}.

Table 8 describes the relationship between the V_{CC} and V_{PP} voltage levels and the required logic level for VCCSEL and VPPSEL (i.e., high or low logic level).

Table 8. VCCSEL & VPPSEL Pin Functions on the EPC2

V_{CC} Voltage Level (V)	V_{PP} Voltage Level (V)	VCCSEL Pin Logic Level	VPPSEL Pin Logic Level
3.3	3.3	High	High
3.3	5.0	High	Low
5.0	5.0	Low	Low

For EPC1 and EPC1441 configuration devices, 3.3-V or 5.0-V operation is controlled by a programming bit in the POF. The programming bit value is determined by the core supply voltage of the targeted device during design compilation with the MAX+PLUS II software. For example, EPC1 devices are programmed automatically to operate in 3.3-V mode when configuring FLEX 10KA devices, which have a V_{CC} voltage of 3.3 V. In this example, the EPC1 device's VCC pin is connected to a 3.3-V power supply.

Designers may choose to set the configuration device for low voltage when using the MultiVolt™ feature, which allows an ACEX, APEX, APEX II, FLEX, or Mercury device to bridge between systems operating with different voltages. When compiling for 3.3-V FLEX 6000 devices, set the configuration device for low-voltage operation. To set the EPC1 and EPC1441 configuration devices for low-voltage operation, turn on the *Low-Voltage I/O* option in the **Global Project Device Options** dialog box (Assign menu) in the MAX+PLUS II software.

Configuration Chain with Multiple Voltage Levels

An EPC2 or EPC1 device can configure a device chain with multiple voltage levels. All 3.3-V and 2.5-V ACEX, APEX, APEX II, FLEX, and Mercury devices can be driven by higher-voltage signals.

When configuring a mixed-voltage device chain, the APEX II, APEX 20K, Mercury, ACEX 1K, or FLEX devices' VCCINT and VCCIO pins may be connected to 2.5 V, 3.3 V, or 5.0 V, depending upon the device. The configuration device may be powered at 3.3 V or 5.0 V. If an EPC1, EPC1441, EPC1213, EPC1064, or EPC1064V configuration device is powered at 3.3 V, the nSTATUS and CONF_DONE pull-up resistors must be connected to 3.3 V. If these configuration devices are powered at 5.0 V, the nSTATUS and CONF_DONE pull-up resistors must be connected to 3.3 V or 5.0 V.

At 3.3-V operation, all EPC2 inputs are 5.0-V tolerant, except DATA, DCLK, and nCASC. The DATA, DCLK, and nCEO pins are used only to interface between the EPC2 configuration device and the APEX II, APEX 20K, Mercury, ACEX 1K, or FLEX 10K device it is configuring. The voltage tolerances of all EPC2 pins at 5.0 V and 3.3 V are listed in Table 9.

Table 9. EPC2 Input & Bidirectional Pin Voltage Tolerance

Pin	5.0-V Operation		3.3-V Operation	
	5.0-V Tolerant	3.3-V Tolerant	5.0-V Tolerant	3.3-V Tolerant
DATA	✓	✓		✓
DCLK	✓	✓		✓
nCASC	✓	✓		✓
OE	✓	✓	✓	✓
nCS	✓	✓	✓	✓
VCCSEL	✓	✓	✓	✓
VPPSEL	✓	✓	✓	✓
nINIT_CONF	✓	✓	✓	✓
TDI	✓	✓	✓	✓
TMS	✓	✓	✓	✓
TCK	✓	✓	✓	✓

For more information on APEX II, APEX 20K, Mercury, ACEX 1K, FLEX 10K, or FLEX 6000 devices, see the following documents:

- *ACEX 1K Programmable Logic Device Family Data Sheet*
- *APEX 20K Programmable Logic Device Family Data Sheet*
- *APEX II Programmable Logic Device Family Data Sheet*
- *FLEX 10K Embedded Programmable Logic Family Data Sheet*
- *FLEX 10KE Embedded Programmable Logic Family Data Sheet*
- *FLEX 8000 Programmable Logic Device Family Data Sheet*
- *FLEX 6000 Programmable Logic Device Family Data Sheet*
- *Mercury Programmable Logic Device Family Data Sheet*

Programming & Configuration File Support

The Quartus II and MAX+PLUS II development systems provide programming support for Altera configuration devices. The Quartus II and MAX+PLUS II software automatically generates a POF to program each configuration device in a project. In a multi-device project, the software can combine the programming files for multiple ACEX, APEX, APEX II, FLEX, or Mercury devices into one or more configuration devices. The software allows you to select the appropriate configuration device to most efficiently store the data for each APEX II, APEX 20K, Mercury, ACEX 1K, or FLEX device. Moreover, when compiling for ACEX 1K, FLEX 10KA, FLEX 10KE, or Mercury devices, the MAX+PLUS II software automatically defaults to generate the EPC1 or EPC1441 POF with the programming bit set for 3.3-V operation.

All Altera configuration devices are programmable using Altera programming hardware in conjunction with the Quartus II or MAX+PLUS II software. In addition, many manufacturers offer programming hardware that supports other Altera configuration devices.

EPC4, EPC8, EPC16, and EPC2 configuration devices can be programmed in-system through its industry-standard 4-pin JTAG interface. ISP capability in the EPC2, EPC4, EPC8, and EPC16 devices provides ease in prototyping and updating APEX II, APEX 20K, Mercury, ACEX 1K, or FLEX device functionality. The EPC8 and EPC16 devices can be programmed in-system via test equipment using SVF Files, Jam STAPL Files (**.jam**), or Jam STAPL Byte-Code Files (**.jbc**), embedded processors using the Jam programming and test language, and the MAX+PLUS II or Quartus II software via the MasterBlaster or ByteBlasterMV download cables. When programming multiple EPC2 devices in a JTAG chain, the Quartus II and MAX+PLUS II software and other programming methods employ concurrent programming to simultaneously program multiple devices and reduce programming time. EPC2, EPC4, EPC8, and EPC16 devices can be programmed and erased up to 100 times.

After programming an EPC2, EPC4, EPC8, or EPC16 device in-system, APEX II, APEX 20K, Mercury, ACEX 1K, or FLEX device configuration can be initiated by including the EPC2 JTAG configuration instruction. See Table 10 on page 28.

For more information on programming and configuration support, see the following documents:

- *Altera Programming Hardware Data Sheet*
- *Programming Hardware Manufacturers*
- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *ByteBlaster Parallel Port Download Cable Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*

IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing

The EPC2 provides JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. The EPC2 device supports the JTAG instructions shown in Table 10.

The ISP circuitry in EPC2, EPC4, EPC8, and EPC16 devices is compatible with tools that support the IEEE Std. 1532. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

For EPC4, EPC8, and EPC16 JTAG instruction, refer to the *Enhanced Configuration Devices (EPC4, EPC8, & EPC16) Data Sheet*.

Table 10. EPC2 JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of a signal at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing results at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	Selects the device IDCODE register and places it between `TDI` and `TDO`, allowing the device IDCODE to be serially shifted out of `TDO`. The device IDCODE for the EPC2 configuration device is shown below: `0000 0001000000000010 00001101110 1`
USERCODE	Selects the USERCODE register and places it between `TDI` and `TDO`, allowing the USERCODE to be serially shifted out of `TDO`. The 32-bit USERCODE is a programmable user-defined pattern.
ISP Instructions	These instructions are used when programming an EPC2 device via JTAG ports with a MasterBlaster, ByteBlaster MV, ByteBlaster, or BitBlaster download cable, or using a Jam STAPL File (**.jam**), Jam STAPL Byte-Code File (**.jbc**), or SVF File via an embedded processor.
INIT_CONF	This function allows the user to initiate the APEX or FLEX configuration process by tying `nINIT_CONF` to the APEX or FLEX device(s) `nCONFIG` pin(s). After this instruction is updated, the `nINIT_CONF` pin is driven low. When the Initiate Configuration instruction is cleared, `nINIT_CONF` is released, which starts the APEX or FLEX device configuration. This instruction is used by the MAX+PLUS II software, Jam STAPL Files, and JBC Files.

For more information, see *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Figure 10 shows the timing requirements for the JTAG signals.

Figure 10. EPC2 JTAG Waveforms

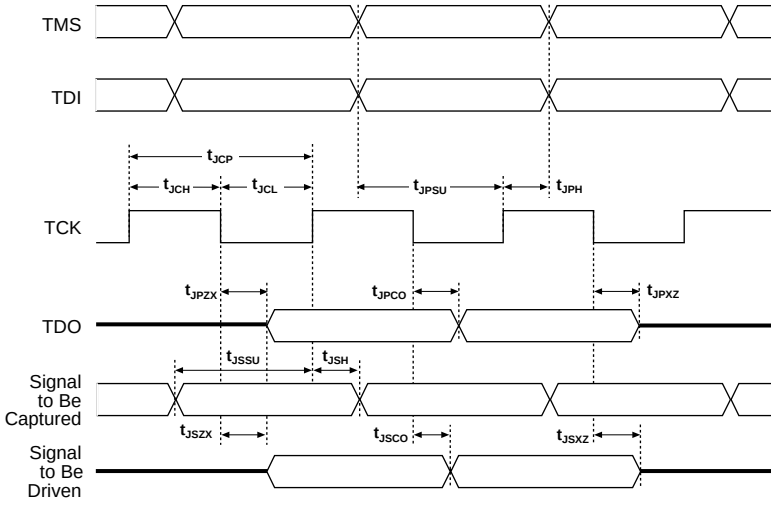


Table 11 shows the timing parameters and values for configuration devices.

Table 11. JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high-impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Operating Conditions

Tables 12 through 19 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for configuration devices.

For EPC4, EPC8, and EPC16 device operating conditions, refer to the *Enhanced Configuration Devices (EPC4, EPC8, & EPC16) Data Sheet*.

Table 12. Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage	With respect to ground *(2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or ground current			50	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			250	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		135	° C

Table 13. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage for 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for 3.3-V operation	*(3)*, *(4)*	3.0 (3.0)	3.6 (3.6)	V
V_I	Input voltage	With respect to ground	–0.3	V_{CC} + 0.3 *(5)*	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

Table 14. DC Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3 *(5)*	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V mode high-level TTL output voltage	I_{OH} = –4 mA DC *(6)*	2.4		V
	3.3-V mode high-level CMOS output voltage	I_{OH} = –0.1 mA DC *(6)*	V_{CC} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(6)*		0.4	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	–10	10	µA

Table 15. EPC1213, EPC1064 & EPC1064V Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100	200	µA
I_{CC1}	V_{CC} supply current (during configuration)			10	50	mA

Table 16. EPC2 Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)	V_{CC} = 5.0 V or 3.3 V		50	100	µA
I_{CC1}	V_{CC} supply current (during configuration)	V_{CC} = 5.0 V or 3.3 V		18	50	mA

Table 17. EPC1 Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			50	100	µA
I_{CC1}	V_{CC} supply current (during configuration)	V_{CC} = 5.0 V		30	50	mA
		V_{CC} = 3.3 V		10	16.5	mA

Table 18. EPC1441 Device I_{CC} Supply Current Values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			30	60	µA
I_{CC1}	V_{CC} supply current (during configuration)	V_{CC} = 5.0 V		15	30	mA
I_{CC1}	V_{CC} supply current (during configuration)	V_{CC} = 3.3 V		5	10	mA

Table 19. Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

***Notes to** Tables 12 – 19:*

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns under no-load conditions.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum V_{CC} rise time is 100 ms.
(5) Certain EPC2 pins may be driven to 5.75 V when operated with a 3.3-V V_{CC}. See Table 9 on page 26.
(6) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL or CMOS output current.
(7) Capacitance is sample-tested only.

Tables 20 through 24 show the device configuration parameters for APEX II, APEX 20K, Mercury, ACEX 1K, or FLEX devices.

Table 20. ACEX 1K, FLEX 10K & FLEX 6000 Device Configuration Parameters Using EPC2 Devices at 5.0-V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CE}	OE high to first clock delay				200	ns
t_{OEZX}	OE high to data output enabled				50	ns
t_{CO}	DCLK to data out delay				20	ns
t_{MCH}	DCLK high time for the first device in the configuration chain		30	50	75	ns
t_{MCL}	DCLK low time for the first device in the configuration chain		30	50	75	ns
f_{CK}	Clock frequency		6.7	10	16.7	MHz
t_{SCH}	DCLK high time for subsequent devices		30			ns
t_{SCL}	DCLK low time for subsequent devices		30			ns
t_{CASC}	CLK rising edge to nCASC				20	ns
t_{CCA}	nCS to nCASC cascade delay				10	ns
f_{CDOE}	CLK to data enable/disable				20	ns
t_{OEC}	OE low to CLK disable delay				20	ns
t_{NRCAS}	OE low (reset) to nCASC delay				25	ns
t_{NRR}	OE low time (reset) minimum		100			ns

Table 21. ACEX 1K, APEX 20K, APEX II, FLEX 10K & Mercury Device Configuration Parameters Using EPC2 Devices at 3.3-V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CE}	OE high to first clock delay				300	ns
t_{OEZX}	OE high to data output enabled				80	ns
t_{CO}	DCLK to data out delay				30	ns
t_{MCH}	DCLK high time for the first device in the configuration chain		40	65	100	ns
t_{MCL}	DCLK low time for the first device in the configuration chain		40	65	100	ns
f_{CK}	Clock frequency		5	7.7	12.5	MHz
t_{SCH}	DCLK high time for subsequent devices		40			ns
t_{SCL}	DCLK low time for subsequent devices		40			ns
t_{CASC}	CLK rising edge to nCASC				25	ns
t_{CCA}	nCS to nCASC cascade delay				15	ns
f_{CDOE}	CLK to data enable/disable				30	ns
t_{OEC}	OE low to CLK disable delay				30	ns
t_{NRCAS}	OE low (reset) to nCASC delay				30	ns
t_{NRR}	OE low time (reset) minimum		100			ns

Table 22. ACEX 1K, FLEX 10K & FLEX 6000 Device Configuration Parameters Using EPC1 & EPC1441 Devices at 5.0-V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CE}	OE high to first clock delay				200	ns
t_{OEZX}	OE high to data output enabled				50	ns
t_{CO}	DCLK to data out delay				20	ns
t_{MCH}	DCLK high time for the first device in the configuration chain		30	50	75	ns
t_{MCL}	DCLK low time for the first device in the configuration chain		30	50	75	ns
f_{CK}	Clock frequency		6.7	10	16.7	MHz
t_{SCH}	DCLK high time for subsequent devices		30			ns
t_{SCL}	DCLK low time for subsequent devices		30			ns
t_{CASC}	CLK rising edge to nCASC				20	ns
t_{CCA}	nCS to nCASC cascade delay				10	ns
f_{CDOE}	CLK to data enable/disable				20	ns
t_{OEC}	OE low to CLK disable delay				20	ns
t_{NRCAS}	OE low (reset) to nCASC delay				25	ns
t_{NRR}	OE low time (reset) minimum		100			ns

Table 23. ACEX 1K, FLEX 10K & FLEX 6000 Device Configuration Parameters Using EPC1 & EPC1441 Devices at 3.3-V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CE}	OE high to first clock delay				300	ns
t_{OEZX}	OE high to data output enabled				80	ns
t_{CO}	DCLK to data out delay				30	ns
t_{MCH}	DCLK high time for the first device in the configuration chain		50	125	250	ns
t_{MCL}	DCLK low time for the first device in the configuration chain		50	125	250	ns
f_{CK}	Clock frequency		2	4	10	MHz
t_{SCH}	DCLK high time for subsequent devices		50			ns
t_{SCL}	DCLK low time for subsequent devices		50			ns
t_{CASC}	CLK rising edge to nCASC				25	ns
t_{CCA}	nCS to nCASC cascade delay				15	ns
f_{CDOE}	CLK to data enable/disable				30	ns
t_{OEC}	OE low to CLK disable delay				30	ns
t_{NRCAS}	OE low (reset) to nCASC delay				30	ns
t_{NRR}	OE low time (reset) minimum		100			ns

Table 24. FLEX 8000 Device Configuration Parameters Using EPC1, EPC1441, EPC1213, EPC1064 & EPC1064V Devices

Symbol	Parameter	Conditions	EPC1064V		EPC1064 EPC1213		EPC1 EPC1441		Unit
			Min	Max	Min	Max	Min	Max	
t_{OEZX}	OE high to DATA output enabled			75		50		50	ns
t_{CSZX}	nCS low to DATA output enabled			75		50		50	ns
t_{CSXZ}	nCS high to DATA output disabled			75		50		50	ns
t_{CSS}	nCS low setup time to first DCLK rising edge		150		100		50		ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		0		0		ns
t_{DSU}	Data setup time before rising edge on DCLK		75		50		50		ns
t_{DH}	Data hold time after rising edge on DCLK		0		0		0		ns
t_{CO}	DCLK to DATA out delay			100		75		75	ns
t_{CK}	Clock period		240		160		100		ns
f_{CK}	Clock frequency			4		6		8	MHz
t_{CL}	DCLK low time		120		80		50		ns
t_{CH}	DCLK high time		120		80		50		ns
t_{XZ}	OE low or nCS high to DATA output disabled			75		50		50	ns
t_{OEW}	OE pulse width to guarantee counter reset		150		100		100		ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			90		60		50	ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			75		50		50	ns
t_{CEOUT}	nCS high to nCASC high delay			150		100		100	ns

Revision History

The information contained in the *Configuration Devices for SRAM-Based LUT Devices Data Sheet* version 12.2 supersedes information published in pervious versions. The following changes were made to the *Configuration Devices for SRAM-Based LUT Devices Data Sheet* version 12.2:

Version 12.2

- Corrected the APEX 20KE voltate in Table 2 to 1.8 V.
- Updated Figure 5.

Version 12.1

- Updated Table 2.
- Updated notes to Figures 4, 5, and 6.
- Added APEX 20KE device diagrams to Figures 4 and 6.

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