ECMF02-2AMX6

Common mode filter with ESD protection for USB 2.0 and MIPI D-PHY/MDDI interface

Features

- Very large differential bandwidth > 6 GHz
- High common mode attenuation:
  - -34 dB at 900 MHz
  - -20 dB between 800 MHz and 2.2 GHz
- Very low PCB space consumption
- Thin package: 0.55 mm max
- Lead-free package
- High reduction of parasitic elements through integration

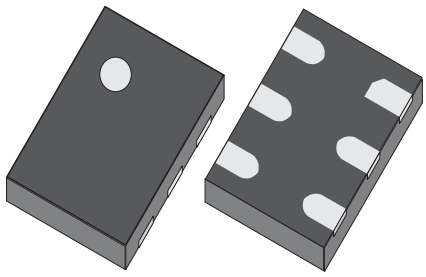
Applications

- Mobile phones
- Notebook, laptop
- Portable devices
- PND

Description

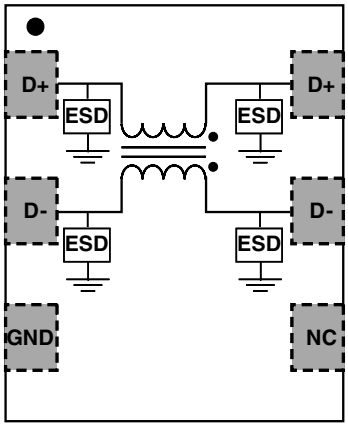
The ECMF02-2AMX6 is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like MIPI D-PHY, MDDI or USB 2.0.

The ECMF02-2AMX6 can protect and filter one differential lane.



Micro QFN-6L: 1.7 mm x 1.5 mm

Figure 1. Pin configuration (top view)



1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	Peak pulse voltage: IEC 61000-4-2, level 4 contact discharge	8	kV
T_j	Junction temperature	125	°C
T_{op}	Operating junction temperature range	-30 to +85	°C
T_{stg}	Storage temperature range	- 55 to +150	°C

Figure 2. Electrical characteristics (definitions)

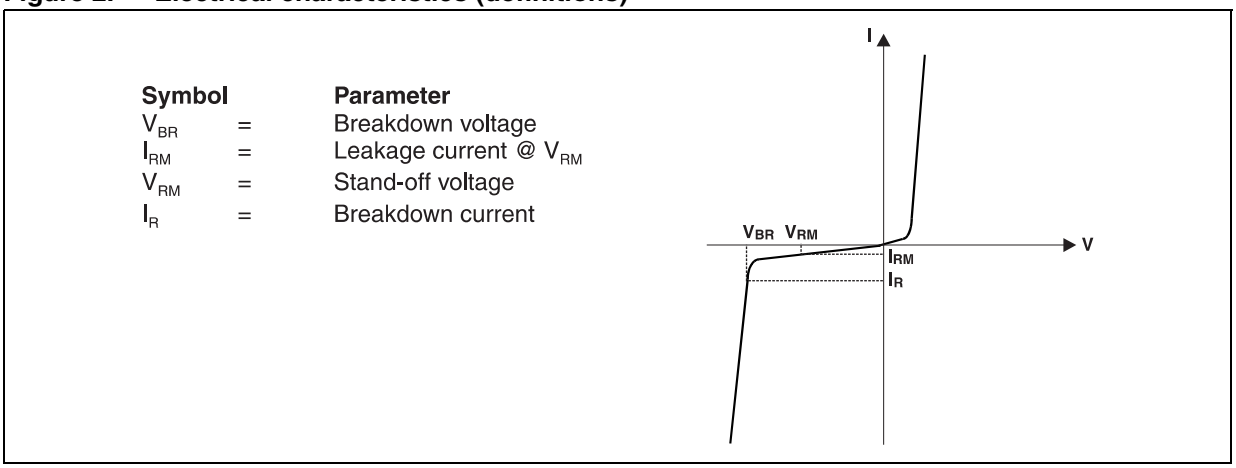


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 1.5 V per line			100	nA
R_{DC}	DC serial resistance		1.8	2.5	Ω

Compliant with USB 2.0 high speed sync field test (150 mV diff).

Figure 3. S_{dd21} differential attenuation measurements ($Z_{0\ diff}$ = 100 Ω)

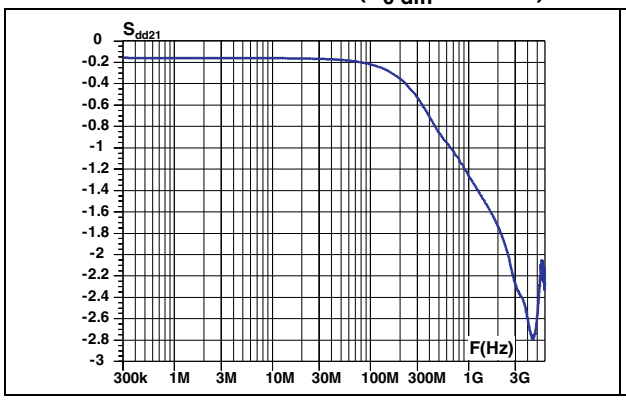


Figure 4. S_{cc21} common mode attenuation measurements ($Z_{0\ com}$ = 50 Ω)

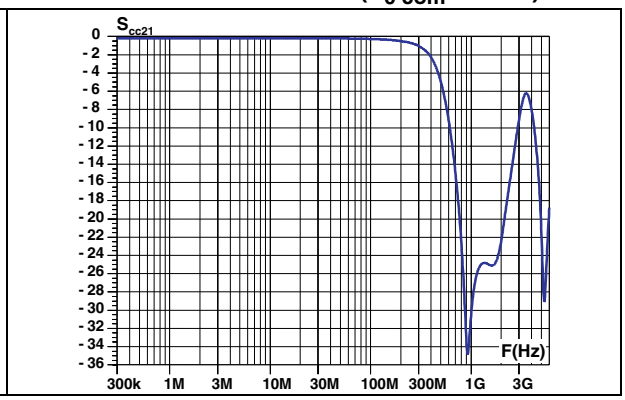


Figure 5. S_{dd11}, S_{dd22} differential return loss measurements ($Z_{0\ diff}$ = 100 Ω)

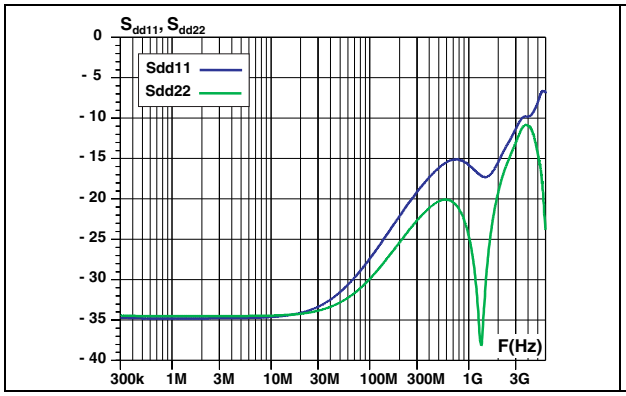


Figure 6. S_{dd41} / S_{dd23} inter-lane differential cross-coupling measurements ($Z_{0\ diff}$ = 100 Ω)

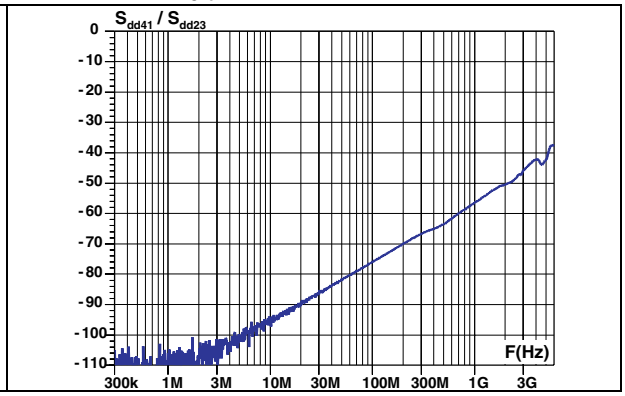


Figure 7. S_{dd21} differential attenuation measurements ($Z_{0\ diff}$ = 90 Ω)

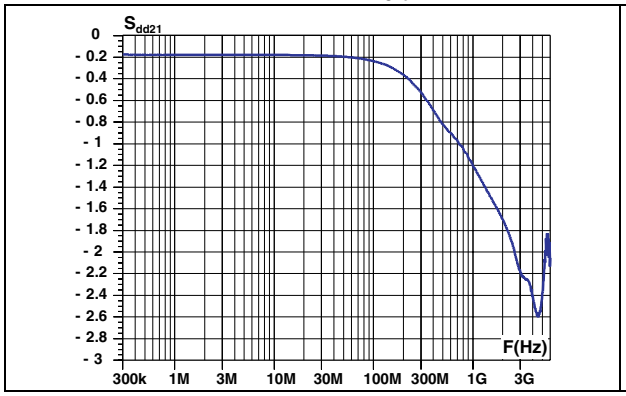


Figure 8. S_{cc21} common mode attenuation measurements ($Z_{0\ com}$ = 45 Ω)

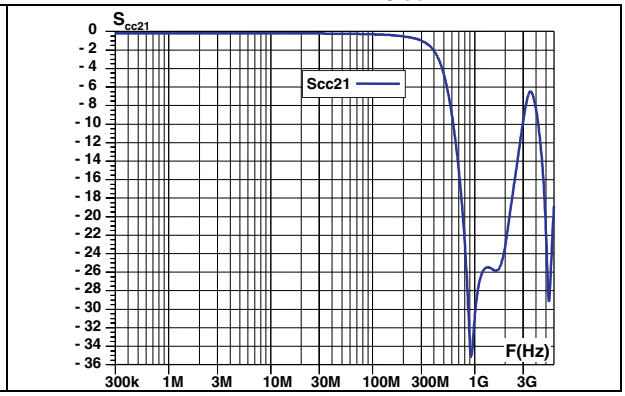


Figure 9. ESD measurement test setup

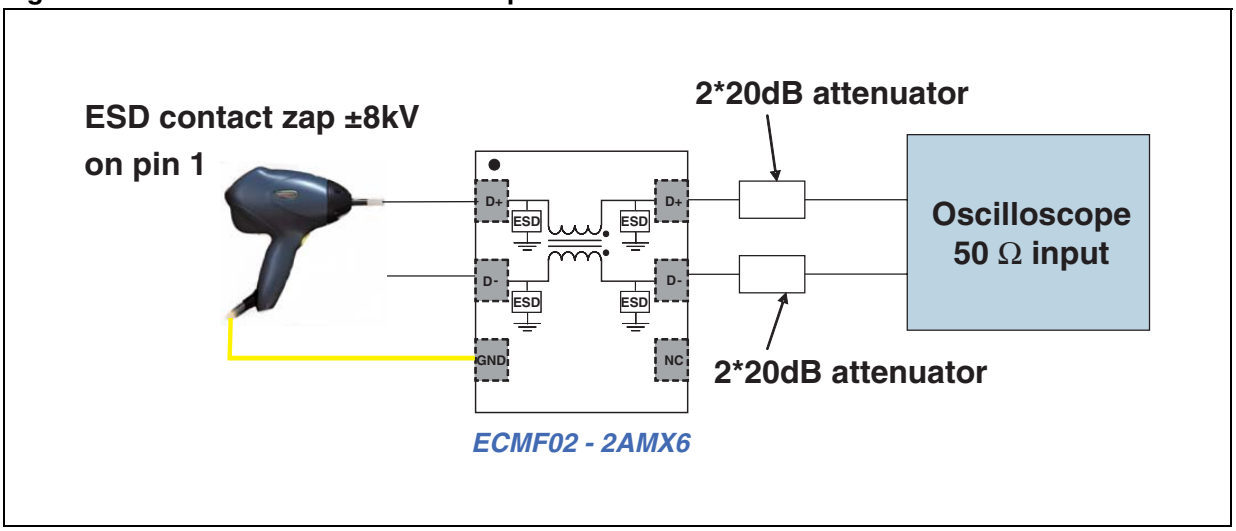


Figure 10. ESD response to IEC 61000-4-2 (+8 kV contact discharge) - see *Figure 9* for test setup

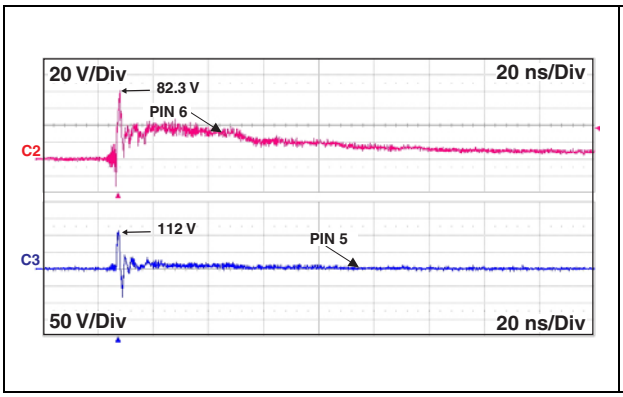


Figure 11. ESD response to IEC 61000-4-2 (-8 kV contact discharge) - see *Figure 9* for test setup

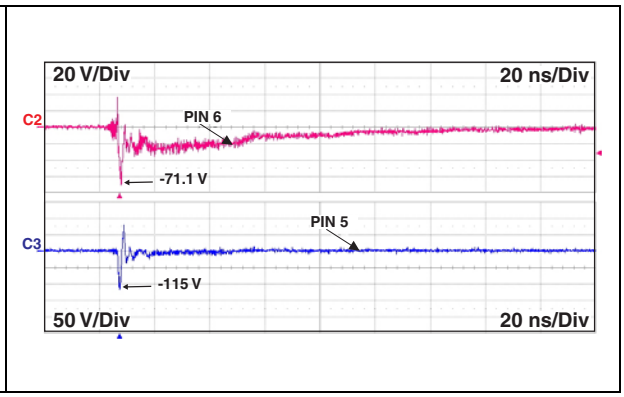


Figure 12. MIPI D-PHY low power mode test setup

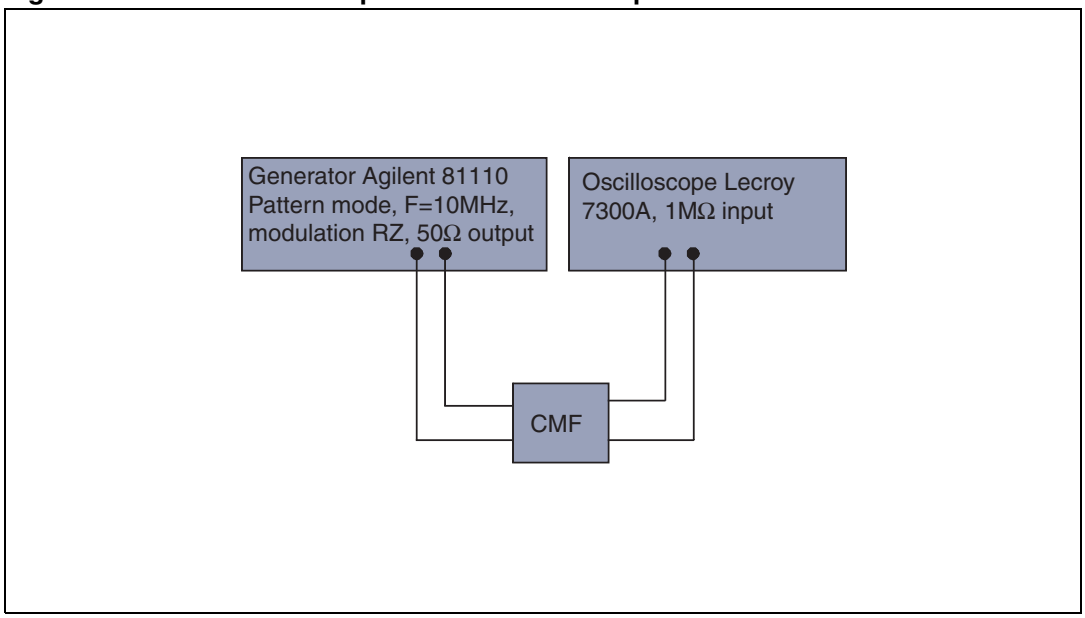


Figure 13. Low power pulse response - see *Figure 12* for test setup

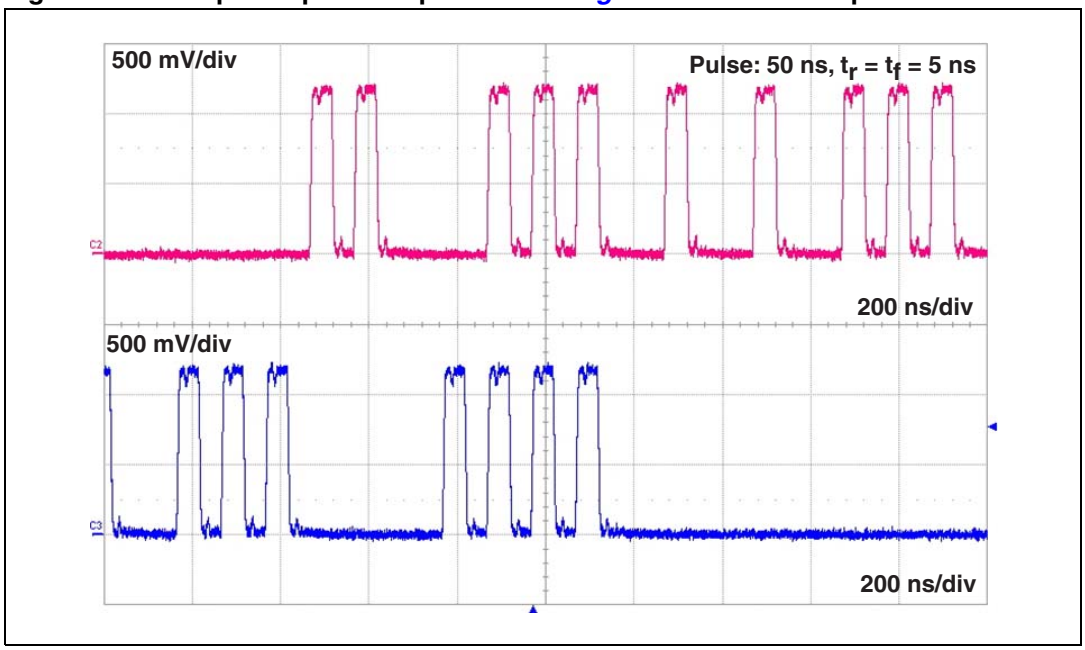


Figure 14. USB 2.0 HSync measurement test setup

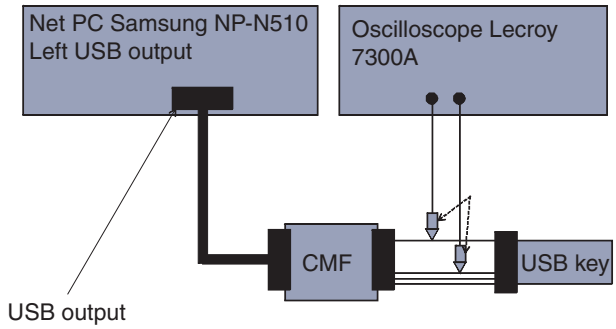


Figure 15. USB 2.0 HSync measurement result

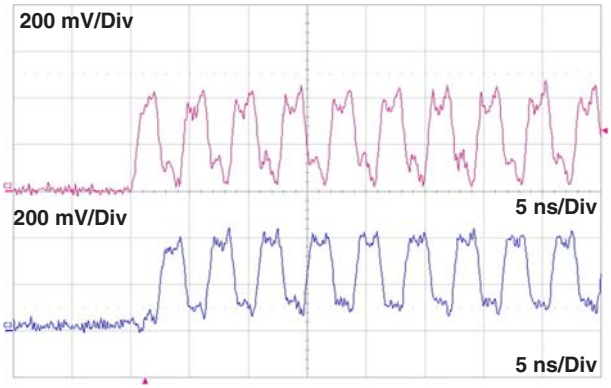
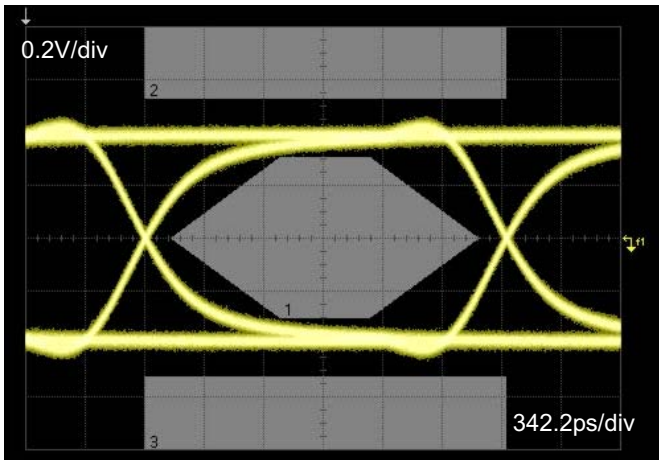


Figure 16. USB 2.0 eye diagram, mask T1



2 Application schematics

Figure 17. MIPI D-PHY

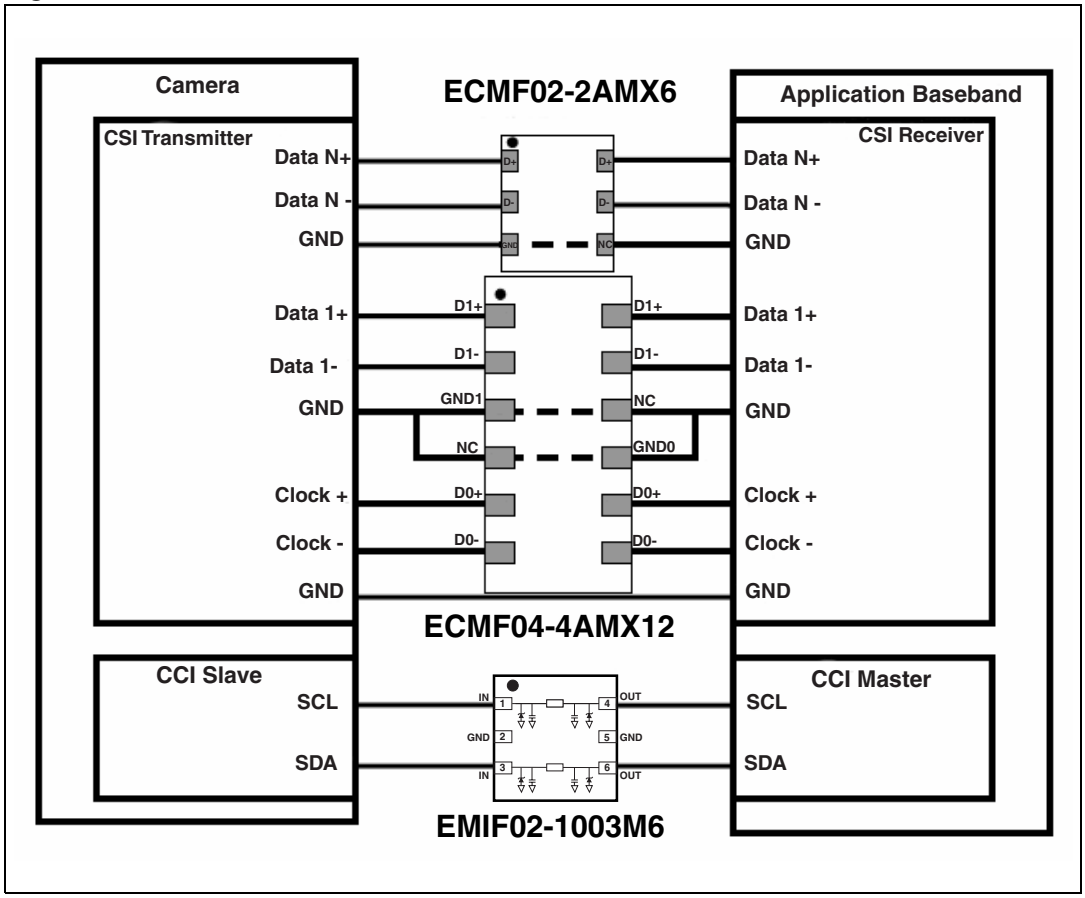
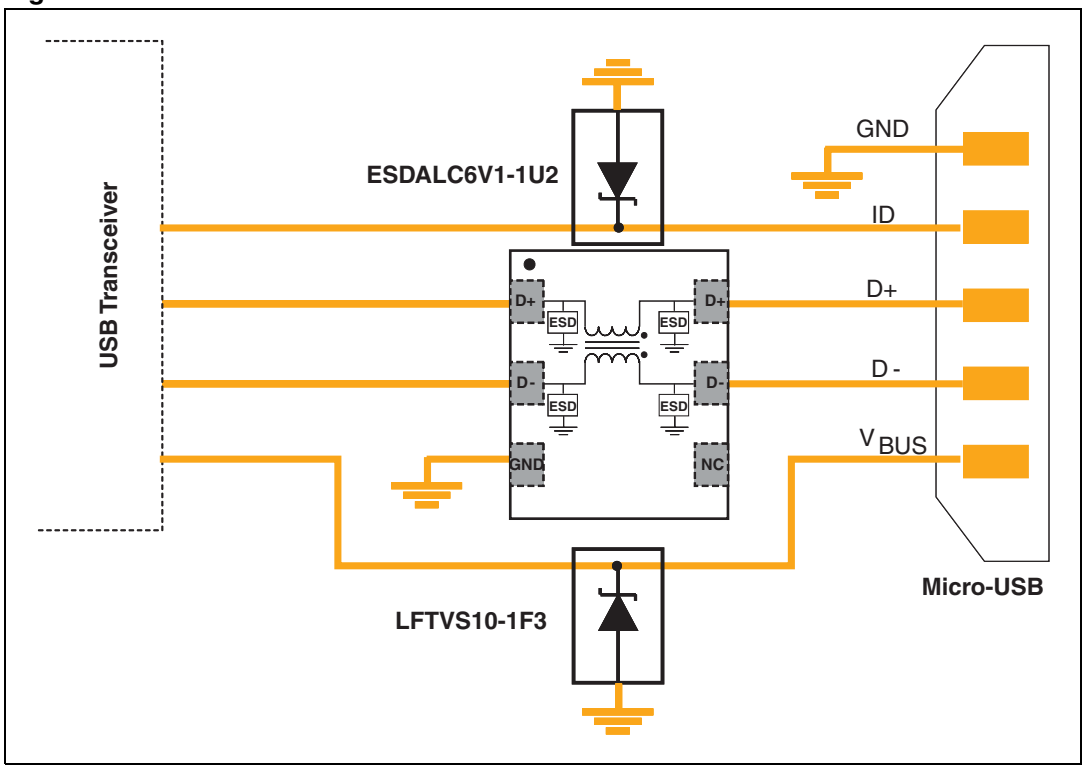
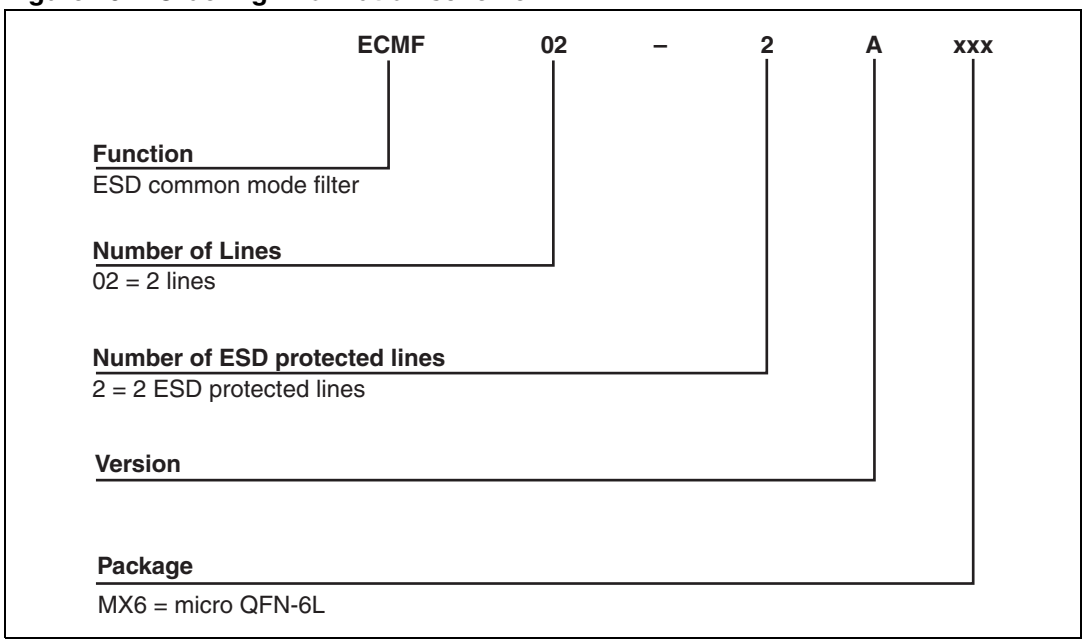


Figure 18. USB 2.0



3 Ordering information scheme

Figure 19. Ordering information scheme

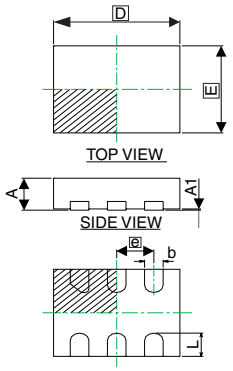


4 Package information

- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. Micro QFN-6L 1.7x1.5 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.00	0.0008	0.0009
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.65	1.70	1.75	0.065	0.067	0.069
E	1.45	1.50	1.55	0.057	0.059	0.061
e	0.45	0.50	0.55	0.018	0.020	0.022
L	0.30	0.40	0.50	0.012	0.016	0.020

Figure 20. Footprint (dimensions in mm)

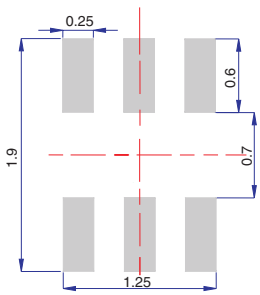
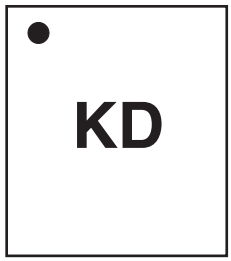
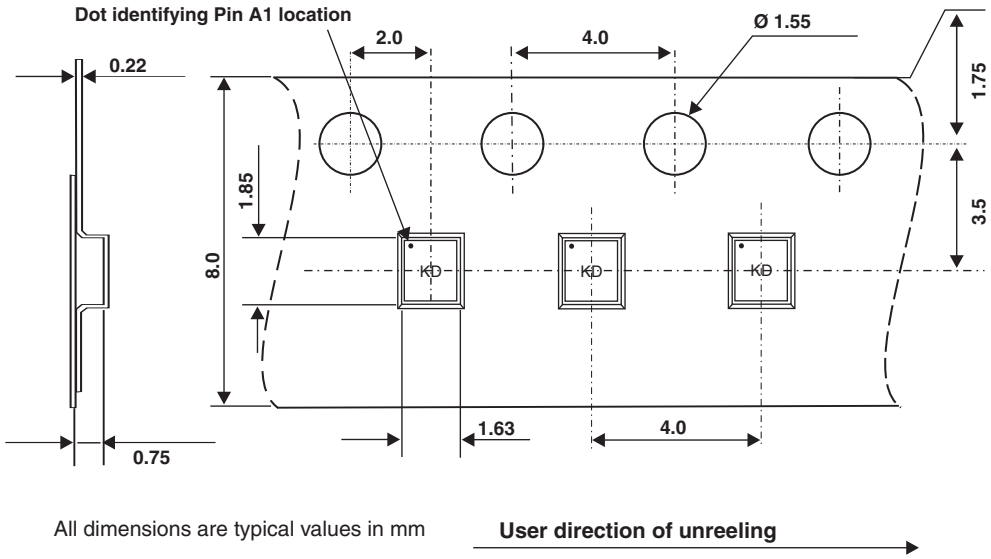


Figure 21. Marking



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 22. Tape and reel specifications

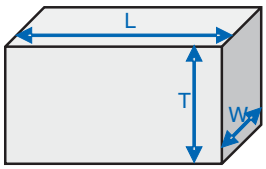


5 Recommendation on PCB assembly

5.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 23. Stencil opening dimensions



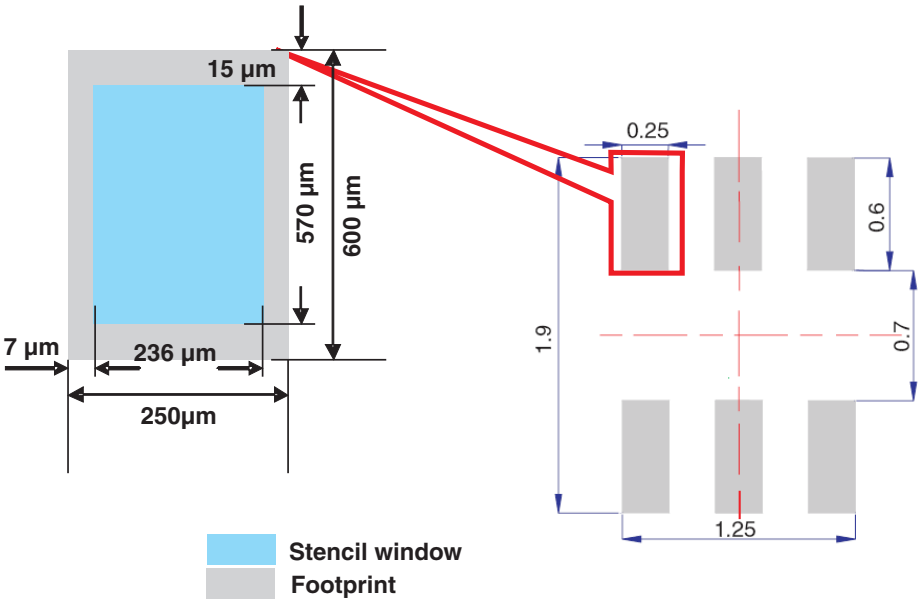
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 24. Recommended stencil window position



5.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

5.3 Placement

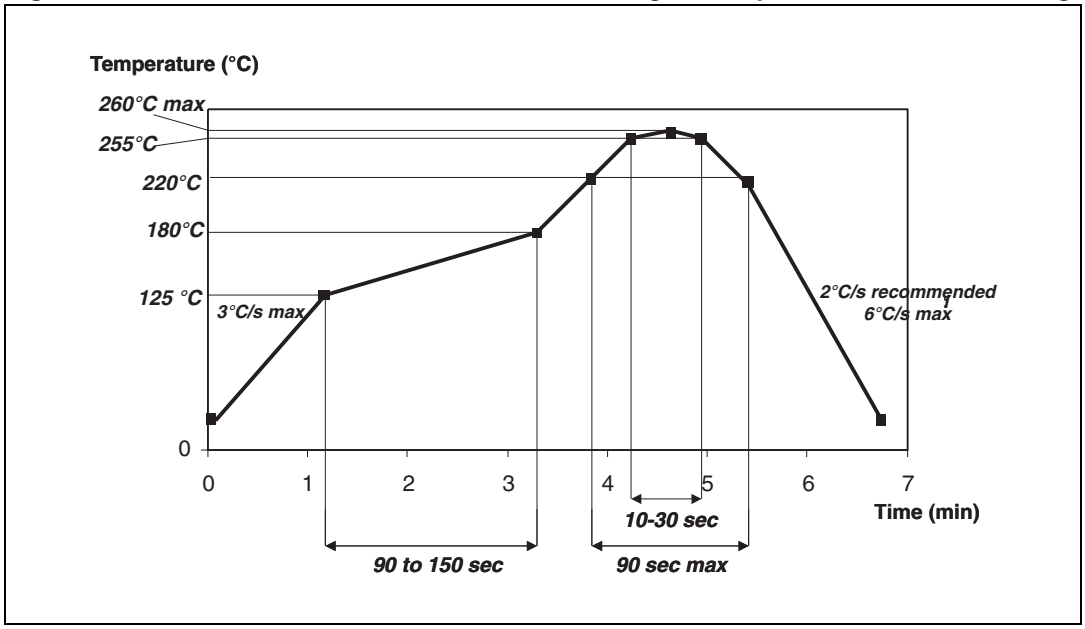
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.5 Reflow profile

Figure 25. ST ECOPACK® recommended soldering reflow profile for PCB mounting

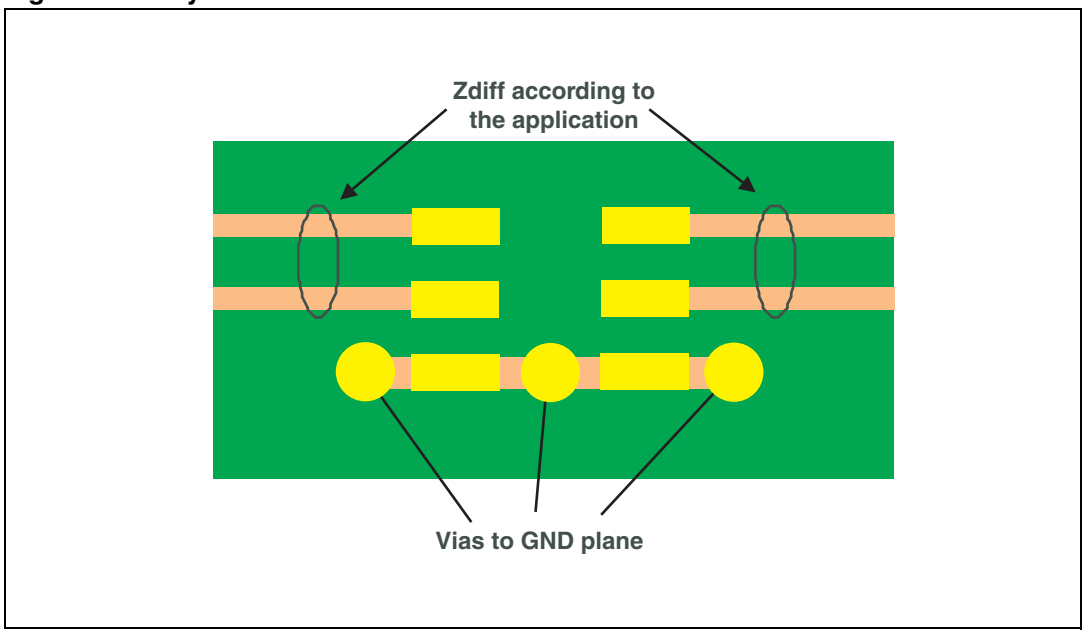


Note: Minimize air convection currents in the reflow oven to avoid component movement.

5.6 Layout recommendation

Connection to PCB GND must be as short as possible to ensure ESD remaining voltage and S_{CC21} performance.

Figure 26. Layout recommendation



6 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ECMF02-2AMX6	KD(1)	µQFN-6L	3.55 mg	3000	Tape and reel 7”

1. The marking can be rotated by 90° to differentiate assembly location

For the latest information on available order codes see the product pages on www.st.com.

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
10-Aug-2010	1	Initial release.

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