INTEGRATED CIRCUITS

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

# HEF4014B MSI
## 8-bit static shift register

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

## DESCRIPTION

The HEF4014B is a fully synchronous edge-triggered 8-bit static shift register with eight synchronous parallel inputs ($P_0$ to $P_7$), a synchronous serial data input ($D_S$), a synchronous parallel enable input (PE), a LOW to HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages ($O_5$ to $O_7$).

Operation is synchronous and the device is edge-triggered on the LOW to HIGH transition of CP. Each register stage is of a D-type master-slave flip-flop. When PE is HIGH, data is loaded into the register from $P_0$ to $P_7$ on the LOW to HIGH transition of CP. When PE is LOW, data is shifted to the first position from $D_S$, and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times

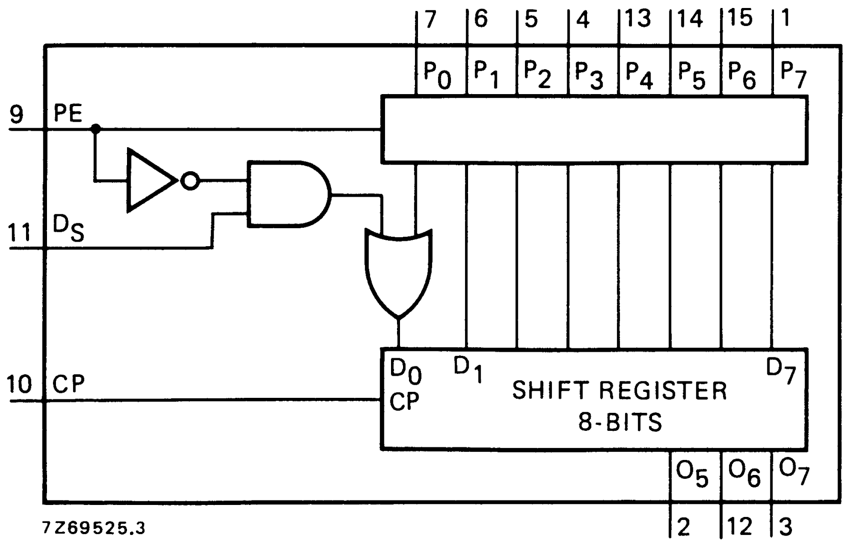


Fig.1 Functional diagram.

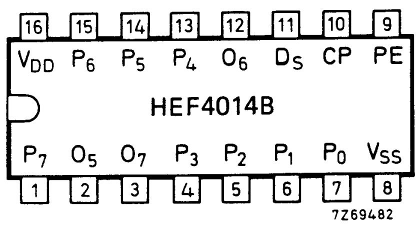


Fig.2 Pinning diagram.

HEF4014BP(N): 16-lead DIL; plastic (SOT38-1)

HEF4014BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF4014BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

**FAMILY DATA, $I_{DD}$ LIMITS category MSI**

See Family Specifications

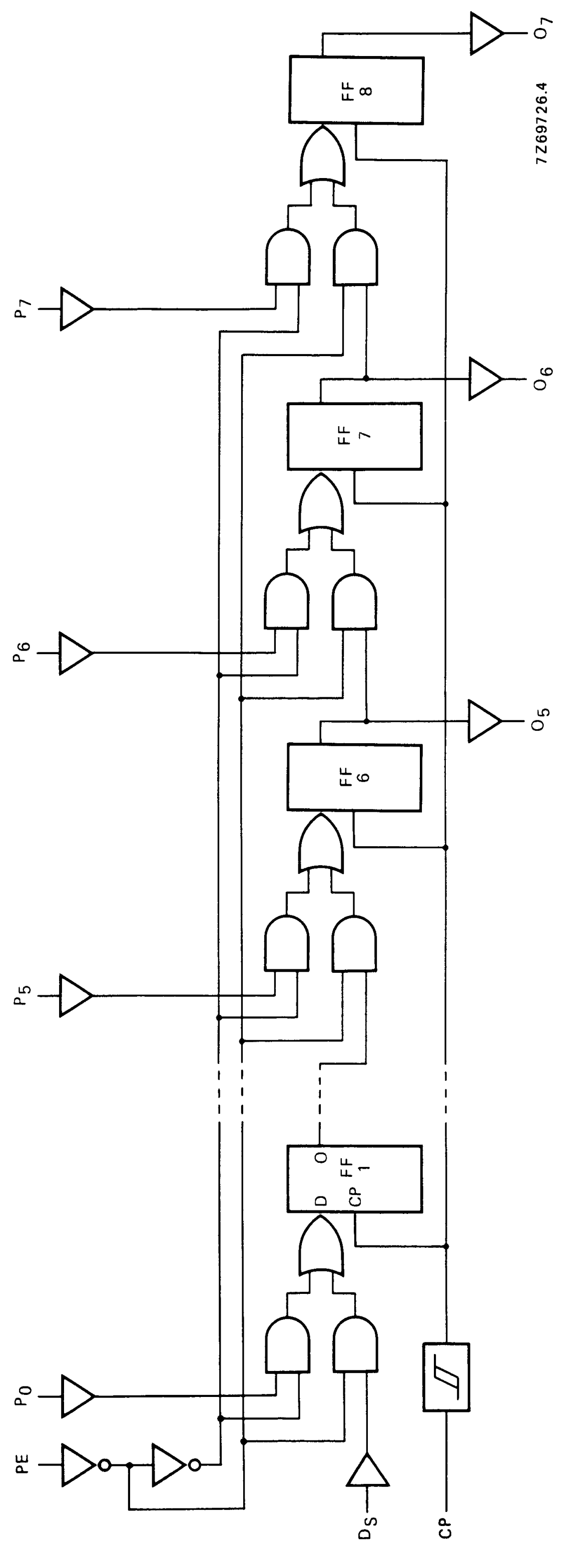


Fig.3 Logic diagram.

## PINNING

| | |
|---|---|
| PE | parallel enable input |
| $P_0$ to $P_7$ | parallel data inputs |
| $D_S$ | serial data input |
| CP | clock input (LOW to HIGH edge-triggered) |
| $O_5$ to $O_7$ | buffered parallel outputs from the last three stages |

## FUNCTION TABLES

Serial operation

| n | INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| | **CP** | **$D_S$** | **PE** | **$O_5$** | **$O_6$** | **$O_7$** |
| 1 | ↑ | $D_1$ | L | X | X | X |
| 2 | ↑ | $D_2$ | L | X | X | X |
| 3 | ↑ | $D_3$ | L | X | X | X |
| 6 | ↑ | X | L | $D_1$ | X | X |
| 7 | ↑ | X | L | $D_2$ | $D_1$ | X |
| 8 | ↑ | X | L | $D_3$ | $D_2$ | $D_1$ |
| | ↓ | X | X | no change | | |

Parallel operation

| n | INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| | **CP** | **$D_S$** | **PE** | **$O_5$** | **$O_6$** | **$O_7$** |
| 1 | ↑ | X | H | $P_5$ | $P_6$ | $P_7$ |
| | ↓ | X | X | no change | | |

### Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ↑ = positive-going transition
   ↓ = negative-going transition
   $D_n$ = either HIGH or LOW
   n = number of clock pulse transitions

## AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leq 20$ ns

| | $V_{DD}$ V | TYPICAL FORMULA FOR P (μW) | |
|---|---|---|---|
| Dynamic power dissipation per package (P) | 5 | $900\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | where |
| | 10 | $4\ 300\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | $f_i$ = input freq. (MHz) |
| | 15 | $12\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | $f_o$ = output freq. (MHz) |
| | | | $C_L$ = load cap. (pF) |
| | | | $\sum (f_o C_L)$ = sum of outputs |
| | | | $V_{DD}$ = supply voltage (V) |

## AC CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ≤ 20 ns

| | $V_{DD}$ V | SYMBOL | MIN. | TYP. | MAX. | | TYPICAL EXTRAPOLATION FORMULA |
|---|---|---|---|---|---|---|---|
| Propagation delays | | | | | | | |
| $C_P \to O_n$ | 5 | | | 130 | 260 | ns | 103 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 115 | 230 | ns | 88 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| Output transition times | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{THL}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{TLH}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| Set-up times | 5 | | 40 | 10 | | ns | |
| PE → CP | 10 | $t_{su}$ | 25 | 5 | | ns | |
| | 15 | | 15 | 0 | | ns | |
| | 5 | | 35 | – 5 | | ns | |
| $D_S \to$ CP | 10 | $t_{su}$ | 25 | –5 | | ns | |
| | 15 | | 25 | 0 | | ns | |
| | 5 | | 35 | –5 | | ns | |
| $P_n \to$ CP | 10 | $t_{su}$ | 25 | –5 | | ns | |
| | 15 | | 25 | 0 | | ns | |
| Hold times | 5 | | 25 | –5 | | ns | |
| PE → CP | 10 | $t_{hold}$ | 20 | 0 | | ns | see also waveforms Fig.4 |
| | 15 | | 15 | 0 | | ns | |
| | 5 | | 30 | 15 | | ns | |
| $D_S \to$ CP | 10 | $t_{hold}$ | 20 | 10 | | ns | |
| | 15 | | 15 | 7 | | ns | |
| | 5 | | 30 | 15 | | ns | |
| $P_n \to$ CP | 10 | $t_{hold}$ | 20 | 10 | | ns | |
| | 15 | | 15 | 7 | | ns | |
| Minimum clock | 5 | | 70 | 35 | | ns | |
| pulse width; LOW | 10 | $t_{WCPL}$ | 30 | 15 | | ns | |
| | 15 | | 24 | 12 | | ns | |
| Maximum clock | 5 | | 6 | 13 | | MHz | |
| pulse frequency | 10 | $f_{max}$ | 15 | 30 | | MHz | |
| | 15 | | 20 | 40 | | MHz | |

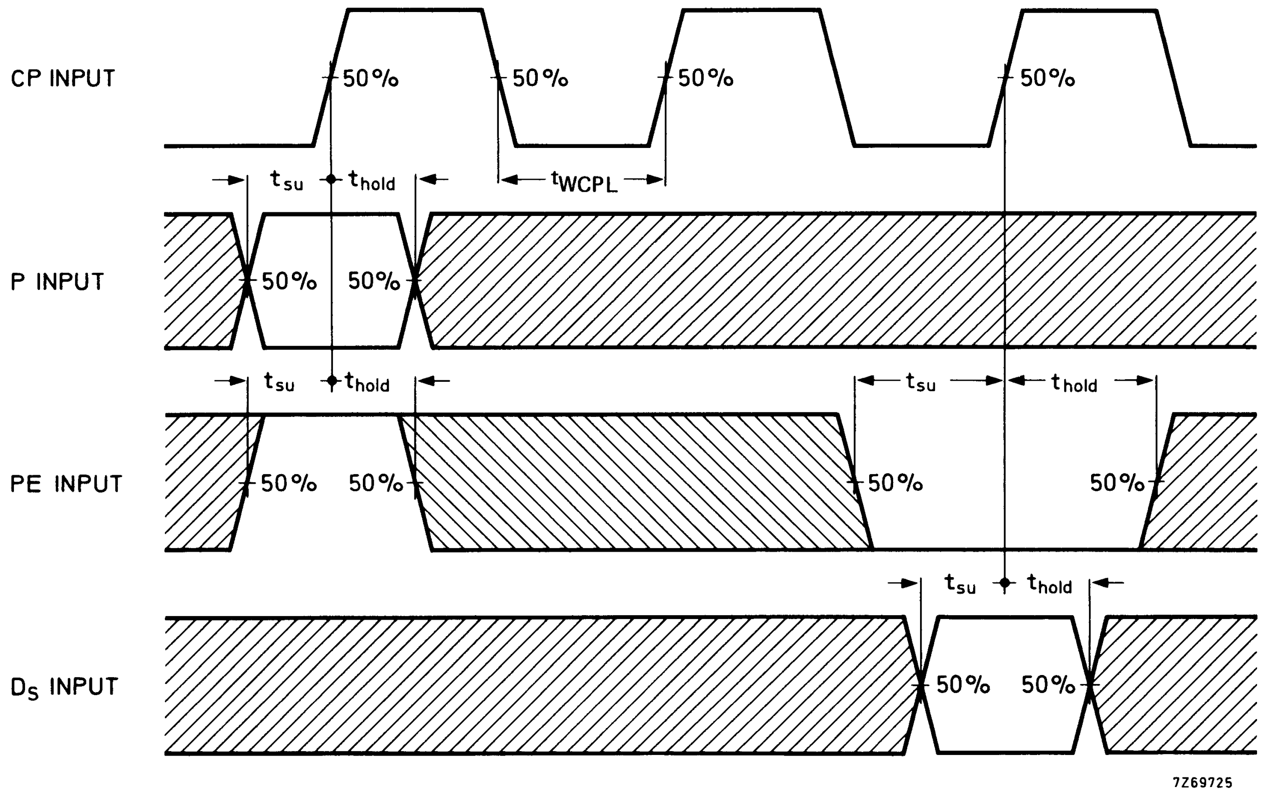


Fig.4 Waveforms showing minimum clock pulse width, and set-up and hold times for PE to CP, $D_S$ to CP, and P to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

## APPLICATION INFORMATION

Some examples of applications for the HEF4014B are:

- Parallel-to-serial converter
- Serial data queueing
- General purpose register