

GENERAL DESCRIPTION

The W83787IF is a derivative product of W83787F with one of UARTs support HPSIR and ASKIR. The W83787IF integrates a disk drive adapter ,two 16550 compatible UARTs, and one parallel port with EPP mode, ECP mode, and joystick mode.

The disk drive adapter functions of the W83787IF is same as W83787F which including a floppy disk drive controller compatible with the industry standard 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83787IF greatly reduces the number of components required for interfacing with floppy disk drives. The W83787IF supports four 360K, 720K, 1.2M, 1.44M disk drives and data transfer rates of 250Kb/S, 300Kb/S, 500Kb/S.

There are two high-speed serial communication ports (UARTs) on the W83787IF, one of them support serial infrared communication. The UARTs include 16-byte send/receive FIFOs, a programmable baud rate generator, complete modem control capability, and a processor interrupt system.

The W83787IF supports three optional PC-compatible printer ports: 378h, 278h and 3BCh. Additional bi-directional I/O capability is available by hardware control or software programming. The parallel port also supports the Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP).

The W83787IF supports two embedded hard disk drive (AT bus) interfaces and a game port with decoded read/write output.

The W83787IF's Extension FDD Mode and Extension 2FDD Mode allow one or two external floppy disk drives to be connected to the computer through the printer interface pins in notebook computer applications.

The Extension Adapter Mode of the W83787IF allows pocket devices to be installed through the printer interface pins in notebook computer applications according to a protocol set by Winbond, but with upgraded performance.

The JOYSTICK mode allows a joystick to be connected to a parallel port with a signal switching cable.

The configuration register supports address selection, mode selection, function enable/disable, and power down function selection.

FEATURES

- **1.44MB Floppy Disk Controller**

- Support four 360K,720K,1.2M,1.44M floppy disk drives
- Data Transfer Rate 250Kb/s,300Kb/s,500Kb/s
- Single 24Mhz crystal input
- FDD anti-virus function with software write protect and FDD write enable signal, write data signal force inactive

- **Serial Ports**

- Two high speed **16550 UART** with **16 byte FIFO**
- Programmable baud rate generator
- Modem Control Circuitry
- Support **IrDA(HPSIR)** and Amplitude Shift Keyed IR(**ASKIR**) Infrared communication
- MIDI compatible

- **Parallel Port**

- Support **Standard Parallel Port(SPP),Enhanced Parallel Port(EPP), Enhanced Capability Port(ECP)**
- **Joystick mode** supports joystick through parallel port
- **Extension FDD mode** support disk drive B through parallel port
- **Extension Adapter Mode** support pocket devices through parallel port
- **Extension 2FDD mode** support disk drive A and B through parallel port
- Compatible with IBM Parallel Port
- Support parallel port with bi-directional lines

- **IDE Interface**

- Support two embedded hard disk drives(IDE AT BUS)

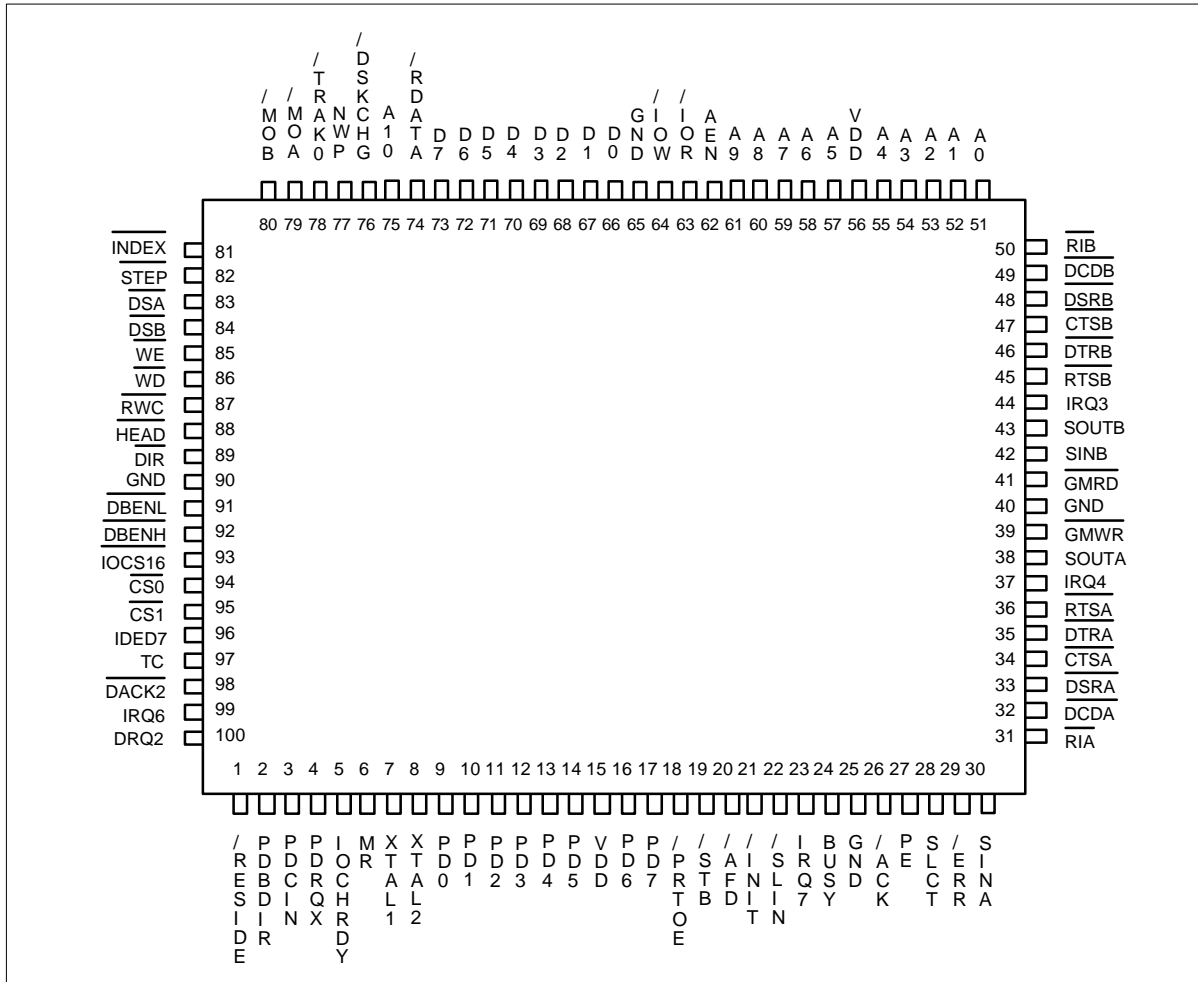
- **Game Port Supported**

- **Based on pinout of W83777/787F**

- **Two General Purpose I/O pins**

- **100 PQFP**

PIN CONFIGURATION



1.0 PIN DESCRIPTION

Note I: Input pin, O: Output pin, I/O: Bi-directional pin, OD: Open Drain pin.

1.1 Host Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---------|----------------|-----|---|
| D0-D7 | 66-73 | I/O | System data bus bits 0-7 |
| A0-A9 | 51-55 57-61 | I | System address bus bits 0-9 |
| A10 | 75 | I | In ECP Mode, this pin is the A10 address input. |
| IOCHRDY | 5 | OD | In EPP Mode, this pin is the IO Channel Ready output to extend the host read/write cycle. |
| MR | 6 | I | Master Reset. Active high. MR is low during normal operations. |

Host Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|---|-----|-----|---|
| AEN | 62 | I | System address bus enable |
| $\overline{\text{IOR}}$ | 63 | I | CPU I/O read signal |
| $\overline{\text{IOW}}$ | 64 | I | CPU I/O write signal |
| DRQ2 | 100 | O | When DRQ2 = 1, a DMA request is being made by the FDC |
| $\overline{\text{DACK2}}$ | 98 | I | DMA Acknowledge. When this pin is active, a DMA cycle is underway and the controller is executing a DMA transfer. |
| TC | 97 | I | Terminal Count. When active, this pin indicates termination of a DMA transfer. |
| IRQ6 | 99 | O | Interrupt request generated by FDC |
| IRQ4 | 37 | O | Interrupt request generated by UART A or UART B when their addresses are COM1 or COM3. This interrupt request can be tri-stated by setting bit 3 of HCR low. This signal is at high impedance after each reset operation. |
| IRQ3 | 44 | O | Interrupt request generated by UART A or UART B when their addresses are COM2 or COM4. Same as IRQ4 |
| IRQ7 | 23 | O | When IRQ7 = 1 and interrupt request is being made by the printer, this pin is pulled high internally. In EPP or ECP mode, IRQ7 is pulsed low, then released to allow sharing of interrupts. |
| PDRQX HPRTM1 | 4 | I/O | In Extension Adapter mode this pin is a DMA Request generated by Extension Adapter. This request is output directly from XDRQ. In ECP mode, this pin is the parallel port DMA Request output. During power-on reset, this pin is pulled down internally and is defined as HPRTM1, which is used for selecting the mode of the parallel port (see Table 1-1). |
| $\overline{\text{PRTOE}}$ $\overline{\text{PDACKX}}$ | 18 | I | In printer mode, this pin is for data direction control. When it is set to low, the parallel port functions as an output port. When it is set to high, the direction of the data bus is controlled by Bit 5 (DIR) of the printer control register and Bit 7 (PRTBEN) of CR3. This pin is pulled up internally. In Extension Adapter mode, this pin is the DMA acknowledge for the Extension Adapter. When this pin is active, a DMA cycle is underway and the controller is executing a DMA transfer. In ECP mode, this pin is the parallel port DMA Acknowledge input. |
| XTAL1 | 7 | I | 24Mhz XTAL/Oscillator/Clock input |
| XTAL2 | 8 | O | XTAL output |

1.2 Serial Port Interface

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|---|
| CTSA | 34 | I | Clear To Send is the modem control input. |
| CTSB | 47 | | The function of these pins can be tested by reading Bit 4 of the handshake status register. |
| DSRA | 33 | I | Data Set Ready. An active low indicates the modem or data set is ready to establish a communication link and transfer data to the UART. |
| DSRB | 48 | | |
| DCDA | 32 | I | Data Carrier Detect. An active low indicates the modem or data set has detected a data carrier. |
| DCDB | 49 | | |
| RIA | 31 | I | Ring Indicator. An active low indicates that a ring signal is being received by the modem or data set. |
| RIB | 50 | | |
| SINA | 30 | I | Serial Input. Used to receive serial data from the communication link. |
| SINB | 42 | | SINB can be programmed by CR0D register as input pin IRRX1 for serial infrared communication |
| IRRX1 | | | |
| SOUTA | 38 | I/O | UART A Serial Output. Used to transmit serial data out to the communication link. During power-on reset, this pin is pulled up internally and is defined as HURAS1, which is used for selecting the I/O address of the UART A. (See Table 1-2.) |
| HURAS1 | | | |
| SOUTB | 43 | I/O | UART B Serial Output. Used to transmit serial data out to the communication link. SOUTB can be programmed by CR0D register as output pin IRTX1 for serial infrared communication. |
| HURBS1 | | O | During power-on reset, this pin is pulled up internally and is defined as HURBS1, which is used for selecting the I/O address of UARTB. (See Table 1-2.) |
| IRTX1 | | | |
| DTRA | 35 | I/O | UART A Data Terminal Ready. An active low informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as HPRAS0. It is used for selecting the address of the parallel port. (See Table 1-3.) |
| HPRAS0 | | | |
| DTRB | 46 | I/O | UART B Data Terminal Ready. An active low informs the modem or data set that controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as HURAS0. It is used for setting the I/O address of UART A. (See Table 1-2.) |
| HURAS0 | | | |

Serial Port Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|-------------------------------------|-----|-----|---|
| $\overline{\text{RTSA}}$ HPRTAS1 | 36 | I/O | <p>UART A Request To Send. An active low informs the modem or data set that the controller is ready to send data.</p> <p>During power-on reset, this pin is pulled up internally and is defined as HPRTAS1. It is used for setting the address of the parallel port. (See Table 1-3.)</p> |
| $\overline{\text{RTSB}}$ HURBS0 | 45 | I/O | <p>UART B Request To Send. An active low informs the modem or data set that the controller is ready to send data.</p> <p>During power-on reset, this pin is pulled down internally and is defined as HURBS0. It is used for setting the I/O address of UART B. (See Table 1-2.)</p> |

1.3 Game Port/Power Down Interface

Bit 4 of CR3 (GMODS0) determines whether the game port is in Adapter mode or Portable mode (default is Adapter mode).

Game I/O port address is 201h.

| SYMBOL | PIN | I/O | FUNCTION |
|--|-----|-------------|--|
| $\overline{\text{GMRD}}$ PFDCEN HEFERE | 41 | O O I | <p>Adapter mode: Game port read control signal.</p> <p>Portable mode: When parallel port is selected as Extension FDD/Extension 2FDD mode, this pin will be active. The active state is dependent on bit 7 of CRA (PFDCACT), and default is low active.</p> <p>During power-on reset, this pin is pulled up internally and is defined as HEFERE for determining whether Extended Function Enable Register enable value is 88h or 89h. If the HEFERE= H (default) at power-on reset, then EFER enable value is 89h. If HEFERE = L at power-on reset, the enable value is 88h.</p> |
| $\overline{\text{GMWR}}$ PEXTEN HPRTM0 | 39 | O O I | <p>Adapter mode: Game port write control signal.</p> <p>Portable mode: When a particular extended mode is selected for the parallel port, this pin will be active. The extended modes include Extension Adapter mode, EPP mode, ECP mode, and ECP/EPP mode, which are selected using bit 3 - bit 0 of CRA. The active state is dependent on bit 6 of CRA (PEXTACT); the default is low active.</p> <p>During power-on reset, this pin is pulled down internally and is defined as HPRTM0. It is used to determine the mode of the parallel port. (See Table 1-1.)</p> |

Game Port/Power Down Interface, continued

| | | | |
|----------------|---|------------|---|
| PDCIN IRRX2 | 3 | I I | <p>This input pin controls the chip power down. When this pin is active, the clock supply to the chip will be inhibited and the output pins will be tri-stated as defined in CR4 and CR6. The PDCIN is pulled down internally. Its active state is defined by bit 4 of CRA (PDCHACT). Default is high active.</p> <p>PDCIN can be programmed by CR0D register as input pin IRRX2 for serial infrared communication.</p> |
|----------------|---|------------|---|

1.4 Multi-Mode Parallel Port

The following pins have eight functions, which are controlled by bits PRTMOD0, PRTMOD1, and PRTMOD2 of CR0 and CR9 (refer to section 6.0, Extended Functions).

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|--|
| BUSY | 24 | I | <p>PRINTER MODE: BUSY</p> <p>An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> |
| | | OD | <p>EXTENSION FDD MODE: $\overline{MOB2}$</p> <p>This pin is for Extension FDD B; the function of this pin is the same as that of the \overline{MOB} pin.</p> |
| | | I | <p>EXTENSION ADAPTER MODE: XIRQ</p> <p>This pin is an interrupt request generated by the Extension Adapter and is an active high input.</p> |
| | | OD | <p>EXTENSION 2FDD MODE: $\overline{MOB2}$</p> <p>This pin is for Extension FDD A and B; the function of this pin is the same as that of the \overline{MOB} pin.</p> |
| | | - | <p>JOYSTICK MODE: NC pin.</p> |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|---|---|
| ACK | 26 | I OD I OD - | <p>PRINTER MODE: $\overline{\text{ACK}}$</p> <p>An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: $\overline{\text{DSB2}}$</p> <p>This pin is for the Extension FDD B; its functions are the same as those of the $\overline{\text{DSB}}$ pin.</p> <p>EXTENSION ADAPTER MODE: XDRQ</p> <p>DMA request generated by the Extension Adapter. An active high input.</p> <p>EXTENSION 2FDD MODE: $\overline{\text{DSB2}}$</p> <p>This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{\text{DSB}}$ pin.</p> <p>JOYSTICK MODE: NC pin.</p> |
| PE | 27 | I OD O OD - | <p>PRINTER MODE: PE</p> <p>An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.</p> <p>Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: $\overline{\text{WD2}}$</p> <p>This pin is for Extension FDD B; its function is the same as that of the $\overline{\text{WD}}$ pin.</p> <p>EXTENSION ADAPTER MODE: XA0</p> <p>This pin is system address A0 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: $\overline{\text{WD2}}$</p> <p>This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{\text{WD}}$ pin.</p> <p>JOYSTICK MODE: NC pin.</p> |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|---|--|
| SLCT | 28 | I OD O OD - | <p>PRINTER MODE: SLCT An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: WE2 This pin is for Extension FDD B; its functions are the same as those of the WE pin.</p> <p>EXTENSION ADAPTER MODE: XA1 This pin is system address A1 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: WE2 This pin is for Extension FDD A and B; this function of this pin is the same as that of the WE pin.</p> <p>JOYSTICK MODE: NC pin.</p> |
| ERR | 29 | I OD O OD - | <p>PRINTER MODE: ERR An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: HEAD2 This pin is for Extension FDD B; its function is the same as that of the HEAD pin.</p> <p>EXTENSION ADAPTER MODE: XA2 This pin is system address A2 for the Extension Adapter.</p> <p>EXTENSION 2FDD MODE: HEAD2 This pin is for Extension FDD A and B; its function is the same as that of the HEAD pin.</p> <p>JOYSTICK MODE: NC pin.</p> |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------------------------|-----|--------------------------------------|--|
| SLIN | 22 | OD OD O OD O | <p>PRINTER MODE: $\overline{\text{SLIN}}$ Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: $\overline{\text{STEP2}}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{\text{STEP}}$ pin.</p> <p>EXTENSION ADAPTER MODE: XTC This pin is the DMA terminal count for the Extension Adapter. The count is sent by TC directly.</p> <p>EXTENSION 2FDD MODE: $\overline{\text{STEP2}}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{\text{STEP}}$ pin .</p> <p>JOYSTICK MODE: VDD for joystick.</p> |
| $\overline{\text{INIT}}$ | 21 | OD OD O OD O | <p>PRINTER MODE: $\overline{\text{INIT}}$ Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: $\overline{\text{DIR2}}$ This pin is for Extension FDD B; its function is the same as that of the $\overline{\text{DIR}}$ pin.</p> <p>EXTENSION ADAPTER MODE: $\overline{\text{XDACK}}$ This pin is the DMA acknowledge output for the Extension Adapter; the output is sent directly from $\overline{\text{PDACKX}}$.</p> <p>EXTENSION 2FDD MODE: $\overline{\text{DIR2}}$ This pin is for Extension FDD A and B; its function is the same as that of the $\overline{\text{DIR}}$ pin.</p> <p>JOYSTICK MODE: VDD for joystick.</p> |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|-------------------------|-----|--|--|
| AFD | 20 | OD OD O OD O | <p>PRINTER MODE: $\overline{\text{AFD}}$</p> <p>An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: $\overline{\text{RWC2}}$</p> <p>This pin is for Extension FDD B; its function is the same as that of the $\overline{\text{RWC}}$ pin.</p> <p>EXTENSION ADAPTER MODE: $\overline{\text{XRD}}$</p> <p>This pin is the I/O read command for the Extension Adapter. When the Extension Adapter base address is written to the Extension Adapter address register, $\overline{\text{XRD}}$ and $\overline{\text{XWR}}$ go low simultaneously so that the command register on the Extension Adapter can latch the same base address.</p> <p>EXTENSION 2FDD MODE: $\overline{\text{RWC2}}$</p> <p>This pin is for Extension FDD A and B; its function is the same as that of the $\overline{\text{RWC}}$ pin.</p> <p>JOYSTICK MODE: V_{DD} for joystick.</p> |
| $\overline{\text{STB}}$ | 19 | OD - O - O | <p>PRINTER MODE: $\overline{\text{STB}}$</p> <p>An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>EXTENSION FDD MODE: This pin is a tri-state output.</p> <p>EXTENSION ADAPTER MODE: $\overline{\text{XWR}}$</p> <p>This pin is the I/O write command for the Extension Adapter. When the Extension Adapter base address is written to the Extension Adapter address register, $\overline{\text{XRD}}$ and $\overline{\text{XWR}}$ go low simultaneously so that the command register on the Extension Adapter can latch the same base address.</p> <p>EXTENSION 2FDD MODE: This pin is a tri-state output.</p> <p>JOYSTICK MODE: V_{DD} for joystick.</p> |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|---|
| PD0 | 9 | I/O | PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | I | EXTENSION FDD MODE: $\overline{\text{INDEX2}}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{\text{INDEX}}$ pin. This pin is pulled high internally. |
| | | I/O | EXTENSION ADAPTER MODE: XD0 This pin is system data bus D0 for the Extension Adapter. |
| | | I | EXTENSION 2FDD MODE: $\overline{\text{INDEX2}}$ This pin is for Extension FDD A and B; this function of this pin is the same as $\overline{\text{INDEX}}$ pin. This pin is pulled high internally. |
| | | I/O | JOYSTICK MODE: JP0 This pin is the paddle 0 input for joystick. |
| PD1 | 10 | I/O | PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. |
| | | I | EXTENSION FDD MODE: $\overline{\text{TRAK02}}$ This pin is for Extension FDD B; the function of this pin is the same as that of the $\overline{\text{TRAK0}}$ pin. This pin is pulled high internally. |
| | | I/O | EXTENSION ADAPTER MODE: XD1 This pin is system data bus D1 for the Extension Adapter. |
| | | I | EXTENSION. 2FDD MODE: $\overline{\text{TRAK02}}$ This pin is for Extension FDD A and B; this function of this pin is the same as $\overline{\text{TRAK0}}$ pin. This pin is pulled high internally. |
| | | I/O | JOYSTICK MODE: JP1 This pin is the paddle 1 input for joystick. |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|---|
| PD2 | 11 | I/O | <p>PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>I EXTENSION FDD MODE: $\overline{WP2}$ This pin is for Extension FDD B; the function of this pin is the same as that of the \overline{WP} pin. This pin is pulled high internally.</p> <p>I/O EXTENSION ADAPTER MODE: XD2 This pin is system data bus D2 for the Extension Adapter.</p> <p>I EXTENSION. 2FDD MODE: $\overline{WP2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the \overline{WP} pin. This pin is pulled high internally.</p> <p>- JOYSTICK MODE: NC pin</p> |
| PD3 | 12 | I/O | <p>PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>I EXTENSION FDD MODE: $\overline{RDATA2}$ Motor on B for Extension FDD B; the function of this pin is the same as that of the \overline{RDATA} pin. This pin is pulled high internally.</p> <p>I/O EXTENSION ADAPTER MODE: XD3 This pin is system data bus D3 for the Extension Adapter.</p> <p>I EXTENSION 2FDD MODE: $\overline{RDATA2}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the \overline{RDATA} pin. This pin is pulled high internally.</p> <p>- JOYSTICK MODE: NC pin</p> |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|---|
| PD4 | 13 | I/O | <p>PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>I EXTENSION FDD MODE: $\overline{\text{DSKCHG2}}$ Drive select B for Extension FDD B; the function of this pin is the same as that of $\overline{\text{DSKCHG}}$ pin. This pin is pulled high internally.</p> <p>I/O EXTENSION ADAPTER MODE: XD4 This pin is system data bus D4 for the Extension Adapter.</p> <p>I EXTENSION 2FDD MODE: $\overline{\text{DSKCHG2}}$ This pin is for Extension FDD A and B; this function of this pin is the same as that of the $\overline{\text{DSKCHG}}$ pin. This pin is pulled high internally.</p> <p>I JOYSTICK MODE: JB0 This pin is the button 0 input for the joystick.</p> |
| PD5 | 14 | I/O | <p>PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.</p> <p>- EXTENSION FDD MODE: This pin is a tri-state output.</p> <p>I/O EXTENSION ADAPTER MODE: XD5 This pin is system data bus D5 for the Extension Adapter</p> <p>- EXTENSION 2FDD MODE: This pin is a tri-state output.</p> <p>I JOYSTICK MODE: JB1 This pin is the button 1 input for the joystick.</p> |

Multi-Mode Parallel Port, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|--|
| PD6 | 16 | I/O | PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. - EXTENSION FDD MODE: This pin is a tri-state output. I/O EXTENSION ADAPTER MODE: XD6 This pin is system data bus D6 for the Extension Adapter OD EXTENSION. 2FDD MODE: $\overline{MOA2}$ This pin is for Extension FDD A; its function is the same as that of the \overline{MOA} pin. - JOYSTICK MODE: NC pin |
| PD7 | 17 | I/O | PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. - EXTENSION FDD MODE: This pin is a tri-state output. I/O EXTENSION ADAPTER MODE: XD7 This pin is system data bus D7 for the Extension Adapter. OD EXTENSION 2FDD MODE: $\overline{DSA2}$ This pin is for Extension FDD A; its function is the same as that of the \overline{DSA} pin. - JOYSTICK MODE: NC pin |

1.5 IDE and FDC Interface

| SYMBOL | PIN | I/O | FUNCTION |
|------------------------------|-----|------------|---|
| $\overline{IOCS16}$ | 93 | I | 16-bit I/O indication from IDE interface |
| IDED7 GIO1 | 96 | I/O I/O | IDE data bus bit 7 GIO1:General Purpose I/O pin 1.If pin #91 GIOSEL=1,this pin act as GIO1.If GIOSEL=0,this pin act as IDED7.It can also be programmed by CR0C register bit 2. |
| \overline{RESIDE} IRRX3 | 1 | O I | Reset signal for IDE, active low to initialize the IDE \overline{RESIDE} can be programmed by CR0D register as input pin IRRX3 for serial infrared communication. |

IDE and FDC Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--|-----|---------------|---|
| $\overline{\text{DBENL}}$ $\overline{\text{IDBEN}}$ GIOSEL | 91 | O O I | <p>During normal operations, $\overline{\text{DBENL}}$ is used to enable the low byte buffer of the IDE bus. When $\overline{\text{DBENL}}$ is active, it accesses I/O addresses 1F0H - 1F7H (170H-177H) and 3F6-3F7H (376H-377H).</p> <p>$\overline{\text{IDBEN}}$: IDE Data Bus Enable (Low Active). If I/O address 1F0~1F7H and 2F7H is access, the pin will activate.</p> <p>During power on reset, if $\text{GIOSEL}=1$, then this pin act as $\overline{\text{IDBEN}}$. If $\text{GIOSEL}=0$, this pin act as $\overline{\text{DBENL}}$. It can also be programmed by CROC register bit 2.</p> <p>GIOSEL: General Purpose I/O pin select at power on setting. (See Table 1-4)</p> |
| $\overline{\text{DBENH}}$ GIO0 URIRSEL | 92 | O I/O I | <p>During normal operations, $\overline{\text{DBENH}}$ is used to enable the high byte buffer of the IDE bus. $\overline{\text{DBENH}}$ is active only when $\overline{\text{IOCS16}}$ is active. When active, $\overline{\text{DBENH}}$ selects I/O port address range 1F0-1F7H (170H-177H).</p> <p>GIO0: General Purpose I/O pin0. If pin #91 $\text{GIOSEL}=1$, this pin act as GIO0. If $\text{GIOSEL}=0$, this pin act as $\overline{\text{nDBENH}}$. It can also be programmed by CROC register bit 2.</p> <p>URIRSEL: UART/IR Selection. During power on reset, if $\text{URIRSEL}=1$, then UARTB act as UART function. If $\text{URIRSEL}=0$, then UARTB act as IR function.</p> |
| $\overline{\text{PDBDIR}}$ $\overline{\text{FDCEN}}$ IRTX2 | 2 | I/O O | <p>During normal operation, this pin ($\overline{\text{PDBDIR}}$) is an output that indicates the direction of the parallel port data bus. If bit 5 of CRA ($\overline{\text{PDIRHISOP}}$) is low, then $\overline{\text{PDBDIR}} = 0$ means output/write, $\overline{\text{PDBDIR}} = 1$ means input/read (default). During power-on reset, this pin ($\overline{\text{FDCEN}}$) is pulled down internally and is used to enable the FDC. A 4.7K resistor is recommend in order to pullup the pin at power on reset to disable the FDC function.</p> <p>When set to low, it enables the FDC port (default).</p> <p>When set to high, it disables the FDC port.</p> <p>$\overline{\text{PDBDIR}}$ can be programmed by CROD register as output pin IRTX2 for serial infrared communication.</p> |

IDE and FDC Interface, continued

| | | | |
|---|----|--------------|--|
| $\overline{\text{CS1}}$ HADSEL IRTX3 | 95 | I/O O | <p>During normal operations this pin is used to select the IDE controller. $\overline{\text{CS1}}$ decodes the HDC addresses 3F6H and 3F7H (376H, 377H).</p> <p>During power-on reset this pin selects the HDC address and is pulled up internally.</p> <p>When set to high, it selects I/O port address range 1F0H-1F7H (3F6H-3F7H) (default).</p> <p>When set to low, it selects I/O port address ranges 376H-377H and 170H-177H.</p> <p>$\overline{\text{CS1}}$ can be programmed by CR0D register as output pin IRTX3 for serial infrared communication.</p> |
| $\overline{\text{CS0}}$ $\overline{\text{IDEEN}}$ IRRX4 | 94 | O I I | <p>During normal operation this pin is used to select the IDE controller. $\overline{\text{CS0}}$ decodes HDC addresses 1F0H-1F7H (170H-177H).</p> <p>During power-on reset this pin is pulled down internally and used to enable or disable the IDE.</p> <p>When it is set to high, IDE is disabled.</p> <p>When it is set low, IDE is enabled (default).</p> <p>$\overline{\text{CS0}}$ can be programmed by CR0D register as input pin IRRX4 for serial infrared communication.</p> |
| $\overline{\text{WE}}$ | 85 | OD | Write enable. An open drain output. |
| $\overline{\text{DIR}}$ | 89 | OD | Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion |
| $\overline{\text{HEAD}}$ | 88 | OD | Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1 |
| $\overline{\text{RWC}}$ | 87 | OD | Reduced write current. This signal can be used on two-speed disk drives to select the transfer rate. An open drain output. Logic 0 = 250Kbps Logic 1 = 500Kbps When bit 5 of CR9 (EN3MODE) is set to high, the three-mode FDD function is enabled, and the pin will have a different definition. Refer to the EN3MODE bit in CR9. |
| $\overline{\text{WD}}$ | 86 | OD | Write data. This logic low open drain writes precompensation serial data to the selected FDD. An open drain output. |

IDE and FDC Interface, continued

| SYMBOL | PIN | I/O | FUNCTION |
|--------|------------------|-----|--|
| STEP | 82 | OD | Step output pulses. This active low open drain output produces a pulse to move the head to another track. |
| INDEX | 81 | I | This schmitt input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| TRAK0 | 78 | I | Track 0. This schmitt input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| WP | 77 | I | Write protected. This active low schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| RDATA | 74 | I | The read data input signal from the FDD. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| DSKCHG | 76 | I | Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by an approximately 1K ohm resistor. The resistor can be disabled by bit 4 of CR6 (FIPURDWN). |
| MOA | 79 | OD | Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output. |
| MOB | 80 | OD | Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output. |
| DSA | 83 | OD | Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output. |
| DSB | 84 | OD | Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output. |
| VDD | 15, 56 | | +5 power supply for the digital circuitry |
| GND | 25, 40 65, 90 | | Ground |

Table 1-1:

| PARALLEL PORT FUNCTION MODE POWER-ON SETTING | | |
|---|----------------|------------------------|
| PDRQX HPRTM1 | GMWR HPRTM0 | |
| L | L | Printer Mode (Default) |
| L | H | ECP/EPP |
| H | L | EPP |
| H | H | EXT2FDD |

Table 1-2:

| UART A | | | UART B | | |
|-----------------|------------------------------------|----------------------|----------------|------------------------------------|----------------------|
| SOUTA HURAS1 | $\overline{\text{DTRB}}$ HURAS0 | | SOUTB HURBS | $\overline{\text{RTSB}}$ HURBS0 | |
| L | L | COM4 (2E8) | L | L | COM3 (3E8) |
| L | H | COM3 (3E8) | L | H | COM4 (2E8) |
| H | L | COM1 (3F8) (Default) | H | L | COM2 (2F8) (Default) |
| H | H | Disabled | H | H | Disabled |

Table 1-3 :

| PARALLEL PORT | | |
|------------------------------------|------------------------------------|----------------------|
| $\overline{\text{RTSA}}$ HPRTS1 | $\overline{\text{DTRA}}$ HPRTS0 | |
| L | L | LPT3 (3BC) |
| L | H | LPT2 (278) |
| H | L | LPT1 (378) (Default) |
| H | H | Disabled |

Note: When the parallel port is disabled, the eight function modes (W83757 mode, EXTFDD mode, EXTADP mode, EXT2FDD mode, JOYSTICK mode, EPP mode, ECP mode, and ECP/EPP mode) are all inhibited.

Table 1-4 :

| PIN | W83787F/777F | W83787IF |
|-----|----------------|---------------------------------------|
| 1 | nRESIDE | nRESIDE/ IRRX3 |
| 2 | PBDBDIR/nFDCEN | PBDBDIR/ IRTX2 /nFDCEN |
| 3 | PDCIN | PDCIN/ IRRX2 |
| 42 | SINB | SINB/ IRRX1 |
| 43 | SOUTB/HURBS1 | SOUTB/ IRTX1 /HURBS1 |
| 91 | nDBENL/ABCHG | nDBENL/n IDBEN / GIOSEL |
| 92 | nDBENH/FADSEL | nDBENH/ GIO0 / URIRSEL |
| 93 | nIOCS16 | nIOCS16 |
| 94 | nCS0/nIDEEN | nCS0/ IRRX4 /nIDEEN |
| 95 | nCS1/HADSEL | nCS1/ IRTX3 /HADSEL |
| 96 | IDED7 | IDED7/ GIO1 |

2.0 FDC FUNCTIONAL DESCRIPTION

2.1 W83787IF FDC

The floppy disk controller of the W83787IF integrates all of the logic required for floppy disk control. The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, and FDC Core.

2.1.1 AT interface

The interface consists of the standard asynchronous signals: /RD, /WR, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers.

2.1.2 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

2.1.3 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

2.1.4 FDC Core

The W83787IF FDC is capable of performing sixteen commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

2.1.5 FDC Commands

Command Symbol Descriptions:

| | |
|----------|---|
| C: | Cylinder number 0 - 256 |
| D: | Data Pattern |
| DIR: | Step Direction DIR = 0, step out DIR = 1, step in |
| DS0: | Disk Drive Select 0 |
| DS1: | Disk Drive Select 1 |
| DTL: | Data Length |
| EC: | Enable Count |
| EOT: | End of Track |
| EFIFO: | Enable FIFO |
| EIS: | Enable Implied Seek |
| EOT: | End of track |
| FIFOTHR: | FIFO Threshold |
| GAP: | Gap length selection |
| GPL: | Gap Length |
| H: | Head number |
| HDS: | Head number select |
| HLT: | Head Load Time |
| HUT: | Head Unload Time |
| LOCK: | Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset |
| MFM: | MFM or FM Mode |
| MT: | Multitrack |
| N: | The number of data bytes written in a sector |
| NCN: | New Cylinder Number |
| ND: | Non-DMA Mode |
| OW: | Overwritten |
| PCN: | Present Cylinder Number |
| POLL: | Polling Disable |
| PRETRK: | Precompensation Start Track Number |
| R: | Record |
| RCN: | Relative Cylinder Number |
| R/W: | Read/Write |
| SC: | Sector/per cylinder |
| SK: | Skip deleted data address mark |
| SRT: | Step Rate Time |
| ST0: | Status Register 0 |
| ST1: | Status Register 1 |
| ST2: | Status Register 2 |
| ST3: | Status Register 3 |
| WG: | Write gate alters timing of WE |

(1) Read Data

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|--|
| Command | W | MT | MFM | SK | 0 | 0 | 1 | 1 | 0 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | Sector ID information prior to command execution |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| | W | ----- DTL ----- | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | Sector ID information after command execution |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(2) Read Deleted Data

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|--|
| Command | W | MT | MFM | SK | 0 | 1 | 1 | 0 | 0 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | Sector ID information prior to command execution |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| | W | ----- DTL ----- | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |

Read Deleted Data,Continued

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS | |
|--------|-----|-----------------|----|----|----|----|----|----|----|--|---|
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution | |
| | R | ----- ST1 ----- | | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | | |
| | R | ----- C ----- | | | | | | | | | Sector ID information after command execution |
| | R | ----- H ----- | | | | | | | | | |
| | R | ----- R ----- | | | | | | | | | |
| | R | ----- N ----- | | | | | | | | | |

(3) Read A Track

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS | |
|-----------|-----------------|-----------------|-----|----|----|----|-----|-----|-----|--|--|
| Command | W | 0 | MFM | 0 | 0 | 0 | 0 | 1 | 0 | Command codes | |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | | |
| | W | ----- C ----- | | | | | | | | | Sector ID information prior to command execution |
| | W | ----- H ----- | | | | | | | | | |
| | W | ----- R ----- | | | | | | | | | |
| | W | ----- N ----- | | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | | |
| W | ----- DTL ----- | | | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT | |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution | |
| | R | ----- ST1 ----- | | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | | |
| | R | ----- C ----- | | | | | | | | | Sector ID information after command execution |
| | R | ----- H ----- | | | | | | | | | |
| | R | ----- R ----- | | | | | | | | | |
| | R | ----- N ----- | | | | | | | | | |

(4) Read ID

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|--|
| Command | W | 0 | MFM | 0 | 0 | 1 | 0 | 1 | 0 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| Execution | | | | | | | | | | The first correct ID information on the cylinder is stored in Data Register |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution Disk status after the command has been completed |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(5) Write Data

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|---|
| Command | W | MT | MFM | 0 | 0 | 0 | 1 | 0 | 1 | Command codes Sector ID information prior to Command execution |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| | W | ----- DTL ----- | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after Command execution Sector ID information after Command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(6) Write Deleted Data

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS | |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|---|--|
| Command | W | MT | MFM | 0 | 0 | 1 | 0 | 0 | 1 | Command codes | |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | | |
| | W | ----- C ----- | | | | | | | | | Sector ID information prior to command execution |
| | W | ----- H ----- | | | | | | | | | |
| | W | ----- R ----- | | | | | | | | | |
| | W | ----- N ----- | | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | | |
| | W | ----- DTL ----- | | | | | | | | | |
| Execution | | | | | | | | | | Data transfer between the FDD and system | |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution | |
| | R | ----- ST1 ----- | | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | | |
| | R | ----- C ----- | | | | | | | | Sector ID information after command execution | |
| | R | ----- H ----- | | | | | | | | | |
| | R | ----- R ----- | | | | | | | | | |
| | R | ----- N ----- | | | | | | | | | |

(7) Format A Track

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS | |
|-----------------------------------|-----|-----------------------|-----|----|----|----|-----|-----|-----|--|------------------|
| Command | W | 0 | MFM | 0 | 0 | 1 | 1 | 0 | 1 | Command codes | |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | | |
| | W | ----- N ----- | | | | | | | | | Bytes/Sector |
| | W | ----- SC ----- | | | | | | | | | Sectors/Cylinder |
| | W | ----- GPL ----- | | | | | | | | | Gap 3 |
| | W | ----- D ----- | | | | | | | | | Filler Byte |
| Execution for Each Sector Repeat: | W | ----- C ----- | | | | | | | | Input Sector Parameters | |
| | W | ----- H ----- | | | | | | | | | |
| | W | ----- R ----- | | | | | | | | | |
| | W | ----- N ----- | | | | | | | | | |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution | |
| | R | ----- ST1 ----- | | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | | |
| | R | ----- Undefined ----- | | | | | | | | | |
| | R | ----- Undefined ----- | | | | | | | | | |
| | R | ----- Undefined ----- | | | | | | | | | |
| | R | ----- Undefined ----- | | | | | | | | | |

(8) Recalibrate

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|----|----|----|----|----|----|-----|-----|-------------------------------------|
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | 0 | DS1 | DS0 | |
| Execution | | | | | | | | | | Head retracted to Track 0 Interrupt |

(9) Sense Interrupt Status

| PHASE | R/W | D7 | 76 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|-----------------|----|----|----|----|----|----|----|--|
| Command | W | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Command code |
| Result | R | ----- ST0 ----- | | | | | | | | Status information at the end of each seek operation |
| | R | ----- PCN ----- | | | | | | | | |

(10) Specify

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|-------------------|----|----|----|---------------|----|----|----|---------------|
| Command | W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Command codes |
| | W | -----SRT----- | | | | -----HUT----- | | | | |
| | W | -----HLT----- ND | | | | | | | | |

(11) Seek

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|---------------|----|----|----|----|-----|-----|-----|--|
| Command | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | -----NCN----- | | | | | | | | |
| Execution | R | | | | | | | | | Head positioned over proper cylinder on diskette |

(12) Sense Drive Status

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|---------------|----|----|----|----|-----|-----|-----|-------------------------------------|
| Command | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | Command Code |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| Result | R | -----ST3----- | | | | | | | | Status information about disk drive |

(13) Invalid

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|---------|-----|---------------------------|----|----|----|----|----|----|----|--|
| Command | W | ----- Invalid Codes ----- | | | | | | | | Invalid codes (no operation - FDC goes into standby state) |
| Result | R | -----ST0----- | | | | | | | | ST0 = 80H |

(14) Scan Equal

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|---|
| Command | W | MT | MFM | SK | 1 | 0 | 0 | 0 | 1 | Command codes Sector ID information prior to command execution |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| | W | ----- DTL ----- | | | | | | | | |
| Execution | | | | | | | | | | Data compare between the FDD and system |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution Sector ID information after command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(15) Scan Low or Equal

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|---|
| Command | W | MT | MFM | SK | 1 | 1 | 0 | 0 | 1 | Command codes Sector ID information prior to command execution |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | |
| | W | ----- C ----- | | | | | | | | |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| | W | ----- DTL ----- | | | | | | | | |
| Execution | | | | | | | | | | Data compare between the FDD and system |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution Sector ID information after command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

(16) Scan High or Equal

| PHASE | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | REMARKS |
|-----------|-----|-----------------|-----|----|----|----|-----|-----|-----|--|
| Command | W | MT | MFM | SK | 1 | 1 | 1 | 0 | 1 | Command codes |
| | W | 0 | 0 | 0 | 0 | 0 | HDS | DS1 | DS0 | Sector ID information prior to command execution |
| | W | ----- C ----- | | | | | | | | |
| | W | ----- H ----- | | | | | | | | |
| | W | ----- R ----- | | | | | | | | |
| | W | ----- N ----- | | | | | | | | |
| | W | ----- EOT ----- | | | | | | | | |
| | W | ----- GPL ----- | | | | | | | | |
| | W | ----- DTL ----- | | | | | | | | |
| Execution | | | | | | | | | | Data compare between the FDD and system |
| Result | R | ----- ST0 ----- | | | | | | | | Status information after command execution |
| | R | ----- ST1 ----- | | | | | | | | |
| | R | ----- ST2 ----- | | | | | | | | |
| | R | ----- C ----- | | | | | | | | Sector ID information after command execution |
| | R | ----- H ----- | | | | | | | | |
| | R | ----- R ----- | | | | | | | | |
| | R | ----- N ----- | | | | | | | | |

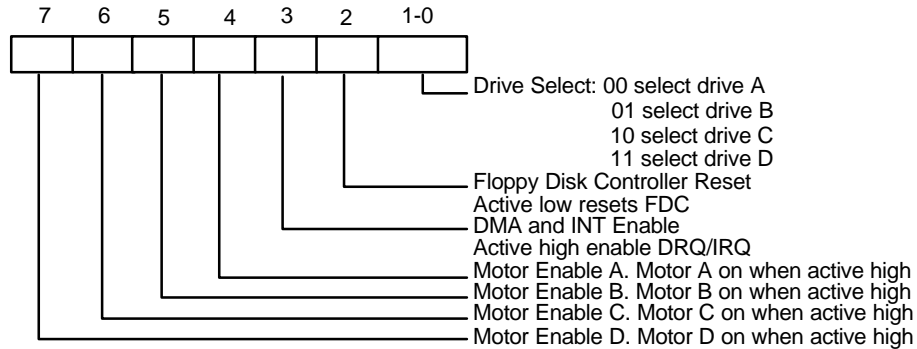
2.3 Register Descriptions

There are status, data, and control registers in the W83787IF. The addresses of these registers are defined below:

| ADDRESS | | REGISTER | |
|---------|-----------|-------------|-------------|
| PRIMARY | SECONDARY | READ | WRITE |
| 3F2 | 372 | | DO REGISTER |
| 3F3 | 373 | | TD REGISTER |
| 3F4 | 374 | MS REGISTER | Reserved |
| 3F5 | 375 | DT REGISTER | DT REGISTER |
| 3F7 | 377 | DI REGISTER | CC REGISTER |

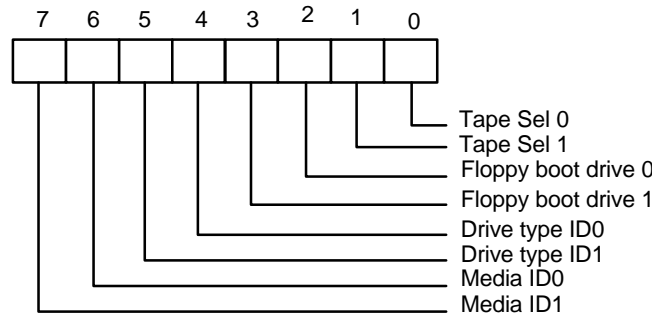
2.3.1 Digital Output Register (DO Register) (Write 3F2H/372H)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:



2.3.2 Tape Drive Register (TD Register) (Read 3F3H/373H)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy disk drive. If three mode FDD function is enabled (EN3MODE = 1 in CR9), the bit definitions are as follows (W83787IF):



Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of CR8 bit 3, 2.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of CR7. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of CR8 bit 1, 0.

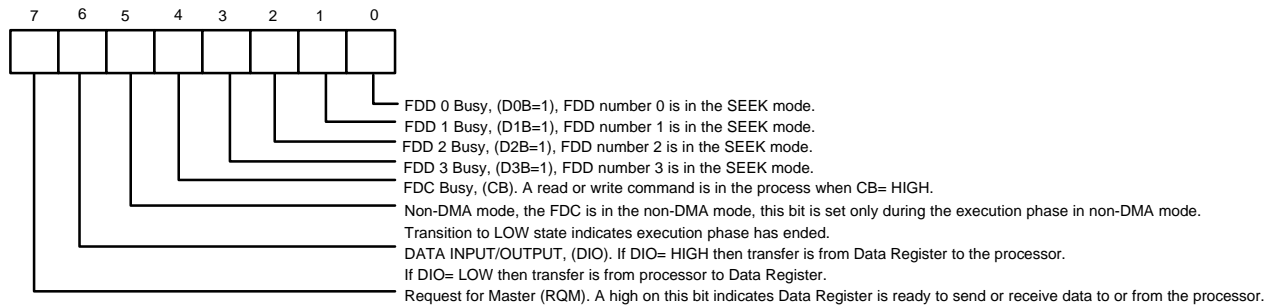
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

| TAPE SEL 1 | TAPE SEL 0 | DRIVE SELECTED |
|------------|------------|----------------|
| 0 | 0 | None |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

2.3.3 Main Status Register (MS Register) (Read 3F4H/374H)

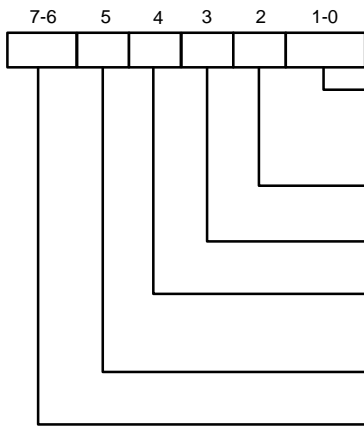
The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



2.3.4 DATA Register (DT Register) (R/W 3F5H/375H)

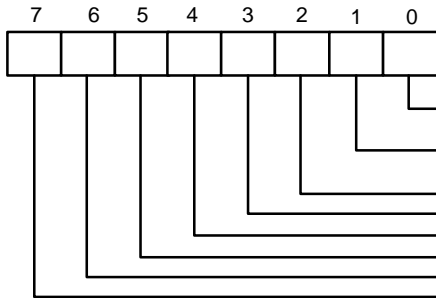
The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command.

Status Register 0 (ST0)



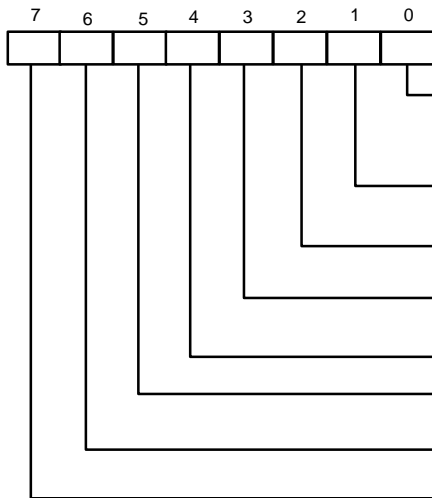
- US1, US0 Drive Select:**
 - 00 Drive A selected
 - 01 Drive B selected
 - 10 Drive C selected
 - 11 Drive D selected
- HD Head address:**
 - 1 Head selected
 - 0 Head selected
- NR Not Ready:**
 - 1 Drive is not ready
 - 0 Drive is ready
- EC Equipment Check:**
 - 1 When a fault signal is received from the FDD or the track signal fails to occur after 77 step pulses
 - 0 No error
- SE Seek end:**
 - 1 seek end
 - 0 seek error
- IC Interrupt Code:**
 - 00 Normal termination of command
 - 01 Abnormal termination of command
 - 10 Invalid command issue
 - 11 Abnormal termination because the ready signal from FDD changed state during command execution

Status Register 1 (ST1)



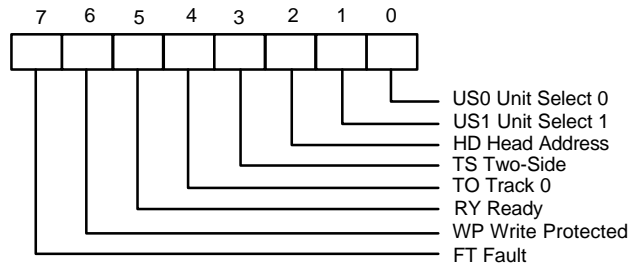
- Missing Address Mark. 1 When the FDC cannot detect the data address mark or the data address mark has been deleted.
- NW (Not Writable). 1 If a write Protect signal is detected from the diskette drive during execution of write data.
- ND (No DATA). 1 If specified sector cannot be found during execution of a read, write or verify data.
- Not used. This bit is always 0.
- OR (Over Run). 1 If the FDC is not serviced by the host system within a certain time interval during data transfer.
- DE (data Error). 1 When the FDC detects a CRC error in either the ID field or the data field.
- Not used. This bit is always 0.
- EN (End of track). 1 When the FDC tries to access a sector beyond the final sector of a cylinder.

Status Register 2 (ST2)



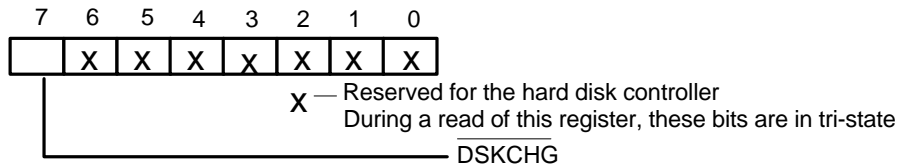
- MD (Missing Address Mark in Data Field). 1 If the FDC cannot find a data address mark (or the address mark has been deleted) when reading data from the media
- 0 No error
- BC (Bad Cylinder) 1 Bad Cylinder
- 0 No error
- SN (Scan Not satisfied) 1 During execution of the Scan command
- 0 No error
- SH (Scan Equal Hit) 1 During execution of the Scan command, if the equal condition is satisfied
- 0 No error
- WC (Wrong Cylinder) 1 Indicates wrong Cylinder
- DD (Data error in the Data field) 1 If the FDC detects a CRC error in the data field
- 0 No error
- CM (Control Mark) 1 During execution of the read data or scan command
- 0 No error
- Not used. This bit is always 0

Status Register 3 (ST3)



2.3.5 Digital Input Register (DI Register) (Read 3F7H/377H)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of DSKCHG, while other bits of the data bus remain in tri-state. Bit definitions are as follows:



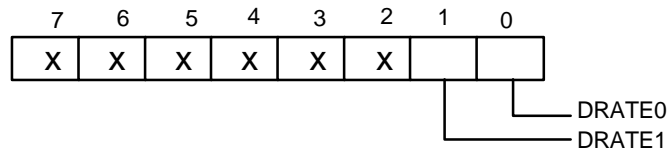
DSKCHG (Bit 7):

This bit indicates the complement of the $\overline{\text{DSKCHG}}$ input.

Bit 6-3: These bits are always a logic 1 during a read.

2.3.6 Configuration Control Register (CC Register) (Write 3F7H/377H)

This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:



X: Reserved

Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

3.0 IDE

The IDE interface is essentially the AT bus ported to the hard disk drive. The hard disk controller resides on the IDE hard disk drive. So the IDE interface provides only chip select signals and AT bus signals between the IDE hard disk drive and ISA slot. Table 3-1 shows the IDE registers and their ISA addresses.

Table 3-1

| I/O ADDRESS | | REGISTERS | |
|-------------|-----------|------------------|--------------------|
| PRIMARY | SECONDARY | READ | WRITE |
| 1F0 | 170 | Data Register | Data Register |
| 1F1 | 171 | Error Register | Write-Precomp |
| 1F2 | 172 | Sector Count | Sector Count |
| 1F3 | 173 | Sector Number | Sector Number |
| 1F4 | 174 | Cylinder LOW | Cylinder LOW |
| 1F5 | 175 | Cylinder HIGH | Cylinder HIGH |
| 1F6 | 176 | SDH Register | SDH Register |
| 1F7 | 177 | Status Register | Command Register |
| 3F6 | 376 | Alternate Status | Fixed Disk Control |
| 3F7 | 377 | Digital Input | Undefined |

3.1 IDE Decode Description

When the processor selects Ports 1F0-1F7 (or 170-177), the chip system enables $\overline{CS0} = \text{LOW}$; otherwise, $\overline{CS0} = \text{HIGH}$. When the processor selects Ports 3F6-3F7 (or 376-377), the chip system enables $\overline{CS1} = \text{LOW}$; otherwise, $\overline{CS1} = \text{HIGH}$.

4.0 UART PORT

4.1 Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65536 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode.

4.2 Register Address

TABLE 4 - 2 UART Register Bit Map

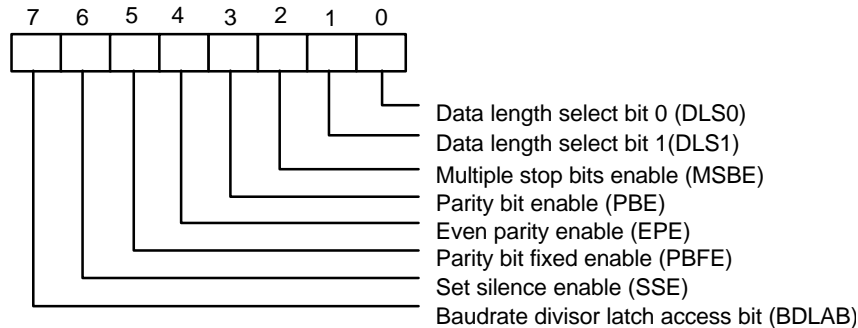
| | | Bit Number | | | | | | | | |
|-----------------------|--|------------|---|-------------------------------------|----------------------------------|------------------------------|----------------------------|--------------------------------|---------------------------------|---|
| Register Address Base | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 8 BDLAB = 0 | Receiver Buffer Register (Read Only) | RBR | RX Data Bit 0 | RX Data Bit 1 | RX Data Bit 2 | RX Data Bit 3 | RX Data Bit 4 | RX Data Bit 5 | RX Data Bit 6 | RX Data Bit 7 |
| 8 BDLAB = 0 | Transmitter Buffer Register (Write Only) | TBR | TX Data Bit 0 | TX Data Bit 1 | TX Data Bit 2 | TX Data Bit 3 | TX Data Bit 4 | TX Data Bit 5 | TX Data Bit 6 | TX Data Bit 7 |
| 9 BDLAB = 0 | Interrupt Control Register | ICR | RBR Data Ready Interrupt Enable (ERDRI) | TBR Empty Interrupt Enable (ETBREI) | USR Interrupt Enable (EUSRI) | HSR Interrupt Enable (EHSRI) | 0 | 0 | 0 | 0 |
| A | Interrupt Status Register (Read Only) | ISR | "0" if Interrupt Pending | Interrupt Status Bit (0) | Interrupt Status Bit (1) | Interrupt Status Bit (2)** | 0 | 0 | FIFOs Enabled ** | FIFOs Enabled ** |
| A | UART FIFO Control Register (Write Only) | UFR | FIFO Enable | RCVR FIFO Reset | XMIT FIFO Reset | DMA Mode Select | Reserved | Reversed | RX Interrupt Active Level (LSB) | RX Interrupt Active Level (MSB) |
| B | UART Control Register | UCR | Data Length Select Bit 0 (DLS0) | Data Length Select Bit 1 (DLS1) | Multiple Stop Bits Enable (MSBE) | Parity Bit Enable (PBE) | Even Parity Enable (EPE) | Parity Bit Fixed Enable (PBFE) | Set Silence Enable (SSE) | Baudrate Divisor Latch Access Bit (BDLAB) |
| C | Handshake Control Register | HCR | Data Terminal Ready (DTR) | Request to Send (RTS) | Loopback RI Input | IRQ Enable | Internal Loopback Enable | 0 | 0 | 0 |
| D | UART Status Register | USR | RBR Data Ready (RDR) | Overrun Error (OER) | Parity Bit Error (PBER) | No Stop Bit Error (NSER) | Silent Byte Detected (SBD) | TBR Empty (TBRE) | TSR Empty (TSRE) | RX FIFO Error Indication (RFEI) ** |
| E | Handshake Status Register | HSR | CTS Toggling (TCTS) | DSR Toggling (TDSR) | RI Falling Edge (FERI) | DCD Toggling (TDCCD) | Clear to Send (CTS) | Data Set Ready (DSR) | Ring Indicator (RI) | Data Carrier Detect (DCD) |
| F | User Defined Register | UDR | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
| 8 BDLAB = 1 | Baudrate Divisor Latch Low | BLL | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 |
| 9 BDLAB = 1 | Baudrate Divisor Latch High | BHL | Bit 8 | Bit 9 | Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 | Bit 15 |

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

** : These bits are always 0 in 16450 Mode.

4.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register controls and defines the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.



Notes:

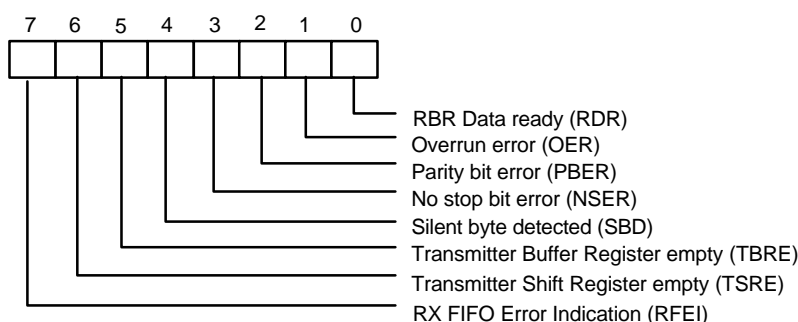
- Bit 7: BDLAB. When this bit is set to a logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baudrate generator during a read or write operation. When this bit is reset, the Receiver Buffer Register, the Transmitter Buffer Register, or the Interrupt Control Register can be accessed.
- Bit 6: SSE. A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only SOUT is affected by this bit; the transmitter is not affected.
- Bit 5: PBFE. When PBE and PBFE of UCR are both set to a logical 1,
 - (1) if EPE is a logical 1, the parity bit is fixed as a logical 0 to transmit and check.
 - (2) if EPE is a logical 0, the parity bit is fixed as a logical 1 to transmit and check.
- Bit 4: EPE. This bit describes the number of logic 1's in the data word bits and parity bit only when bit 3 is programmed. When this bit is set, an even number of logic 1's are sent or checked. When the bit is reset, an odd number of logic 1's are sent or checked.
- Bit 3: PBE. When this bit is set, the position between the last data bit and the stop bit of the SOUT will be stuffed with the parity bit at the transmitter. For the receiver, the parity bit in the same position as the transmitter will be detected.
- Bit 2: MSBE. This bit defines the number of stop bits in each serial character that is transmitted or received.
 - (1) If MSBE is set to a logical 0, one stop bit is sent and checked.
 - (2) If MSBE is set to a logical 1, and data length is 5 bits, one and a half stop bits are sent and checked.
 - (3) If MSBE is set to a logical 1, and data length is 6, 7, or 8 bits, two stop bits are sent and checked.
- Bits 0 and 1: DLS0, DLS1. These two bits define the number of data bits that are sent or checked in each serial character.

TABLE 4 - 3 WORD LENGTH DEFINITION

| DLS1 | DLS0 | DATA LENGTH |
|------|------|-------------|
| 0 | 0 | 5 bits |
| 0 | 1 | 6 bits |
| 1 | 0 | 7 bits |
| 1 | 1 | 8 bits |

4.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of the data transfer during communication.



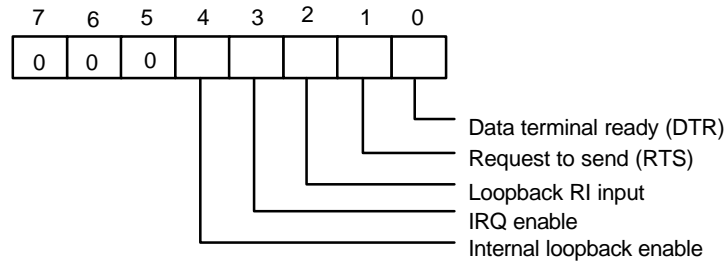
Notes:

- Bit 7: RFEI. In 16450 mode, this bit is always set to a logic 0. In 16550 mode, this bit is set to a logic 1 when there is at least one parity bit error, no stop bit error or silent byte detected in the FIFO. In 16550 mode, this bit is cleared by reading from the USR if there are no remaining errors left in the FIFO.
- Bit 6: TSRE. In 16450 mode, when TBR and TSR are both empty, this bit will be set to a logical 1. In 16550 mode, if the transmit FIFO and TSR are both empty, it will be set to a logical 1. Other than these two cases, this bit will be reset to a logical 0.
- Bit 5: TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit will be set to a logical 1. If ETREI or ICR is a logical 1, an interrupt will be generated to notify the CPU to write the next data. In 16550 mode, this bit will be set to a logical 1 when the transmit FIFO is empty. It will be reset to a logical 0 when the CPU writes data into TBR or FIFO.
- Bit 4: SBD. This bit is set to a logical 1 to indicate that received data are kept in silent state for a full word time, including start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.
- Bit 3: NSER. This bit is set to a logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.
- Bit 2: PBER. This bit is set to a logical 1 to indicate that the parity bit of received data is wrong. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.
- Bit 1: OER. This bit is set to a logical 1 to indicate received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition instead of FIFO full. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 0: RDR. This bit is set to a logical 1 to indicate received data are ready to be read by the CPU in the RBR or FIFO. After no data are left in the RBR or FIFO, the bit will be reset to a logical 0.

4.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls the pins of the UART used for handshaking peripherals such as modem, and controls the diagnostic mode of the UART.



Notes:

Bit 4: When this bit is set to a logical 1, the UART enters diagnostic mode by an internal loopback, as follows:

- (1) SOUT is forced to a logical 1, and SIN is isolated from the communication link instead of the TSR.
- (2) Modem output pins are set to their inactive state.
- (3) Modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) → $\overline{\text{DSR}}$, RTS (bit 1 of HCR) → $\overline{\text{CTS}}$, Loopback RI input (bit 2 of HCR) → $\overline{\text{RI}}$ and IRQ enable (bit 3 of HCR) → $\overline{\text{DCD}}$.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

Bit 3: The UART interrupt output is enabled by setting this bit to a logic 1. In the diagnostic mode this bit is internally connected to the modem control input DCD.

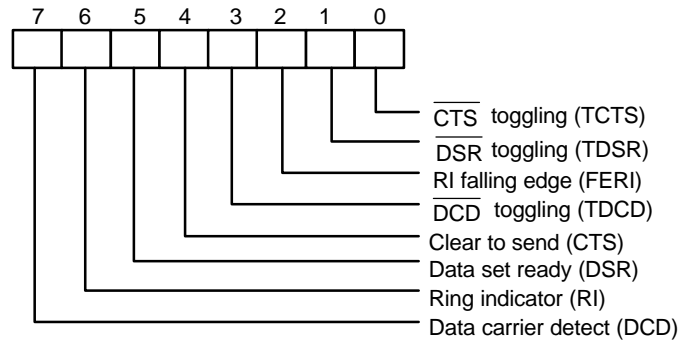
Bit 2: This bit is used only in the diagnostic mode. In the diagnostic mode this bit is internally connected to the modem control input RI.

Bit 1: This bit controls the $\overline{\text{RTS}}$ output. The value of this bit is inverted and output to $\overline{\text{RTS}}$.

Bit 0: This bit controls the $\overline{\text{DTR}}$ output. The value of this bit is inverted and output to $\overline{\text{DTR}}$.

4.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins for handshake peripherals such as a modem and records changes on these pins.



Notes:

Bit 7: This bit is the opposite of the $\overline{\text{DCD}}$ input. This bit is equivalent to bit 3 of HCR in loopback mode.

Bit 6: This bit is the opposite of the $\overline{\text{RI}}$ input. This bit is equivalent to bit 2 of HCR in loopback mode.

Bit 5: This bit is the opposite of the $\overline{\text{DSR}}$ input. This bit is equivalent to bit 0 of HCR in loopback mode.

Bit 4: This bit is the opposite of the $\overline{\text{CTS}}$ input. This bit is equivalent to bit 1 of HCR in loopback mode.

Bit 3: TDCD. This bit indicates that the $\overline{\text{DCD}}$ pin has changed state after HSR was read by the CPU.

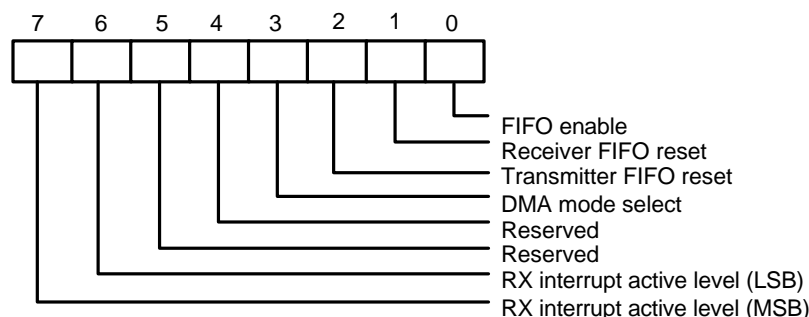
Bit 2: FERI. This bit indicates that the $\overline{\text{RI}}$ pin has changed from low to high state after HSR was read by the CPU.

Bit 1: TDSR. This bit indicates that the $\overline{\text{DSR}}$ pin has changed state after HSR was read by the CPU.

Bit 0: TCTS. This bit indicates that the $\overline{\text{CTS}}$ pin has changed state after HSR was read by the CPU.

4.2.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.



Notes: Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify the CPU to read the data from the FIFO.

TABLE 4-4 FIFO TRIGGER LEVEL

| BIT 7 | BIT 6 | RX FIFO INTERRUPT ACTIVE LEVEL (BYTES) |
|-------|-------|--|
| 0 | 0 | 01 |
| 0 | 1 | 04 |
| 1 | 0 | 08 |
| 1 | 1 | 14 |

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

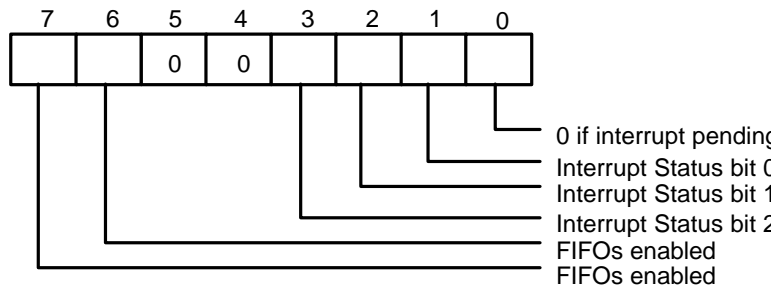
Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 1: Setting this bit to a logical 1 resets the RX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the UART. This bit should be set to a logical 1 before other bits of UFR are programmed.

4.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status, which is encoded by different interrupt sources into 3 bits.



Notes:

Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logic 0.

Bit 3: In 16450 mode, this bit is 0. In 16550 mode, both bit 3 and 2 are set to a logical 1 when a time-out interrupt is pending.

Bit 2, 1: These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to a logical 0.

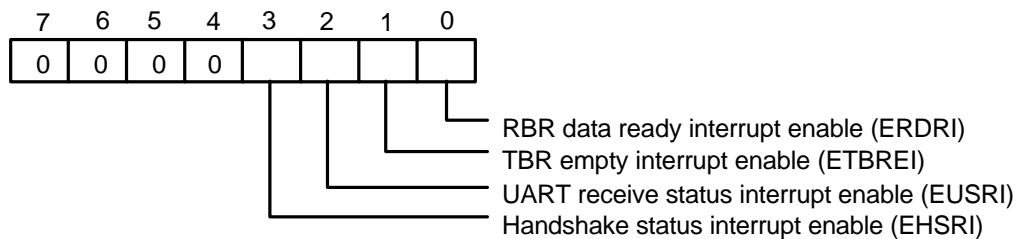
TABLE 4-5 INTERRUPT CONTROL FUNCTION

| ISR | | | | INTERRUPT SET AND FUNCTION | | | |
|-------|-------|-------|-------|----------------------------|---------------------|---|---|
| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Interrupt priority | Interrupt Type | Interrupt Source | Clear Interrupt |
| 0 | 0 | 0 | 1 | - | - | No Interrupt pending | - |
| 0 | 1 | 1 | 0 | First | UART Receive Status | 1. OER = 1 2. PBER = 1 3. NSER = 1 4. SBD = 1 | Read USR |
| 0 | 1 | 0 | 0 | Second | RBR Data Ready | 1. RBR data ready 2. FIFO interrupt active level reached | 1. Read RBR 2. Read RBR until FIFO data under active level |
| 1 | 1 | 0 | 0 | Second | FIFO Data Timeout | Data present in RX FIFO for 4 characters period of time since last access of RX FIFO. | Read RBR |
| 0 | 0 | 1 | 0 | Third | TBR Empty | TBR empty | 1. Write data into TBR 2. Read ISR (if priority is third) |
| 0 | 0 | 0 | 0 | Fourth | Handshake status | 1. TCTS = 1 2. TDSR = 1 3. FER1 = 1 4. TDCD = 1 | Read HSR |

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

4.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register allows the five types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Control Register (ICR). A selected interrupt can be enabled by setting the appropriate bits of this register to a logical 1.



Notes:

Bit 7-4: These four bits are always logic 0.

Bit 3: EHSRI. Setting this bit to a logical 1 enables the handshake status register interrupt.

Bit 2: EUSRI. Setting this bit to a logical 1 enables the UART status register interrupt.

Bit 1: ETBREI. Setting this bit to a logical 1 enables the TBR empty interrupt.

Bit 0: ERDRI. Setting this bit to a logical 1 enables the RBR data ready interrupt.

4.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divides it by a divisor from 1 to $2^{16}-1$. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The following table illustrates the use of the baud generator with frequency of 1.8461 Mhz. In high speed UART mode (refer CR0C.bit7 and CR0C.bit6), the programmable baud generator directly uses 24 MHz and the divider which is same as normal speed divisor. In the high speed mode, the data transmission rate can be up to 1.5 M bps.

TABLE 4-6 BAUD RATE TABLE

| BAUD RATE USING 24 MHZ TO GENERATE 1.8461 MHZ | | |
|---|--|---|
| Desired Baud Rate | Decimal divisor used to generate 16X clock | Percent error difference between desired and actual |
| 50 | 2304 | ** |
| 75 | 1536 | ** |
| 110 | 1047 | 0.18% |
| 134.5 | 857 | 0.099% |
| 150 | 768 | ** |
| 300 | 384 | ** |
| 600 | 192 | ** |
| 1200 | 96 | ** |
| 1800 | 64 | ** |
| 2000 | 58 | 0.53% |
| 2400 | 48 | ** |
| 3600 | 32 | ** |
| 4800 | 24 | ** |
| 7200 | 16 | ** |
| 9600 | 12 | ** |
| 19200 | 6 | ** |
| 38400 | 3 | ** |
| 57600 | 2 | ** |
| 115200 | 1 | ** |
| 230400 | 104* | ** |
| 460800 | 52* | ** |
| 921600 | 26* | ** |
| 1.5M | 1* | 0% |

* Only use in high speed mode (refer CR0C.bit7 and CR0C.bit6).

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

4.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

4.2.10 IRQ3/IRQ4 Setting

IRQ3 and IRQ4 are the interrupt pins for UARTA and UARTB in the W83787IF. These two interrupt pins switch automatically inside the chip depending on the address setting of UARTA and UARTB. When the address of UARTA or UARTB is selected as COM1 or COM3, interrupt requests for the UART are sent out of W83787IF via IRQ4. If the address of UARTA or UARTB is selected as COM2 or COM4, interrupts are sent out via IRQ3. Thus when UARTA is set as COM1, UARTB should not be set as COM3, and vice versa. When UARTA is set as COM2, UARTB should not be set as COM4, and vice versa.

4.3 Infrared Interface

The infrared interface supports a two-way wireless communication using infrared as a transceiver/receive media. It uses a UART B port to serve as data transmission and supports IrDA and Amplitude Shift Keyed IR (ASK-IR).

In the IrDA mode, the serial transmission maximum baud rate can be up to 115.2k. When the UART B send a zero signal, the IRTX encoder encodes a pulse width with 3/16 bit-time or fixed 1.6us to output on IR emitter. If UART B send a high signal, then the encoder have no data output to IR emitter. The decoder receiving a pulse with 3/16 bit-time or 1.6us represents a start bit. (Refer to AC timing for the parameters of the IrDA waveform).

In the ASK-IR mode, the serial transmission maximum baud rate is only 19200 bps. When the UART B send a zero signal, the encoder modulate 500KHZ sending to IR emitter. (Refer to AC timing for the parameters of the ASK-IR waveform).

In the half duplex, the receiver does not receive any input data when transceiver transmit data. That is, during the transmission, the receiver does not disturb it-self from the self-emitter.

5.0 PARALLEL PORT

5.1 Printer Interface Logic

The parallel port of the W83787IF makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level. The W83787IF supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP), Extension FDD mode (EXTFDD), Extension 2FDD mode (EXT2FDD), Extension Adapter mode (EXTADP), and JOYSTICK mode on the parallel port. Refer to the configuration registers for more information on disabling, power-down, and changing the base address of the parallel port and on selecting the mode of operation.

Table 5-1 shows the pin definitions for different modes of the parallel port.

TABLE 5-1 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

| HOST CONNECTOR | PIN NUMBER OF W83787I | PIN ATTRIBUTE | SPP | EPP | ECP |
|----------------|-----------------------|---------------|---------|---------|---|
| 1 | 19 | O | nSTB | nWrite | nSTB |
| 2-9 | 9-14,16-17 | I/O | PD<0:7> | PD<0:7> | PD<0:7> |
| 10 | 26 | I | nACK | Intr | nACK |
| 11 | 24 | I | BUSY | nWait | BUSY, PeriphAck ² |
| 12 | 27 | I | PE | PE | PEerror, nAckReverse ² |
| 13 | 28 | I | SLCT | Select | SLCT |
| 14 | 20 | O | nAFD | nDStrb | nAFD, HostAck ² |
| 15 | 29 | I | nERR | nError | nFault ¹ , nPeriphRequest ² |
| 16 | 21 | O | nINIT | nInit | nINIT ¹ , nReverseRqst ² |
| 17 | 22 | O | nSLIN | nAStrb | nSLIN ^{1, 2} |

Notes:

n<name > : Active Low

1. Compatible Mode

2. High Speed Mode

3. For more information, refer to the IEEE 1284 standard.

| HOST CONNECTOR | PIN NUMBER OF W83787I | PIN ATTRIBUTE | SPP | PIN ATTRIBUTE | EXT2FDD | PIN ATTRIBUTE | EXTFDD |
|----------------|-----------------------|---------------|-------|---------------|-----------------------------|---------------|-----------------------------|
| 1 | 19 | O | nSTB | --- | --- | --- | --- |
| 2 | 9 | I/O | PD0 | I | $\overline{\text{INDEX2}}$ | I | $\overline{\text{INDEX2}}$ |
| 3 | 10 | I/O | PD1 | I | $\overline{\text{TRAK02}}$ | I | $\overline{\text{TRAK02}}$ |
| 4 | 11 | I/O | PD2 | I | $\overline{\text{WP2}}$ | I | $\overline{\text{WP2}}$ |
| 5 | 12 | I/O | PD3 | I | $\overline{\text{RDATA2}}$ | I | $\overline{\text{RDATA2}}$ |
| 6 | 13 | I/O | PD4 | I | $\overline{\text{DSKCHG2}}$ | I | $\overline{\text{DSKCHG2}}$ |
| 7 | 14 | I/O | PD5 | --- | --- | --- | --- |
| 8 | 15 | I/O | PD6 | OD | $\overline{\text{MOA2}}$ | --- | --- |
| 9 | 16 | I/O | PD7 | OD | $\overline{\text{DSA2}}$ | --- | --- |
| 10 | 26 | I | nACK | OD | $\overline{\text{DSB2}}$ | OD | $\overline{\text{DSB2}}$ |
| 11 | 24 | I | BUSY | OD | $\overline{\text{MOB2}}$ | OD | $\overline{\text{MOB2}}$ |
| 12 | 27 | I | PE | OD | $\overline{\text{WD2}}$ | OD | $\overline{\text{WD2}}$ |
| 13 | 28 | I | SLCT | OD | $\overline{\text{WE2}}$ | OD | $\overline{\text{WE2}}$ |
| 14 | 20 | O | nAFD | OD | $\overline{\text{RWC2}}$ | OD | $\overline{\text{RWC2}}$ |
| 15 | 29 | I | nERR | OD | $\overline{\text{NERR2}}$ | OD | $\overline{\text{NERR2}}$ |
| 16 | 21 | O | nINIT | OD | $\overline{\text{DIR2}}$ | OD | $\overline{\text{DIR2}}$ |
| 17 | 22 | O | nSLIN | OD | $\overline{\text{STEP2}}$ | OD | $\overline{\text{STEP2}}$ |

| HOST CONNECTOR | PIN NUMBER OF W83787I | PIN ATTRIBUTE | SPP | PIN ATTRIBUTE | EXTADP MODE | PIN ATTRIBUTE | JOYSTICK MODE |
|----------------|-----------------------|---------------|-------|---------------|-------------|---------------|---------------|
| 1 | 19 | O | nSTB | O | XWR | O | VDD |
| 2 | 9 | I/O | PD0 | I/O | XD0 | I | JP0 |
| 3 | 10 | I/O | PD1 | I/O | XD1 | I | JP1 |
| 4 | 11 | I/O | PD2 | I/O | XD2 | I | --- |
| 5 | 12 | I/O | PD3 | I/O | XD3 | I | --- |
| 6 | 13 | I/O | PD4 | I/O | XD4 | I | JB0 |
| 7 | 14 | I/O | PD5 | I/O | XD5 | I | JB1 |
| 8 | 15 | I/O | PD6 | I/O | XD6 | I | --- |
| 9 | 16 | I/O | PD7 | I/O | XD7 | I | --- |
| 10 | 26 | I | nACK | I | XDRQ | I | --- |
| 11 | 24 | I | BUSY | I | XIRQ | I | --- |
| 12 | 27 | I | PE | O | XA0 | I | --- |
| 13 | 28 | I | SLCT | O | XA1 | I | --- |
| 14 | 20 | O | nAFD | O | XRD | O | VDD |
| 15 | 29 | I | nERR | O | XA2 | I | --- |
| 16 | 21 | O | nINIT | O | XDACK | O | VDD |
| 17 | 22 | O | nSLIN | O | TC | O | VDD |

5.2 Enhanced Parallel Port (EPP)

TABLE 5-2 PRINTER MODE AND EPP REGISTER ADDRESS

| A2 | A1 | A0 | REGISTER | NOTE |
|----|----|----|--------------------------------|------|
| 0 | 0 | 0 | Data port (R/W) | 1 |
| 0 | 0 | 1 | Printer status buffer (Read) | 1 |
| 0 | 1 | 0 | Printer control latch (Write) | 1 |
| 0 | 1 | 0 | Printer control swapper (Read) | 1 |
| 0 | 1 | 1 | EPP address port (R/W) | 2 |
| 1 | 0 | 0 | EPP data port 0 (R/W) | 2 |
| 1 | 0 | 1 | EPP data port 1 (R/W) | 2 |
| 1 | 1 | 0 | EPP data port 2 (R/W) | 2 |
| 1 | 1 | 1 | EPP data port 3 (R/W) | 2 |

Notes:

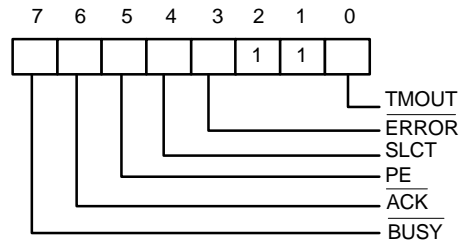
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

5.2.1 Data Swapper

The system microprocessor can read the contents of the printer's data latch by reading the data swapper.

5.2.2 Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the printer status buffer. The bit definitions are as follows:

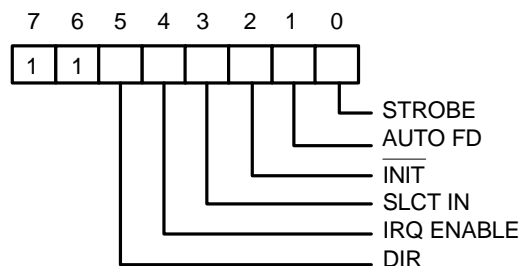


Notes:

- Bit 7: This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
- Bit 6: This bit represents the current state of the printer's $\overline{\text{ACK}}$ signal. A 0 means the printer has received a character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before $\overline{\text{BUSY}}$ stops.
- Bit 5: A 1 means the printer has detected the end of paper.
- Bit 4: A 1 means the printer is selected.
- Bit 3: A 0 means the printer has encountered an error condition.
- Bit 1, 2: These two bits are not implemented and are logic one during a read of the status register.
- Bit 0: This bit is valid in EPP mode only. It indicates that a 10 μS timeout has occurred on the EPP bus. A logic 0 means that no timeout error has occurred; a logic 1 means that a timeout error has been detected. Writing a logic 1 to this bit will clear the timeout status bit; writing a logic 0 has no effect.

5.2.3 Printer Control Latch and Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the printer control swapper. Bit definitions are as follows:



Notes:

- Bit 7, 6: These two bits are a logic one during a read. They can be written.
- Bit 5: Direction control bit

W83757 (SPP) mode: When this bit is a logic 1, pin $\overline{\text{PRTOE}}$ is high, and PRTBEN (CR3 bit 7) is low, the parallel port is in input mode (read); when this bit is a logic 0, the parallel port is in output mode (write). This bit is write-only.

BPP mode: When this bit is a logic 1, the parallel port is in input mode (read); when it is a logic 0, the parallel port is in output mode (write). This bit can be read and written.

Bit 4: A 1 in this position allows an interrupt to occur when $\overline{\text{ACK}}$ changes from low to high.

Bit 3: A 1 in this bit position selects the printer.

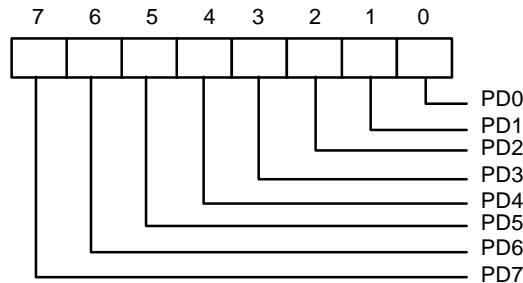
Bit 2: A 0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

5.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

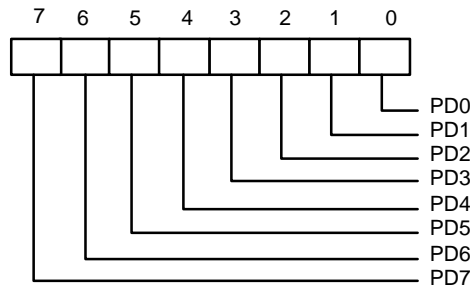


The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of $\overline{\text{IOW}}$ causes an EPP address write cycle to be performed, and the trailing edge of $\overline{\text{IOW}}$ latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of $\overline{\text{IOR}}$ causes an EPP address read cycle to be performed and the data to be output to the host CPU.

5.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. Bit definitions of each data port are as follows:



When accesses are made to any EPP data port, the contents of DB0-DB7 are buffered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of $\overline{\text{IOW}}$ causes

an EPP data write cycle to be performed, and the trailing edge of \overline{IOW} latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of \overline{IOR} causes an EPP read cycle to be performed and the data to be output to the host CPU.

5.2.6 Bit Map of Parallel Port and EPP Registers

| REGISTER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------------|-------------------|------------------|-----|-------|--------------------|-------------------|---------------------|---------------------|
| Data Port (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Status Buffer (Read) | \overline{BUSY} | \overline{ACK} | PE | SLCT | \overline{ERROR} | 1 | 1 | TMOU |
| Control Swapper (Read) | 1 | 1 | 1 | IRQEN | SLIN | \overline{INIT} | \overline{AUTOFD} | \overline{STROBE} |
| Control Latch (Write) | 1 | 1 | DIR | IRQ | SLIN | \overline{INIT} | \overline{AUTOFD} | \overline{STROBE} |
| EPP Address Port (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 0 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 1 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 2 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 3 (R/W) | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |

5.2.7 EPP Pin Descriptions

| EPP NAME | TYPE | EPP DESCRIPTION |
|----------|------|---|
| nWrite | O | Denotes an address or data read or write operation. |
| PD<0:7> | I/O | Bi-directional EPP address and data bus. |
| Intr | I | Used by peripheral device to interrupt the host. |
| nWait | I | Inactive to acknowledge that data transfer is completed. Active to indicate that the device is ready for the next transfer. |
| PE | I | Paper end; same as SPP mode. |
| Select | I | Printer selected status; same as SPP mode. |
| nDStrb | O | This signal is active low. It denotes a data read or write operation. |
| nError | I | Error; same as SPP mode. |
| nInits | O | This signal is active low. When it is active, the EPP device is reset to its initial operating mode, |
| nAStrb | O | This signal is active low. It denotes an address read or write operation. |

5.2.8 EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. The PDx bus is in the standard or bi-directional mode when no EPP read, write, or address cycle is currently being executed. In this condition all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μ S have elapsed from the start of the EPP cycle to the time $\overline{\text{WAIT}}$ is deasserted. The current EPP cycle is aborted when a timeout occurs. The timeout condition is indicated in Status bit 0.

EPP Operation

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

- a. If the $\overline{\text{nWait}}$ is active low, when the read cycle ($\overline{\text{nWrite}}$ inactive high, $\overline{\text{nDStb/nAStrb}}$ active low) or write cycle ($\overline{\text{nWrite}}$ active low, $\overline{\text{nDStb/nAStrb}}$ active low) starts, the read/write cycle proceeds normally and will be completed when $\overline{\text{nWait}}$ goes inactive high.
- b. If $\overline{\text{nWait}}$ is inactive high, the read/write cycle will not start. It must wait until $\overline{\text{nWait}}$ changes to active low, at which time it will start as described above.

EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether $\overline{\text{nWait}}$ is active or inactive. Once the read/write cycle starts, however, it will not terminate until $\overline{\text{nWait}}$ changes from active low to inactive high.

5.2.9 EPP Address Selection

More than four register addresses are required for EPP operation, so parallel port address 3BCh will not support EPP mode when the parallel port is set up for W83757 mode or ECP mode, the SPP/BPP will function normally in 3BCh, 378h, 278h. If 3BCh and EPP mode are selected, then the SPP/BPP/EPP function will not be active.

5.3 Extended Capabilities Parallel (ECP) Port

This port is software and hardware compatible with existing parallel ports, so it may be used as a standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host to peripheral) and reverse (peripheral to host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port supports run-length-encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Hardware support for compression is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

5.3.1 ECP Register and Mode Definitions

| NAME | ADDRESS | I/O | ECP MODES | FUNCTION |
|----------|-----------|-----|-----------|---------------------------|
| data | Base+000h | R/W | 000-001 | Data Register |
| ecpAFifo | Base+000h | R/W | 011 | ECP FIFO (Address) |
| dsr | Base+001h | R | All | Status Register |
| dcr | Base+002h | R/W | All | Control Register |
| cFifo | Base+400h | R/W | 010 | Parallel Port Data FIFO |
| ecpDFifo | Base+400h | R/W | 011 | ECP FIFO (DATA) |
| tFifo | Base+400h | R/W | 110 | Test FIFO |
| cnfgA | Base+400h | R | 111 | Configuration Register A |
| cnfgB | Base+401h | R/W | 111 | Configuration Register B |
| ecr | Base+402h | R/W | All | Extended Control Register |

Note: The base addresses are 3BCH, 378H, and 278H, which are determined by configuration register or hardware setting.

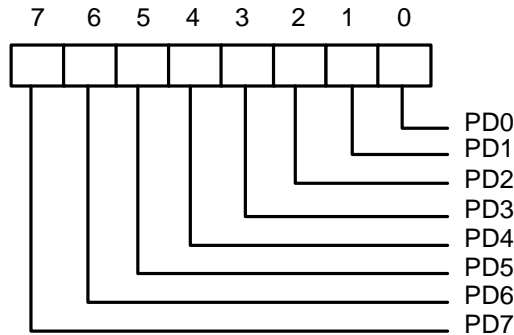
| MODE | DESCRIPTION |
|------|--|
| 000 | SPP mode |
| 001 | PS/2 Parallel Port mode |
| 010 | Parallel Port Data FIFO mode |
| 011 | ECP Parallel Port mode |
| 100 | EPP mode (If this option is enabled in the CR9 and CR0 to select ECP/EPP mode) |
| 101 | Reserved |
| 110 | Test mode |
| 111 | Configuration mode |

Note: The mode selection bits are bit 7-5 of the Extended Control Register.

5.3.2 Data and ecpAFifo Port

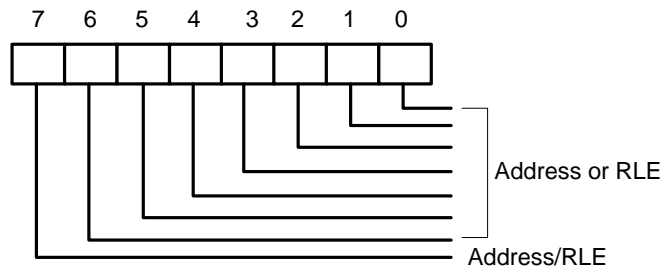
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input. The contents of this register are output to the PD0-PD7 ports. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:



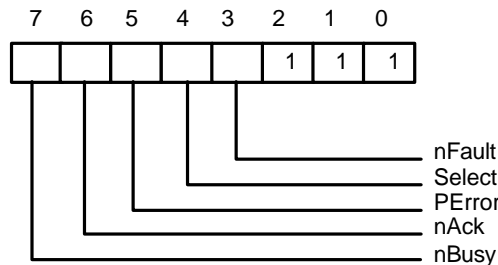
Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is defined only for the forward direction. The bit definitions are as follows:



5.3.3 Device Status Register (DSR)

These bits are at low level during a read of the Printer Status Register. The bits of this status register are defined as follows:



Notes:

Bit 7: This bit reflects the complement of the Busy input.

Bit 6: This bit reflects the nAck input.

Bit 5: This bit reflects the PError input.

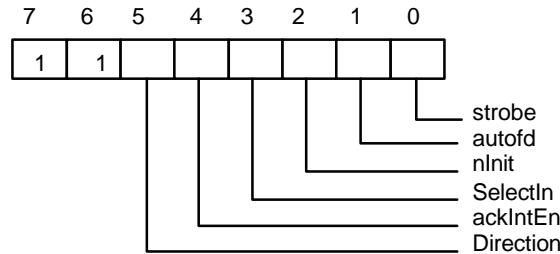
Bit 4: This bit reflects the Select input.

Bit 3: This bit reflects the nFault input.

Bit 2-0: These three bits are not implemented and are always logic one during a read.

5.3.4 Device Control Register (DCR)

The bit definitions are as follows:



Notes:

Bit 6, 7: These two bits are logic one during a read and cannot be written.

Bit 5: This bit has no effect and the direction is always out if mode = 000 or mode = 010. Direction is valid in all other modes.

- 0 the parallel port is in output mode.
- 1 the parallel port is in input mode.

Bit 4: Interrupt request enable. When this bit is set to a high level, it may be used to enable interrupt requests from the parallel port to the CPU due to a low to high transition on the $\overline{\text{ACK}}$ input.

Bit 3: This bit is inverted and output to the $\overline{\text{SLIN}}$ output.

- 0 The printer is not selected.
- 1 The printer is selected.

Bit 2: This bit is output to the $\overline{\text{INIT}}$ output.

Bit 1: This bit is inverted and output to the $\overline{\text{AFD}}$ output.

Bit 0: This bit is inverted and output to the $\overline{\text{STB}}$ output.

5.3.5 cFifo (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. The standard parallel port protocol is used by a hardware handshake to the peripheral to transmit bytes written or DMAed from the system to this FIFO. Transfers to the FIFO are byte aligned.

5.3.6 ecpDFifo (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

When the direction bit is 1, data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO. Reads or DMA's from the FIFO will return bytes of ECP data to the system.

5.3.7 tFifo (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction.

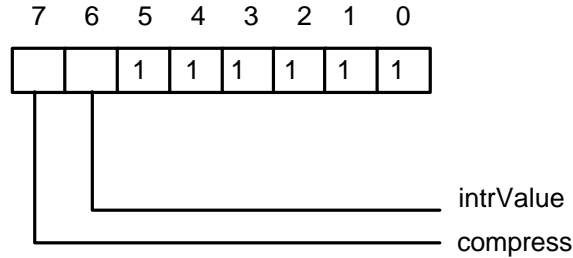
Data in the tFIFO will not be transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

5.3.8 cnfgA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

5.3.9 cnfgB (Configuration Register B) Mode = 111

The bit definitions are as follows:



Notes:

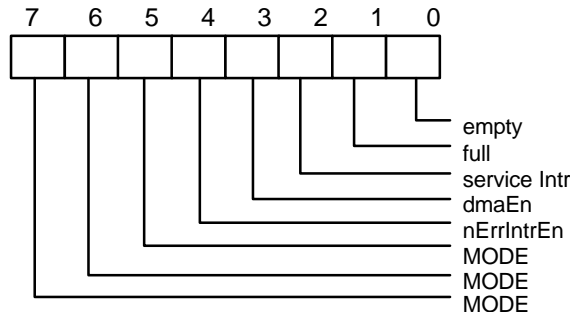
Bit 7: This bit is read-only. It is at low level during a read. This means that this chip does not support hardware RLE compression.

Bit 6: Returns the value on the ISA IRQ line to determine possible conflicts.

Bit 5-0: These five bits are at high level during a read and can be written.

5.3.11 ecr (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:



Notes:

Bit 7-5: These bits are read/write and select the mode.

- 000 Standard Parallel Port mode. The FIFO is reset in this mode.
- 001 PS/2 Parallel Port mode. This is the same as 000 except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register.
- 010 Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
- 011 ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. When the direction is 1 (reverse direction) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
- 100 Selects EPP Mode. In this mode, EPP is selected if the EPP supported option is selected.

- 101 Reserved.
- 110 Test Mode. The FIFO may be written and read in this mode, but the data will not be transmitted on the parallel port.
- 111 Configuration Mode. The configA and configB registers are accessible at 0x400 and 0x401 in this mode.

Bit 4: Read/Write (Valid only in ECP Mode)

- 1 Disables the interrupt generated on the asserting edge of nFault.
- 0 Enables an interrupt pulse on the high to low edge of nFault. If nFault is asserted (interrupt) an interrupt will be generated and this bit is written from a 1 to 0.

Bit 3: Read/Write

- 1 Enables DMA.
- 0 Disables DMA unconditionally.

Bit 2: Read/Write

- 1 Disables DMA and all of the service interrupts.
- 0 Enables one of the following cases of interrupts. When one of the service interrupts has occurred, the serviceIntr bit is set to a 1 by hardware. This bit must be reset to 0 to re-enable the interrupts. Writing a 1 to this bit will not cause an interrupt.
 - (a) dmaEn = 1:
During DMA this bit is set to a 1 when terminal count is reached.
 - (b) dmaEn = 0 direction = 0:
This bit is set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.
 - (c) dmaEn = 0 direction = 1:
This bit is set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

- 0 The FIFO has at least 1 free byte.
- 1 The FIFO cannot accept another byte or the FIFO is completely full.

Bit 0: Read only

- 0 The FIFO contains at least 1 byte of data.
- 1 The FIFO is completely empty.

5.3.11 Bit Map of ECP Port Registers

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NOTE |
|----------|-------------------------|----------------------|----------|----------|----------|-------|--------|--------|------|
| data | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 | |
| ecpAFifo | Addr/RLE | Address or RLE field | | | | | | | 2 |
| dsr | nBusy | nAck | PError | Select | nFault | 1 | 1 | 1 | 1 |
| dcr | 1 | 1 | Directio | ackIntEn | SelectIn | nIntr | autofd | strobe | 1 |
| cFifo | Parallel Port Data FIFO | | | | | | | | 2 |

5.3.11 Bit map of ECP port registers, continued

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NOTE |
|----------|---------------|-----------|----|------------|-------|-------------|------|-------|------|
| ecpDFifo | ECP Data FIFO | | | | | | | | 2 |
| tFifo | Test FIFO | | | | | | | | 2 |
| cnfgA | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| cnfgB | compress | intrValue | 1 | 1 | 1 | 1 | 1 | 1 | |
| ecr | MODE | | | nErrIntrEn | dmaEn | serviceIntr | full | empty | |

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

5.3.12 ECP Pin Descriptions

| NAME | TYPE | DESCRIPTION |
|----------------------|------|---|
| nStrobe (HostClk) | O | The nStrobe registers data or address into the slave on the asserting edge during write operations. This signal handshakes with Busy. |
| PD<7:0> | I/O | These signals contains address or data or RLE data. |
| nAck (PeriphClk) | I | This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse. |
| Busy (PeriphAck) | I | This signal deasserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low. |
| PError (nAckReverse) | I | This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus. |
| Select (Xflag) | I | Indicates printer on line. |
| nAutoFd (HostAck) | O | Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when nAutoFd (HostAck) is high and an 8-bit command is transferred when it is low. |

ECP Pin descriptions, continued

| NAME | TYPE | DESCRIPTION |
|-------------------------|------|---|
| nFault (nPeriphRequest) | I | Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode. |
| nInit (nReverseRequest) | O | This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. |
| nSelectIn (ECPMode) | O | This signal is always deasserted in ECP mode. |

5.3.13 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits. The following are required:

- (a) Set direction = 0, enabling the drivers.
- (b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
- (c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
- (d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

Mode Switching

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (mode 011 or 010). If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can be changed only in mode 001. When in extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001.

Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

Data Compression

The W83787IF supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Note that the odd (RLE) compression in hardware is not supported. In order to transfer data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

5.3.14 FIFO Operation

The FIFO threshold is set in configuration register 5. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

5.3.15 DMA Transfers

DMA transfers are always to or from the `ecpDFifo`, `tFifo`, or `CFifo`. The DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and `serviceIntr` is asserted, which will disable the DMA.

5.3.16 Programmed I/O (NON-DMA) Mode

The ECP or parallel port FIFOs can also be operated using interrupt driven programmed I/O. Programmed I/O transfers are to the `ecpDFifo` at 400H and `ecpAFifo` at 000H or from the `ecpDFifo` located at 400H, or to/from the `tFifo` at 400H. The host must set the direction, state, `dmaEn = 0` and `serviceIntr = 0` in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

5.4 Extension FDD Mode (EXTFDD)

In this mode, the W83787IF changes the printer interface pins to FDC input/output pins, allowing the user to install a second floppy disk drive (FDD B) through the DB-25 printer connector. The pin assignments for the FDC input/output pins are shown in Table 5-1.

After the printer interface is set to EXTFDD mode, the following occur:

- (1) Pins `MOB` and `DSB` will be forced to inactive state.
- (2) Pins `DSKCHG`, `RDATA`, `WP`, `TRAK0`, `INDEX` will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.
- (3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.
- (4) If the parallel port is set to EXTFDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

5.5 Extension 2FDD Mode (EXT2FDD)

In this mode, the W83787IF changes the printer interface pins to FDC input/output pins, allowing the user to install two external floppy disk drives through the DB-25 printer connector to replace internal floppy disk drives A and B. The pin assignments for the FDC input/output pins are shown in Table 5-1.

After the printer interface is set to EXTFDD mode, the following occur:

- (1) Pins `MOA`, `DSA`, `MOB`, and `DSB` will be forced to inactive state.
- (2) Pins `DSKCHG`, `RDATA`, `WP`, `TRAK0`, and `INDEX` will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.
- (3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.
- (4) If the parallel port is set to EXT2FDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

5.6 Extension Adapter Mode (EXTADP)*

In this mode, the W83787IF redefines the printer interface pins for use as an extension adapter, allowing a pocket peripheral adapter card to be installed through the DB-25 printer connector. The pin assignments for the extension adapter are shown in table 5-1.

XDO-XD7 are the system data bus for the extension adapter.

XA0-XA2 are the system address bus.

XWR and XRD are the I/O read/write commands with address comparing match or in DMA access mode.

XDACK, XTC, and XDRQ are used in conjunction with PDACKX, TC, and PDRQX to execute a DMA cycle.

The extension adapter can issue a DMA request by setting pin XDRQ high, thus sending the W83787IF output to the host system by pin PDRQX. The DMA controller should recognize the DMA request and output a relative DACK to pin PDACKX of the W83787IF, which will output the DACK without any change from pin XDACK to the extension adapter. Once the DMA transfer is completed, a terminal count (TC) should be issued from the DMA controller to pin TC of W83787IF and output to the extension adapter via pin XTC. XIRQ is the interrupt request of the extension adapter. The value of XIRQ coming from the extension adapter will directly pass through pin IRQ7 to the host system.

XIRQ and IRQ7, XDACK and PDACKX, and XDRQ and PDRQX are three input/output pairs of W83787IF pins. Although these pins are defined as DMA and interrupt functions, they can be redefined by users for other specific functions.

5.6.1 Operation

The idea behind EXTADP mode is to treat the parallel port DB-25 connector as an ISA slot, except that its addresses are not issued to the extension adapter. The operation of EXTADP mode is described below:

1. Set the W83787IF to EXTADP mode by programming bit 7 of CR7 as low and bit 3 and bit 2 of CR0 as high and low, respectively.
2. The W83787IF CR2 is an address register that records the address of the extension adapter. When the desired address is written into CR2, pins XWR and XRD of the W83787IF will simultaneously go low and the desired address will also appear on the printer data bus PD7-PD0. Users can logically OR these two signals as an initial reset.
3. After the above two steps, every time the host system issues an IOR or IOW command, the W83787IF will compare the I/O address with the CR2 register. If the comparison matches, the data, low bits addresses (XA2-XA0), and XWR/XRD will be presented on the parallel port DB-25 connector.
4. DMA operations are handled in the same way as item 3, except that the relevant PDACKX, PDRQX will be active on the DB-25 connector.

** Patent pending

5.7 Joystick Mode*

The joystick mode allows users to plug a joystick into the parallel port DB-25 connector. The pin definitions are shown in Table 5-1.

Pins $\overline{\text{NSTB}}$, $\overline{\text{AFD}}$, $\overline{\text{NSLIN}}$, and $\overline{\text{INIT}}$ output high as a voltage supply to the joystick.

Pins PD5 and PD4 are the button input of the joystick.

Pins PD1 and PD0 are the X/Y axis paddle input of the joystick.

There are two one-shot timers (556) inside the W83787IF for use with the joystick.

6.0 GAME PORT DECODER

The W83787IF provides $\overline{\text{GMRD}}$ and $\overline{\text{GMWR}}$ pins that decode address 201H and I/O read/write commands.

If the host issues IOR 201H, the $\overline{\text{GMRD}}$ pin is low active; if it issues IOW 201H, the $\overline{\text{GMWR}}$ pin is low active.

7.0 EXTENDED FUNCTION REGISTERS

The W83787IF provides many configuration registers for setting up different types of configurations. After power-on reset, the state of the hardware setting of each pin will be latched by the relevant configuration register to allow the W83787IF to enter the proper operating configuration. To protect the chip from invalid reads or writes, the configuration registers cannot be accessed by the user. To enable the configuration registers to be read and written, first the value 89H/88H must be written to the Extended Functions Enable Register (I/O port address 250H). Second, a value from 00H to 0BH must be written to the Extended Functions Index Register (I/O port address 251H) to identify which configuration register is to be accessed. The user can then access the desired configuration register through the Extended Functions Data Register (I/O port address 252H). After programming of the configuration register is finished, a value other than 89H/88H should be written to EFER or bit 6 of CR9 (LOCKREG) should be set to high to protect the configuration registers against accidental accesses. The configuration registers can be reset to their default or hardware setting values only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

7.1 Extended Functions Enable Register (EFER)

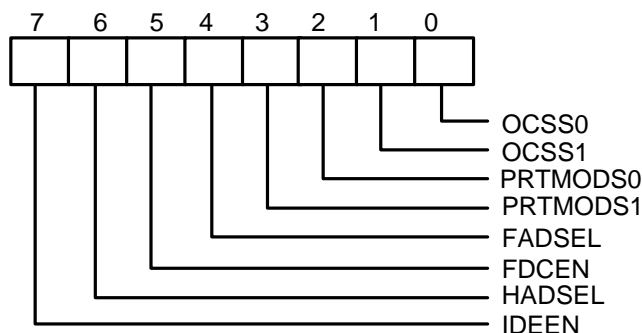
After a power-on reset, the W83787IF enters the default operating mode. Before the W83787IF enters the Extended Function mode, a 89H/88H (dependent on power-on setting value of pin $\overline{\text{GMRD}}$) must be programmed to the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Register is a write-only register. Its port address is 250H on a PC/AT system.

7.2 Extended Function Index Register(EFIR), Extended Function Data Register(EFDR)

After 89H/88H is programmed into EFER, the Extended Function Index Register (EFIR) must be loaded with index value 0H, 1H, 2H, ..., or AH to access Configuration Register 0 (CR0), Configuration Register 1 (CR1), Configuration Register 2 (CR2), ..., or Configuration Register A (CRA) through the Extended Function Data Register (EFDR). EFIR is a write-only register with port address 251H on PC/AT systems; EFDR is a read/write register with port address 252H on PC/AT systems. The function of each configuration register is described below.

7.2.1 Configuration Register 0 (CR0), EFER = 89H, EFIR = 0H

When EFER is loaded with 89H and EFIR with 0H, the CR0 register can be accessed through EFDR. The bit definitions for CR0 are as follows:



Notes:

IDEEN (Bit 7):

This bit enables/disables the IDE port. At power-on reset, this bit will latch the value set on the $\overline{CS0}$ /IDEEN pin. If there is no setting, a default enable will be latched by this bit because of the pull-down resistor on the $\overline{CS0}$ /IDEEN pin.

- 0 Enables IDE port.
- 1 Disables IDE port.

HADSEL (Bit 6):

This bit selects the HDC port address. At power-on reset, this bit will latch the value set on the $\overline{CS1}$ /HADSEL pin. If there is no setting, a default 1F0H-1F7H, 3F6H, 3F7H will be latched by this bit because of the pull-up resistor on the $\overline{CS1}$ /HADSEL pin.

- 0 Selects address range 170H-177H, 376H, 377H for IDE.
- 1 Selects address range 1F0H-1F7H, 3F6H, 3F7H for IDE.

FDCEN (Bit 5):

This bit enables/disables the FDC port. At power-on reset, this bit will latch the value set on the FDCEN pin. If there is no setting, a default enable will be latched by this bit because of the pull-down resistor on the FDCEN pin.

- 0 Enables FDC port.
- 1 Disables FDC port (when FDC port is disabled, no clock will be input to this port in order to save power)

FADSEL (Bit 4):

This bit is used to select the FDC port address. At power-on reset, this bit will latch the value set on the \overline{DBENH} /FADSEL pin. If there is no setting, a default 3F0H-3F7H will be latched by this bit because of the pull-up resistor on the \overline{DBENH} /FADSEL pin.

- 0 Selects address range 370H-377H.
- 1 Selects address range 3F0H-3F7H.

PRTMOD1 PRTMOD0 (Bit 3, Bit 2):

These two bits and PRTMOD2 (CR9 bit7) determine the parallel port mode of the W83787IF (see Table 7-1 on next page).

Table 7-1

| PRTMODS2 (BIT 7 OF CR9) | PRTMOD1 (BIT 3 OF CR0) | PRTMODS0 (BIT 2 OF CR0) | |
|------------------------------------|-----------------------------------|------------------------------------|----------|
| 0 | 0 | 0 | W83757 |
| 0 | 0 | 1 | EXTFDC |
| 0 | 1 | 0 | EXTADP |
| 0 | 1 | 1 | EXT2FDD |
| 1 | 0 | 0 | JOYSTICK |
| 1 | 0 | 1 | EPP/SPP |
| 1 | 1 | 0 | ECP |
| 1 | 1 | 1 | ECP/EPP |

- 00 W83757 Mode (Default), PRTMOD2 = 0
Default state after power-on reset. In this mode, the W83787IF is fully compatible with the W83757F/W83757AF.
- 01 Extension FDD Mode (EXTFDD), PRTMOD2 = 0
- 10 Extension Adapter Mode (EXTADP), PRTMOD2 = 0
- 11 Extension 2FDD Mode (EXT2FDD), PRTMOD2 = 0
- 00 JOYSTICK Mode, PRTMOD2 = 1
- 01 EPP Mode and SPP Mode, PRTMOD2 = 1
- 10 ECP Mode, PRTMOD2 = 1
- 11 ECP Mode and EPP Mode, PRTMOD2 = 1

OSCS1, OSCS0 (Bit 1, Bit 0):

These two bits and OSCS2 (CR6 bit 6) are used to select one of the W83787IF's power-down functions. These bits may be programmed in four different ways:

- 00 Default power-on state after power-on reset (OSCS2 = 0).
- 00 OSC on, 24 MHz clock is stopped internally (OSCS2 = 1). Clock can be restarted by clearing OSCS2.
- 01 Immediate power-down (IPD) state, OSCS2 = 0

When bit 0 is 1 and bit 1 is set to 0, the W83787IF will stop its oscillator and enter power-down mode immediately. The W83787IF will not leave the power-down mode until either a system power-on reset from the MR pin or these two bits are used to program the chip back to power-on state. After leaving the power-down mode, the W83787IF must wait 128 mS for the oscillator to stabilize.

- 10 Standby for automatic power-down (APD), OSCS2 = 0
When bit 1 is set to 1 and bit 0 is set to 0, the W83787IF will stand by for automatic power-down. A power-down will occur when the following conditions obtain:

- FDC not busy
- FDD motor off
- Interrupt source of line status, modem status, and data ready is inactive (neglecting IER enable/disable)
- Master Reset inactive
- SOUTA and SOUTB in idle state

- SINA and SINB in idle state
- No register read or write to chip

If all of these conditions are met, a counter begins to count down. While the timer is counting down, the W83787IF remains in normal operating mode, and if any of the above conditions changes, the counter will be reset. If the set time (set by bit 7 and bit 6 of CR8) elapses without a change in any of the above conditions, bits 1 and 0 will be set to (1, 1) and the chip will enter automatic power-down mode. The oscillator of the W83787IF will remain running, but the internal clock will be disabled to save power. Once the above conditions are no longer met, the internal clock will be resupplied and the chip will return to normal operation.

11 Automatic power-down (ADP) state, OSCS2 = 0

The W83787IF enters this state automatically after the counter described above has counted down. If there is a change in any of the conditions listed above, the W83787IF's clock will be restarted and bits 1 and 0 will be set to (1, 0), i.e., standby for automatic power-down. When the clock is restarted, the chip is ready for normal operation, with no need to wait for the oscillator to stabilize.

Example 7.1: Enable IDE (1F0H-1F7H, 3F6H, 3F7H), FDC (3F0H-3F7H); W83757 mode: power-on mode.

Ex. 7.1 (DOS DEBUG.COM inst.)

- O 250 89
- O 251 00
- O 252 50
- O 250 00

Example 7.2: Disable IDE; enable FDC (370H-377H); Extension FDC Mode; immediate power-down mode.

Ex. 7.2 (DOS DEBUG.COM inst.)

- O 250 89
- O 251 00
- O 252 C5
- O 250 00

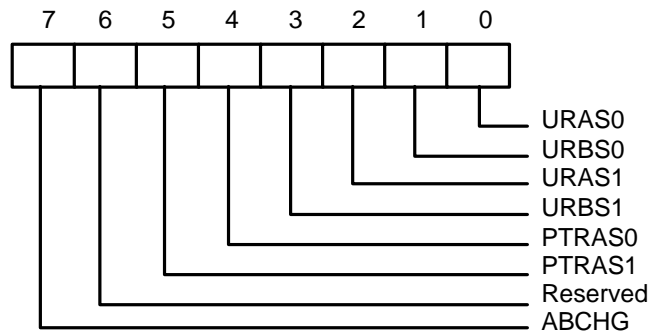
Example 7.3: Enable IDE (170H-177H, 376H, 377H), disable FDC; Extension Adapter Mode; standby for automatic power-down mode.

Ex. 7.3 (DOS DEBUG.COM inst.)

- O 250 89
- O 251 00
- O 252 3A
- O 250 00

7.2.2 Configuration Register 1 (CR1) EFER = 89H, EFIR = 1H

When 89H is loaded into EFER and 01H is loaded into EFIR, the CR1 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

URAS1 URAS0 (Bit 2, 0):

These two bits and URAS2 (CR3 bit 3) = 0 determine the base address of UARTA. (The default value depends on SOUTA and DTRB at power-on setting. If there is no setting, UARTA is set to COM1 by default.) When URAS2 = 1, see the description of CR3 bit 3.

- 00 Selects COM4 address, 2E8H
- 01 Selects COM3 address, 3E8H
- 10 Selects COM1 address, 3F8H
- 11 Disables UARTA port (when UARTA port is disabled, no clock will be input to this port in order to save power)

URBS1 URBS0 (Bit 3, 1):

These two bits and URBS2 (CR3 bit 2) = 0 determine the base address of UARTB. (The default value depends on SOUTB and RTSB at power-on setting. If there is no setting, UARTB is set to COM2 by default.) When URBS2 = 1, see the description of CR3 bit 2.

- 00 Selects COM3 address, 3E8H
- 01 Selects COM4 address, 2E8H
- 10 Selects COM2 address, 2F8H
- 11 Disables UARTB port (when UARTB port is disabled, no clock will be input to this port in order to save power)

PTRAS1, PTRAS0 (Bit 5, 4):

These two bits determine the base address of the parallel port. (The default value depends on RTSA and DTRA at power-on setting. If there is no setting, the default is LPT1.)

- 00 Selects LPT3 address, 3BCH
- 01 Selects LPT2 address, 278H
- 10 Selects LPT1 address, 378H
- 11 Disables parallel port all function modes

ABCHG (Bit 7):

This bit enables the FDC AB Change Mode. (The default value depends on $\overline{DBENL}/ABCHG$ at power-on setting. If there is no setting, the default is normal mode.)

- 0 Drives A and B assigned as usual
- 1 Drive A and drive B assignments exchanged

Examples (debug instructions):

Example 7.4: Enable COM1 (3F8), COM2 (2F8), LPT1 (3BC); drives A and B assigned as in normal operation.

Ex. 7.4

- O 250 89
- O 251 01
- O 252 0C
- O 250 00

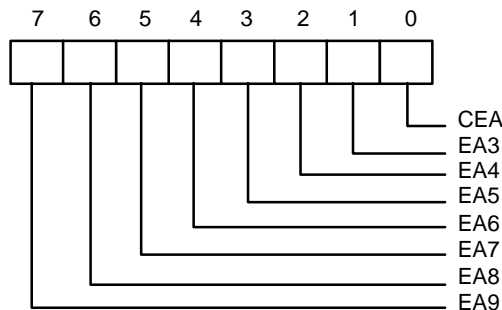
Example 7.5: Enable only COM3 (3E8), LPT2 (278); assignments of drives A and B exchanged.

Ex. 7.5

- O 250 89
- O 251 01
- O 252 DB
- O 250 00

7.2.3 Configuration Register 2 (CR2) EFER = 89, EFIR = 2H

When EFER = 89H and EFIR = 02H, the CR2 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

When the W83787IF is programmed into extension adapter mode, the contents of this register are a base address for the extension adapter. When base addresses EA3-EA9 are written into CR2, both the \overline{XRD} and \overline{XWR} pins will be active low simultaneously and an adapter connected to the parallel port can latch the same base address through pins XD1-XD7. After the base address is latched into CR2, a subsequent read/write cycle to this same base address will generate an \overline{XRD} or \overline{XWR} signal.

If CEA is set to 0, then the W83787IF will compare system addresses SA9-SA3 with EA9-EA3 to generate a compare-equal signal for this read/write command to access the Extension adapter. If CEA is set to 1, then only EA9-EA4 are used in this comparison.

Examples (debug instructions):

Example 7.6: Enable IDE, FDC; enable extension adapter mode (assume I/O port is 300H).

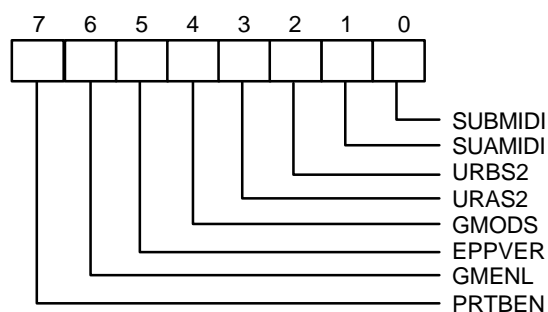
- O 250 89
- O 251 00
- O 252 58 (Set Extension Adapter Mode)
- O 251 02 (\overline{XRD} and \overline{XWR} will be active low and C0H will appear at XD1- XD7)
- O 252 C0 (Compare EA3-EA9)
- O 250 00

Example 7.7: Each time host reads/writes 300H-307H, \overline{XRD} or \overline{XWR} is active.

In DMA cycles, IOR/W activates DACKX, which will also activate XRD or XWR separately.

7.2.4 Configuration Register 3 (CR3) EFER = 89, EFIR = 3H

When 89H is loaded into EFER and 03H is loaded into EFIR, the CR3 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

SUBMIDI (Bit 0):

This bit selects the clock divide rate of UARTB.

- 0 disables MIDI support, UARTB clock = 24MHz divided by 13 (default)
- 1 enables MIDI support, UARTB clock = 24MHz divided by 12

SUAMIDI (Bit 1):

This bit selects the clock divide rate of UARTA.

- 0 Disables MIDI support, UARTA clock = 24MHz divided by 13 (default)
- 1 Enables MIDI support, UARTA clock = 24MHz divided by 12

URBS2 (Bit 2):

This bit determines the base address of UARTB.

- 0 Refer to the description of CR1 bit 1, 3
- 1 Selects COM1 address, 3F8H

URAS2 (bit 3):

This bit determines the base address of UARTA.

- 0 Refer to the description of CR1 bit 0, 2
- 1 Selects COM2 address, 2F8H

GMODS (Bit 4):

This bit selects the adapter mode or portable mode.

- 0 Selects the portable mode. Pins 41 and 39 will function as PFD $\overline{\text{CEN}}$ and PEXTEN
- 1 Selects the adapter mode. Pins 41 and 39 will function as $\overline{\text{GMRD}}$ and $\overline{\text{GMWR}}$

EPPVER (Bit 5):

This bit selects the EPP version of parallel port:

- 0 Selects the EPP 1.9 version
- 1 Selects the EPP 1.7 version (default)

GMENL (Bit 6):

This bit enables or disables game port.

- 0 Enables game port
- 1 Disables game port

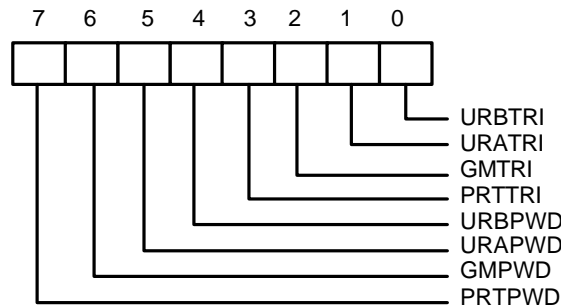
PRTBEN (Bit 7):

This bit enables or disables the bi-directional capability of the parallel port in W83757 mode.

- 1 Disables the bi-directional capability of the parallel port
- 0 Enables the bi-directional capability of the parallel port. If the PRTOE pin is pulled high or left floating, then the direction of the parallel port is controlled by bit 5 of the printer control register (power-on default)

7.2.5 Configuration Register 4 (CR4) EFER = 89H, EFIR = 04H

When 89H is loaded into EFER and 04H is loaded into EFIR, the CR4 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

P RTPWD (Bit 7):

- 0 Supplies power to the parallel port
- 1 Puts the parallel port in power-down mode

G MPWD (Bit 6):

- 0 Supplies power to the game port
- 1 Puts the game port in power-down mode

U RAPWD (Bit 5):

- 0 Supplies power to COMA
- 1 Puts COMA in power-down mode

U RBPWD (Bit 4):

- 0 Supplies power to COMB
- 1 Puts COMB in power-down mode

PRTTRI (Bit 3):

This bit enables or disables the tri-state outputs of parallel port in power-down mode.

- 0 The output pins of the parallel port will not be tri-stated when parallel port is in power-down mode.
- 1 The output pins of the parallel port will be tri-stated when parallel port is in power-down mode.

GMTRI (Bit 2):

This bit enables or disables the tri-state outputs of the game port in power-down mode.

- 0 The output pins of the game port will not be tri-stated when game port is in power-down mode.
- 1 The output pins of the game port will be tri-stated when game port is in power-down mode.

URATRI (Bit 1):

This bit enables or disables the tri-state outputs of UARTA in power-down mode.

- 0 The output pins of UARTA will not be tri-stated when UARTA is in power-down mode.
- 1 The output pins of UARTA will be tri-stated when UARTA is in power-down mode.

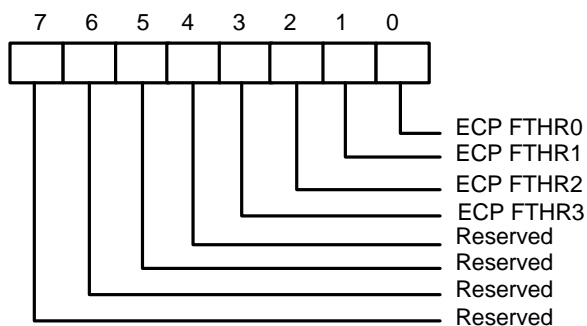
URBTRI (Bit 0):

This bit enables or disables the tri-state outputs of UARTB in power-down mode.

- 0 The output pins of UARTB will not be tri-stated when UARTB is in power-down mode.
- 1 The output pins of UARTB will be tri-stated when UARTB is in power-down mode.

7.2.6 Configuration Register 5 (CR5) EFER = 89H, EFIR = 05H

When 89H is loaded into EFER and 05H is loaded into EFIR, the CR5 register can be accessed through EFDR. The bit definitions are as follows:



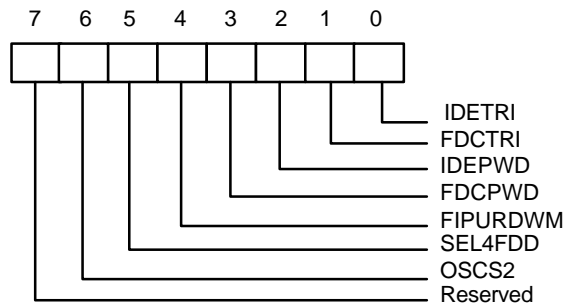
Notes:

Bit 7-4: Reserved

Bit 3-0: These four bits define the FIFO threshold for the ECP mode parallel port. The default value is 0000 after power-up.

7.2.7 Configuration Register 6 (CR6) EFER = 89H, EFIR = 06H

When 89H is loaded into EFER and 06H is loaded into EFIR, the CR6 register can be accessed through EFDR. The bit definitions are as follows:



Bit 7: Reserved

OSCS2 (Bit 6): This bit and OSCS1, OSCS0 (bit 1, 0 of CR0) select one of the W83787IF's power-down functions. Refer to descriptions of CR0.

SEL4FDD (Bit 5): Selects four FDD mode

- 0 Selects two FDD mode (see Table 7-2)
- 1 Selects four FDD mode

\overline{DSA} , \overline{DSB} , \overline{MOA} and \overline{MOB} output pins are encoded as show in Table 7-3 to select four drives.

Table 7-2

| DO REGISTER (3F2H) | | | | | | \overline{MOB} | \overline{MOA} | \overline{DSB} | \overline{DSA} | DRIVE SELECTED |
|----------------------|-------|-------|-------|-------|-------|------------------|------------------|------------------|------------------|----------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 1 | Bit 0 | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | -- |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | FDD A |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | FDD B |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | -- |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | -- |

Table 7-3

| DO REGISTER (3F2H) | | | | | | \overline{MOB} | \overline{MOA} | \overline{DSB} | \overline{DSA} | DRIVE SELECTED |
|----------------------|-------|-------|-------|-------|-------|------------------|------------------|------------------|------------------|----------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 1 | Bit 0 | | | | | |
| 0 | 0 | 0 | 0 | x | x | 1 | 1 | x | x | -- |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | FDD A |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | FDD B |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | FDD C |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | FDD D |

FIPURDWN (Bit 4):

This bit controls the internal pull-up resistors of the FDC input pins \overline{RDATA} , \overline{INDEX} , $\overline{TRAK0}$, \overline{DSKCHG} , and \overline{WP} .

- 0 The internal pull-up resistors of FDC are turned on.
- 1 The internal pull-up resistors of FDC are turned off.

FDCPWD (Bit 3):

This bit controls the power to the FDC.

- 0 Power is supplied to the FDC.
- 1 Puts the FDC in power-down mode.

IDEPWD (Bit 2):

This bit controls the power of the IDE.

- 0 Power is supplied to the IDE.
- 1 Puts the IDE in power-down mode.

FDCTRI (Bit 1):

This bit enables or disables the tri-state outputs of the FDC in power-down mode.

- 0 The output pins of the FDC will not be tri-stated when FDC is in power-down mode.
- 1 The output pins of the FDC will be tri-stated when FDC is in power-down mode.

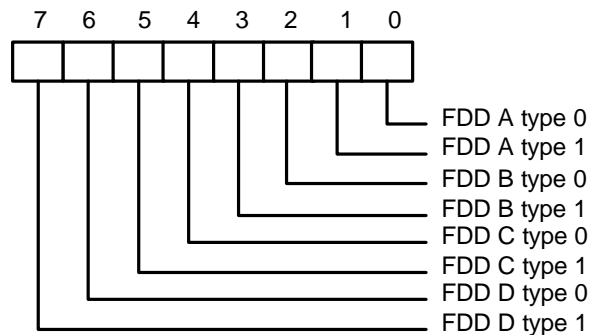
IDETRI (Bit 0):

This bit enables or disables the tri-state outputs of the IDE in power-down mode.

- 0 The output pins of the IDE will not be tri-stated when IDE is in power-down mode.
- 1 The output pins of the IDE will be tri-stated when IDE is in power-down mode.

7.2.8 Configuration Register 7 (CR7) EFER = 89H, EFIR = 07H

When 89H is loaded into EFER and 07H is loaded into EFIR, the CR7 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

FDD A type 1, 0 (Bit 1, 0):

These two bits select the type of FDD A.

- 00 Selects normal mode. When $\overline{RWC} = 0$, the data transfer rate is 250 kb/s. When $\overline{RWC} = 1$, the data transfer rate is 500 kb/s.

Three mode FDD select (EN3MODE = 1):

- 01 $\overline{RWC} = 0$, selects 1.2 MB high-density FDD.
- 10 $\overline{RWC} = 1$, selects 1.44 MB high-density FDD.
- 11 Don't care \overline{RWC} , selects 720 KB double-density FDD.

FDD B type 1,0 (Bit 3,2):

These two bits select the type of FDD B.

- 00 Selects normal mode. When $\overline{RWC} = 0$, the data transfer rate is 250 kb/s. When $\overline{RWC} = 1$, the data transfer rate is 500 kb/s.

Three mode FDD select (EN3MODE = 1):

- 01 \overline{RWC} = 0, selects 1.2 MB high-density FDD.
- 10 \overline{RWC} = 1, selects 1.44 MB high-density FDD.
- 11 Don't care \overline{RWC} , selects 720 KB double-density FDD.

FDD C type 1,0 (Bit 5,4):

These two bits select the type of FDD C.

- 00 Selects normal mode. When \overline{RWC} = 0, the data transfer rate is 250 kb/s. When \overline{RWC} = 1, the data transfer rate is 500 kb/s.

Three mode FDD select (EN 3 MODE = 1):

- 01 \overline{RWC} = 0, selects 1.2 MB high-density FDD.
- 10 \overline{RWC} = 1, selects 1.44 MB high-density FDD.
- 11 Don't care \overline{RWC} , selects 720 KB double-density FDD.

FDD D type 1, 0 (Bit 7,6):

These two bits select the type of FDD D.

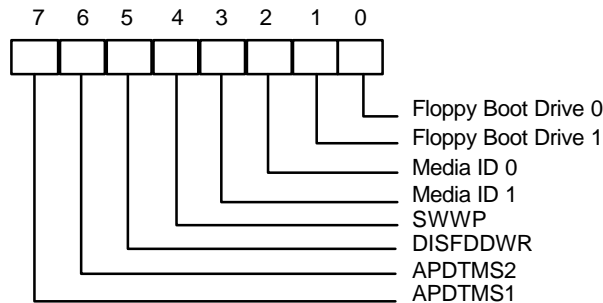
- 00 Selects normal mode. When \overline{RWC} = 0, the data transfer rate is 250 kb/s. When \overline{RWC} = 1, the data transfer rate is 500 kb/s.

Three mode FDD select (EN3MODE = 1):

- 01 \overline{RWC} = 0, selects 1.2 MB high-density FDD.
- 10 \overline{RWC} = 1, selects 1.44 MB high-density FDD.
- 11 Don't care \overline{RWC} , selects 720 KB double-density FDD.

7.2.9 Configuration Register 8 (CR8) EFER = 89H, EFIR = 08H

When 89H is loaded into EFER and 08H is loaded into EFIR, the CR8 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

APDTMS2 APDTMS1 (Bit 6, 7):

These two bits select the count-down time of the automatic power-down mode counter.

- 00 4 seconds
- 01 32 seconds
- 10 64 seconds
- 11 4 minutes

DISFDDWR (Bit 5):

This bit enables or disables FDD write data.

- 0 Enables FDD write
- 1 Disables FDD write (forces pins \overline{WE} , \overline{WD} to stay high)

Once this bit is set high, the FDC operates normally, but because pin \overline{WE} is inactive, the FDD will not write data to diskettes. For example, if a diskette is formatted with DISFDDWR = 1, after the format command has been executed, messages will be displayed that appear to indicate that the format is complete. If the diskette is removed from the disk drive and inserted again, however, typing the DIR command will reveal that the contents of the diskette have not been modified and the diskette was not actually reformatted.

The reason for this is that as the operating system (e.g., DOS) reads the diskette files, it keeps the files in memory. If there is a write operation, DOS will write data to the diskette and memory simultaneously. When DOS wants to read the diskette, it will first search the files in memory. If DOS finds the file in memory, it will not issue a read command to read the diskette. When DISFDDWR = 1, DOS still writes data to the diskette and memory, but only the data in memory are updated. If a read operation is performed, data are read from memory first, and not from the diskette. The action of removing the diskette from the drive and inserting it again forces the \overline{DSKCHG} pin active. DOS will then read the contents of the diskette and will show that the contents have not been modified. The same holds true with write commands.

The disable FDD write function allows users to protect diskettes against computer viruses by ensuring that no data are written to the diskette.

SWWP (Bit 4):

- | | |
|---|--|
| 0 | Normal, use \overline{WP} to determine whether the FDD is write-protected or not |
| 1 | FDD is always write-protected |

Media ID 1 Media ID 0 (Bit 3, 2):

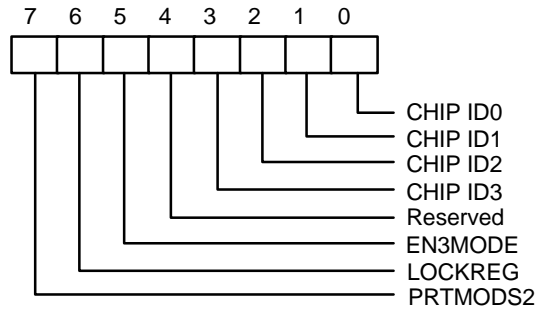
These two bits hold the media ID bit 1, 0 for three mode

Floppy Boot Drive 1 Floppy Boot Drive 0 (bit 1, 0)

These two bits hold the value of floppy boot drive 1 and drive 0 for three mode

7.2.10 Configuration Register 9 (CR9) EFER = 89H, EFIR = 09H

When 89H is loaded into EFER and 09H is loaded into EFIR, the CR9 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

PRTMODS2 (Bit 7):

This bit and PRTMODS1, PRTMODS0 (bits 3, 2 of CR0) select the operating mode of the W83787IF. Refer to the descriptions of CR0.

LOCKREG (Bit 6):

This bit enables or disables the reading and writing of all configuration registers.

- 0 Enables the reading and writing of CR0-CRB
- 1 Disables the reading and writing of CR0-CRB (locks W83787IF extension functions)

EN3MODE (Bit 5):

This bit enables or disables three mode FDD selection. When this bit is high, it enables the read/write 3F3H register.

- 0 Disables 3 mode FDD selection
- 1 Enables 3 mode FDD selection

When three mode FDD function is enabled, the value of \overline{RWC} depends on bit 5 and bit 4 of TDR(3F3H). The values of \overline{RWC} and their meaning are shown in Table 7-4.

Table 7-4

| BIT 5 OF TDR | BIT 4 OF TDR | \overline{RWC} | $\overline{RWC} = 0$ | $\overline{RWC} = 1$ |
|--------------|--------------|------------------|----------------------|----------------------|
| 0 | 0 | Normal | 250K bps | 500K bps |
| 0 | 1 | 0 | 1.2 M FDD | X |
| 1 | 0 | 1 | X | 1.4M FDD |
| 1 | 1 | X | X | X |

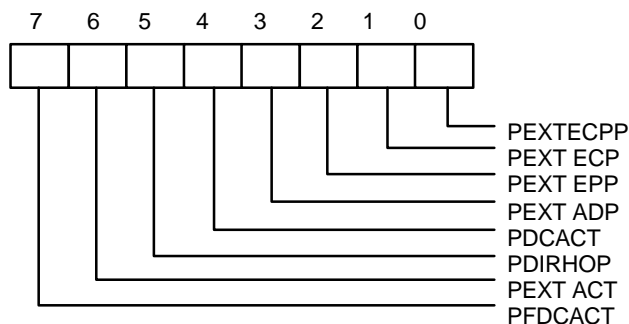
Bit 4: Reserved.

CHIP ID 3, CHIP ID 2, CHIP ID 1, CHIP ID 0 (Bit 3-0):

These four bits are read-only bits that contain chip identification information. The value is 9H for W83787IF during a read.

7.2.11 Configuration Register A (CRA) EFER = 89H, EFIR = 0AH

When 89H is loaded into EFER and 0AH is loaded into EFIR, the CRA register can be accessed through EFDR. The bit definitions are as follows:



Notes:

PFDCACT (Bit 7):

This bit controls whether PFDCEN (pin 41) is active high or low in portable mode.

- 0 PFDCEN is active low
- 1 PFDCEN is active high

PEXTACT (Bit 6):

This bit controls whether PEXTEN (pin 39) is active high or low in portable mode. This pin can also reflect the mode of the parallel port: EXTADP mode, EPP mode, ECP mode, or ECP/EPP mode, or any combination of these modes.

- 0 PEXTEN is active low
- 1 PEXTEN is active high

PDIRHOP (Bit 5):

This bit determines how the state of pin PDBDIR reflects (in all modes) whether the parallel port data bus is input or output.

- 0 If PDBDIR is high, the parallel port data bus direction is input (read);
if PDBDIR is low, the parallel port data bus direction is output (write)
- 1 If PDBDIR is high, the parallel port data bus direction is output (write);
if PDBDIR is low, the parallel port data bus direction is input (read)

PDCACT (Bit 4):

This bit controls whether the PDCIN pin is active high or low.

- 0 PDCIN is active low
- 1 PDCIN is active high

PEXTADP (Bit 3):

This bit controls whether the PEXTEN pin is active in EXTADP mode.

- 0 PEXTEN is not active in EXTADP mode
- 1 PEXTEN is active in EXTADP mode

PEXTEPP (Bit 2):

This bit controls whether the PEXTEN pin is active in EPP mode.

- 0 PEXTEN is not active in EPP mode
- 1 PEXTEN is active in EPP mode

PEXTECP (Bit 1):

This bit controls whether the PEXTEN pin is active in ECP mode.

- 0 PEXTEN is not active in ECP mode
- 1 PEXTEN is active in ECP mode

PEXTECPP (Bit 0):

This bit controls whether the PEXTEN pin is active in ECP/EPP mode.

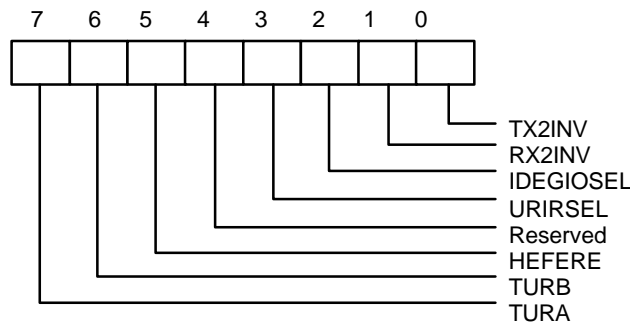
- 0 PEXTEN is not active in ECP/EPP mode
- 1 PEXTEN is active in ECP/EPP mode

7.2.12 Configuration Register B (CRB) EFER = 89H, EFIR = 0BH

This register is reserved.

7.2.13 Configuration Register C (CR0C) EFER = 89H, EFIR = 0CH (R/W)

When 89H is loaded into EFER and 0CH is loaded into EFIR, the CRC register can be accessed through EFDR. The bit definitions are as follows:



Notes:

TURA (Bit 7):

This bit is represent the clcok source of UART A.

- 0 The clock source is 1.8462MHZ (24 MHZ divide 13). Hence, the maximum baud rate of UART A is 115.2K bps. (Default)
- 1 The clock source is 24MHZ, that is, the maximum baud can be obtained 24/16 MHZ. This can be used in loopback testing or higher data transfer.

TURB (Bit 6):

This bit is the clock source of UART B described as Bit7.

HEFERE (Bit5):

This bit is EFER enable value.

- 0 The Extended Function Enable Register (EFER) enable value is set to 88H.
- 1 The Extended Function Enable Register (EFER) enable value is set to 89H.

During power-on reset, the default vaule is set by the Pin 41 (GMRD#) pulled high or low. This pin is internal pull-high.

Bit 4: Reserved

URIRSEL (Bit 3):

This bit select UART B operating in normal function or in IR function.

- 0 Select UART B as Infrared function.
- 1 Select UART B as normal function.

During power-on reset, the default value is set by Pin 92 (HURIRSEL) pulled high or low. This pin is internal pull-high.

GIOSEL (Bit 2):

This bit select IDE function or GIO function.

- 0 Select the IDE pins definition compatible to W83787IF IDE pins definition.
- 1 Select the W83787IF IDE pins definition and general purpose I/O function.

During power-on reset, the default value is set by Pin 91 (HGIOSEL) pulled high or low. This pin is pulled high internally.

RX2INV (Bit 1):

This bit is inverting or non-inverting the IR receiver data or SOUTB of UART B.

- 0 Non-inverting the SINB pin of UART B function or IRRX pin of IR function.
- 1 Inverting the SINB pin of UART B function or IRRX pin of IR function.

During the power-on reset, the default value is low.

TX2INV (Bit 0):

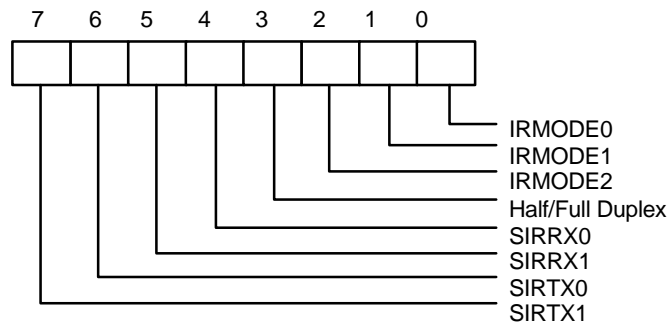
This bit is inverting or non-inverting IR transceiver data or SINB of UART B.

- 0 Non-inverting the SINB pin of UART B or IRTX pin of IR function.
- 1 Inverting the SINB pin of UART B or IRTX pin of IR function.

During the power-on reset, the default value is low.

7.2.14 Configuration Register D (CR0D) EFER = 89H, EFIR = 0DH (R/W)

When 89H is loaded into EFER and 0DH is loaded into EFIR, the CR0D register can be accessed through EFDR. The bit definitions are as follows:



Notes:

SIRTX1 SIRTX0 (Bit 7, 6):

These two bits select IRTX pin in the IR function.

- 00 or 11 IRTX2 (Pin 2, PDBDIR)
- 01 IRTX1 (Pin 43, SOUTB)
- 10 IRTX3 (Pin 95, nCS1)

During the power-on reset, the default value is 00.

SIRRX1, SIRRX0 (Bit 5, 4):

These two bits select IRRX in the IR function.

- 00 IRRX2 (Pin 3, PDCIN)
- 01 IRRX1 (Pin 42, SINB)
- 10 IRRX4 (Pin 94, nCS0)
- 11 IRRX3 (Pin 1, nRESIDE)

During the power-on reset, the default value is 00. .

Half/Full DUPLEX (Bit 3):

This bit select IR function operating in Half or Full Duplex mode.

- 0 The IR function is Full Duplex.
- 1 The IR function is Half Duplex.

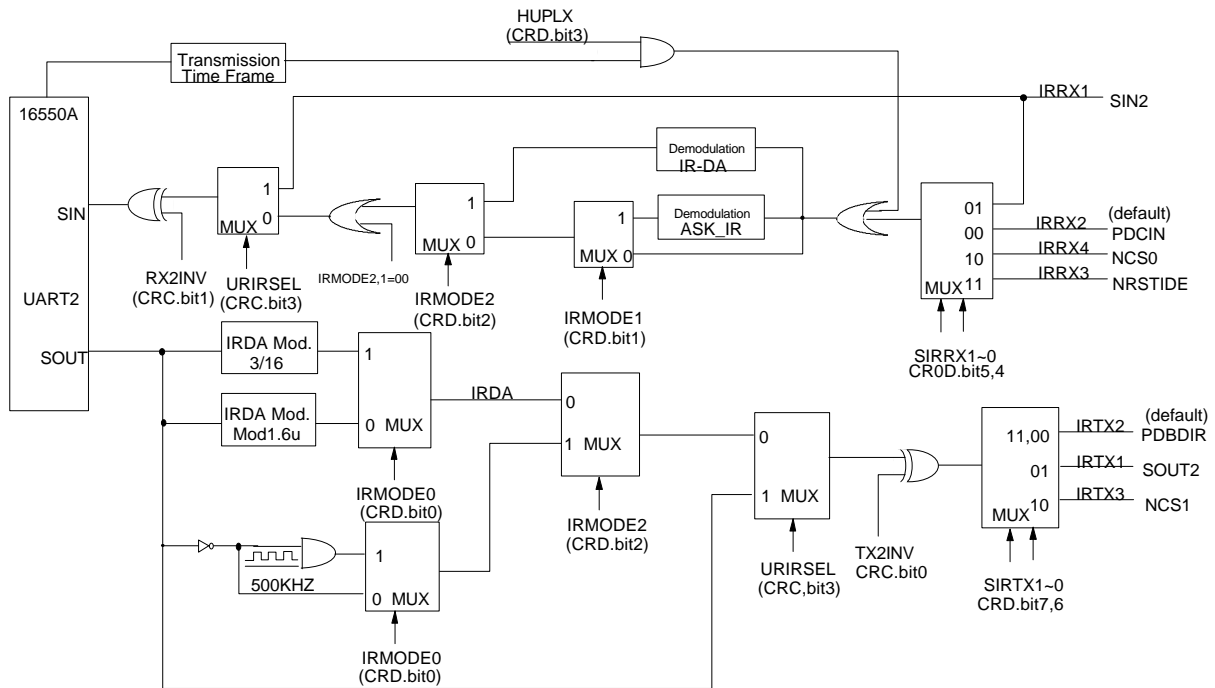
IRMODE2, IRMODE1, IRMODE0 (Bit 2, 1, 0):

These three bits select IR operation mode.

| IR MODE | IR Function | IRTX | IRRX |
|---------|-------------|-------------------------------|------------------------|
| 00X | Disable | tri-state | high |
| 010* | IrDA | Active pulse 1.6 us | Demodulation into SINB |
| 011* | IrDA | Active pulse 3/16 bit time | Demodulation into SINB |
| 100 | ASK-IR | Inverting IRTX pin | routed to SINB |
| 101 | ASK-IR | Inverting IRTX & 500KHZ clock | routed to SINB |
| 110 | ASK-IR | Inverting IRTX | Demodulation into SINB |
| 111* | ASK-IR | Inverting IRTX & 500KHZ clock | Demodulation into SINB |

Note: The notation is normal mode in the IR function.

The SIR schematic diagram controlled the register CRC and CRD is shown as follows.

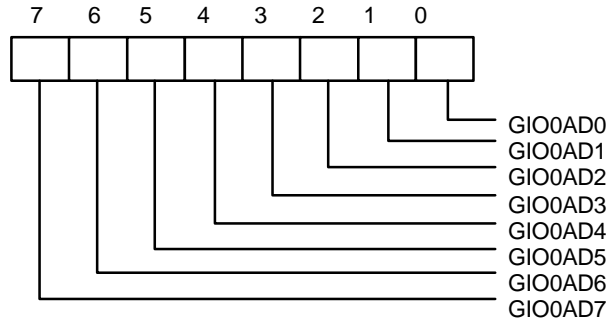


7.2.15 Configuration Register E, F (CR0E, CR0F) EFER = 89H, EFIR = 0EH, 0FH

Bit 7~ Bit 0: Reserved for testing.

7.2.16 Configuration Register 10H (CR10) EFER = 89H, EFIR = 10H (R/W)

When 89H is loaded into EFER and 10H is loaded into EFIR, the CR10 register can be accessed through EFDR. The bit definitions are as follows:



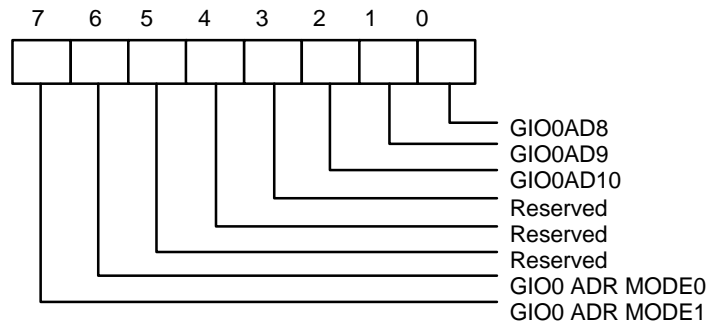
Notes:

GIO0ADR7~0 (Bit 7 ~ Bit0):

These 8 bits select GIO0 (Pin 92) address bit 7 ~ bit 0, another GIO0 address bit 10 ~ bit 8 are defined in CR11 bit 3 ~ bit 0.

7.2.17 Configuration Register 11H (CR11) EFER = 89H, EFIR = 11H (R/W)

When 89H is loaded into EFER and 11H is loaded into EFIR, the CR11 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

GIO0 ADR MODE1 ~ 0 (Bit7 ~ Bit6):

These two bits select address mode. (Defined as following table)

| GIO0 ADR MODE1 ~ 0 | Decode Mode |
|--------------------|--|
| 00 | 1 byte decode (Compare GIO0ADR10~0 with SA10~0) |
| 01 | 2 bytes decode (Compare GIO0ADR10~1 with SA10~1) |
| 10 | 4 bytes decode (Compare GIO0ADR10~2 with SA10~2) |
| 11 | 8 bytes decode (Compare GIO0ADR10~3 with SA10~3) |

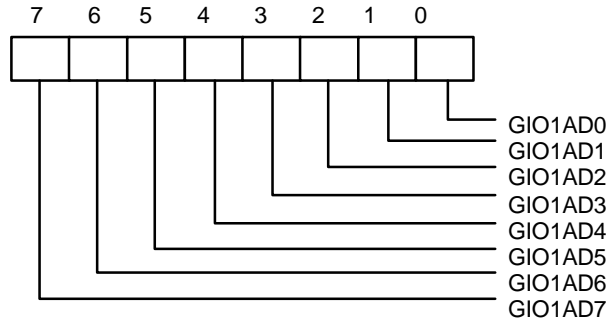
Bit 5 ~ Bit 3: Reserved.

GIO0ADR10~8 (Bit 2 ~ Bit0):

These 3 bits select GIO0 address bit 10 ~ bit 8, another GIO0 address bit 7 ~ bit 0 are defined in CR10 bit 7 ~ bit 0.

7.2.18 Configuration Register 12H (CR12) EFER = 89H, EFIR = 12H (R/W)

When 89H is loaded into EFER and 12H is loaded into EFIR, the CR12 register can be accessed through EFDR. The bit definitions are as follows:



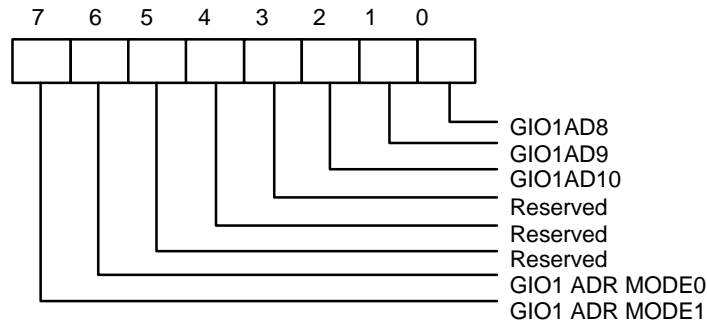
Notes:

GIO1ADR7~0 (Bit 7 ~ Bit0):

These 8 bits select GIO1 (Pin 96) address bit 7 ~ bit 0, another GIO1 address bit 10 ~ bit 8 are defined in CR13 bit 3 ~ bit 0.

7.2.19 Configuration Register 13H (CR13) EFER = 89H, EFIR = 13H (R/W)

When 89H is loaded into EFER and 13H is loaded into EFIR, the CR13 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

GIO1 ADR MODE1 ~ 0 (Bit7 ~ Bit6):

These two bits select address mode. (Defined as following table)

| GIO1 ADR MODE1 ~ 0 | Decode Mode |
|--------------------|--|
| 00 | 1 byte decode (Compare GIO1ADR10~0 with SA10~0) |
| 01 | 2 bytes decode (Compare GIO1ADR10~1 with SA10~1) |
| 10 | 4 bytes decode (Compare GIO1ADR10~2 with SA10~2) |
| 11 | 8 bytes decode (Compare GIO1ADR10~3 with SA10~3) |

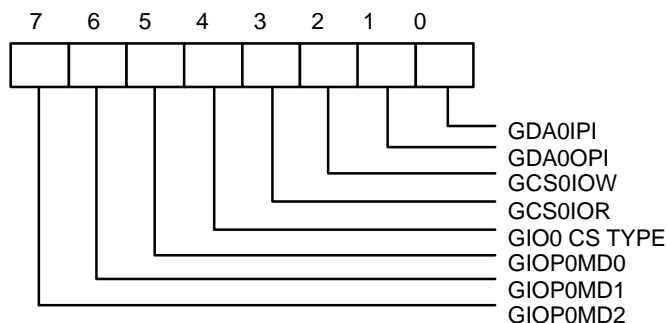
Bit 5 ~ Bit 3: Reserved.

GIO1ADR10~8 (Bit 2 ~ Bit0):

These 3 bits select GIO1 address bit 10 ~ bit 8, another GIO1 address bit 7 ~ bit 0 are defined in CR12 bit 7 ~ bit 0.

7.2.20 Configuration Register 14H (CR14) EFER = 89H, EFIR = 14H (R/W)

When 89H is loaded into EFER and 14H is loaded into EFIR, the CR14 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

GIOP0MD2~0 (Bit 7 ~ Bit 5):

These three bits define GIO0 pin mode, that is either Chip-Select or Data Port, as shown in following table.

| GIOP0M D2 | GIOP0MD1~0 | GIOP0 Pin Mode |
|-----------|------------|--|
| 0 | 00 | Inactive (tri-state) |
| 0 | 01 | Data output port (SD0 → GIOP0). When (AEN=L) & ($\overline{\text{IOR}}=L$) & (SA10~0=GPIOAD10~0), the value of SD0 will present at GIOP0 |
| 0 | 10 | Data input port (SD0 ← GIOP0). When (AEN=L) & ($\overline{\text{IOR}}=L$) & (SA10~0=GPIOAD10~0), the value of GIOP0 will present at SD0 |
| 0 | 11 | Data I/O port (SD0 ↔ GIOP0). 1. When (AEN=L) & ($\overline{\text{IOW}}=L$) & (SA10~0=GPIOAD10~0), the value of SD0 will present at GIOP0, or when (AEN=L) & ($\overline{\text{IOR}}=L$) & (SA10~0=GPIOAD10~0), the value of GIOP0 will present at SD0 |
| 1 | XX | Chip Select Pin. <ul style="list-style-type: none"> When (AEN=L) & ($\overline{\text{IOW}}=L$ or $\overline{\text{IOR}}=L$) & (SA10~0=GPIOAD10~0), the pin will be activated. The active level is defined in CR14.bit4 and the IORN or IOWN are defined in CR14.bit3~2. |

GPIO CS TYPE (Bit 4):

This bit define the pin active state when GPIO0 acts as Chip Select pin.

- 0 Active LOW when (AEN=L) & (IOWN=L or IORN=L) & (SA10~0=GPIOAD10~0).
- 1 Active HIGH when (AEN=L) & (IOWN=L or IORN=L) & (SA10~0=GPIOAD10~0).

GCS0IOR, GCS0IOW (Bit 3, Bit2):

These two bits define GPIO0 Chip Select Active Mode, that is in IORL, or IOWL, or IOR/WN, as shown in the following table.

| GCS0IOR | GCS0IOW | Chip Select Pin Type |
|---------|---------|--|
| 0 | 0 | The GIOPO functions as a Chip select pin, and will active when (AEN=L) & (SA10~0 = GIOAD10~0) |
| 0 | 1 | The GIOPO functions as a Chip select pin, and will active when (AEN=L) & (SA10~0 = GIOAD10~0) & (IOW =L) |
| 1 | 0 | The GIOPO functions as a Chip select pin, and will active when (AEN=L) & (SA10~0 = GIOAD10~0) & (IOR =L) |
| 1 | 1 | The GIOPO functions as a Chip select pin, and will active when (AEN=L) & (SA10~0 = GIOAD10~0) & (IOR =L or IOW =L) |

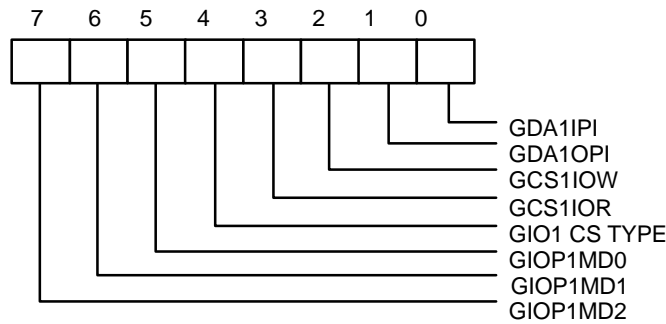
GDA0OPI, FDA0IPI (Bit 1, Bit0):

These two bits define GIOPO Data Pin type as shown in the following table.

| GDA0OPI | GDA0IPI | GIOPO Data Pin Type |
|---------|---------|---|
| 0 | 0 | The GIO0 function as a data pin, and GIOPO → SD0, SD0 → GIOPO |
| 0 | 1 | The GIO0 function as a data pin, and inverse GIOPO → SD0, SD0 → GIOPO |
| 1 | 0 | The GIO0 function as a data pin, and GIOPO → SD0, inverse SD0 → GIOPO |
| 1 | 1 | The GIO0 function as a data pin, and inverse GIOPO → SD0, inverse SD0 → GIOPO |

7.2.21 Configuration Register 15H (CR15) EFER = 89H, EFIR = 15H (R/W)

When 89H is loaded into EFER and 15H is loaded into EFIR, the CR15 register can be accessed through EFDR. The bit definitions are as follows:



Notes:

GIOP1MD2~0 (Bit 7 ~ Bit 5):

These three bits define GIOP1 pin mode, that is either Chip-Select or Data Port, as shown in following table.

| GIOP1M D2 | GIOP1MD1~0 | GIO1 Pin Mode |
|-----------|------------|---|
| 0 | 00 | Inactive (tri-state) |
| 0 | 01 | <p>Data output port (SDP0 → GIOP0).</p> <ul style="list-style-type: none"> When (AEN=L) & (\overline{IOW} =L) & (SA10~0=GIO0AD10~0), the value of SD0 will present at GIOP1 |
| 0 | 10 | <p>Data input port (SD0 ← GIOP0).</p> <ul style="list-style-type: none"> When (AEN=L) & (\overline{IOR} =L) & (SA10~0=GIO0AD10~0), the value of GIOP1 will present at SD0 |
| 0 | 11 | <p>Data I/O port (SD0 ↔ GIOP0).</p> <ol style="list-style-type: none"> When (AEN=L) & (\overline{IOW} =L) & (SA10~0=GIO0AD10~0), the value of SD0 will present at GIOP1, or when (AEN=L)&(\overline{IOR} =L) &(SA10~0=GIO0AD10~0), the value of GIOP1 will present at SD0 |
| 1 | XX | <p>Chip Select Pin.</p> <ul style="list-style-type: none"> When (AEN=L) & (\overline{IOW} =L or \overline{IOR} =L) & (SA10~0=GIO0AD10~0), the pin will be activated. The active level is defined in CR15.bit4 and the IORN or IOWN are defined in CR15.bit3~2. |

GIO1 CS TYPE (Bit 4):

This bit define the pin active state when GIOP1 acts as Chip Select pin.

- 0 Active LOW when (AEN=L) & (\overline{IOW} =L or \overline{IOR} =L) & (SA10~0=GIO0AD10~0).
- 1 Active HIGH when (AEN=L) & (\overline{IOW} =L or \overline{IOR} =L) & (SA10~0=GIO0AD10~0).

GCS1IOR, GCS1IOW (Bit 3, Bit2):

These two bits define GIO1 Chip Select Active Mode, that is in \overline{IOR} , or \overline{IOW} , or $\overline{IOR}/\overline{IOW}$, as shown in the following table.

| GCS1IOR | GCS1IOW | Chip Select Pin Type |
|---------|---------|--|
| 0 | 0 | The GIOP1 function as a Chip select pin, and will active when (AEN=L) & (SA10~0 = GIOAD10~0) |
| 0 | 1 | The GIOP1 function as a Chip select pin, and will active when (AEN=L) & (SA10~0 = GIOAD10~0) & (\overline{IOW} =L) |
| 1 | 0 | The GIOP1 function as a Chip select pin, and will active when (AEN=L) & (SA10~0 = GIOAD10~0) & (\overline{IOR} =L) |
| 1 | 1 | The GIOP1 function as a Chip select pin, and will active when (AEN=L) & (SA10~0 = GIOAD10~0) & (\overline{IOR} =L or \overline{IOW} =L) |

GDA1OPI, FDA1IPI (Bit 1, Bit0):

These two bits define GIO1 Data Pin type as shown in the following table.

| GDA1OPI | GDA1IPI | GIOP1 Data Pin Type |
|---------|---------|--|
| 0 | 0 | The GIOP1 functions as a data pin, and $GIOP1 \rightarrow SD1$, $SD1 \rightarrow GIOP1$ |
| 0 | 1 | The GIOP1 functions as a data pin, and inverse $GIOP1 \rightarrow SD1$, $SD1 \rightarrow GIOP1$ |
| 1 | 0 | The GIOP1 functions as a data pin, and $GIOP1 \rightarrow SD1$, inverse $SD1 \rightarrow GIOP1$ |
| 1 | 1 | The GIOP1 functions as a data pin, and inverse $GIOP1 \rightarrow SD1$, inverse $SD1 \rightarrow GIOP1$ |

7.2.12 Bit Map Configuration Registers

Table 7-6

| Reg. | Power-on Reset Value (D7-D0) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------------------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| CR0 | sss1 ss00 | IDEEN | HADSEL | FDCEN | FADSEL | PRTMODS1 | PRTMODS0 | APD | IPD |
| CR1 | 00ss ssss | ABCHG | 0 | PRTAS1 | PRTAS0 | URBS1 | URAS1 | URBS0 | URAS0 |
| CR2 | 0000 0000 | RA9 | RA8 | RA7 | RA6 | RA5 | RA4 | RA3 | CEA |
| CR3 | 0011 0000 | PRTBEN | GMENL | EPPVER | GMODS | URAS2 | URBS2 | SUAMIDI | SUBMIDI |
| CR4 | 0000 0000 | PRTPWD | GMPWD | URAPWD | URBPWD | PRTRRI | GMTRI | URATRI | URBTRI |
| CR5 | 0000 0000 | 0 | 0 | 0 | 0 | ECPTHR3 | ECPTHR2 | ECPTHR1 | ECPTHR0 |
| CR6 | 0000 0000 | 0 | OSCS2 | SEL4FDD | FPURDWN | FDCPWD | IDEPWD | FDCTRI | IDETRI |
| CR7 | 0000 0000 | FDD D T1 | FDD D T0 | FDD C T1 | FDD C T0 | FDD B T1 | FDD B T0 | FDD A T1 | FDD A T0 |
| CR8 | 0000 0000 | APDTMS1 | APDTMS0 | DISFDDWR | SWWP | MEDIA 1 | MEDIA 0 | BOOT 1 | BOOT 0 |
| CR9 | s000 1001 | PRTMODS2 | LOCKREG | EN3MODE | 0 | CHIP ID 3 | CHIP ID 2 | CHIP ID 1 | CHIP ID 0 |
| CRA | 0001 1111 | PFDCACT | PEXTACT | PDRHSOP | PDCHACT | PEXTADP | PEXTEPP | PEXTECP | PEXTECP |
| CRB | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CRC | 00s0 ss00 | TURA | TURB | HEFERE | 0 | URIRSEL | G0SEL | RX2INV | TX2INV |
| CRD | 0000 0011 | SIRTX1 | SIRTX0 | SIRRX1 | SIRRX0 | H DUPLX | IRMODE2 | IRMODE1 | IRMODE0 |
| CR10 | 0000 0000 | GIO0AD7 | GIO0AD6 | GIO0AD5 | GIO0AD4 | GIO0AD3 | GIO0AD2 | GIO0AD1 | GIO0AD0 |
| CR11 | 0000 0000 | G0CADM1 | G0CADM0 | 0 | 0 | 0 | GIO0AD10 | GIO0AD9 | GIO0AD8 |
| CR12 | 0000 0000 | GIO1AD7 | GIO1AD6 | GIO1AD5 | GIO1AD4 | GIO1AD3 | GIO1AD2 | GIO1AD1 | GIO1AD0 |
| CR13 | 0000 0000 | G1CADM1 | G1CADM0 | 0 | 0 | 0 | GIO1AD10 | GIO1AD9 | GIO1AD8 |
| CR14 | 0000 0000 | GIOP0MD2 | GIOP0MD1 | GIOP0MD0 | GIO0CSH | GCS0IOR | GCS0IOW | GDA0OPI | GDA0IPI |
| CR15 | 0000 0000 | GIOP1MD2 | GIOP1MD1 | GIOP1MD0 | GIO1CSH | GCS1IOR | GCS1IOW | GDA1OPI | GDA1IPI |

Notes:

- 's' means dependent on power-on setting of pin.

8.0 SPECIFICATIONS
8.1 ABSOLUTE MAXIMUM RATINGS

| | |
|----------------------------|---|
| Power Supply Voltage..... | -0.3 to 7.0V |
| Input Voltage..... | V _{SS} -0.3 to V _{DD} +0.3V |
| Operating Temperature..... | 0° C to+70° C |
| Storage Temperature..... | -55° C to+150° C |

8.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, VDD = 5V ± 5%, VSS = 0V)

| PARAMETER | SYM. | MIN. | MAX. | UNIT | CONDITIONS |
|--|------|------|---------|------|---|
| Input Low Voltage | VIL | -0.3 | 0.8 | V | |
| Input High Voltage | VIH | 2.0 | VDD+0.3 | V | |
| Input Leakage Current | ILIH | | +10 | μS | VIN = VDD |
| Input Leakage Current | ILIL | | -10 | μS | VIN = 0V |
| HOST INTERFACE PINS | | | | | |
| Output Low Voltage | VOL | | 0.4 | V | IO _L = 12 mA (D0-D7) 4 mA (other pins) |
| Input High Voltage | VOH | 2.4 | VDD | V | IO _H = -12 mA (D0-D7) 4 mA (other pins) |
| Leakage Current | ILOB | | 10 | μS | VIN = VDD |
| Leakage Current | ILOB | | -10 | μS | VIN = 0V |
| DISK INTERFACE INPUT (\overline{WP} , \overline{INDEX} , $\overline{TRK0}$, \overline{RDATA} , \overline{DSKCHG} , $\overline{WP2}$, $\overline{IDX2}$, $\overline{TRAK02}$, $\overline{RDD2}$, $\overline{DCH2}$) | | | | | |
| Input Hysteresis | VH | 0.25 | | V | |
| DISK INTERFACE OUTPUTS (\overline{MOA} , \overline{MOB} , \overline{DSA} , \overline{DSB} , \overline{RWC} , \overline{DIR} , \overline{STEP} , \overline{WE} , \overline{WD} , \overline{HEAD} , $\overline{MOB2}$, $\overline{DSB2}$, $\overline{RWC2}$, $\overline{DIR2}$, \overline{STEP} , $\overline{WE2}$, $\overline{WD2}$, $\overline{HEAD2}$) | | | | | |
| Output Low Voltage | VOLD | | 0.4 | V | IO _L = 24 mA |
| Leakage Current | ILOH | | 10 | μS | VOUT = VDD |
| IDE INTERFACE OUTPUT ($\overline{CS0-1}$, \overline{DBENH} , \overline{DBENL} , \overline{RESIDE} , $\overline{IDED7}$) | | | | | |
| Output Low Voltage | VOLD | | 0.4 | V | IO _L = 4 mA |
| Leakage Current | ILOH | | 10 | μS | VOUT = VDD |
| Leakage Current | ILOH | | -10 | μS | |
| UART, PARALLEL INTERFACE | | | | | |
| Output Voltage | VOL | | 0.4 | V | IO _L = 4 mA on all outputs |
| | VOH | 2.4 | VDD | V | IO _H = -4 mA on all outputs |
| EXTENSION ADAPTER INTERFACE | | | | | |
| Output Low Voltage | VOL | | 0.4 | V | IO _L = 12 mA |
| Output High Voltage | VOHB | 2.4 | VDD | V | IO _H = -12 mA |
| VDD Supply Current | IDD | | 20 | mA | |

8.3 AC Characteristics
8.3.1 FDC: Data rate = 500Kb/300Kb/250Kb/sec

| PARAMETER | SYM. | MIN. | TYP. (NOTE 1) | MAX. | UNIT | TEST CONDITIONS |
|--|------|-----------------|------------------|-----------------|---------|--------------------|
| SA9-SA0, AEN, \overline{DACK} , \overline{CS} , setup time to $\overline{IOR} \downarrow \hat{0}$ | TAR | 25 | | | nS | |
| SA9-SA0, AEN, \overline{DACK} , hold time for $\overline{IOR} \downarrow \hat{0}$ | TAR | 0 | | | nS | |
| \overline{IOR} width | TRR | 80 | | | nS | |
| Data access time from $\overline{IOR} \downarrow \hat{0}$ | TFD | | | 80 | nS | CL = 100 pf |
| Data hold from $\overline{IOR} \downarrow \hat{0}$ | TDH | 10 | | | nS | CL = 100 pf |
| SD to from $\overline{IOR} \downarrow \hat{0}$ | TDF | 10 | | 50 | nS | CL = 100 pf |
| IRQ delay from $\overline{IOR} \downarrow \hat{0}$ | TRI | | | 360/570 /675 | nS | |
| SA9-SA0, AEN, \overline{DACK} , setup time to $\overline{IOW} \downarrow \hat{0}$ | TAW | 25 | | | nS | |
| SA9-SA0, AEN, \overline{DACK} , hold time for $\overline{IOW} \downarrow \hat{0}$ | TWA | 0 | | | nS | |
| \overline{IOW} width | TWW | 60 | | | nS | |
| Data setup time to $\overline{IOW} \downarrow \hat{0}$ | TDW | 60 | | | nS | |
| Data hold time from $\overline{IOW} \downarrow \hat{0}$ | TWD | 0 | | | nS | |
| IRQ delay from $\overline{IOW} \downarrow \hat{0}$ | TWI | | | 360/570 /675 | nS | |
| DRQ cycle time | TMCY | 27 | | | μ S | |
| DRQ delay time $\overline{DACK} \downarrow \hat{0}$ | TAM | | | 50 | nS | |
| DRQ to \overline{DACK} delay | TMA | 0 | | | nS | |
| \overline{DACK} width | TAA | 260/430 /510 | | | nS | |
| \overline{IOR} delay from \overline{DRQ} | TMR | 0 | | | nS | |
| \overline{IOW} delay from \overline{DRQ} | TMW | 0 | | | nS | |

8.3 AC Characteristics, FDC continued

| PARAMETER | SYM. | MIN. | TYP. (NOTE 1) | MAX. | UNIT | TEST CONDITION S |
|---|------|-------------------|------------------|-------------------|---------------|------------------------|
| $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ response time from DRQ | TMRW | | 6/12 /20/24 | | μS | |
| TC width | TTC | 135/220 /260 | | | nS | |
| RESET width | TRST | 1.8/3/3.5 | | | μS | |
| $\overline{\text{INDEX}}$ width | TIDX | 0.5/0.9 /1.0 | | | μS | |
| $\overline{\text{DIR}}$ setup time to $\overline{\text{STEP}}$ | TDST | 1.0/1.6 /2.0 | | | μS | |
| $\overline{\text{DIR}}$ hold time from $\overline{\text{STEP}}$ | TSTD | 24/40/48 | | | μS | |
| $\overline{\text{STEP}}$ pulse width | TSTP | 6.8/11.5 /13.8 | 7/11.7 /14 | 7.2/11.9 /14.2 | μS | |
| $\overline{\text{STEP}}$ cycle width | TSC | Note 2 | Note 2 | Note 2 | μS | |
| $\overline{\text{WD}}$ pulse width | TWDD | 100/185 /225 | 125/210 /250 | 150/235 /275 | μS | |
| Write precompensation | TWPC | 100/138 /225 | 125/210 /250 | 150/235 /275 | μS | |

Notes:

1. Typical values for T = 25° C and normal supply voltage.
2. Programmable from 2 mS through 32 mS in 2 mS increments.

8.3.2 IDE

| PARAMETER | SYMBOL | MAX. | UNIT |
|---|--------|------|------|
| $\overline{\text{CS0}}$, $\overline{\text{CS1}}$ delay from SA valid | T1 | 50 | nS |
| DBENL, DBENH delay from AEN, IOCS16, SA | T2 | 50 | nS |
| IDED7 to D7 delay (read cycle) | T4 | 50 | nS |
| D7 to IDED7 delay (write cycle) | T3 | 50 | nS |

8.3.3 UART/Parallel Port

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT | TEST CONDITIONS |
|---|--------|------|------------|---------------|-----------------|
| Delay from Stop to Set Interrupt | TSINT | 9/16 | | Baud Rate | |
| Delay from $\overline{\text{IOR}}$ Reset Interrupt | TRINT | | 1 | μS | 100pF Loading |
| Delay from Initial IRQ Reset to Transmit Start | TIRS | 1/16 | 8/16 | Baud Rate | |
| Delay from to Reset interrupt | THR | | 175 | nS | 100pF Loading |
| Delay from Initial $\overline{\text{IOW}}$ to interrupt | TSI | 9/16 | 16/16 | Baud Rate | |
| Delay from Stop to Set Interrupt | TSTI | | 1/2 | Baud Rate | |
| Delay from $\overline{\text{IOR}}$ to Reset Interrupt | TIR | | 250 | nS | 100pF Loading |
| Delay from $\overline{\text{IOR}}$ to Output | TMWO | | 200 | nS | 100pF Loading |
| Set Interrupt Delay from Modem Input | TSIM | | 250 | nS | |
| Reset Interrupt Delay from $\overline{\text{IOR}}$ | TRIM | | 250 | nS | |
| Interrupt Active Delay | TIAD | | 25 | nS | 100pF Loading |
| Interrupt Inactive Delay | TIID | | 30 | nS | 100pF Loading |
| Baud Divisor | N | | $2^{16}-1$ | | 100pF Loading |

8.3.4 Extension Adapter Mode

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|--|------|------|------|------|------|-----------------|
| $\overline{\text{XRD}}$, $\overline{\text{XWR}}$ Delay from $\overline{\text{IOR}}$, $\overline{\text{IOW}}$ | tx1 | | | 50 | nS | |
| $\text{XA}<0:2>$ Delay from $\text{SA}<0:2>$ | tx2 | | | 50 | nS | |
| $\text{XD}<0:7>$ Setup time | tx3 | 50 | | | nS | |
| $\text{XD}<0:7>$ Hold time | tx4 | 0 | | | nS | |
| IRQ & Delay from XIRQ | tx5 | | | 50 | nS | |
| DRQX Delay from XDRQ | tx6 | | | 50 | nS | |
| $\overline{\text{XDACK}}$ Delay from $\overline{\text{DACKX}}$ | tx7 | | | 50 | nS | |
| XTC Delay from TC | tx8 | | | 50 | nS | |

8.3.5 Parallel Port Mode Parameters

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT |
|---|------|------|------|------|------|
| PD0-7, INDEX, STROBE, AUTOFD Delay from IOW | t1 | | | 100 | nS |
| IRQ Delay from ACK, nFAULT | t2 | | | 60 | nS |
| IRQ Delay from IOW | t3 | | | 105 | nS |
| IRQ Active Low in ECP and EPP Modes | t4 | 200 | | 300 | nS |
| ERROR Active to IRQ Active | t5 | | | 105 | nS |

8.3.6 EPP Data or Address Read Cycle Timing Parameters

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---------------------------------------|------|------|------|------|
| Ax Valid to IOR Asserted | t1 | 40 | | nS |
| IOCHRDY Deasserted to IOR Deasserted | t2 | 0 | | nS |
| IOR Deasserted to Ax Valid | t3 | 10 | 10 | nS |
| IOR Deasserted to IOW or IOR Asserted | t4 | 40 | | |
| IOR Asserted to IOCHRDY Asserted | t5 | 0 | 24 | nS |
| PD Valid to SD Valid | t6 | 0 | 75 | nS |
| IOR Deasserted to SD Hi-Z (Hold Time) | t7 | 0 | 40 | μS |
| SD Valid to IOCHRDY Deasserted | t8 | 0 | 85 | nS |
| WAIT Deasserted to IOCHRDY Deasserted | t9 | 60 | 160 | nS |
| PD Hi-Z to PDBIR Set | t10 | 0 | | nS |
| WRITE Deasserted to IOR Asserted | t13 | 0 | | nS |
| WAIT Asserted to WRITE Deasserted | t14 | 0 | 185 | nS |
| WAIT Deasserted to WRITE Modified | t15 | 60 | 190 | nS |
| IOR Asserted to PD Hi-Z | t16 | 0 | 50 | nS |
| WAIT Asserted to PD Hi-Z | t17 | 60 | 180 | nS |
| Command Asserted to PD Valid | t18 | 0 | | nS |
| Command Deasserted to PD Hi-Z | t19 | 0 | | nS |
| WAIT Deasserted to PD Drive | t20 | 60 | 190 | nS |
| WRITE Deasserted to Command | t21 | 1 | | nS |

8.3.6 EPP Data or Address Read Cycle Timing Parameters, continued

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---|------|------|------|---------------|
| PBDIR Set to Command | t22 | 0 | 20 | nS |
| PD Hi-Z to Command Asserted | t23 | 0 | 30 | nS |
| $\overline{\text{WAIT}}$ Asserted to Command Asserted | t24 | 0 | 195 | nS |
| $\overline{\text{WAIT}}$ Deasserted to Command Deasserted | t25 | 60 | 180 | nS |
| Time out | t26 | 10 | 12 | nS |
| PD Valid to $\overline{\text{WAIT}}$ Deasserted | t27 | 0 | | nS |
| PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted | t28 | 0 | | μS |

8.3.7 EPP Data or Address Write Cycle Timing Parameters

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---|------|------|------|---------------|
| Ax Valid to $\overline{\text{IOW}}$ Asserted | t1 | 40 | | nS |
| SD Valid to $\overline{\text{IOW}}$ Asserted | t2 | 10 | | nS |
| $\overline{\text{IOW}}$ Deasserted to Ax Invalid | t3 | 10 | | nS |
| $\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted | t4 | 0 | | nS |
| Command Asserted to $\overline{\text{WAIT}}$ Deasserted | t5 | 10 | | nS |
| $\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted | t6 | 40 | | nS |
| IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted | t7 | 0 | 24 | nS |
| $\overline{\text{WAIT}}$ Asserted to Command Asserted | t8 | 60 | 160 | nS |
| $\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted | t9 | 0 | 70 | nS |
| PBDIR Low to $\overline{\text{WRITE}}$ Asserted | t10 | 0 | | nS |
| $\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted | t11 | 60 | 185 | nS |
| $\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change | t12 | 60 | 185 | nS |
| $\overline{\text{IOW}}$ Asserted to PD Valid | t13 | 0 | 50 | nS |
| $\overline{\text{WAIT}}$ Asserted to PD Invalid | t14 | 0 | | nS |
| PD Invalid to Command Asserted | t15 | 10 | | nS |
| $\overline{\text{IOW}}$ to Command Asserted | t16 | 5 | 35 | nS |
| $\overline{\text{WAIT}}$ Asserted to Command Asserted | t17 | 60 | 210 | nS |
| $\overline{\text{WAIT}}$ Deasserted to Command Deasserted | t18 | 60 | 190 | nS |
| Command Asserted to $\overline{\text{WAIT}}$ Deasserted | t19 | 0 | 10 | μS |

8.3.7 EPP Data or Address Write Cycle Timing Parameters, continued

| PARAMETER | SYM. | MIN. | MAX. | UNIT |
|---|------|------|------|------|
| Time out | t20 | 10 | 12 | μS |
| Command Deasserted to $\overline{\text{WAIT}}$ Asserted | t21 | 0 | | nS |
| $\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid | t22 | 0 | | nS |

8.3.8 Parallel Port FIFO Timing Parameters

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---------------------------------|--------|------|------|------|
| DATA Valid to nSTROBE Active | t1 | 600 | | nS |
| nSTROBE Active Pulse Width | t2 | 600 | | nS |
| DATA Hold from nSTROBE Inactive | t3 | 450 | | nS |
| BUSY Inactive to PD Inactive | t4 | 80 | | nS |
| BUSY Inactive to nSTROBE Active | t5 | 680 | | nS |
| nSTROBE Active to BUSY Active | t6 | | 500 | nS |

8.3.9 ECP Parallel Port Forward Timing Parameters

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---------------------------------------|--------|------|------|------|
| nAUTOFD Valid to nSTROBE Asserted | t1 | 0 | 60 | nS |
| PD Valid to nSTROBE Asserted | t2 | 0 | 60 | nS |
| BUSY Deasserted to nAUTOFD Changed | t3 | 80 | 180 | nS |
| BUSY Deasserted to PD Changed | t4 | 80 | 180 | nS |
| nSTROBE Deasserted to BUSY Deasserted | t5 | 0 | | nS |
| BUSY Deasserted to nSTROBE Asserted | t6 | 80 | 200 | nS |
| nSTROBE Asserted to BUSY Asserted | t7 | 0 | | nS |
| BUSY Asserted to nSTROBE Deasserted | t8 | 80 | 180 | nS |

8.9.10 ECP Parallel Port Reverse Timing Parameters

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---------------------------------------|--------|------|------|------|
| PD Valid to nACK Asserted | t1 | 0 | | nS |
| nAUTOFD Deasserted to PD Changed | t2 | 0 | | nS |
| nAUTOFD Asserted to nACK Asserted | t3 | 0 | | nS |
| nAUTOFD Deasserted to nACK Deasserted | t4 | 0 | | nS |
| nACK Deasserted to nAUTOFD Asserted | t5 | 80 | 200 | nS |
| PD Changed to nAUTOFD Deasserted | t6 | 80 | 200 | nS |

8.9.11 IrDA Receive Timing Parameters

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|----------------------------|--------|------|------|-------|------|
| Pulse Width at 115.2k baud | T1 | 1.4 | 1.6 | 2.71 | μS |
| Pulse Width at 57600 baud | T1 | 1.4 | 3.22 | 3.69 | μS |
| Pulse Width at 38400 baud | T1 | 1.4 | 4.8 | 5.53 | μS |
| Pulse Width at 19200 baud | T1 | 1.4 | 9.7 | 11.07 | μS |
| Pulse Width at 9600 baud | T1 | 1.4 | 19.5 | 22.13 | μS |
| Pulse Width at 4800 baud | T1 | 1.4 | 39 | 44.27 | μS |
| Pulse Width at 2400 baud | T1 | 1.4 | 78 | 88.55 | μS |
| Bit Time at 115.2k baud | T2 | | 8.68 | | μS |
| Bit Time at 57600 baud | T2 | | 17.4 | | μS |
| Bit Time at 38400 baud | T2 | | 26 | | μS |
| Bit Time at 19200 baud | T2 | | 52 | | μS |
| Bit Time at 9600 baud | T2 | | 104 | | μS |
| Bit Time at 4800 baud | T2 | | 208 | | μS |
| Bit Time at 2400 baud | T2 | | 416 | | μS |

8.9.12 IrDA Transmit Timing Parameters

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|----------------------------|--------|------|------|-------|------|
| Pulse Width at 115.2k baud | T1 | 1.4 | 1.6 | 2.71 | μS |
| Pulse Width at 57600 baud | T1 | 1.4 | 3.22 | 3.69 | μS |
| Pulse Width at 38400 baud | T1 | 1.4 | 4.8 | 5.53 | μS |
| Pulse Width at 19200 baud | T1 | 1.4 | 9.7 | 11.07 | μS |
| Pulse Width at 9600 baud | T1 | 1.4 | 19.5 | 22.13 | μS |
| Pulse Width at 4800 baud | T1 | 1.4 | 39 | 44.27 | μS |
| Pulse Width at 2400 baud | T1 | 1.4 | 78 | 88.55 | μS |
| Bit Time at 115.2k baud | T2 | | 8.68 | | μS |
| Bit Time at 57600 baud | T2 | | 17.4 | | μS |
| Bit Time at 38400 baud | T2 | | 26 | | μS |
| Bit Time at 19200 baud | T2 | | 52 | | μS |
| Bit Time at 9600 baud | T2 | | 104 | | μS |
| Bit Time at 4800 baud | T2 | | 208 | | μS |
| Bit Time at 2400 baud | T2 | | 416 | | μS |

8.9.13 Amplitude Shift Keyed IR (ASK-IR) Receiver Timing Parameters

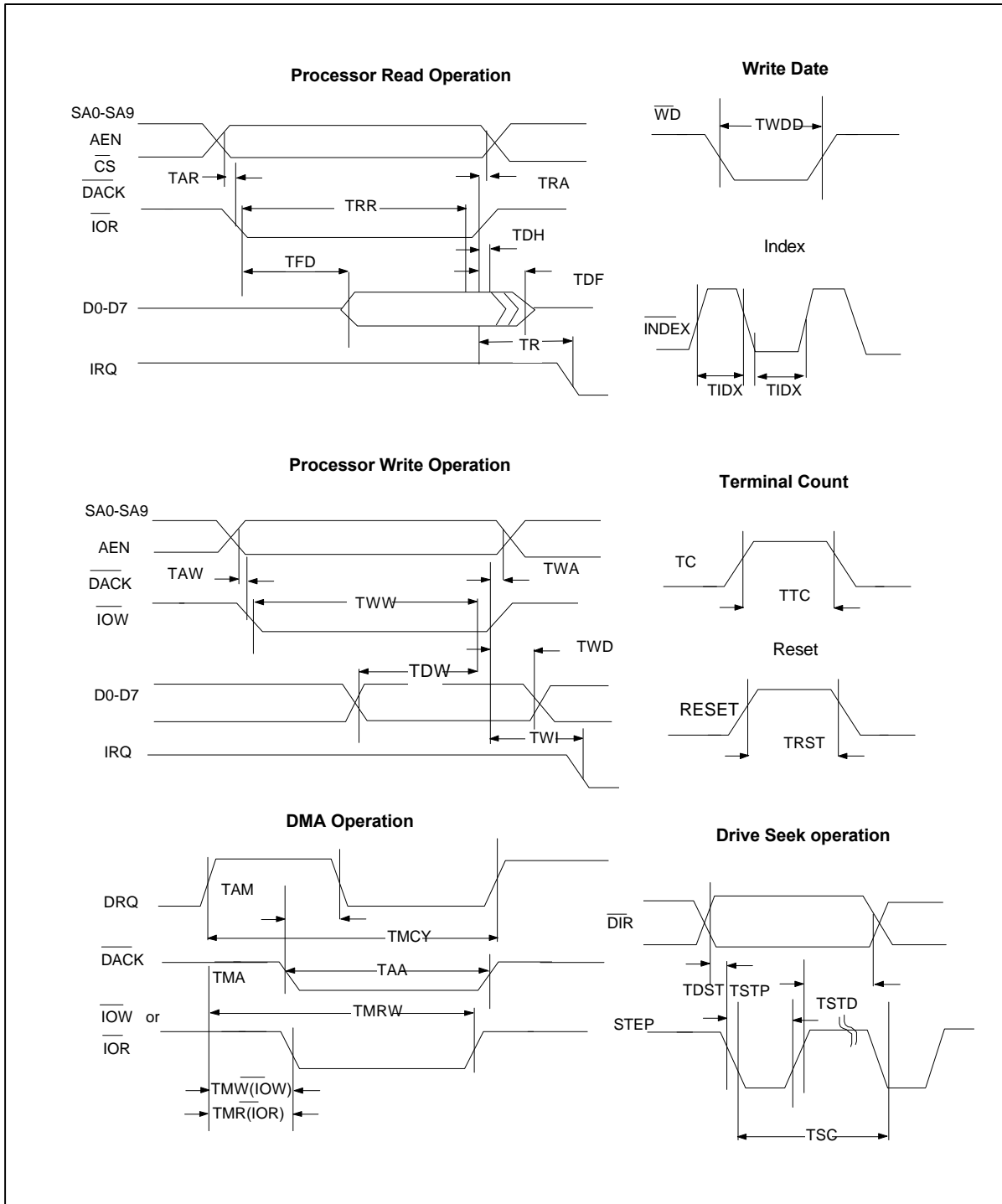
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---------------------------|--------|------|------|------|------|
| Modulated Output Bit Time | T1 | | | | μS |
| Off Bit Time | T2 | | | | μS |
| Modulated Output ON | T3 | 0.8 | 1 | 1.2 | μS |
| Modulated Output OFF | T4 | 0.8 | 1 | 1.2 | μS |
| Modulated Output ON | T5 | 0.8 | 1 | 1.2 | μS |
| Modulated Output OFF | T6 | 0.8 | 1 | 1.2 | μS |

8.9.14 Amplitude Shift Keyed IR (ASK-IR) Transmit Timing Parameters

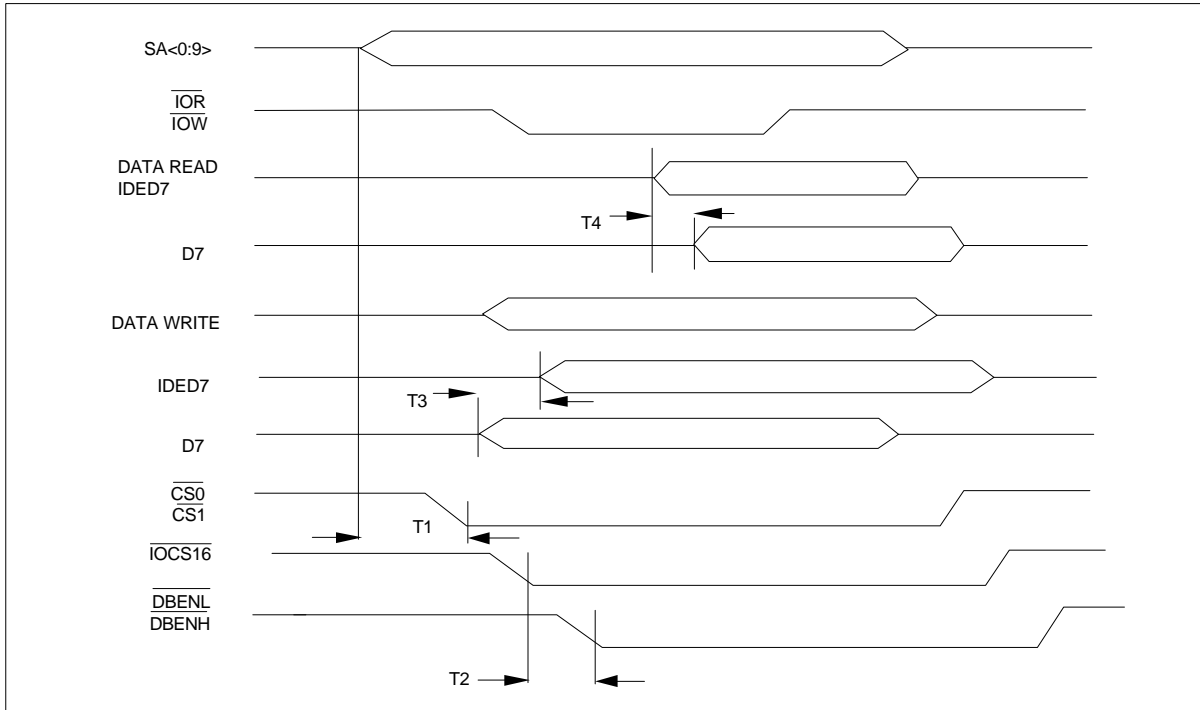
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---------------------------|--------|------|------|------|------|
| Modulated Output Bit Time | T1 | | | | μS |
| Off Bit Time | T2 | | | | μS |
| Modulated Output ON | T3 | 0.8 | 1 | 1.2 | μS |
| Modulated Output OFF | T4 | 0.8 | 1 | 1.2 | μS |
| Modulated Output ON | T5 | 0.8 | 1 | 1.2 | μS |
| Modulated Output OFF | T6 | 0.8 | 1 | 1.2 | μS |

9.0 TIMING WAVEFORMS

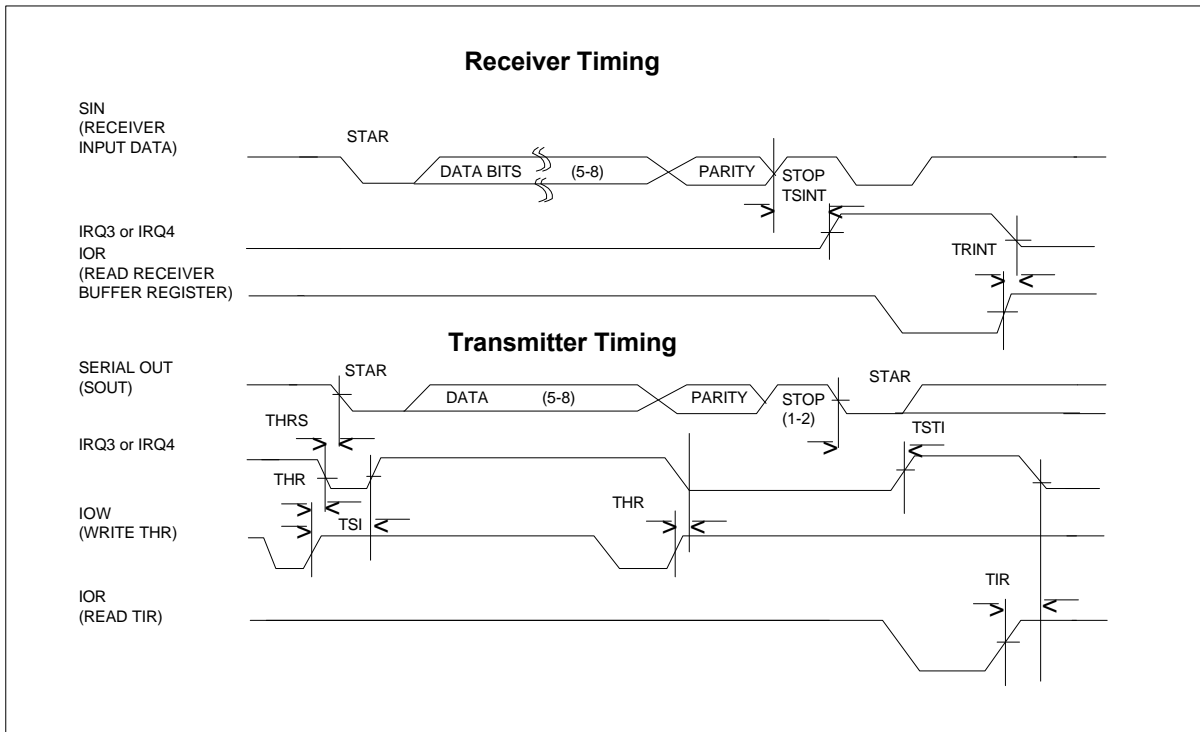
9.1 FDC



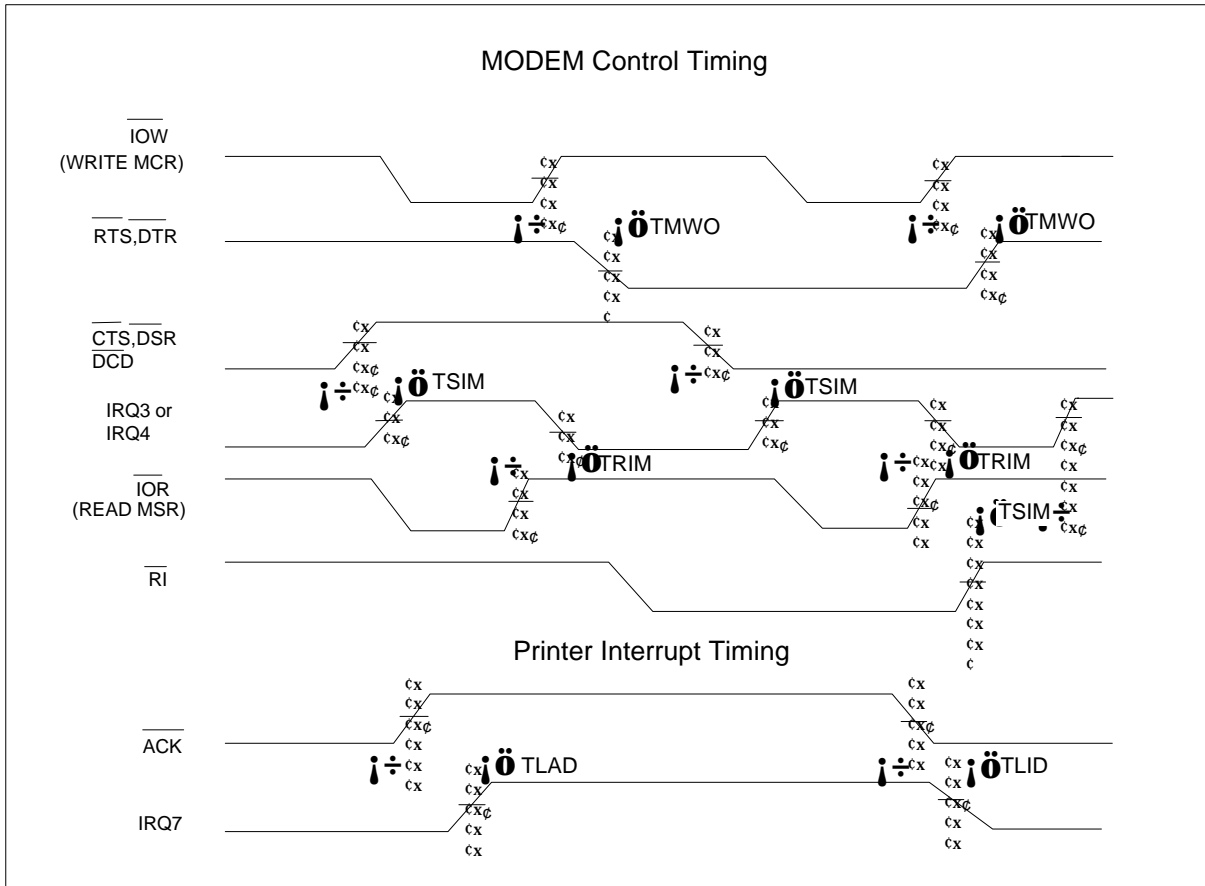
9.2 IDE



9.3 UART/Parallel

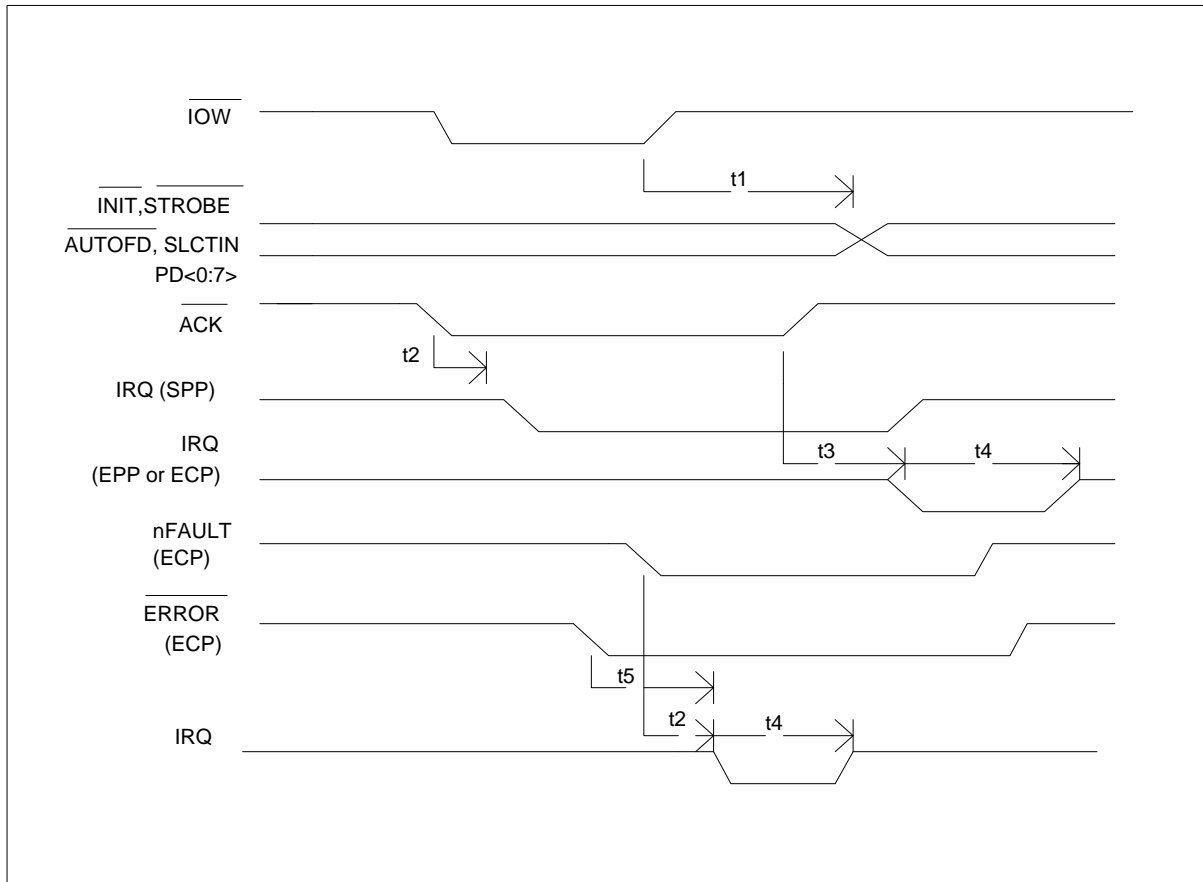


9.3.1 Modem Control Timing

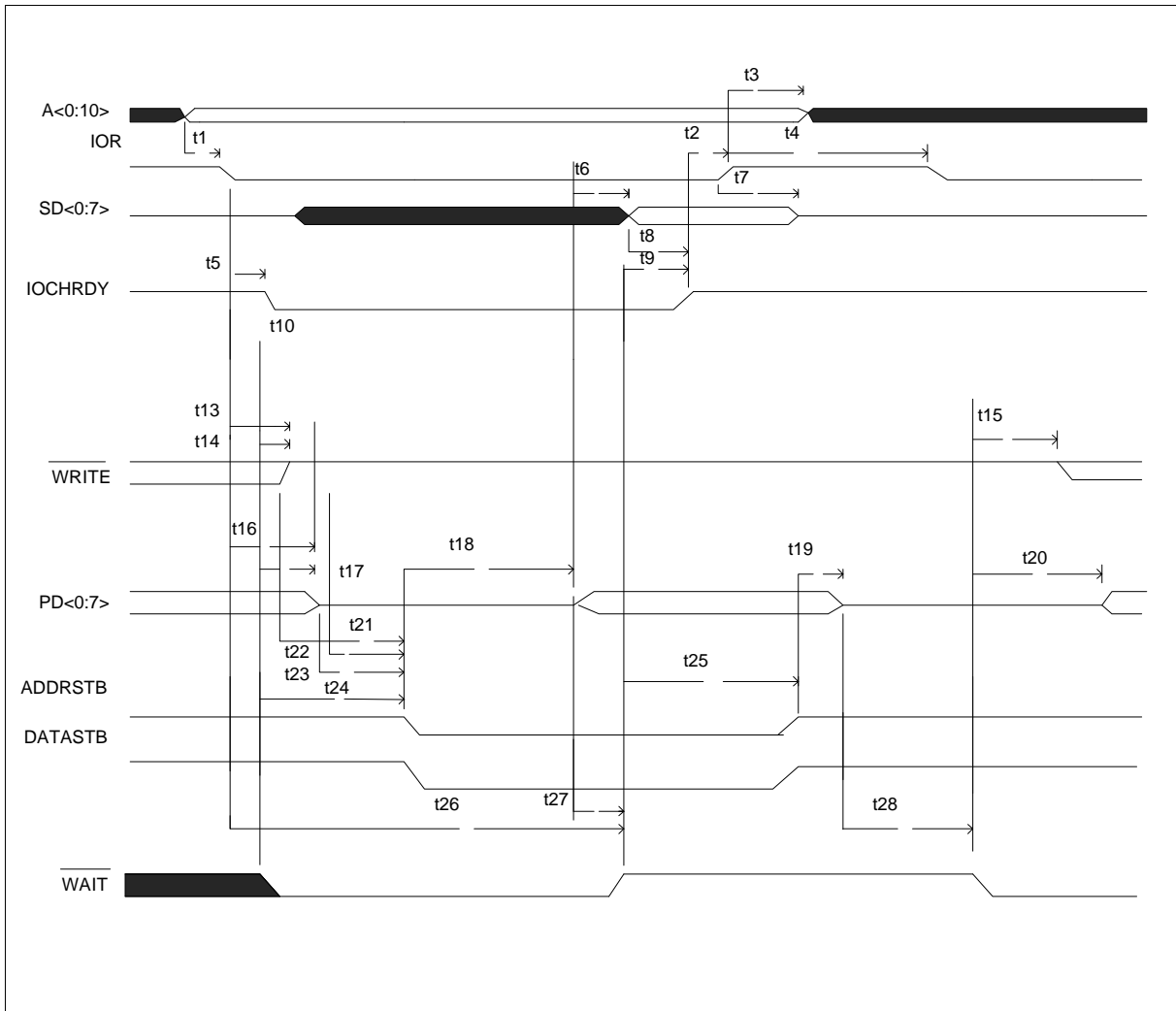


9.4 Parallel Port

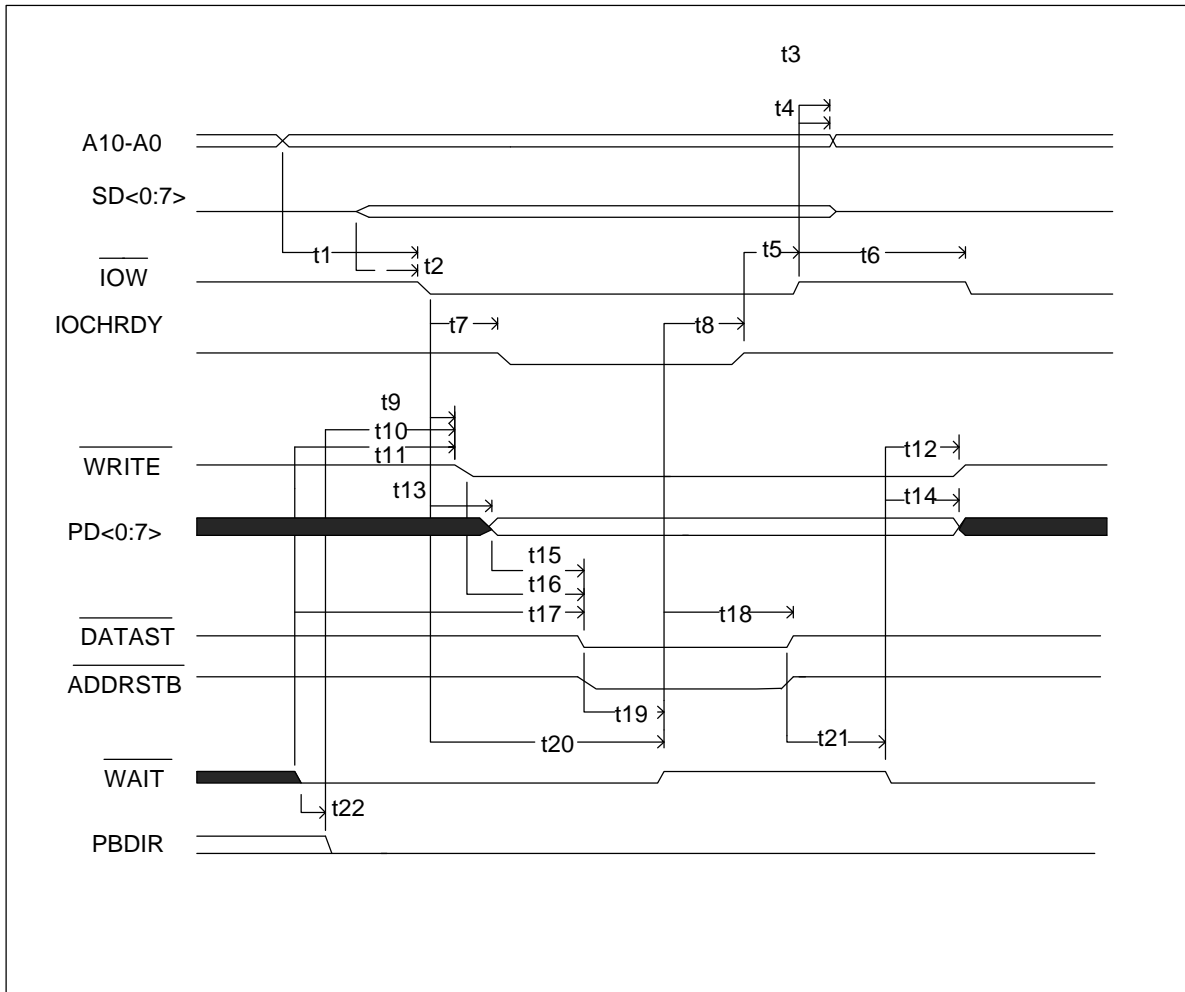
9.4.1 Parallel Port Timing



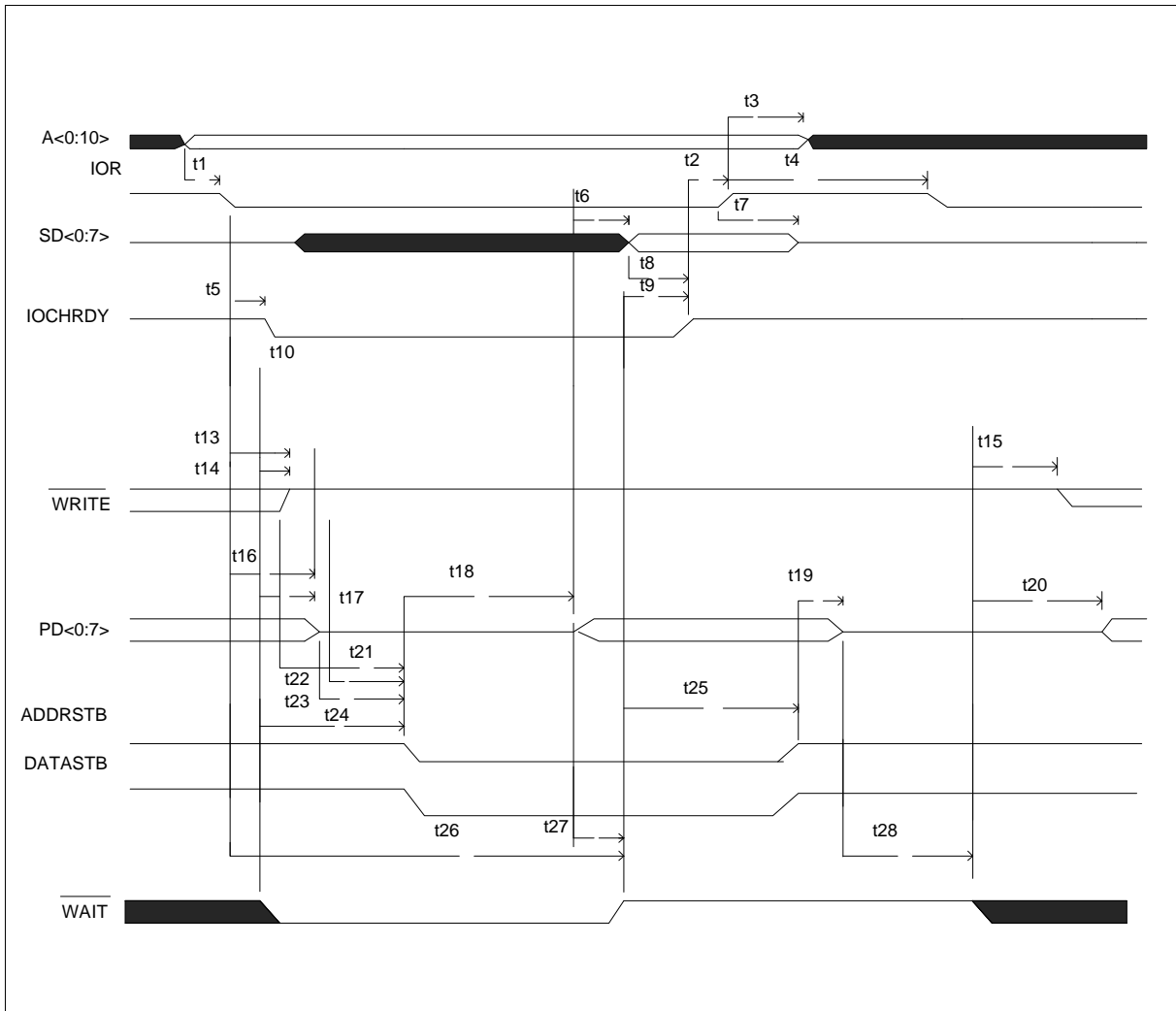
9.4.2 EPP Data or Address Read Cycle (EPP Version 1.9)



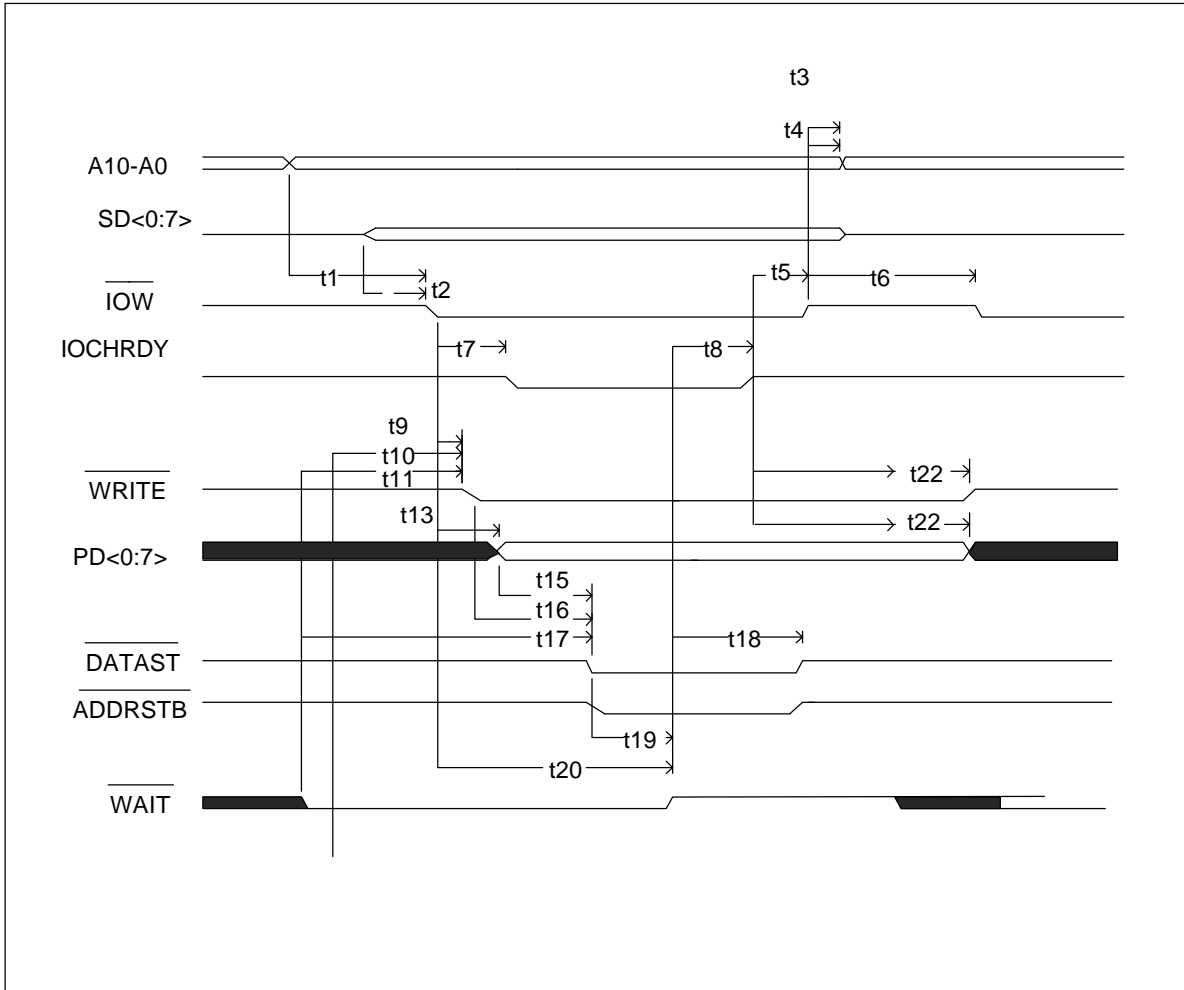
9.4.3 EPP Data or Address Write Cycle (EPP Version 1.9)



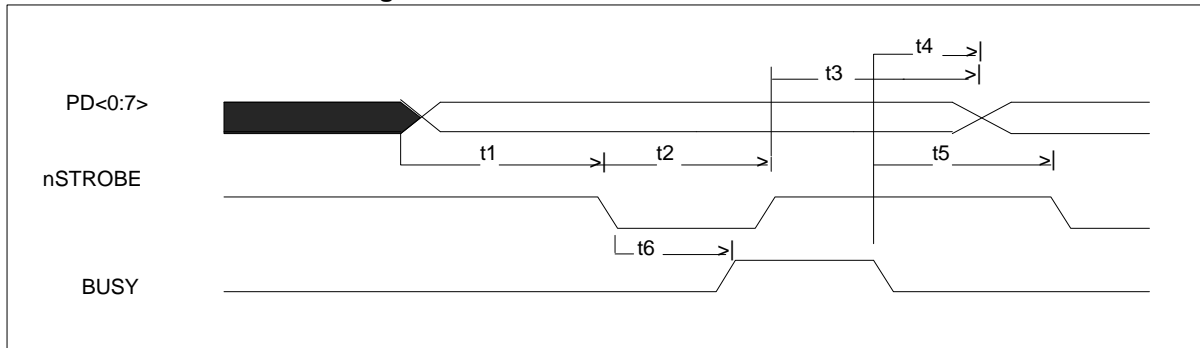
9.4.4 EPP Data or Address Read Cycle (EPP Version 1.7)



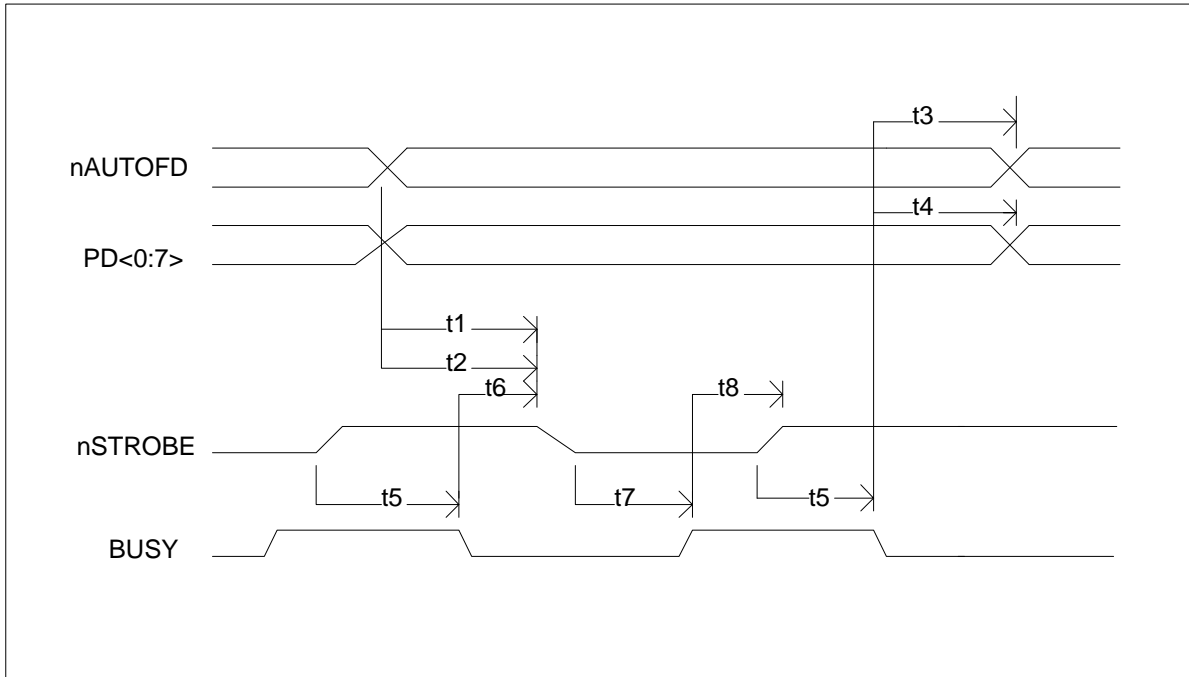
9.4.5 EPP Data or Address Write Cycle (EPP Version 1.7)



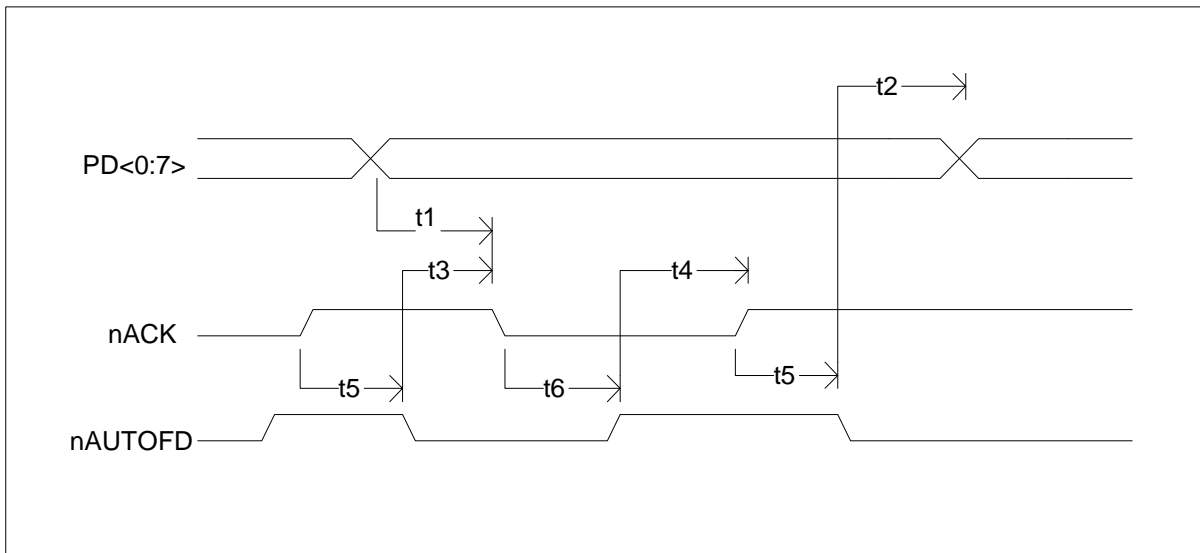
9.4.6 Parallel Port FIFO Timing



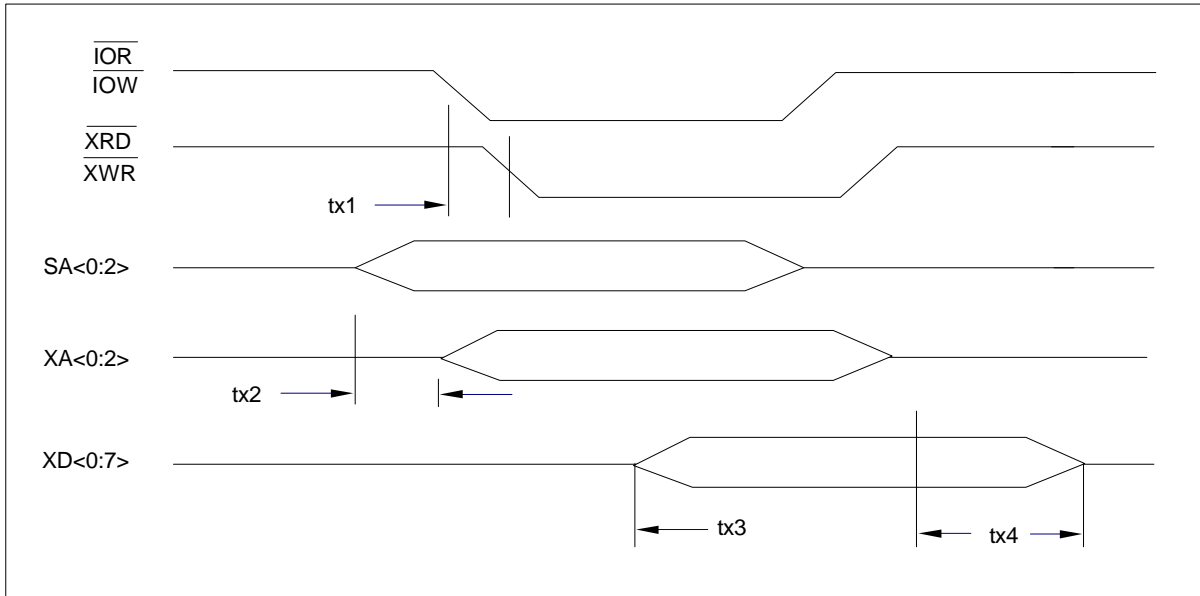
9.4.7 ECP Parallel Port Forward Timing



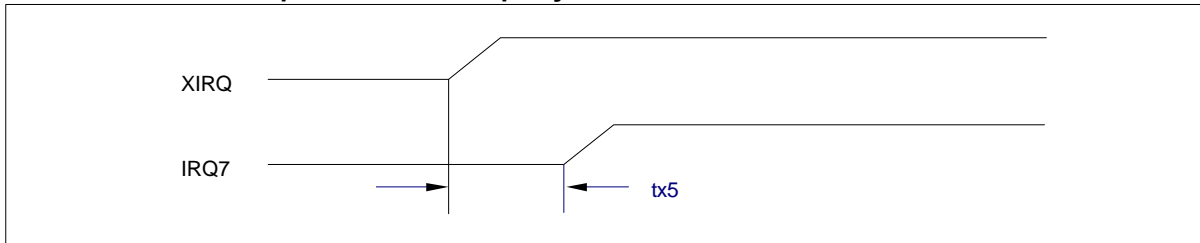
9.4.8 ECP Parallel Port Reverse Timing



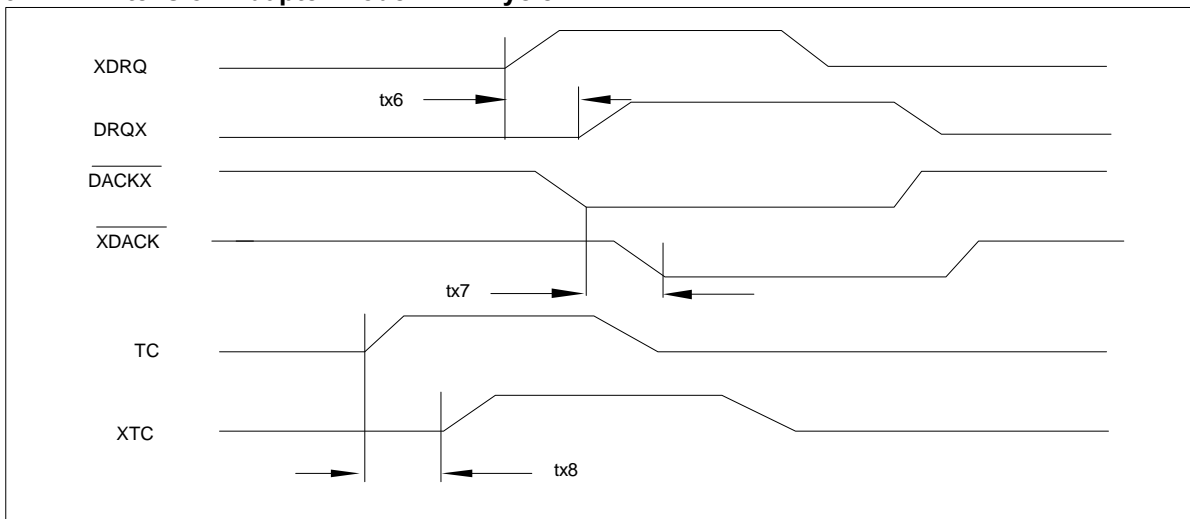
9.4.9 Extension Adapter Mode Command Cycle



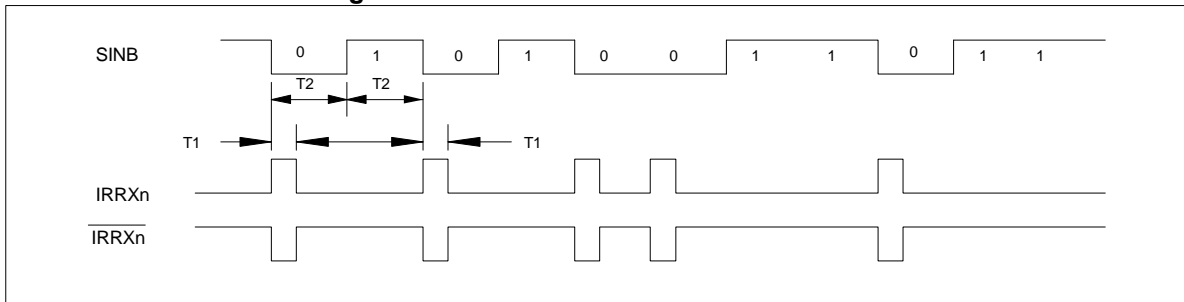
9.4.10 Extension Adapter Mode Interrupt Cycle



9.4.11 Extension Adapter Mode DMA Cycle



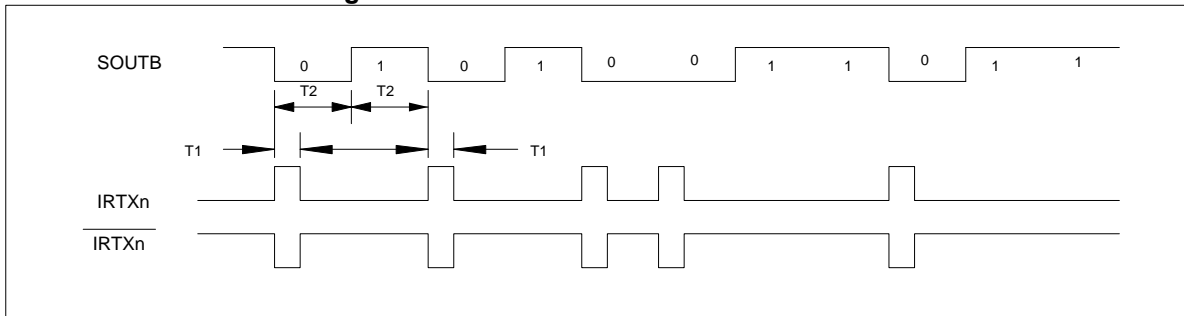
9.4.12 IrDA Receiver Timing



Note:

1. IRRXn: CR0C.bit0 (TX2INV) = 0 active high (default).
 $\overline{\text{IRRXn}}$: CR0C.bit0 (TX2INV) = 1 active low.

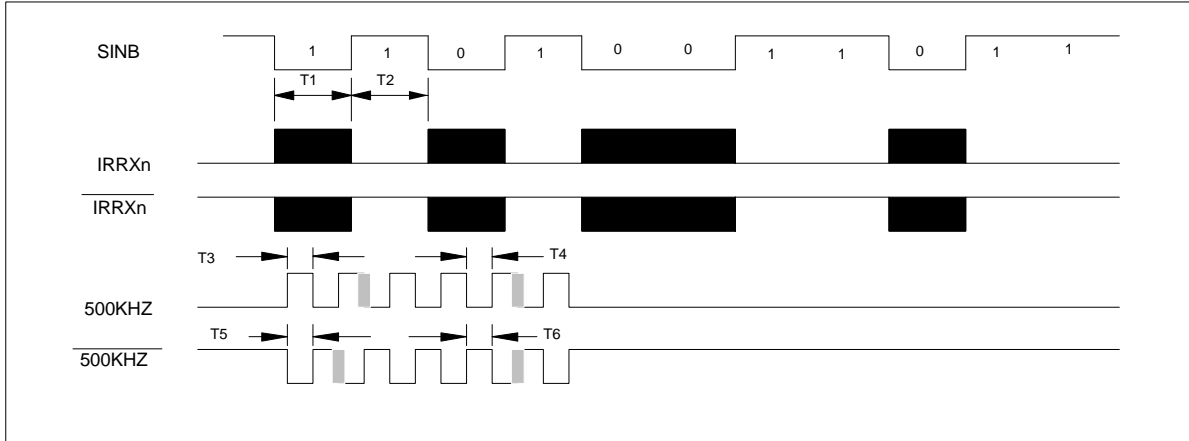
9.4.13 IrDA Transmit Timing



Notes:

1. IRTXn: CR0C.bit1 (RX2INV) = 0 active high (default).
 $\overline{\text{IRTXn}}$: CR0C.bit1 (RX2INV) = 1 active low.

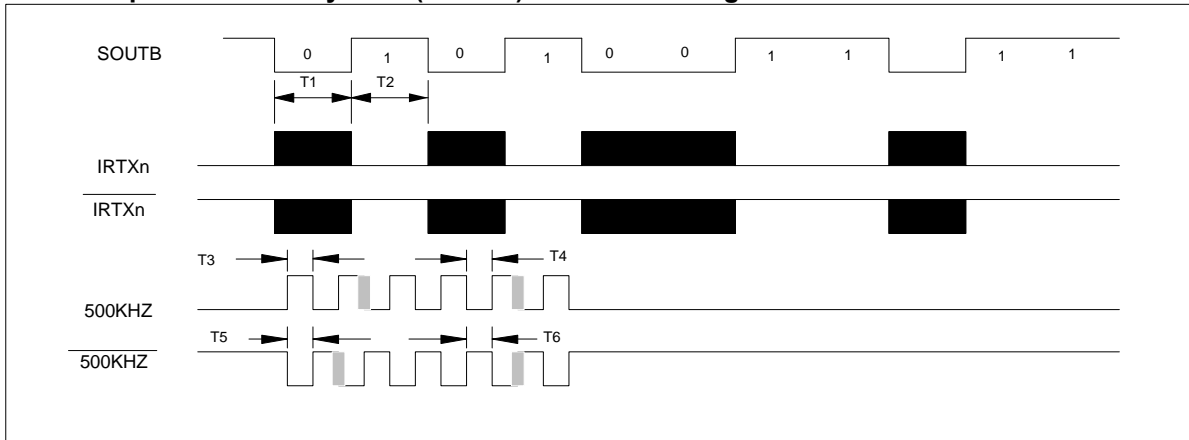
9.4.13 Amplitude Shift Keyed IR (ASK-IR) Receiver Timing



Notes:

- 1: Receive 500KHZ Pulse Detection Criteria: A received pulse is detected if the received pulse is minimum of 0.8μs.
2. IRRXn: CR0C.bit1 (RX2INV) = 0 active high (default).
 \overline{IRRXn} : CR0C.bit1 (RX2INV) = 1 active low.

9.4.13 Amplitude Shift Keyed IR (ASK-IR) Receiver Timing

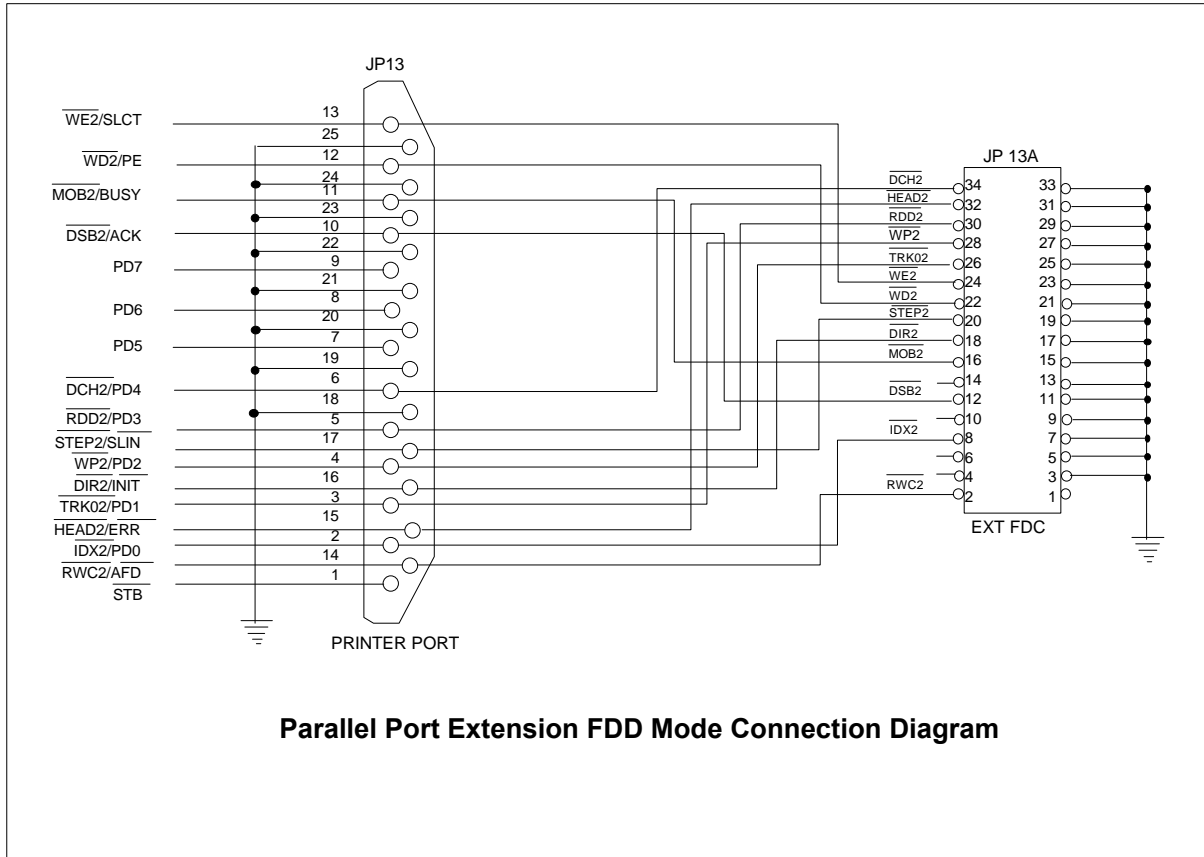


Notes:

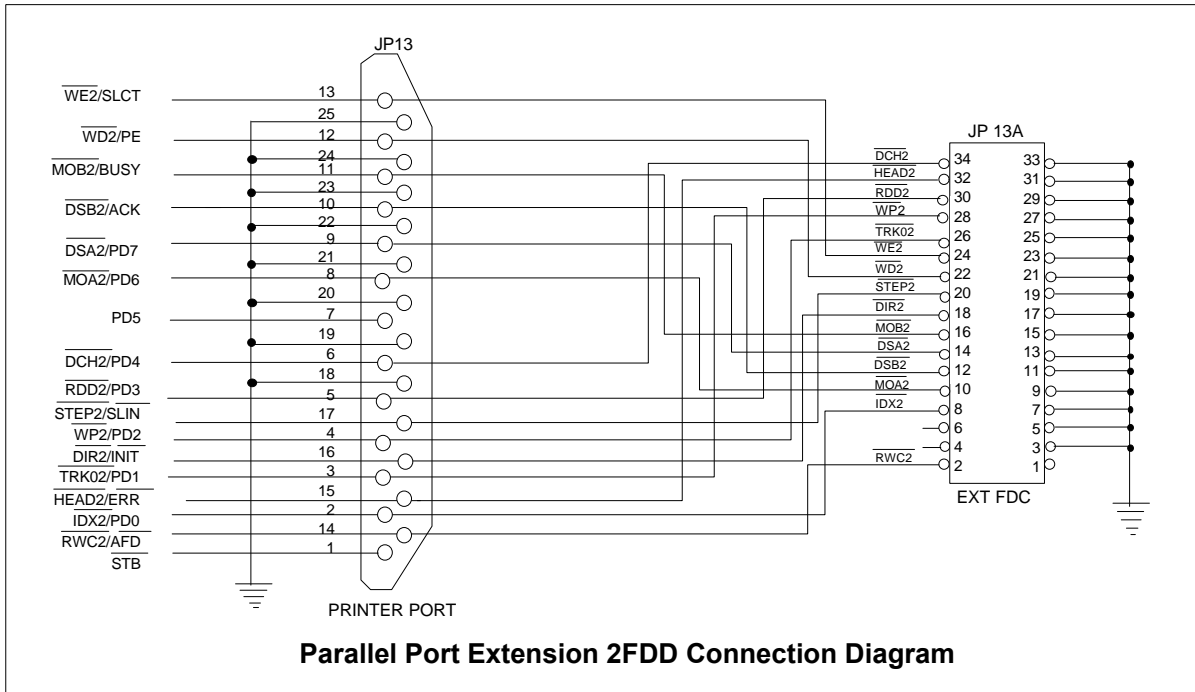
- 1: Receive 500KHZ Pulse Detection Criteria: A received pulse is detected if the received pulse is minimum of 0.8μs.
2. IRTXn: CR0C.bit0 (TX2INV) = 0 active high (default).
 \overline{IRTXn} : CR0C.bit0 (TX2INV) = 1 active low.

10.0 APPLICATION CIRCUITS

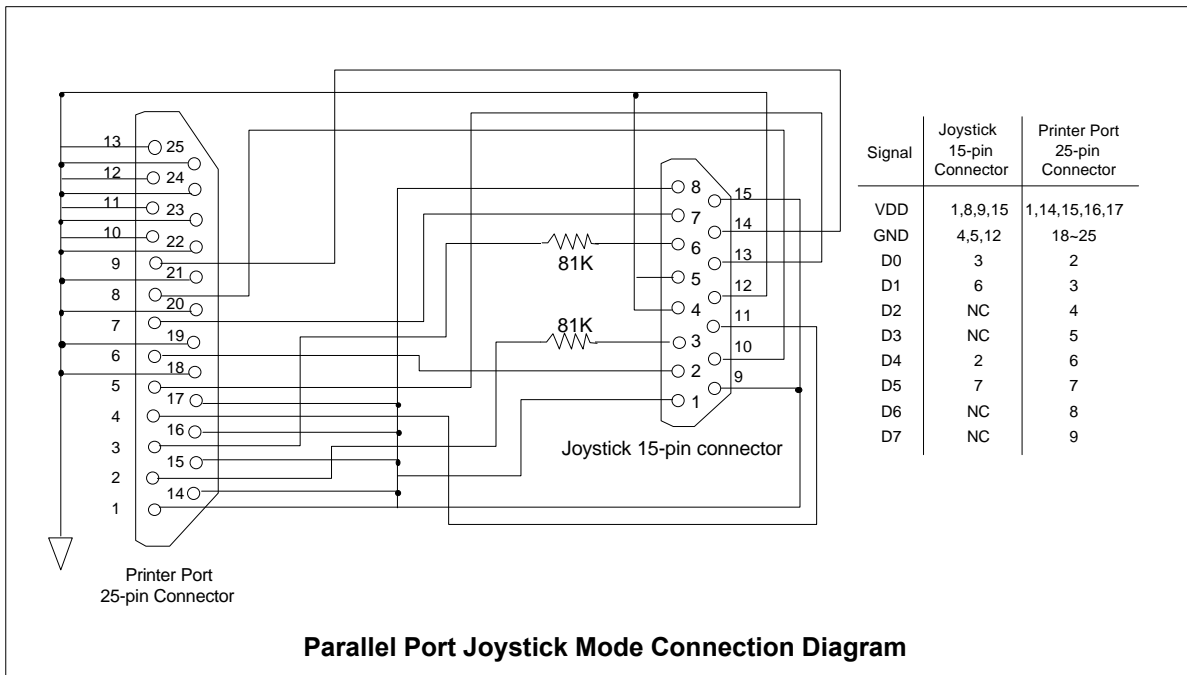
10.1 Parallel Port Extension FDD



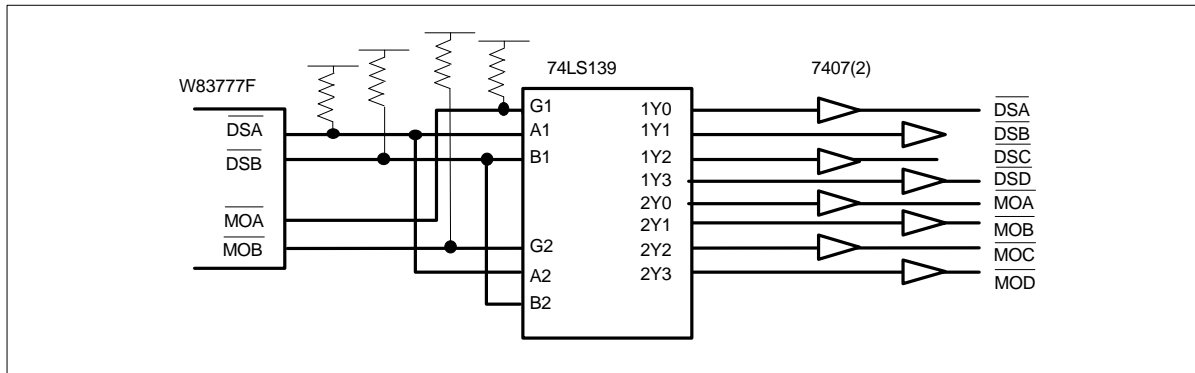
10.2 Parallel Port Extension 2FDD



10.3 Parallel Port Joystick Mode

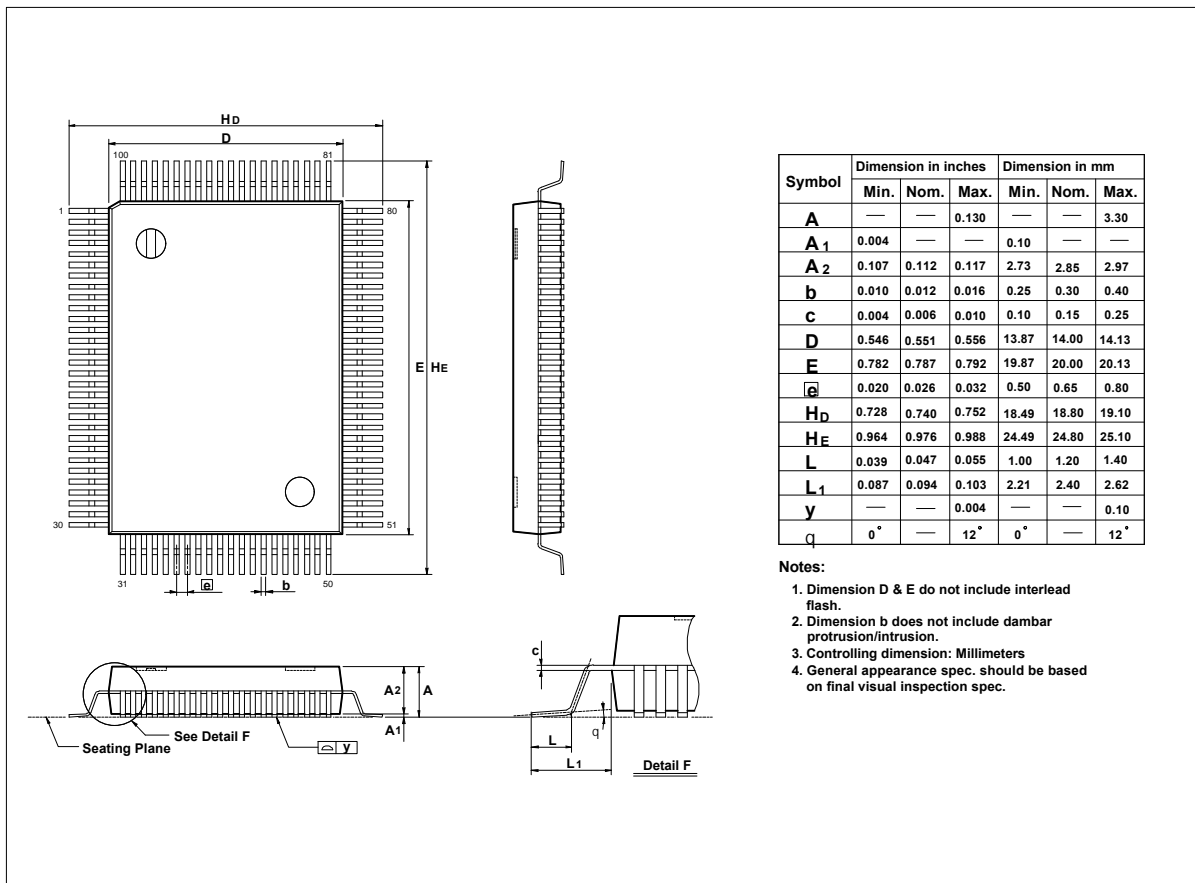


10.4 Four FDD Mode



11.0 PACKAGE DIMENSIONS

(100-pin QFP)



| Symbol | Dimension in inches | | | Dimension in mm | | |
|----------------|---------------------|-------|-------|-----------------|-------|-------|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | — | — | 0.130 | — | — | 3.30 |
| A ₁ | 0.004 | — | — | 0.10 | — | — |
| A ₂ | 0.107 | 0.112 | 0.117 | 2.73 | 2.85 | 2.97 |
| b | 0.010 | 0.012 | 0.016 | 0.25 | 0.30 | 0.40 |
| c | 0.004 | 0.006 | 0.010 | 0.10 | 0.15 | 0.25 |
| D | 0.546 | 0.551 | 0.556 | 13.87 | 14.00 | 14.13 |
| E | 0.782 | 0.787 | 0.792 | 19.87 | 20.00 | 20.13 |
| e | 0.020 | 0.026 | 0.032 | 0.50 | 0.65 | 0.80 |
| H _D | 0.728 | 0.740 | 0.752 | 18.49 | 18.80 | 19.10 |
| H _E | 0.964 | 0.976 | 0.988 | 24.49 | 24.80 | 25.10 |
| L | 0.039 | 0.047 | 0.055 | 1.00 | 1.20 | 1.40 |
| L ₁ | 0.087 | 0.094 | 0.103 | 2.21 | 2.40 | 2.62 |
| y | — | — | 0.004 | — | — | 0.10 |
| q | 0° | — | 12° | 0° | — | 12° |

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

W83877F/787IF/787F

Application Note 2

June 14, 1995

Differences between W83877 and W83787IF/F

Feature Brief

W83877: W83777F + Dummy Plug and Play + IR

W83787IF: W83787F + IR

Description

Illustrates the pins that have different functionality on the W83787F, W83787IF and the W83877F. The following table lists the pins that differ.

| Pin | W83787F/777F | W83787IF | W83877F |
|-----|---------------|------------------------------|---------------------------|
| 1 | nRESIDE | nRESIDE/ IRRX3 | nRESIDE/ IRQ_G |
| 2 | PDBDIR/nFDCEN | PDBDIR/ IRTX2 /nFDCEN | nCS |
| 3 | PDCIN | PDCIN/ IRRX2 | PDCIN |
| 4 | PDRQX/HPRTM1 | same as 787 | DRQ_C |
| 18 | PRTOE/nPDACKX | same as 787 | nDACK_C |
| 23 | IRQ7 | same as 787 | IRQ_E |
| 35 | nDTRA/HPRTAS0 | same as 787 | nDTRA/ HEFRAS |
| 36 | nRTSA/HPRTAS1 | same as 787 | nRTSA/ PNPCVS |
| 37 | IRQ4 | same as 787 | IRQ_D |
| 38 | SOUTA/HURAS1 | same as 787 | SOUTA/ IRIDE |
| 39 | nGMWR/HPRTM0 | same as 787 | nGMWR/ DRQ_A |
| 41 | nGMRD/HEFERE | same as 787 | nGMRD/ nDACK_A |
| 42 | SINB | SINB/ IRRX1 | SINB/ IRRX1 |
| 43 | SOUTB/HURBS1 | SOUTB/ IRTX1 /HURBS1 | SOUTB/ IRTX1/GMDRQ |
| 44 | IRQ3 | same as 787 | IRQ_C |
| 45 | nRTSB/HURBS0 | same as 787 | nRTSB/ IGIOSEL |
| 46 | nDTRB/HURAS0 | same as 787 | nDTRB |
| 91 | nDBENL/ABCHG | nDBENL/ nIDBEN/GIOSEL | nIDBEN/IRQ_H |
| 92 | nDBENH/FADSEL | nDBENH/ GIO0/URIRSEL | IRQ_B/GIO0 |
| 93 | nIOCS16 | nIOCS16 | nIRQIN |
| 94 | nCS0/nIDEEN | nCS0/ IRRX4 /nIDEEN | nCS0/ IRRX2 |
| 95 | nCS1/HADSEL | nCS1/ IRTX3 /HADSEL | nCS1/ IRTX2 |
| 96 | IDED7 | IDED7/ GIO1 | IRQ_A/GIO1 |

| Pin | W83787F/777F | W83787IF | W83877F |
|-----|--------------|-------------|----------------|
| 98 | nDACK2 | same as 787 | nDACK_B |
| 99 | IRQ6 | same as 787 | IRQ_F |
| 100 | DRQ2 | same as 787 | DRQ_B |

A description of the functional differences for each pin follows.

W83787IF:

- Pin 1: If the nRESIDE is not used, the alternate functions can be used for serial infrared receive input. Select IRRX3 by setting bits 5:4 in CR0D to be 10.
- Pin 2: In CARD features this pin is not used, so can be used for IRTX2. Set bits 6:7 in CR0D to 00 (that is default setting).
- Pin 3: same as pin 2. Set bits 5:4 in CR0D to 00 (that is default setting).
- Pin 42-43: They can be programmed by CR0D register as input/output pin IRRX1/IRTX1 for serial infrared communication.
- Pin 91: During power-on reset, this pin is pulled down internally and is defined as GIOSEL. If GIOSEL =0, this pin act as nDBENL. If GIOSEL =1, this pin act as nIDBEN (IDE Data Bus Enable).
- Pin 92: During power-on reset, if Pin #91GIOSEL =0, this pin act as nDBENH. If GIOSEL =1, this pin act as GIO0 (General Purpose I/O). It can also be programmed by CR0C register bit 2. During power-on reset, this pin is pulled up internally and is defined as URIRSEL. If URIRSEL =1, then UARTB act as UART function. If URIRSEL =0, then UARTB act as IR function.
- Pin 94-95: They can be programmed by CR0D register as input/output pin IRRX4/IRTX3 for serial infrared communication.
- Pin 96: During power-on reset, if Pin #91GIOSEL =0, this pin act as IDED7. If GIOSEL =1, this pin act as GIO1 (General Purpose I/O).

W83877F/787IF/787F

Application Note 3

June 20, 1995

W83787IF and W83877F Configuration Register

Feature Brief

W83877: W8377F + Dummy Plug and Play + IR

W83787IF: W83787F + IR

Description

A. W83787IF Configuration Register

CR0C

bit 7: TURA =0 the clock source of UART A is 1.8462 MHZ (24 MHZ divide 13) (default)
=1 the clock source of UART A is 24 MHZ

bit 6: TURB =0 the clock source of UART B is 1.8462 MHZ (24 MHZ divide 13) (default)
=1 the clock source of UART B is 24 MHZ

bit 5: HEFERE =0 the Extended Function Enable Register enable value is 88H.
=1 the Extended Function Enable Register enable value is 89H.

The default value of HEFERE is dependent on pin 41 at power on setting.

bit 4: Reserved

bit 3: URIRSEL = 0 select UART B as IR function.
=1 select UART B as normal function.

The default value of URIRSEL is dependent on pin 92 at power on setting

bit 2: GIOSEL = 0 select the IDE pins definition compatible to W83787F IDE pins definition.
=1 select the W83787IF IDE pins definition and general purpose I/O function.

The default value of GIOSEL is dependent on pin 91 at power on setting.

bit 1: RX2INV =0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.
=1 inverse the SINB pin of UART B function or IRRX pin of IR function

bit 0: TX2INV =0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.
=1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

CR0D

bit 7: SIRTX1 => IRTX pin selection bit 1

bit 6: SIRTX0 => IRTX pin selection bit 0

| SIRTX1 | SIRTX0 | IRTX output on pin |
|--------|--------|-------------------------|
| 0 | 0 | IRTX2 (pin 2) (default) |
| 0 | 1 | IRTX1 (pin 43) |
| 1 | 0 | IRTX3 (pin 95) |
| 1 | 1 | IRTX2 (pin 2) |

bit 5: SIRRX1 => IRRX pin selection bit 1

bit 4: SIRRX0 => IRRX pin selection bit 0

| SIRRX1 | SIRRX0 | IRRX input on pin |
|--------|--------|-------------------------|
| 0 | 0 | IRRX2 (pin 3) (default) |
| 0 | 1 | IRRX1 (pin 42) |
| 1 | 0 | IRRX4 (pin 94) |
| 1 | 1 | IRRX3 (pin 1) |

bit 3: HDUPLX =0 The IR function is Full Duplex.
 =1 The IR function is Half Duplex.

bit 2: IRMODE2 => IR function mode selection bit 2

bit 1: IRMODE1 => IR function mode selection bit 1

bit 0: IRMODE0 => IR function mode selection bit 0

| IRMODE2 | IRMODE1 | IRMODE0 | IR function | IRTX | IRRX |
|---------|---------|---------|-------------|--|------------------|
| 0 | 0 | X | disable | high | high |
| 0 | 1 | 0 | IrDA | active pulse is 1.6 us | demod. into SIN2 |
| 0 | 1 | 1 | IrDA | active pulse is 3/16 baud | demod. into SIN2 |
| 1 | 0 | 0 | Sharp-IR | inversion of SOUTB | routed to SINB |
| 1 | 0 | 1 | Sharp-IR | inversion of SOUTB AND 500KHZ clock | routed to SINB |
| 1 | 1 | 0 | Sharp-IR | inversion of SOUTB | demod. into SINB |
| 1 | 1 | 1 | Sharp-IR | inversion of SOUTB AND 500KHZ clock | demod. into SINB |

CR0E. CR0F :

bit 7 - bit 0 : Reversed for testing

CR10:

bit 7 -bit 0 : GIO0AD7 - GIO0AD0 => GIOP0 (pin 92) address bit 7 - bit 0.

CR11:

bit 3 - bit 0: GIO0AD10 - GIO0AD8 => GIOP0 (pin 92) address bit 10 - bit 8
 bit 5- bit 3 : Reversed

bit 7 - bit 6: G0CADM1 - G0CADM0 => GIOP0 address bit compare mode selection

| G0CADM1 | G0CADM0 | GIOP0 pin |
|---------|---------|---|
| 0 | 0 | compare GIO0AD10 - GIO0AD0 with SA10 -SA0 |
| 0 | 1 | compare GIO0AD10 - GIO0AD1 with SA10 -SA1 |
| 1 | 0 | compare GIO0AD10 - GIO0AD2 with SA10 -SA2 |
| 1 | 1 | compare GIO0AD10 - GIO0AD3 with SA10 -SA3 |

CR12:

bit 7 -bit 0 : GIO1AD7 - GIO1AD0 => GIOP1 (pin 96) address bit 7 - bit 0.

CR13:

bit 3 - bit 0: GIO1AD10 - GIO1AD8 => GIOP1 (pin 96) address bit 10 - bit 8

bit 5- bit 3 : Reversed

bit 7 - bit 6: G1CADM1 - G1CADM0 => GIOP1 address bit compare mode selection

| G1CADM1 | G1CADM0 | GIOP1 pin |
|---------|---------|---|
| 0 | 0 | compare GIO1AD10 - GIO1AD0 with SA10 -SA0 |
| 0 | 1 | compare GIO1AD10 - GIO1AD1 with SA10 -SA1 |
| 1 | 0 | compare GIO1AD10 - GIO1AD2 with SA10 -SA2 |
| 1 | 1 | compare GIO1AD10 - GIO1AD3 with SA10 -SA3 |

CR14:

bit 7 - bit 5: GIOP0MD2 - GIOP0MD 0 = > GIOP0 pin mode selection

| GIOP0MD2 | GIOP0MD1 | GIOP0MD0 | GIOP0 pin |
|----------|----------|----------|--|
| 0 | 0 | 0 | inactive (tri-state) |
| 0 | 0 | 1 | as a data output pin (SD0 --> GIOP0), when (AEN=L) AND (NIOW=L) AND (SA10-0 = GIO0AD10-0), the value of SD0 will present at GIOP0 |
| 0 | 1 | 0 | as a data input pin (GIOP0 --> SD0), when (AEN=L) AND (NIOR=L) AND (SA10-0 = GIO0AD10-0), the value of GIOP0 will present at SD0 |
| 0 | 1 | 1 | as a data input/output pin (GIOP0 <--> SD0). When (AEN=L) AND (NIOW=L) AND (SA10-0 = GIO0AD10-0), the value of SD0 will present at GIOP0 When (AEN=L) AND (NIOR=L) AND (SA10-0 = GIO0AD10-0), the value of GIOP0 will present at SD0 |

1 X X as a Chip Select pin, the pin will active at (AEN=L) AND (SA10-0 = GIO0AD10-0) OR (NIOR=L) OR (NIOW=L)

bit 4: GIO0CSH =0 the Chip Select pin will active LOW when (AEN=L) AND (SA10-0 = GIO0AD10-0) OR (NIOR=L) OR (NIOW=L)
 =1 the Chip Select pin will active HIGH when (AEN=L) AND (SA10-0 = GIO0AD10-0) OR (NIOR=L) OR (NIOW=L)

bit 3: GCS0IOR

bit 2: GCS0IOW

| GCS0IOR | GCS0IOW | |
|---------|---------|--|
| 0 | 0 | The GIOP0 function as a Chip Select pin, and will active when (AEN=L) AND (SA10-0 = GIO1AD10-0) |
| 0 | 1 | The GIOP0 function as a Chip Select pin, and will active when (AEN=L) AND (SA10-0 = GIO1AD10-0) AND (NIOW=L) |
| 1 | 0 | The GIOP0 function as a Chip Select pin, and will active when (AEN=L) AND (SA10-0 = GIO1AD10-0) AND (NIOR=L) |
| 1 | 1 | The GIOP0 function as a Chip Select pin, and will active when (AEN=L) AND (SA10-0 = GIO1AD10-0) AND (NIOW=L OR NIOR=L) |

bit 1 : GDA0OPI

bit 0 : GDA0IPI

| GDA0OPI | GDA0IPI | |
|---------|---------|---|
| 0 | 0 | The GIOP0 function as a data pin, and GIOP0 --> SD0, SD0 -->GIOP0 |
| 0 | 1 | The GIOP0 function as a data pin, and inverse GIOP0 --> SD0, SD0 -->GIOP0 |
| 1 | 0 | The GIOP0 function as a data pin, and GIOP0 --> SD0, inverse SD0 -->GIOP0 |
| 1 | 1 | The GIOP0 function as a data pin, and inverse GIOP0 --> SD0, inverse SD0 -->GIOP0 |

CR15:

bit 7 - bit 5: GIOP1MD2 - GIOP1MD 0 = > GIOP1 pin mode selection

| GIOP1MD2 | GIOP1MD1 | GIOP1MD0 | GIOP1 pin |
|----------|----------|----------|---|
| 0 | 0 | 0 | inactive (tri-state) |
| 0 | 0 | 1 | as a data output pin (SD1 --> GIOP1), when (AEN=L) AND (NIOW=L) AND (SA10-0 = GIO1AD10-0), the value of SD1 will present at GIOP1 |

| | | | |
|---|---|---|--|
| 0 | 1 | 0 | as a data input pin (GIOP1 --> SD1), when (AEN=L) AND (NIOR=L) AND (SA10-0 = GIO1AD10-0), the value of GIOP1 will present at SD1 |
| 0 | 1 | 1 | as a data input/output pin (GIOP1 <--> SD1). When (AEN=L) AND (NIOW=L) AND (SA10-0 = GIO1AD10-0), the value of SD1 will present at GIOP1 When (AEN=L) AND (NIOR=L) AND (SA10-0 = GIO1AD10-0), the value of GIOP1 will present at SD1 |
| 1 | X | X | as a Chip Select pin, the pin will active at (AEN=L) AND (SA10-0 = GIO1AD10-0) OR (NIOR=L) OR (NIOW=L) |

bit 4: GIO1CSH =0 the Chip Select pin will active LOW when (AEN=L) AND (SA10-0 = GIOAD10-0) OR (NIOR=L) OR (NIOW=L)
 =1 the Chip Select pin will active HIGH when (AEN=L) AND (SA10-0 = GIOAD10-0) OR (NIOR=L) OR (NIOW=L)

bit 3: GCS1IOR

bit 2: GCS1IOW

| GCS1IOR | GCS1IOW | |
|---------|---------|--|
| 0 | 0 | The GIOP1 function as a Chip Select pin, and will active when (AEN=L) AND (SA10-0 = GIO1AD10-0) |
| 0 | 1 | The GIOP1 function as a Chip Select pin, and will active when (AEN=L) AND (SA10-0 = GIO1AD10-0) AND (NIOW=L) |
| 1 | 0 | The GIOP1 function as a Chip Select pin, and will active when (AEN=L) AND (SA10-0 = GIO1AD10-0) AND (NIOR=L) |
| 1 | 1 | The GIOP1 function as a Chip Select pin, and will active when (AEN=L) AND (SA10-0 = GIO1AD10-0) AND (NIOW=L OR NIOR=L) |

bit 1 : GDA0OPI

bit 0 : GDA1IPI

| GDA1OPI | GDA1IPI | |
|---------|---------|---|
| 0 | 0 | The GIOP1 function as a data pin, and GIOP1 --> SD1, SD1 -->GIOP1 |
| 0 | 1 | The GIOP1 function as a data pin, and inverse GIOP1 --> SD1, SD1 -->GIOP1 |
| 1 | 0 | The GIOP1 function as a data pin, and GIOP1 --> SD1, inverse SD1 -->GIOP1 |
| 1 | 1 | The GIOP1 function as a data pin, and inverse GIOP1 --> SD1, inverse SD1 -->GIOP1 |

B. W83877F Configuration Register

CR0D ~ CR15

Same as W83787IF

CR1E

This register is used to select the base address of Game Chip Select Decoder (GAMECS) from 100H - 3F0H on 16-byte boundaries. The default value is 81H. NCS=0 and A10=0 are required to qualify the GAMECS output.

bit 7 - bit 2: match A[9:4].

bit 1 - bit 0: GAMECS configuration.

| | |
|----|--------------------------------|
| 00 | GAMECS disable |
| 01 | 1-byte decode, A[3:0] = 0001b |
| 10 | 8-byte decode, A[3:0] = 0xxxb |
| 11 | 16-byte decode, A[3:0] = xxxxb |

CR20

This register is used to select the base address of the Floppy Disk Controller (FDC) from 100H - 3F0H on 16-byte boundaries. The default value is FCH. NCS=0 and A10=0 are required to access the FDC registers. A[3:0] are always decoded as 0xxxb.

bit 7 - bit 2: match A[9:4]. Bit 7=0 and bit 6=0 disable this decode.

bit 1 - bit 0: fixed at zero.

CR21

This register is used to select the base address of the IDE Interface Control Registers from 100H - 3F0H on 16-byte boundaries. The default value is 7CH. NCS=0 and A10=0 are required to access the IDE registers. A[3:0] are always decoded as 0xxxb.

bit 7 - bit 2: match A[9:4]. Bit 7=0 and bit 6=0 disable this decode.

bit 1 - bit 0: fixed at zero.

CR22

This register is used to select the base address of the IDE Interface Alternate Status Register from 106H - 3F6H on 16-byte boundaries + 6. The default value is FDH. NCS=0 and A10=0 are required to access the IDE Alternate Status register.

A[3:0] must be 0110b.

bit 7 - bit 2: match A[9:4]. Bit 7=0 and bit 6=0 disable this decode.

bit 1: fixed at zero.

bit 0: fixed at one.

CR23

This register is used to select the base address of the parallel port. If EPP is disable, the parallel port can be set from 100H - 3FCH on 4-byte boundaries. If EPP is enable, the parallel port can be set from 100H - 3F8H on 8-byte boundaries. The default value is DEH. NCS=0 and A10=0 are required to access the parallel port when in compatible, bi-directional, or EPP modes. A10 is active in ECP mode.

bit 7 - bit 0: match A[9:2]. Bit 7=0 and bit 6=0 disable this decode.

CR24

This register is used to select the base address of the UART A from 100H - 3F8H on 8-byte boundaries. The default value is FEH. NCS=0 and A10=0 are required to access the UART A registers. A[2:0] are don't-care conditions.

bit 7 - bit 1: match A[9:3]. Bit 7=0 and bit 6=0 disable this decode.

bit 0: fixed at zero.

CR25

This register is used to select the base address of the UART B from 100H - 3F8H on 8-byte boundaries. The default value is BEH. NCS=0 and A10=0 are required to access the UART B registers. A[2:0] are don't-care conditions.

bit 7 - bit 1: match A[9:3]. Bit 7=0 and bit 6=0 disable this decode.

bit 0: fixed at zero.

CR26

This register is used to select DMA resources for the FDC (bits 7 - 4) and the parallel port (bits 3 - 0). Any unselected DMA is in tristate. The default value is 23H.

| bit 7- bit4, bit 3 - bit 0 | DMA selected |
|----------------------------|--------------|
| 0000 | None |
| 0001 | DMA_A |
| 0010 | DMA_B |
| 0011 | DMA_C |

CR27

This register is used to select IRQ resources for the FDC (bits 7 - 4) and the parallel port (bits 3 - 0). Any unselected IRQ is in tristate. The default value is 67H.

| bit 7- bit4, bit 3 - bit 0 | IRQ selected |
|----------------------------|--------------|
| 0000 | None |
| 0001 | IRQ_A |
| 0010 | IRQ_B |
| 0011 | IRQ_C |
| 0100 | IRQ_D |
| 0101 | IRQ_E |
| 0110 | IRQ_F |
| 0111 | IRQ_G |
| 1000 | IRQ_H |

CR28

This register is used to select IRQ resources for the UART A (bits 7 - 4) and the UART B (bits 3 - 0). Any unselected IRQ is in tristate. The default value is 43H.

CR29

This register is used to select IRQ resources for the IRQIN A (bits 3 - 0). Bits 7 - 4 are reserved and return zero when read. Any unselected IRQ is in tristate. The default value is 02H

W83787IF Application Note 4

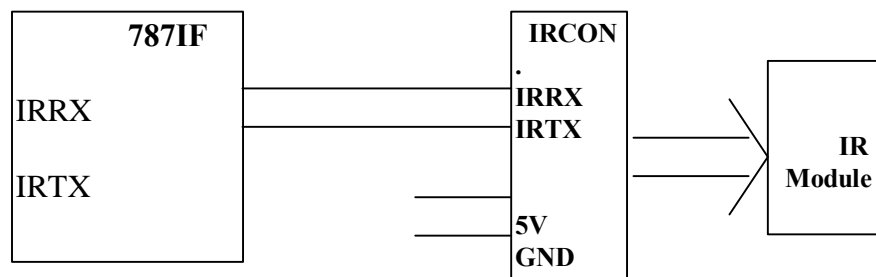
Aug 9, 1995

How to test IR function in 787IF?

It is very easy to test the IR Function within the 787IF. I suggest some methods to test it, you can follow below steps to do it.

A. If you only have an old board with 787F, you can mount 787IF to this old board, i.e., 787IF is pin to pin compatible with 787F. If you only have a new board with 787IF, you can directly mount 787IF on the board. Then you can check the 787IF all functions including FDC, PRT, COMA, COMB, and IDE function whether they can normal work or not. If it can normal operation, the first phase has been finished.

B. If you an old board with 787F, then stick up the Pin2 (PDCIN) and Pin3 (PDBDIR) or another Pins which are IR Receiver (IRRX) and IR Transceiver (IRTX) respectively. Then connected them using another wire and put together with VDD (5V) and GND to a connector which shows as follows.



C. Loopback test IR function:

1-1. First, you must configure the configuration registers of 787IF which you can use the program supplied by Winbond such as W787I.EXE.

How to use the program W787I.EXE?

You should be in the DOS prompt and type W787I command then it show a config IR's draft. In the row of URIRSEL, you select IR function. (Default is normal function, i.e., COMB)

1-2. Also you can use the DEBUG.EXE command in DOS prompt, then configure 787IF register as shown follows:

```
- O 250 89
- O 251 0c
- I 252 20 // This configure COMB from normal function to IR function.
- O 250 00
```


2-1. Short the terminal of IRTX and IRRX, then use the program TIR.EXE supplied by Winbond.

2-2. Also you can use DEBUG.EXE command in DOS prompt. The commands are shown as follows:

```
-O 2fb 80          // First you must set Baud rate in COMB.
-O 2f8 0c          // Set Baud rate 9600bps
-O 2f9 00
-O 2fb 03
***  Test IR function  ***
- I 2f8  // Clear the data buffer
- I 2fd  // The return value must be 60, if not, you must execute "-i 2f8" until "-i 2fd" return 60
- O 2f8 aa
- I 2fd  // Must return "61", i.e, there is a data in data register.
- I 2f8  // Must return "AA", that is, read data from data register
- O 2f8 55
- I 2fd  // Must return "61"
- I 2f8  / Must return "55"
```

You can output any 8-bit value to the data register, and then you can receiver an original send value. If you have finished the above phase and obtained correct results, I congratulate you, i.e., you have finished the IR testing roughly.

3-1. If you have IR module such as HPSIR or SIR2 or TEMIC, you can connect the module to 787IF. Then repeat above method, and you should obtain same results.

D. Application test:

Our 787IF have been tested by the some applications such lap-linker (LL5.EXE, version 5.0), fx-linker (FX.EXE, version 2.0), and PUMA's tranxit (executing for windows). In this testing you must have two computers with IR function.

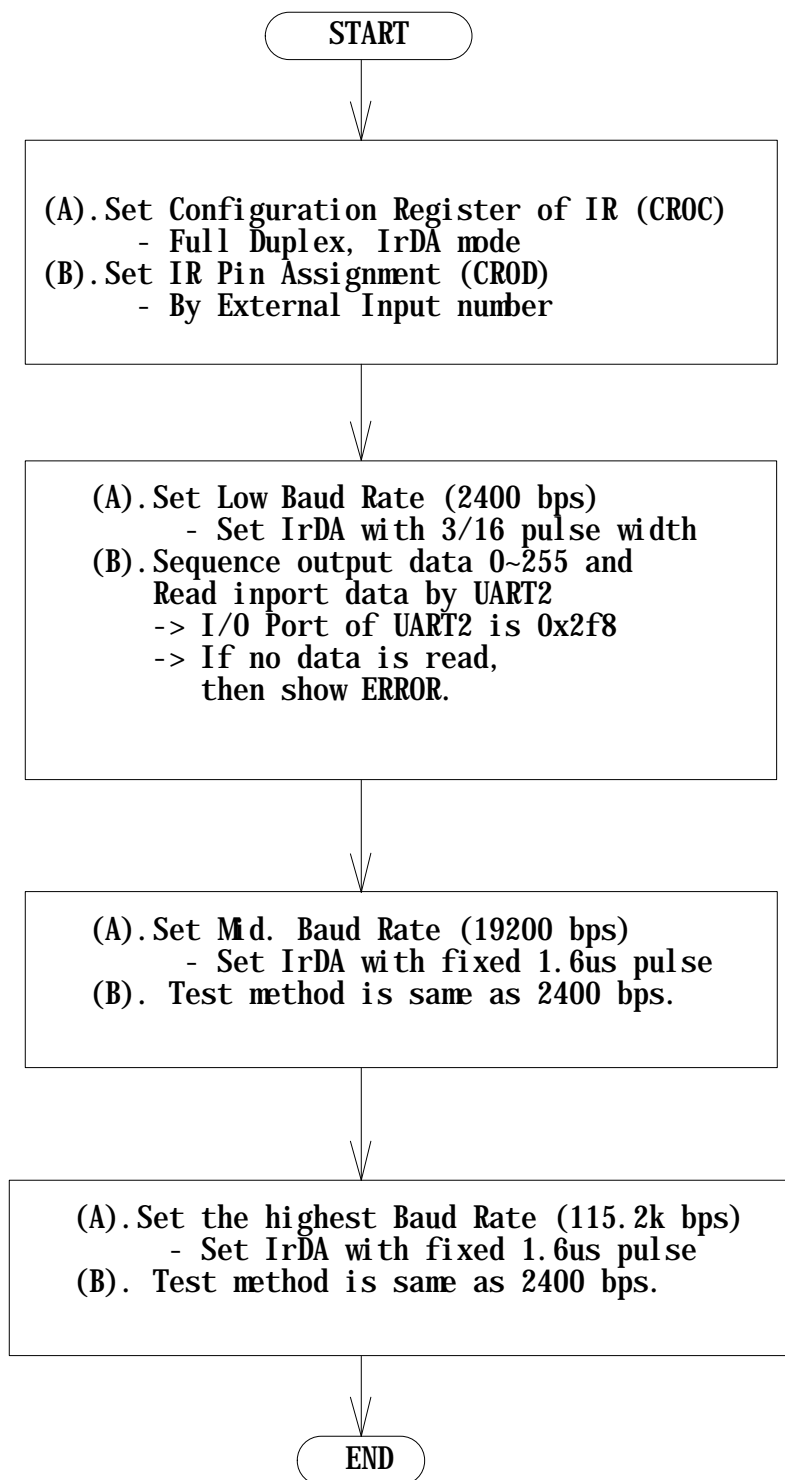
Note that: (1) if you use LL5.EXE or FX.EXE, you should configure the register of 787IR to *half duplex* because the applications are old version which do not support IR function and the IR is only using in half duplex.

What is half duplex? That is, IR receiver (IRRX) *could not* receive any data when the IR transceiver (IRTX) transmit data. This is called *half duplex*. In the other word, *full duplex* can receive and transmit data simultaneously.

(2) If you use Trasxit or another application tools which support IR function, you must set the configuration register of 787IF to *Full duplex*, otherwise they can not be normal operation.

Introduction of SELFTIR.EXE

The program is self-test W83787IF IR function in the full duplex which is similar to UART loopback function. If you have no IR module, you still to test the IR function. As follows, we show the procedure of this program.



Command usage:

1. In DOS prompt, type SELFTIR <IRTX> <IRRX>
2. Put on the IR module or short the terminal of IRTX and IRRX

Press any key to continue.

Example: Use Pin94 and Pin95 as IRTX and IRRX respectively, then the command is shown as follows:

```
C:\>SELFTIR 3 4
```

The number of IRTX and IRRX as shown follows:

```
IRTX = 1  => SOUT2 (Pin 2)
          2  => PDBDIR (Pin 43)
          3  => nCS1 (Pin 95)
```

```
IRRX= 1  => SIN2 (Pin42)
          2  => PDCIN (Pin 3)
          3  => nRESIDE (Pin 1)
          4  => nCS0 (Pin 94)
```