LOW POWER SCHOTTKY INTEGRATED CIRCUITS

T54LS24
T74LS24

67C 16056 D T-43-15

PRELIMINARY DATA

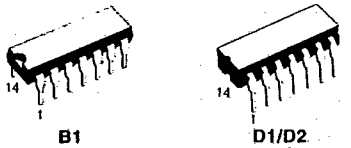
QUAD 2-INPUT SCHMITT TRIGGER NAND GATE

DESCRIPTION

The T54LS24/T74LS24 contains four 2-input NAND Gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. Additionally, they have greater noise margin than conventional NAND Gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter that drive a TTL totem pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input thereshold voltages for positive and negative-going transition. This hysteresis between the positive-going and negative-going input therestholds (typically 700 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage varations. As long as one input remains at a more positive voltage than V_{T+}(MAX), the gate will respond to the transitions of the other input as shown in figure 1.

- FUNCTIONALLY AND MECHANICALLY IDENTICAL TO LS132
- PNP INPUTS REDUCE SYSTEM LOADING



B1
Plastic Package

D1/D2
Ceramic Package

M1
Micro Package

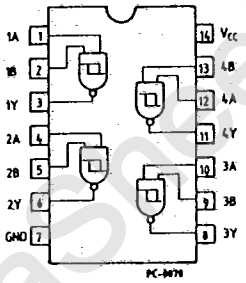
C1
Plastic Chip Carrier

ORDERING NUMBERS:

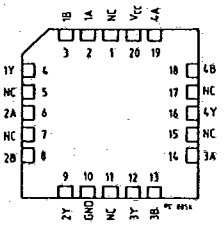
T54LS24 D2	T74LS24 C1
T74LS24 D1	T74LS24 M1
T74LS24 B1	

PIN CONNECTION
(top view)

DUAL IN LINE



CHIP CARRIER



NC = No Internal Connection

T54LS24
T74LS24

LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	X	H
X	L	H
H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.6 to 5.5	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS24D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS24XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{T+}	Positive-Going Threshold Voltage		1.65	1.85	2.15	$V_{CC}=5.0V$	V
V_{T-}	Negative-Going Threshold Voltage		0.75	1.0	1.25	$V_{CC}=5.0V$	V
$V_{T+}-V_{T-}$	Hysteresis		0.4	0.7		$V_{CC}=5.0V$	V
V_{CD}	Input Clamp Diode Voltage				−1.5	$V_{CC}=MIN, I_{IN}=-18mA$	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		$V_{CC}=MIN, I_{OH}=-400\mu A, V_{IN}=V_{T-MIN}$	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	$I_{OL}=4.0mA$; $V_{CC}=MIN$, $V_{IN}=V_{T+MAX}$	V
		74		0.35	0.5	$I_{OL}=8.0mA$; $V_{CC}=MIN$, $V_{IN}=V_{T+MAX}$	
I_{T+}	Input Current at Positive-Going Threshold			−2	20	$V_{CC}=5.0V, V_{IN}=V_{T+}$	μA
I_{T-}	Input Current at Negative-Going Threshold			−5	30	$V_{CC}=5.0V, V_{IN}=V_{T-}$	μA
I_{IH}	Input HIGH Current				20 0.1	$V_{CC}=MAX, V_{IN}=2.7V$ $V_{CC}=MAX, V_{IN}=7.0V$	μA mA
I_{IL}	Input LOW Current				−0.05	$V_{CC}=MAX, V_{IN}=0.4V$	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	$V_{CC}=MAX, V_{OUT}=0V$	mA
I_{CCH}	Power Supply Current HIGH			6.6	12	$V_{CC}=MAX, V_{IN}=0V$	mA
I_{CCL}	Power Supply Current LOW			11	20	$V_{CC}=MAX, V_{IN}=4.5V$	mA

AC CHARACTERISTICS: $T_A=25°C$

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions	Units
t_{PLH}	Turn Off Delay, Input to Output		13	20	$V_{CC}=5.0V$ $C_L=15pF, R_L=2\ k\Omega$	ns
t_{PHL}	Turn On Delay, Input to Output		21	40		ns

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at $V_{CC}=5.0V$, $T_A=25°C$

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T74LS24

Fig. 1

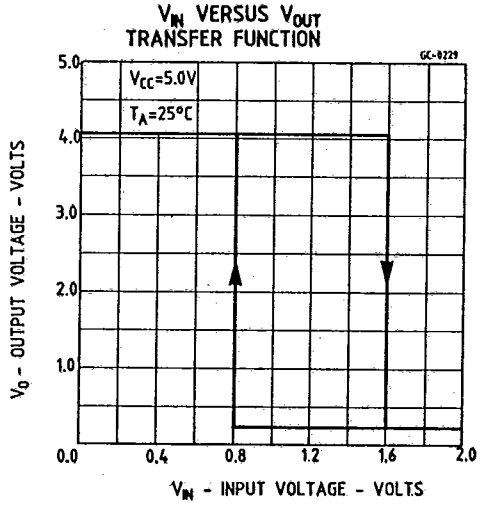


Fig. 2

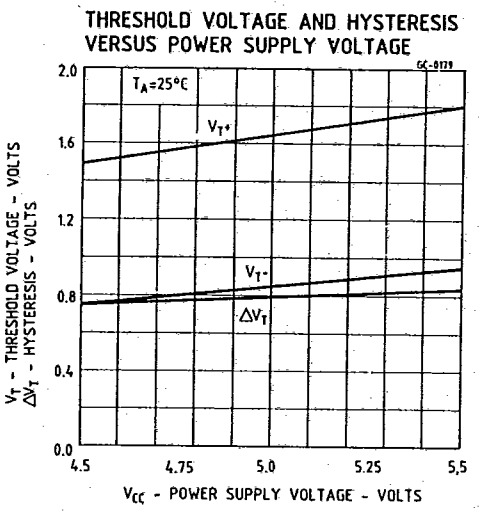


Fig. 3

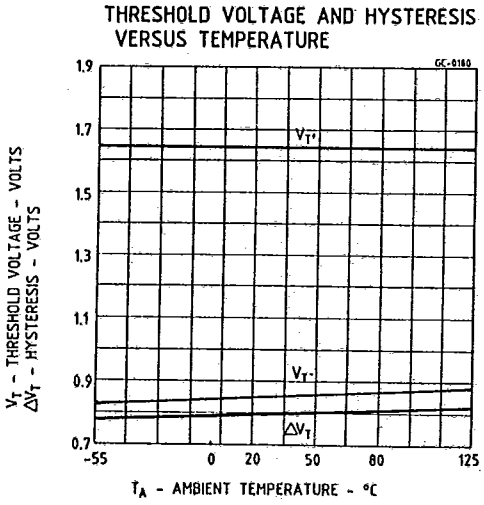
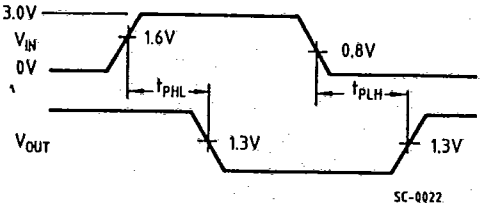
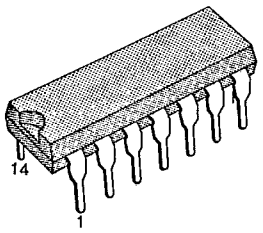
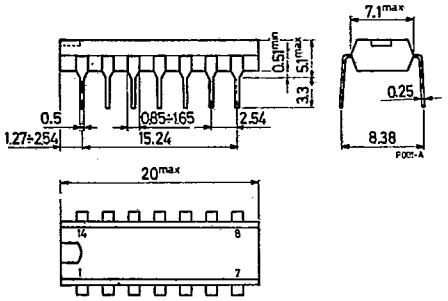


Fig. 4

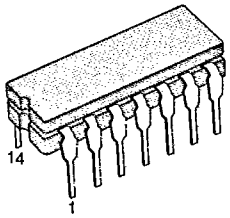


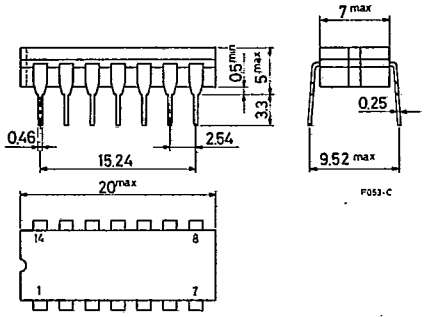
14-LEAD PLASTIC DIP



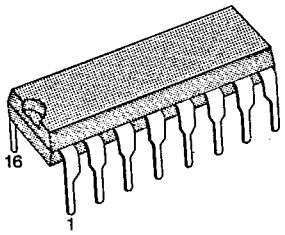


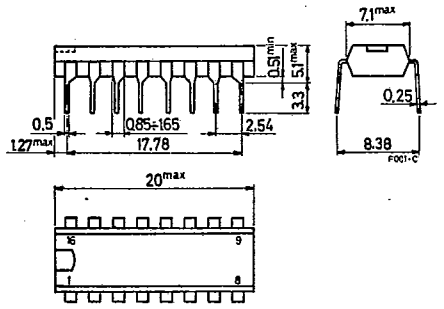
14-LEAD CERAMIC DIP





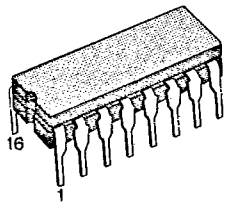
16-LEAD PLASTIC DIP

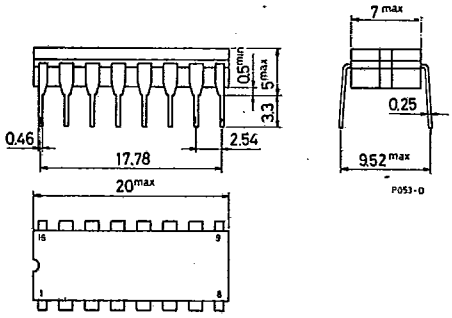




Packages

16-LEAD CERAMIC DIP





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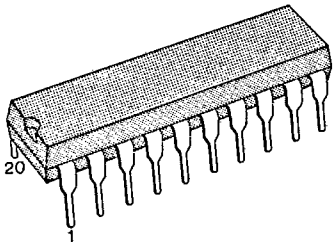

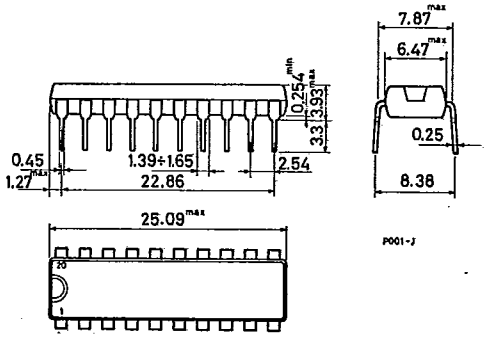

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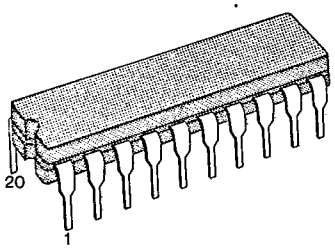
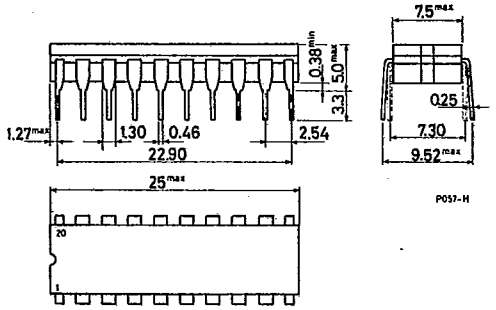
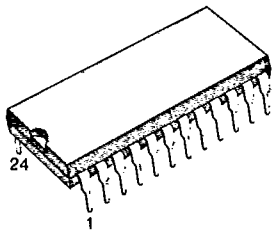
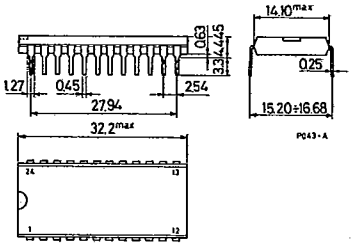




Packages

24-LEAD PLASTIC DIP





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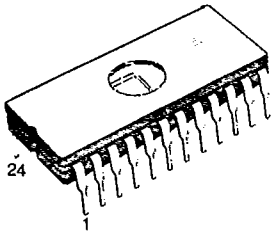
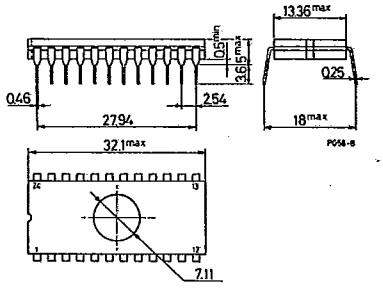
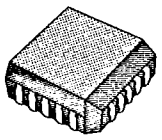
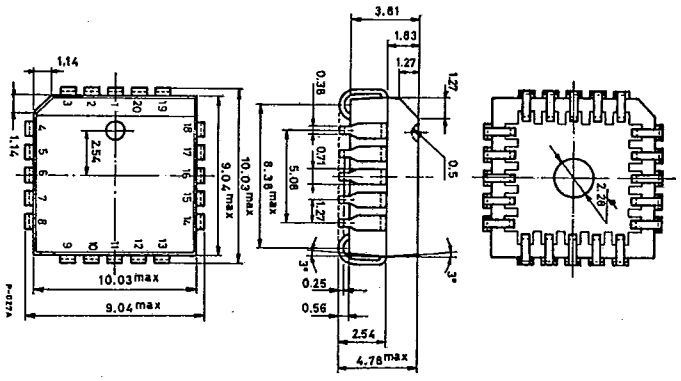




CHIP CARRIER 20 LEAD PLASTIC

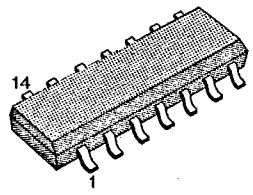


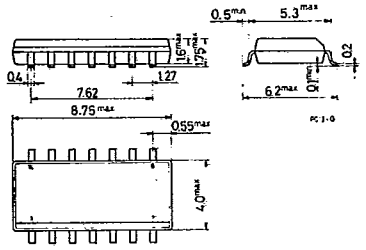


Packages

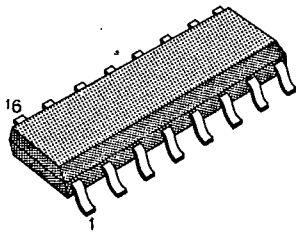
T-90-20

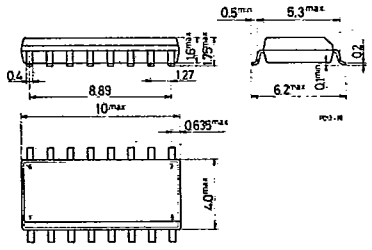
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.