

### POWER MANAGEMENT

#### Description

The SC4215 is a high performance positive voltage regulator designed for use in applications requiring very low Input voltage and very low dropout voltage at up to 2 amps. It operates with a  $V_{in}$  as low as 1.6V, with output voltage programmable as low as 0.8V. The SC4215 features ultra low dropout, ideal for applications where  $V_{out}$  is very close to  $V_{in}$ . Additionally, the SC4215 has an enable pin to further reduce power dissipation while shutdown. The SC4215 provides excellent regulation over variations in line, load and temperature.

The SC4215 is available in the SOIC-8EDP package. The output voltage can be set via an external or an internal resistive divider (2.5V) or to 0.8V depending on how the adjust pin is configured.

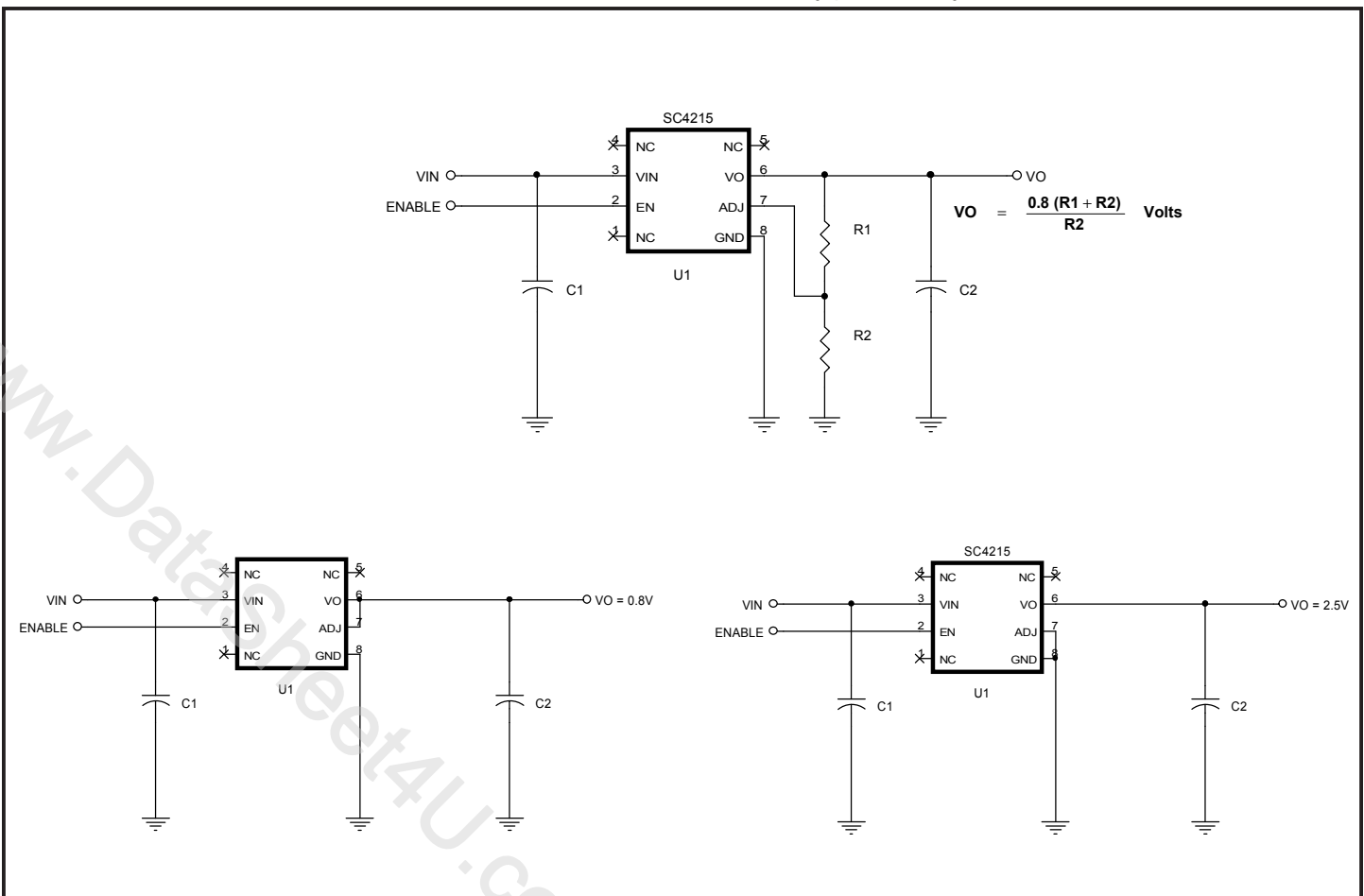
#### Features

- ◆ Input Voltage as low as 1.6V
- ◆ 500mV dropout @ 2A
- ◆ Adjustable output from 0.8V to 3.3V
- ◆ Over current and over temperature protection
- ◆ Enable pin
- ◆ 10 $\mu$ A quiescent current in shutdown
- ◆ Low reverse leakage (output to input)
- ◆ Full industrial temperature range
- ◆ Available in SOIC-8EDP package

#### Applications

- ◆ Telecom/Networking cards
- ◆ Motherboards/Peripheral cards
- ◆ Industrial Applications
- ◆ Wireless infrastructure
- ◆ Set top boxes
- ◆ Medical equipment
- ◆ Notebook computers
- ◆ Battery powered systems

#### Typical Application Circuits



**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Max	Units
V <sub>in</sub> , EN, V <sub>o</sub> , ADJ Absolute Voltage		6	V
Power Dissipation	P <sub>D</sub>	Internally Limited	W
Thermal Resistance Junction to Ambient SOIC-8EDP <sup>(1)</sup>	θ <sub>JA</sub>	36	°C/W
Thermal Resistance Junction to Case SOIC-8EDP <sup>(1)</sup>	θ <sub>JC</sub>	5.5	°C/W
Operating Ambient Temperature Range	T <sub>A</sub>	-40 to +85	°C
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +150	°C
Storage Temperature Range	T <sub>STG</sub>	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T <sub>LEAD</sub>	300	°C
ESD Rating (Human Body Model)	V <sub>ESD</sub>	2	kV

Note: (1) 2 square inch of FR-4, double sided, 1 oz. minimum copper weight.

**Electrical Characteristics**

Unless specified: V<sub>EN</sub> = V<sub>IN</sub>. Adjustable Option (V<sub>ADJ</sub> > V<sub>TH(ADJ)</sub>): V<sub>IN</sub> = 1.6V to 5.5V and I<sub>O</sub> = 10μA to 2A.

Fixed Options (V<sub>ADJ</sub> = GND): V<sub>IN</sub> = (V<sub>O</sub> + 0.5V) to 5.5V and I<sub>O</sub> = 10μA to 2A. Values in **bold** apply over the full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>VIN</b>						
Supply Voltage Range	V <sub>IN</sub>		<b>1.6</b>		<b>5.5</b>	V
Quiescent Current	I <sub>Q</sub>	V <sub>IN</sub> = 3.3V		0.75	<b>1.75</b>	mA
		V <sub>IN</sub> = 5.5V, V <sub>EN</sub> = 0V		10	<b>50</b>	μA
<b>VO</b>						
Output Voltage <sup>(1)</sup> (Internal Fixed Voltage)	V <sub>O</sub>	V <sub>IN</sub> = V <sub>O</sub> + 0.5V, I <sub>O</sub> = 10mA	-1%	V <sub>O</sub>	+1%	V
			<b>-2%</b>		<b>+2%</b>	
Line Regulation <sup>(1)</sup>	REG <sub>(LINE)</sub>	V <sub>IN</sub> = (V <sub>O</sub> + 0.5V), V <sub>IN</sub> < 3.65V, I <sub>OUT</sub> = 10mA		0.2	<b>0.5</b>	%
		V <sub>IN</sub> = (V <sub>O</sub> + 0.5V), V <sub>IN</sub> > 3.65V, I <sub>OUT</sub> = 10mA		0.5	<b>1.0</b>	%
Load Regulation <sup>(1)</sup>	REG <sub>(LOAD)</sub>	V <sub>IN</sub> = V <sub>O</sub> + 0.5V, V <sub>IN</sub> < 3.65V		0.2	<b>0.5</b>	%
		V <sub>IN</sub> = V <sub>O</sub> + 0.5V, V <sub>IN</sub> > 3.65V		0.5	<b>1.0</b>	%
Dropout Voltage <sup>(1)(2)</sup>	V <sub>D</sub>	I <sub>O</sub> = 1A		90	300	mV
					<b>400</b>	
		I <sub>O</sub> = 1.5A		200	400	mV
					<b>500</b>	

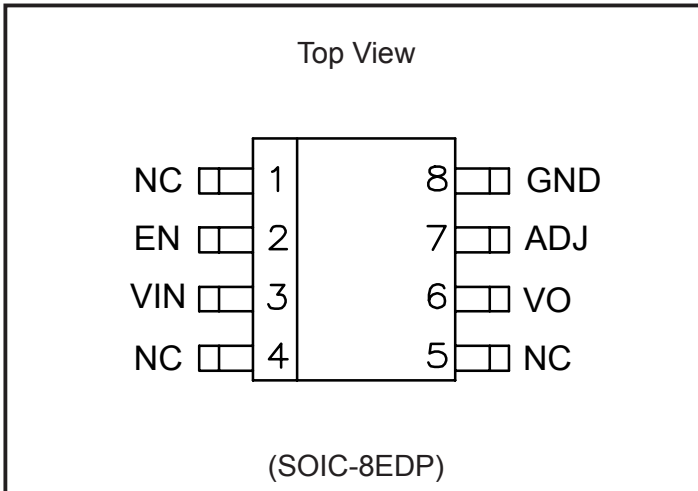
**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Unless specified:  $V_{EN} = V_{IN}$ . Adjustable Option ( $V_{ADJ} > V_{TH(ADJ)}$ ):  $V_{IN} = 1.6V$  to  $5.5V$  and  $I_O = 10\mu A$  to  $2A$ .  
 Fixed Options ( $V_{ADJ} = GND$ ):  $V_{IN} = (V_O + 0.5V)$  to  $5.5V$  and  $I_O = 10\mu A$  to  $2A$ . Values in **bold** apply over the full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>VO (Cont.)</b>						
Dropout Voltage <sup>(1)(2)</sup>		$I_O = 2A$		300	500	mV
					<b>600</b>	
Minimum Load Current <sup>(3)</sup>	$I_O$	$V_{IN} = V_O + 0.5V$		1	<b>10</b>	$\mu A$
Current Limit	$I_{CL}$		<b>2.2</b>	2.6	<b>3</b>	A
<b>ADJ</b>						
Reference Voltage <sup>(1)</sup>	$V_{REF}$	$V_{IN} = 2.2V, V_{ADJ} = V_{OUT}, I_O = 10mA$	0.792	0.8	0.808	V
			<b>0.784</b>		<b>0.816</b>	
Adjust Pin Current <sup>(4)</sup>	$I_{ADJ}$	$V_{ADJ} = V_{REF}$		80	<b>200</b>	nA
Adjust Pin Threshold <sup>(5)</sup>	$V_{TH(ADJ)}$		<b>0.05</b>	0.16	<b>0.40</b>	V
<b>EN</b>						
Enable Pin Current	$I_{EN}$	$V_{EN} = 0V, V_{IN} = 3.3V$		1.5	<b>10</b>	$\mu A$
Enable Pin Threshold	$V_{IH}$	$V_{IN} = 3.3V$	<b>1.6</b>			V
	$V_{IL}$	$V_{IN} = 3.3V$			<b>0.4</b>	
<b>Over Temperature Protection</b>						
High Trip level	$T_{HI}$			160		$^{\circ}C$
Hysteresis	$T_{HYST}$			10		$^{\circ}C$

**Notes:**

- (1) Low duty cycle pulse testing with Kelvin connections required.
- (2) Defined as the input to output differential at which the output voltage drops to 1% below the value measured at a differential of 0.5V.
- (3) Required to maintain regulation. Voltage set resistors R1 and R2 are usually utilized to meet this requirement. Adjustable versions only.
- (4) Guaranteed by design.
- (5) When  $V_{ADJ}$  exceeds this threshold, the "Sense Select" switch disconnects the internal feedback chain from the error amplifier and connects  $V_{ADJ}$  instead.

**POWER MANAGEMENT**
**Pin Configuration**

**Ordering Information**

Part Number	Package	Temp. Range (T <sub>A</sub> )
SC4215ISTR <sup>(1)(2)</sup>	SOIC-8EDP	-40 to +85 °C
SC4215EVB	Evaluation Board	

**Note:**

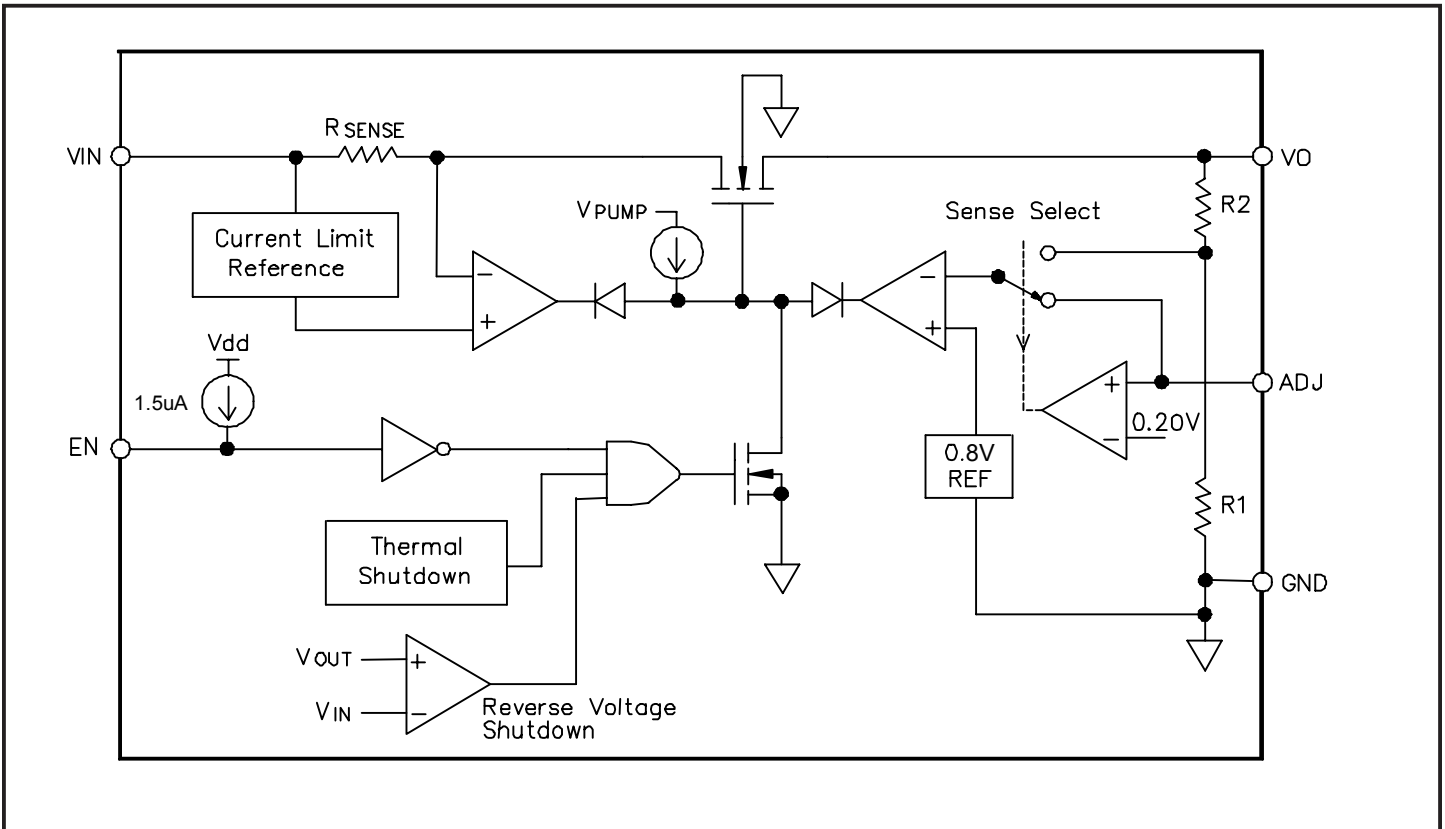
- (1) Available voltage is : 2.5V. Output voltage can be adjusted using external resistors, see Pin Descriptions.
- (2) Only available in tape and reel packaging. A reel contains 2500 devices for the SOIC-8EDP package.

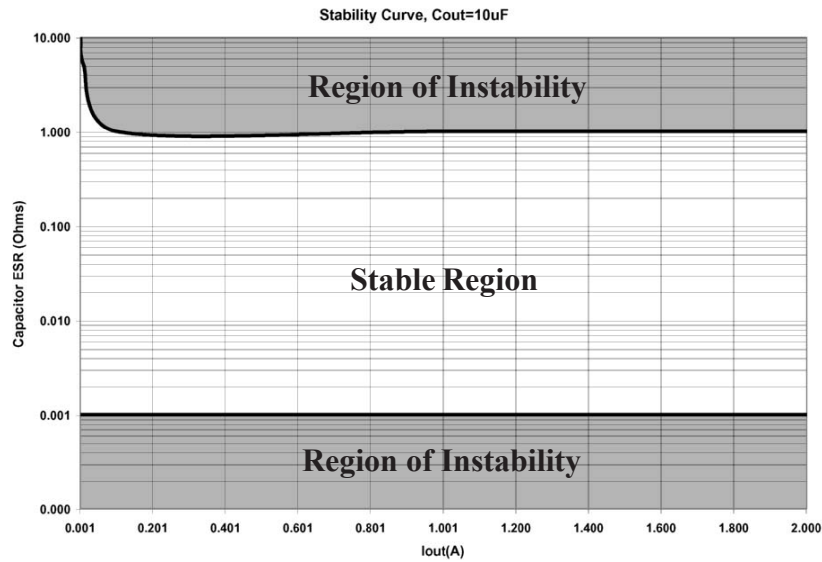
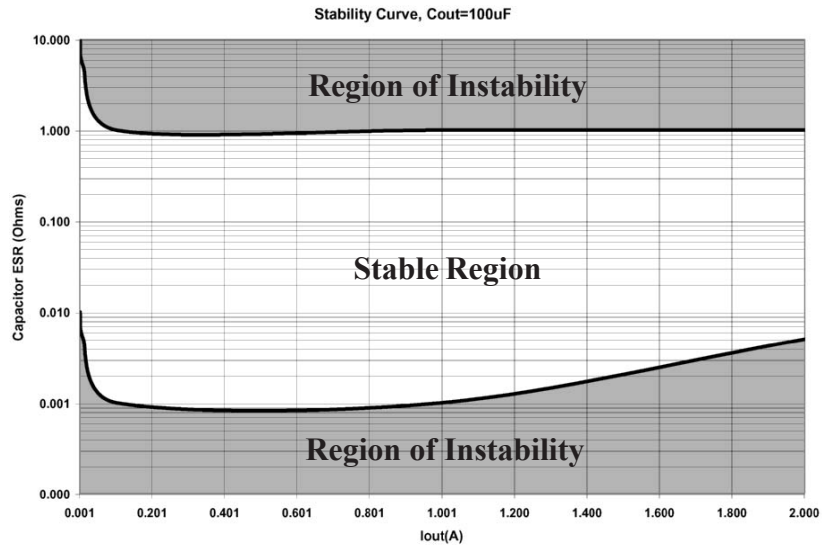
**Pin Descriptions**

Pin Name	Pin Description
ADJ	When this pin is grounded, an internal resistor divider sets the output voltage to 2.5V. If this pin is connected to the Vo pin, the output voltage will be set at 0.8V. If external feedback resistors are used, the output voltage will be (See Application Circuits on page 1):  $V_O = \frac{0.8 (R_1 + R_2)}{R_2} \text{ Volts}$
EN	Enable Input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be enabled if this pin is left open. Connect to VIN if not being used.
GND	Reference ground.
VIN	Input voltage. For regulation at full load, the input to this pin must be between (V <sub>O</sub> + 0.5V) and 5.5V. Minimum VIN = 1.6V. A large bulk capacitance should be placed closely to this pin to ensure that the input supply does not sag below 1.6V. Also a minimum of 4.7uF ceramic capacitor should be placed directly at this pin.
VO	The pin is the power output of the device. A minimum of 10uF ceramic capacitor should be placed directly at this pin.

POWER MANAGEMENT

Block Diagram





**POWER MANAGEMENT**
**Applications Information**
**Introduction**

The SC4215 is intended for applications where high current capability and very low dropout voltage are required. It provides a very simple, low cost solution that uses very little pcb real estate. Additional features include an enable pin to allow for a very low power consumption standby mode, and a fully adjustable output.

**Component Selection**

**Input capacitor:** A minimum of 4.7µF ceramic capacitor is recommended to be placed directly next to the Vin pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, bulk capacitance of about 100µF may be added closely to the input supply pin of the SC4215 to ensure that Vin does not sag, improving load transient response.

**Output capacitor:** A minimum bulk capacitance of 10µF, along with a 0.1µF ceramic decoupling capacitor is recommended. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the SC4215 is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

**Noise immunity:** In very electrically noisy environments, it is recommended that 0.1µF ceramic capacitors be placed from IN to GND and OUT to GND as close to the device pins as possible.

**External voltage selection resistors:** the use of 1% resistors, and designing for a current flow  $\geq 10\mu\text{A}$  is recommended to ensure a well regulated output (thus  $R2 \leq 120\text{k}\Omega$ ).

**Thermal Considerations**

The power dissipation in the SC4215 is approximately equal to the product of the output current and the input to output voltage differential:

$$P_D \approx (V_{IN} - V_{OUT}) \cdot I_O$$

The absolute worst-case dissipation is given by:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \cdot I_{O(MAX)} + V_{IN(MAX)} \cdot I_{Q(MAX)}$$

For a typical scenario,  $V_{IN} = 3.3\text{V} \pm 5\%$ ,  $V_{OUT} = 2.8\text{V}$  and  $I_O = 1.5\text{A}$ , therefore:

$$V_{IN(MAX)} = 3.465\text{V}, V_{OUT(MIN)} = 2.744\text{V} \text{ and } I_{Q(MAX)} = 1.75\text{mA},$$

$$\text{Thus } P_{D(MAX)} = 1.09\text{W}.$$

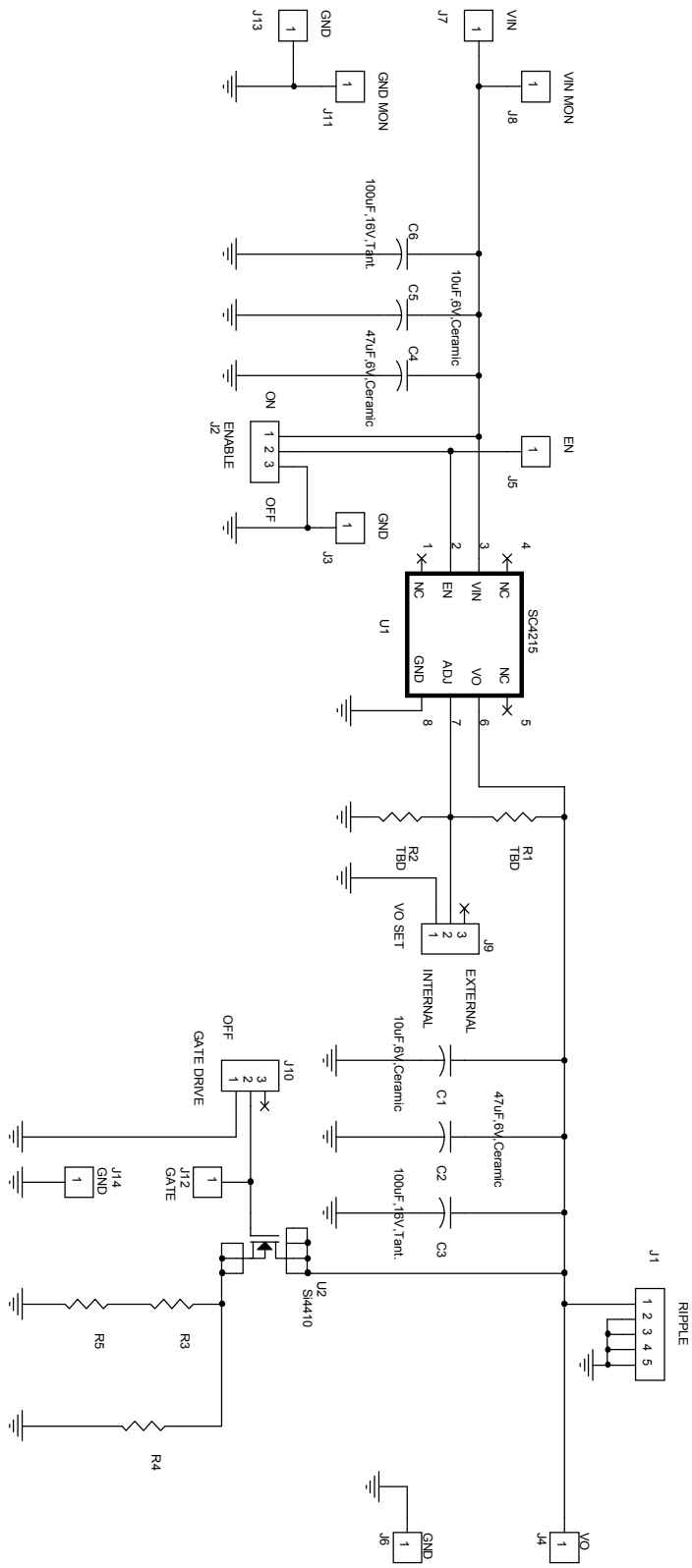
Using this figure, and assuming  $T_{A(MAX)} = 70^\circ\text{C}$ , we can calculate the maximum thermal impedance allowable to maintain  $T_J \leq 150^\circ\text{C}$ :

$$R_{TH(J-A)(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{P_{D(MAX)}} = \frac{(150 - 70)}{1.09} = 73.4^\circ\text{C} / \text{W}$$

This should be achievable for the SOIC-8EDP package using pcb copper area to aid in conducting the heat away, such as one square inch of copper connected to the exposed die pad of the device. Internal ground/power planes and air flow will also assist in removing heat. For higher ambient temperatures it may be necessary to use additional copper area.

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Evaluation Board Schematics



Title	SC4215 Evaluation Board		
Size	Document Number	Rev	
	SC4215_EVB_1a	1A	
Date	Friday, February 14, 2003	Sheet	1 of 1



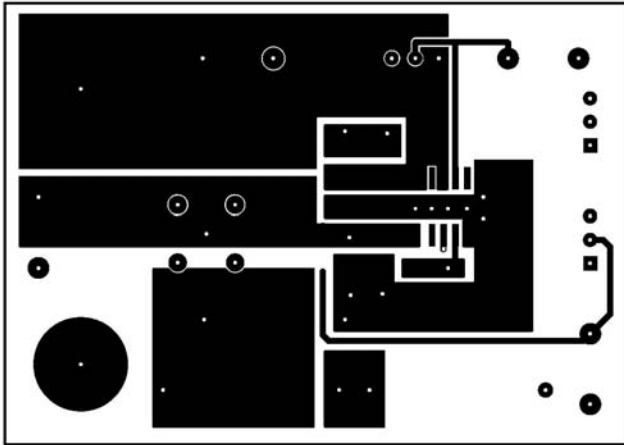
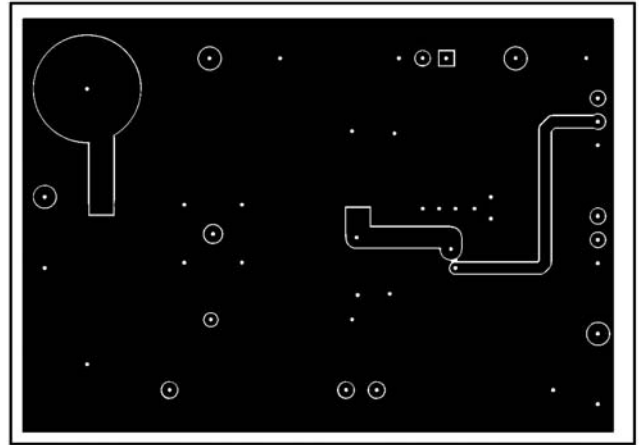
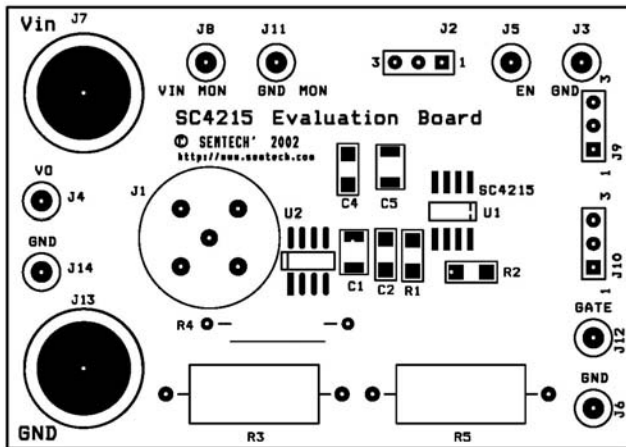
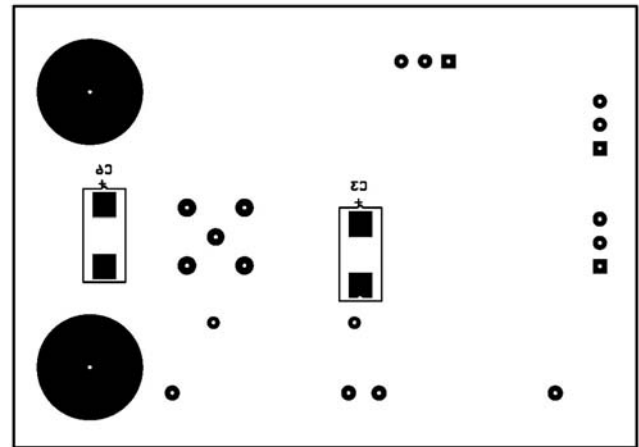
**POWER MANAGEMENT**

**Evaluation Board Bill of Materials**

Revised: Friday, February 14, 2003  
 SC4215 Evaluation Board      Revision: 1A

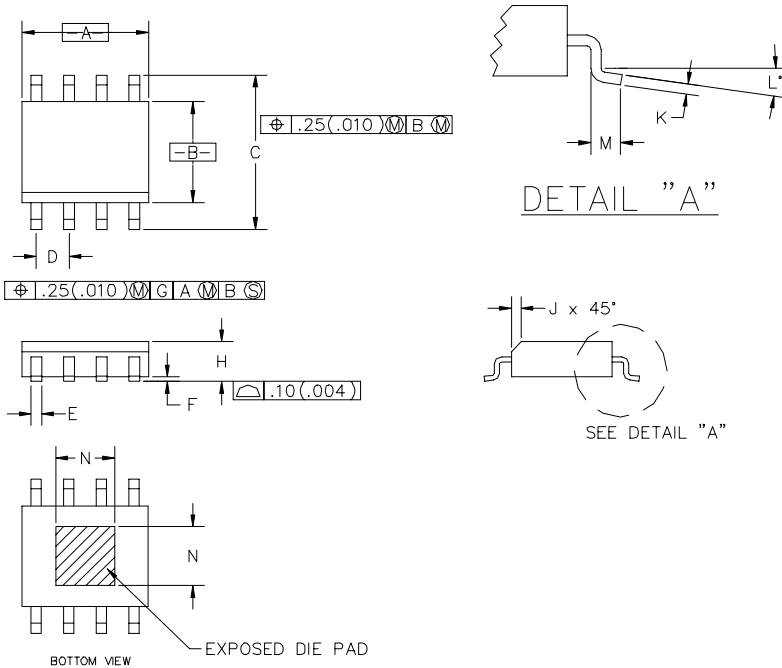
Bill Of Materials    February 14,2003    12:06:33

Item	Quantity	Reference	Part	Manufacturer #	Foot Print
1	2	C5,C1	10uF,6V,Ceramic		murata 3225
2	2	C4,C2	47uF,6V,Ceramic		sm/c 1206
3	2	C3,C6	100uF,16V,Tant.		EEJL1CD476R
4	1	J1	RIPPLE		585-558
5	1	J2	ENABLE		blkcon.100/vh/tm1sq/w.100/3
6	3	J3,J6,J14	GND		5010
7	1	J4	VO		5010
8	1	J5	EN		5010
9	1	J7	VIN		bananasocket
10	1	J8	VIN MON		5010
11	1	J9	VO SET		blkcon.100/vh/tm1sq/w.100/3
12	1	J10	GATE DRIVE		blkcon.100/vh/tm1sq/w.100/3
13	1	J11	GND MON		5010
14	1	J12	GATE		5010
15	1	J13	GND		bananasocket
16	2	R1,R2	TBD		sm/r 1206
17	2	R3,R5			alsr-3
18	1	R4			alsr-1
19	1	U1	SC4215		SO8
20	1	U2	Si4410		sog.050/8/wg.244/l.225

**POWER MANAGEMENT**
**Evaluation Board Gerber Plots**

**Board Layout Assembly Top**

**Board Layout Bottom**

**Board Layout Top**

**Board Layout INNER1**

**POWER MANAGEMENT**

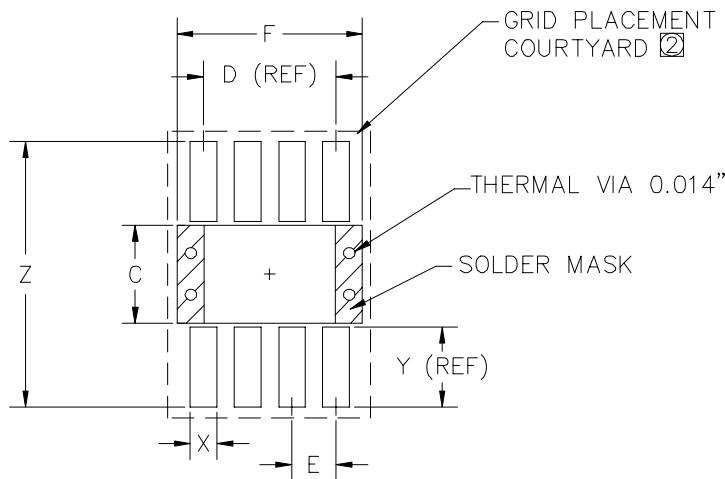
**Outline Drawing - SOIC-8EDP**



DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.189	.195	4.80	4.95	2
B	.152	.157	3.86	4.00	3
C	.230	.244	5.84	6.20	
D	.050	BSC	1.27	BSC	
E	.014	.020	0.35	0.51	
F	.001	.005	.025	.127	
H	.056	.066	1.42	1.68	
J	.010	.016	0.25	0.41	
K	.007	.010	0.19	0.25	
L	0°	8°	0°	8°	
M	.016	.035	0.41	0.89	
N	.086	.094	2.19	2.39	4

- ④ END USER SHOULD VERIFY ACTUAL SIZE OF EXPOSED THERMAL DIE PAD FOR SPECIFIC DEVICE APPLICATION.
- ③ DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTUSIONS. INTER-LEAD FLASH AND PROTUSIONS SHALL NOT EXCEED .25 mm (.010") PER SIDE.
- ② DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTUSIONS OR GATE BURRS. MOLD FLASH, PROTUSIONS AND GATE BURRS SHALL NOT EXCEED .15 mm (.010") PER SIDE.
- ① CONTROLLING DIMENSION : MILLIMETER

**Land Pattern - SOIC-8EDP**



DIM <sup>N</sup>	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	.095	.100	2.41	2.54	—
D	—	.150	—	3.81	REF
E	—	.050	—	1.27	BSC
F	.200	.210	5.08	5.33	—
X	.025	.030	0.64	0.80	—
Y	.070	.075	1.78	1.91	REF
Z	.310	.320	7.87	8.13	—

- ② GRID PLACEMENT COURTYARD IS 12 X 16 ELEMENTS (6mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.
- ① CONTROLLING DIMENSIONS: MILLIMETERS.

**POWER MANAGEMENT****Contact Information**

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