OV7660/OV7161 CMOS VGA (640x480) CAMERACHIP™ with OmniPixel™ Technology

General Description

The OV7660/OV7161 CAMERACHIP™ is a low voltage CMOS image sensor that provides the full functionality of a single-chip VGA camera and image processor in a small footprint package. The OV7660/OV7161 provides full-frame, sub-sampled or windowed 8-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 30 frames per second (fps) in VGA with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface. In addition, OmniVision CAMERACHIPS use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise (FPN), smearing, blooming, etc., to produce a clean, fully stable color image.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable applications
- Standard SCCB interface
- VGA, QVGA, QQVGA, CIF, QCIF, QQCIF and windowed outputs with Raw RGB, RGB (GRB 4:2:2), YUV (4:2:2) and YCbCr (4:2:2) formats
- VarioPixel™ method for sub-sampling formats
- Automatic image control functions including: Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Brightness Control (ABC), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), and anti-blooming

Ordering Information

Product	Package
OV07660-KL6A (Color)	CSP-22
OV07161-KL6A (B&W with microlens)	CSP-22

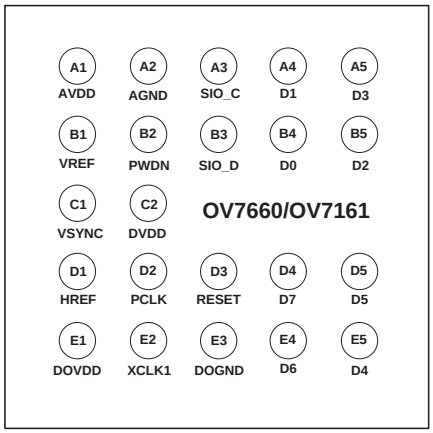
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

Array Element (VGA)		664 x 492
Power Supply	**Digital Core**	1.8VDC
	Analog	2.45V to 2.8V
	I/O	2.5V to (V_{DD-A}+0.3V)
Power Requirements	**Active**	40 mW without loading
	Standby	< 10 µA
Temperature Range	**Operation**	-20°C to 80°C
	Stable Image	-10°C to 60°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB 4:2:2 • Raw RGB Data
Lens Size		1/5"
Lens Chief Ray Angle		~20°
Max Image Transfer Rate	**VGA, CIF, QCIF, QQCIF**	30 fps
	QVGA, QQVGA	60 fps
Sensitivity		1.0 V/Lux-sec
S/N Ratio		> 48 dB (AGC off, Gamma=1)
Dynamic Range		> 72 dB
Scan Mode		Progressive
Electronics Exposure		Up to 510:1 (for selected fps)
Gamma Correction		0.45/0.55/1.00
Pixel Size		4.2 µm x 4.2 µm
Dark Current		30 mV/s at 60°C
Well Capacity		35 K e
Fixed Pattern Noise		< 0.03% of $V_{PEAK-TO-PEAK}$
Image Area		2.76 mm x 2.05 mm
Package Dimensions		4155 µm x 3975 µm

Figure 1 OV7660/OV7161 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV7660/OV7161 image sensor. The OV7660/OV7161 includes:

- Image Sensor Array
- Analog Signal Processor
- A/D Converters
- Digital Signal Processor (DSP)
- Output Formatter
- Timing Generator
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram

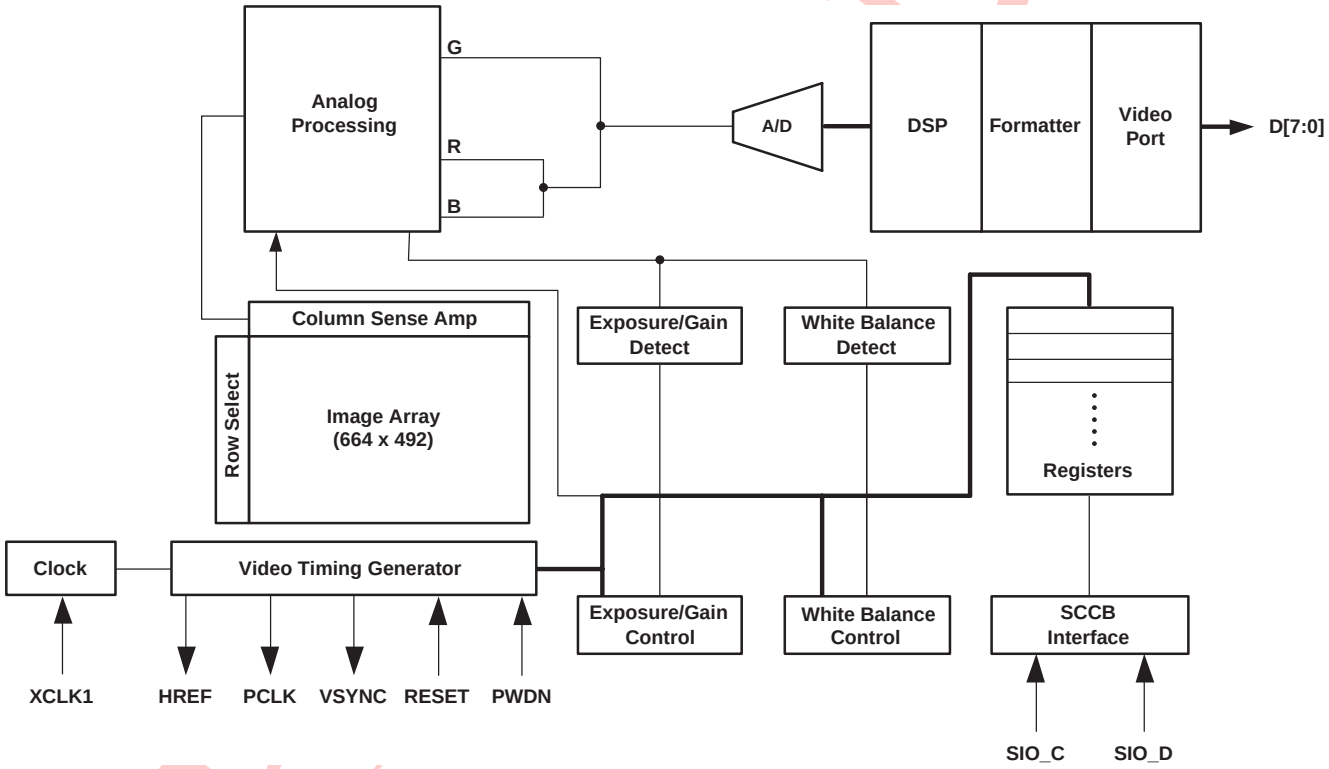
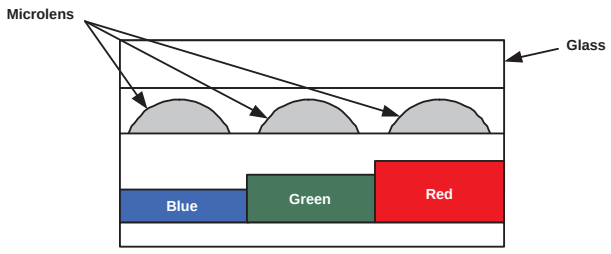


Image Sensor Array

The OV7660/OV7161 sensor has an active image array of 640 columns x 480 rows (307,200 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation (7 different format outputs)
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)

A/D Converters

After the Analog Processing block, the bayer pattern Raw signal is fed to a 10-bit analog-to-digital (A/D) converter shared by G and BR channels. This A/D converter operates at speeds up to 12 MHz and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Digital Video Port

Register bits COM2[1:0] increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Number	Name	Pin Type	Function/Description
A1	AVDD	Power	Analog power supply (+2.5 VDC)
A2	AGND	Power	Analog ground
A3	SIO_C	Input	SCCB serial interface clock input
A4	D1[a]	Output	YUV/RGB video component output bit[1]
A5	D3	Output	YUV/RGB video component output bit[3]
B1	VREF	Reference	Reference voltage - connect to ground using a 0.1 µF capacitor
B2	PWDN	Input (0)[b]	Power Down Mode Selection 0: Normal mode 1: Power down mode
B3	SIO_D	I/O	SCCB serial interface data I/O
B4	D0	Output	YUV/RGB video component output bit[0]
B5	D2	Output	YUV/RGB video component output bit[2]
C1	VSYNC	Output	Vertical sync output
C2	DVDD	Power	Power supply (+1.8 VDC) for digital logic core
D1	HREF	Output	HREF output
D2	PCLK	Output	Pixel clock output
D3	RESET	Input (0)	Clears all registers and resets them to their default values.
D4	D7	Output	YUV/RGB video component output bit[7]
D5	D5	Output	YUV/RGB video component output bit[5]
E1	DOVDD	Power	Digital power supply for I/O (V_{DD-IO} = 2.5 to (V_{DD-A}+03.V))
E2	XCLK1	Input	System clock input
E3	DOGND	Power	Digital ground
E4	D6	Output	YUV/RGB video component output bit[6]
E5	D4	Output	YUV/RGB video component output bit[4]

a. D[7:0] for 8-bit YUV or RGB (D[7] MSB, D[0] LSB)

b. Input (0) represents an internal pull-down resistor.

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-C}	3 V
	V_{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+1V
Lead-free Temperature, Surface-mount process		245ºC
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	–	2.45	2.5	2.8	V
V_{DD-C}	DC supply voltage – Digital Core	–	1.62	1.8	1.98	V
V_{DD-IO}	DC supply voltage – I/O power	–	2.25		V_{DD-A}+0.3V	V
I_{DDA}	Active (Operating) Current	See Note [a]		20		mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current			10	20	µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 2.5V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 7.5 fps YUV output, no I/O loading

b. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 2.5V
$I_{DDS:SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS:PWDN}$ refers to a PWDN pin-initiated Standby

c. Standard Output Loading = 25pF, 1.2KΩ

Table 4 Functional and AC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			18	dB
	Red/Blue Adjustment Range			12	dB
Inputs (PWDN, CLK, RESET)					
f_{CLK}	Input Clock Frequency	10	24	48	MHz
t_{CLK}	Input Clock Period	21	42	100	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB Timing (see Figure 4)					
f_{SIO_C}	Clock Frequency			150	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and D[7:0] (see Figure 5, Figure 6, Figure 7, Figure 9, and Figure 10)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	D[7:0] Setup time	15			ns
t_{HD}	D[7:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-C} = 1.8V, V_{DD-A} = 2.5V, V_{DD-IO} = 2.5V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 2.5V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

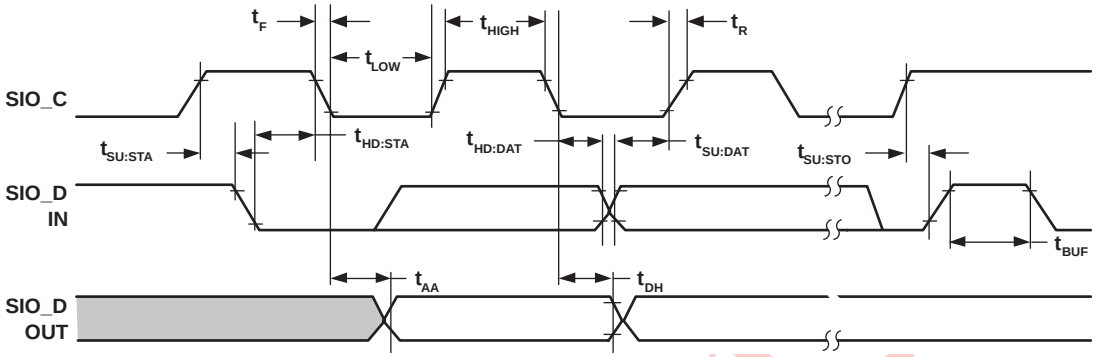


Figure 5 Horizontal Timing

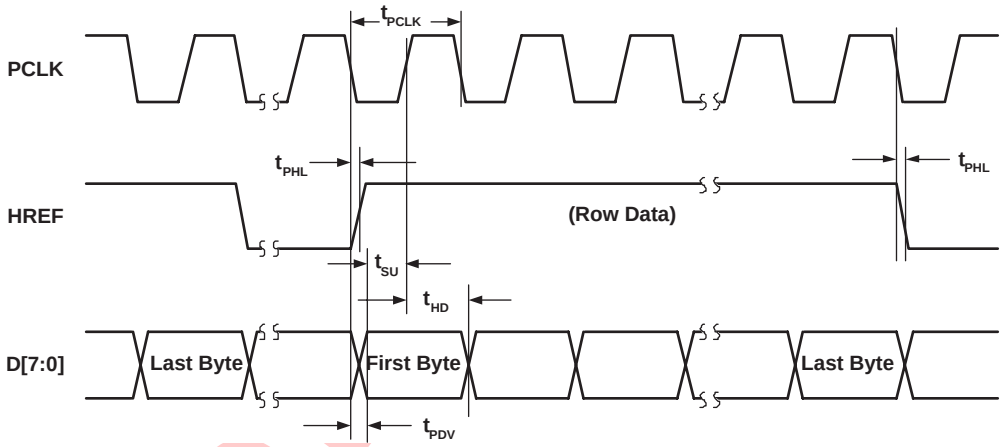
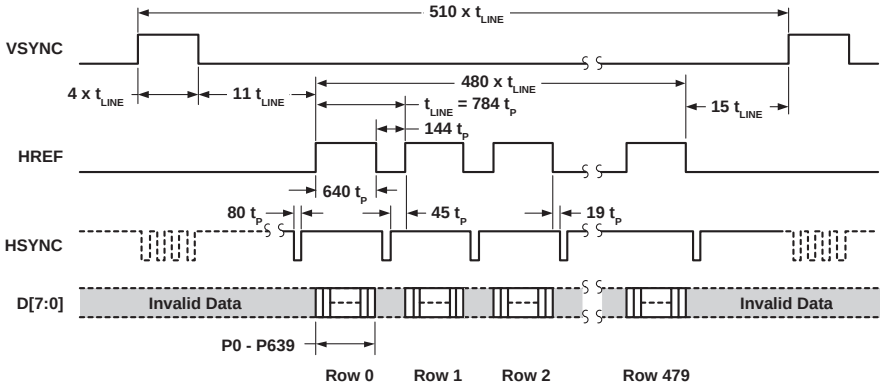
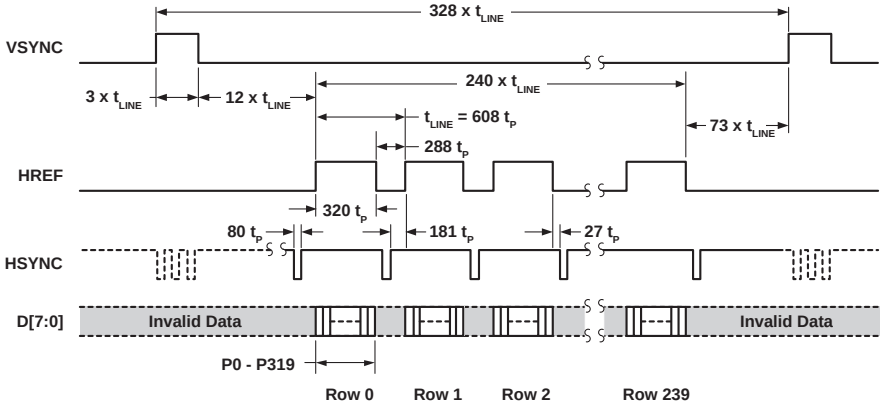


Figure 6 VGA Frame Timing



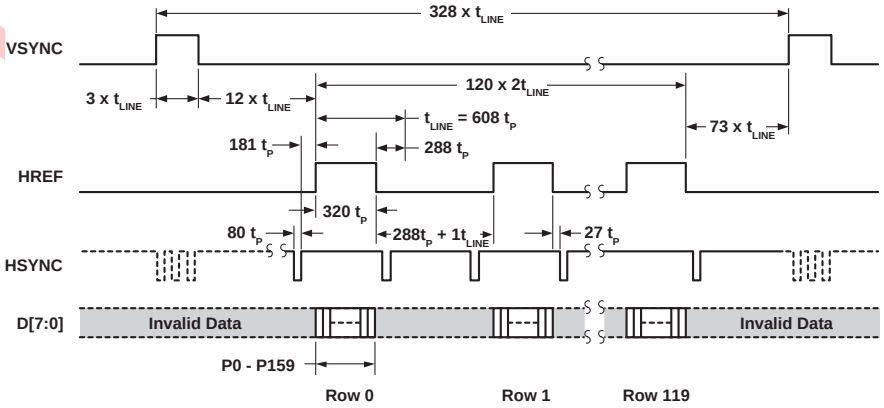
NOTE:
For Raw data, $t_P = t_{PCLK}$
For YUV/RGB, $t_P = 2 \times t_{PCLK}$

Figure 7 QVGA Frame Timing



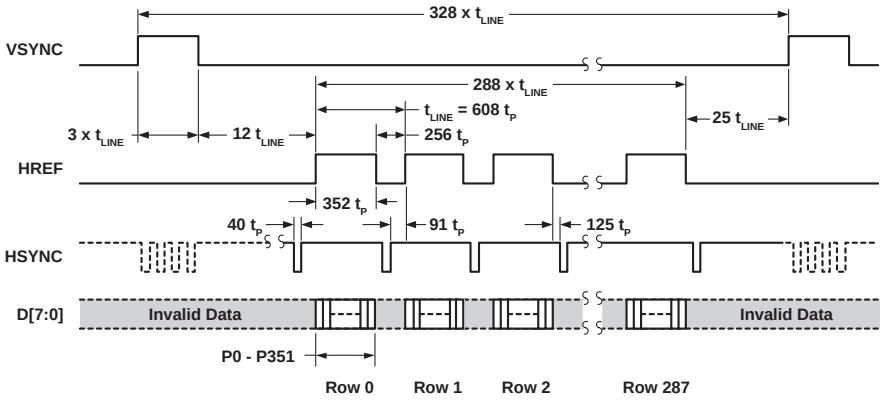
NOTE:
For Raw data, $t_P = t_{PCLK}$
For YUV/RGB, $t_P = 2 \times t_{PCLK}$

Figure 8 QQVGA Frame Timing



NOTE:
For Raw data, $t_P = t_{PCLK} / 2$
For YUV/RGB, $t_P = t_{PCLK}$

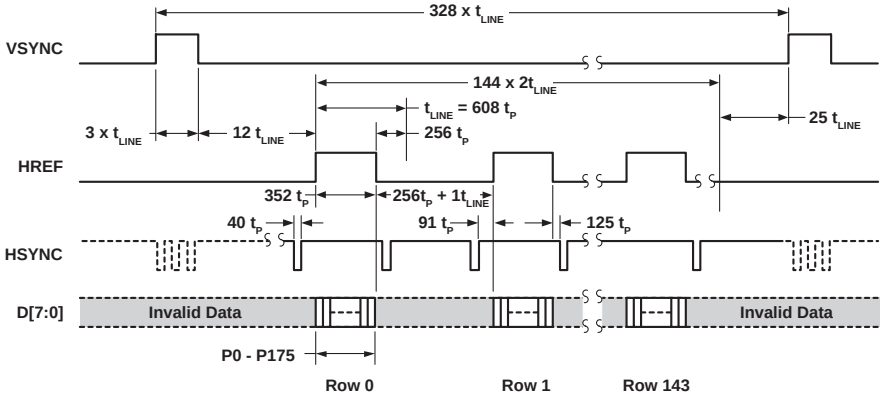
Figure 9 CIF Frame Timing



NOTE:
For Raw data, $t_P = t_{PCLK}$

For YUV/RGB, $t_P = 2 \times t_{PCLK}$

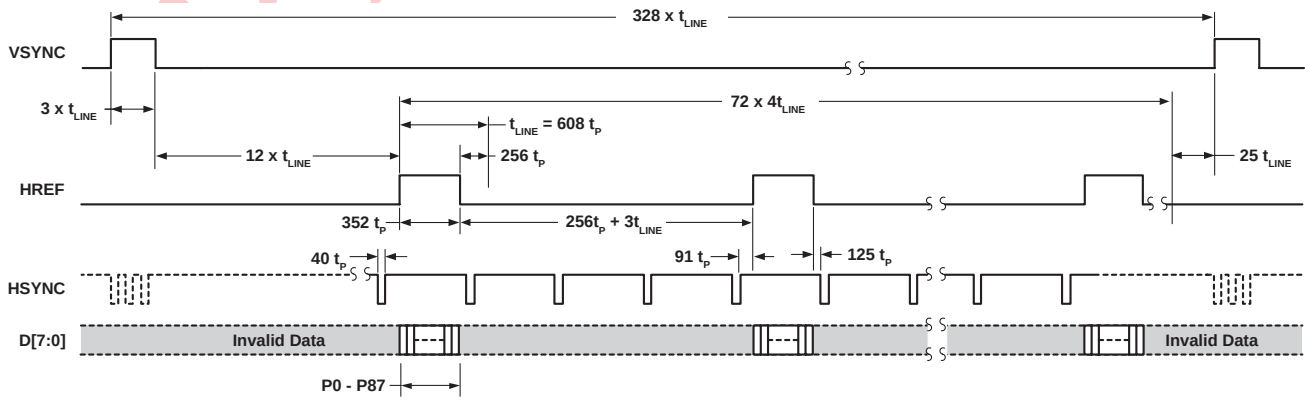
Figure 10 QCIF Frame Timing



NOTE:
For Raw data, $t_P = t_{PCLK} / 2$

For YUV/RGB, $t_P = t_{PCLK}$

Figure 11 QQCIF Frame Timing



NOTE:
For Raw data, $t_P = t_{PCLK} / 4$

For YUV/RGB, $t_P = t_{PCLK} / 2$

Figure 12 RGB 565 Output Timing Diagram

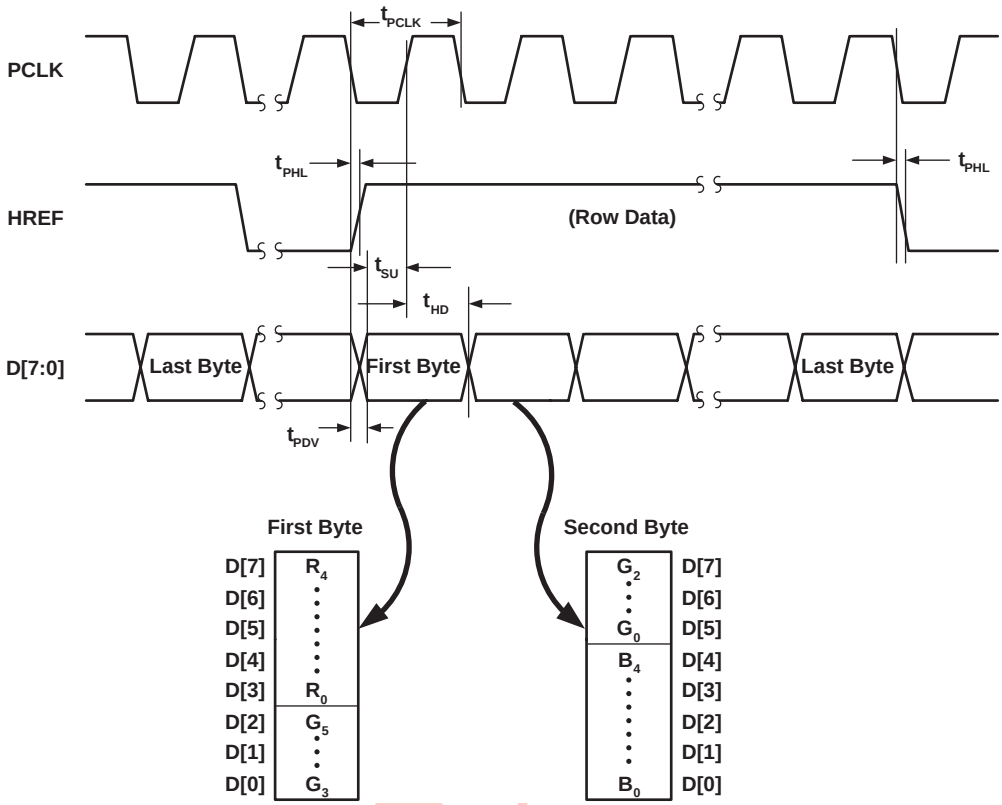
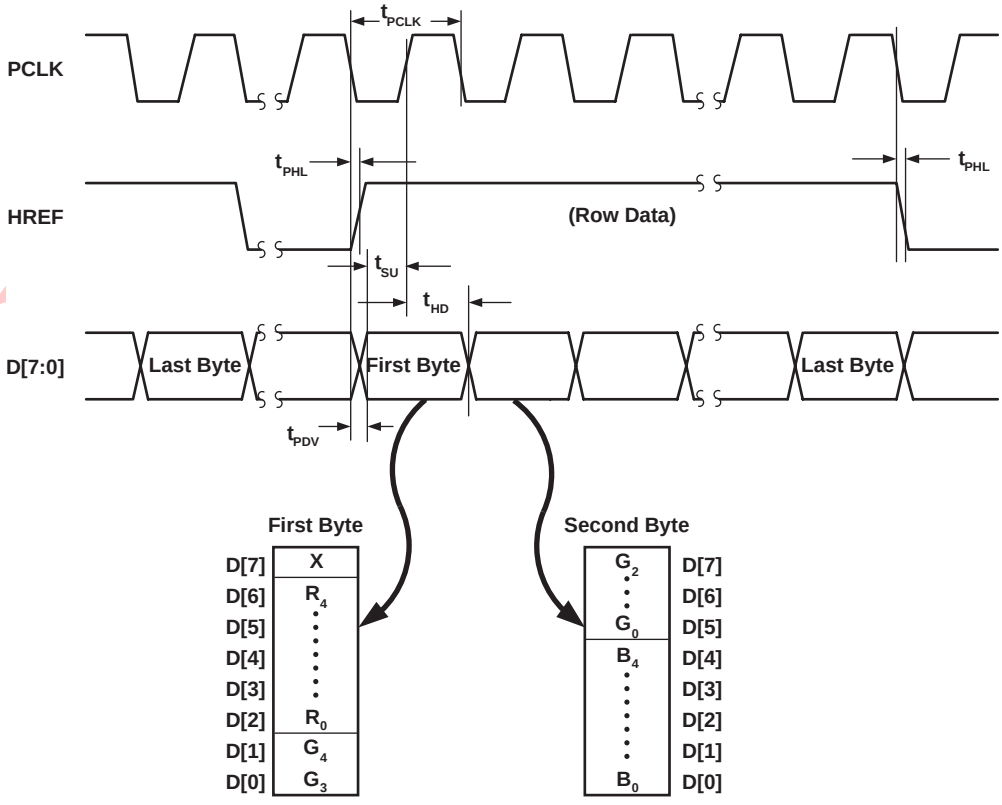
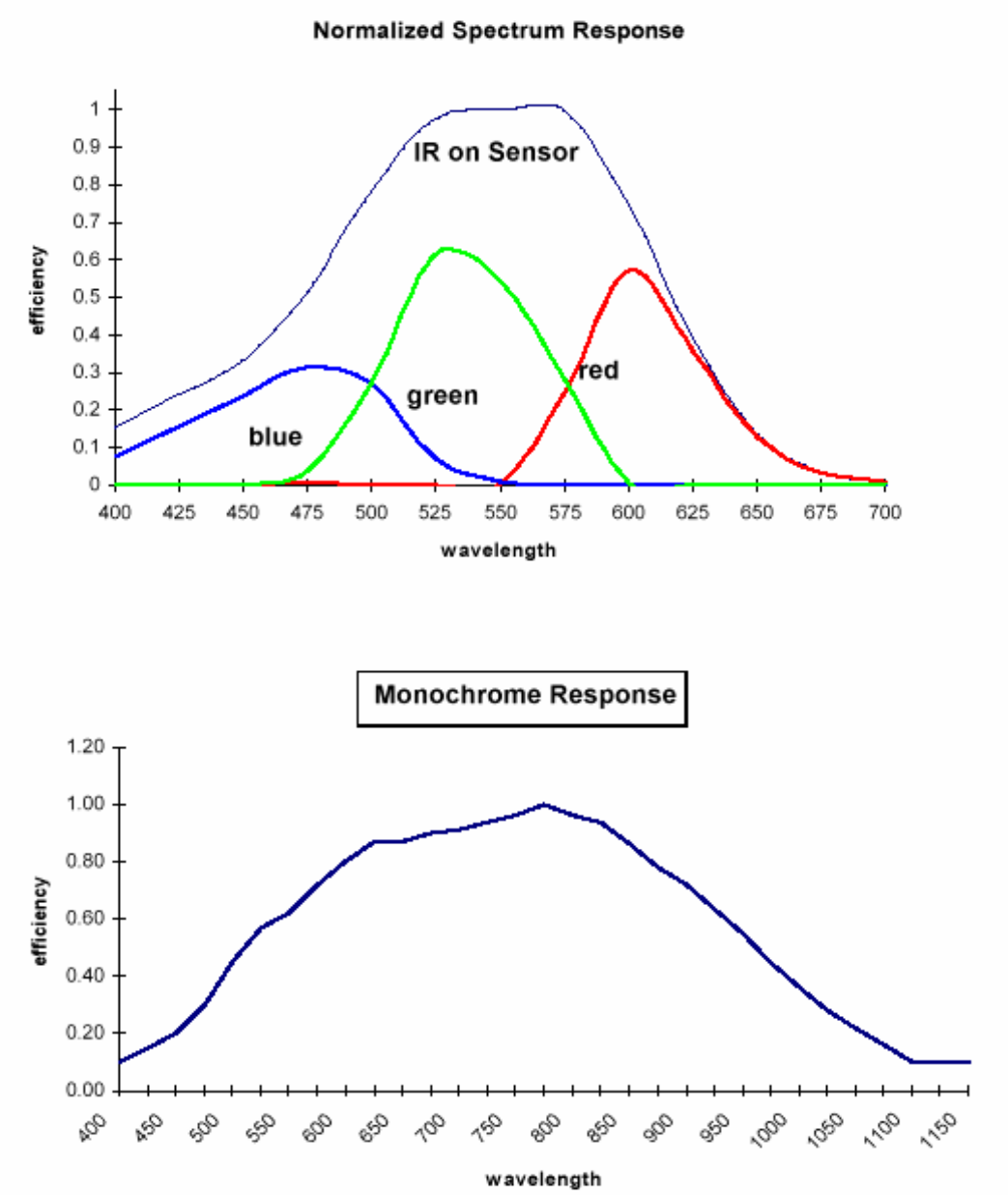


Figure 13 RGB 555 Output Timing Diagram



OV7660/OV7161 Light Response

Figure 14 OV7660/OV7161 Light Response



Register Set

Table 5 provides a list and description of the Device Control registers contained in the OV7660/OV7161. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 42 for write and 43 for read.

Table 5 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting • Range: [00] to [7F]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF]
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF]
03	VREF	00	RW	Vertical Frame Control Bit[7:6]: AGC[9:8] Bit[5]: Fix gain1 Bit[4]: Fix gain0 Bit[3:2]: VREF end low 2 bits (high 8 bits at VSTOP[7:0] Bit[1:0]: VREF start low 2 bits (high 8 bits at VSTRT[7:0]
04	COM1	00	RW	Common Control 1 Bit[7]: Reserved Bit[6]: CCIR656 format Bit[5]: QQVGA or QQCIF format. Effective only when QVGA or QCIF output is selected (register bit COM7[4] or COM7[3]) and related HREF skip mode based on format is selected (register COM1[3:2]) Bit[4]: Reserved Bit[3:2]: HREF skip option 00: No skip 01: YUV/RGB skip every other row for YUV/RGB, skip 2 rows for every 4 rows for Raw data 1x: Skip 3 rows for every 4 rows for YUV/RGB, skip 6 rows for every 8 rows for Raw data Bit[1:0]: AEC low 2 LSB (see registers AECHH for AEC[15:10] and AECH for AEC[9:2])
05	BAVE	00	RW	U/B Average Level Automatically updated based on chip output format
06	GEAVE	00	RW	Y/Ge Average Level Automatically updated based on chip output format
07	AECHH	00	RW	Exposure Value - AEC MSB 5 bits Bit[7:6]: Reserved Bit[5:0]: AEC[15:10] (see registers AECH for AEC[9:2] and COM1 for AEC[1:0])
08	RAVE	00	RW	V/R Average Level Automatically updated based on chip output format

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
09	COM2	01	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Soft sleep mode Bit[3:2]: Reserved Bit[1:0]: Output Drive Capability 00: 1x 01: 2x 10: 2x 11: 4x
0A	PID	76	R	Product ID Number MSB (Read only)
0B	VER	60	R	Product ID Number LSB (Read only)
0C	COM3	00	RW	Common Control 3 Bit[7]: Reserved Bit[6]: Output data MSB and LSB swap Bit[5]: Tri-state option for output clock at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[4]: Tri-state option for output data at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[3:2]: Horizontal average control x0: No average 01: 2 pixel average 11: 4 pixel average Bit[1]: VarioPixel for QVGA, QQVGA, CIF, QCIF, and QQCIF Bit[0]: Single frame output (used for Frame Exposure mode only)
0D	COM4	40	RW	Common Control 4 Bit[7:0]: Reserved
0E	COM5	01	RW	Common Control 5 Bit[7]: System clock selection. If the system clock is 48 MHz, this bit should be set to high to get a higher frame rate Bit[6:0]: Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0F	COM6	43	RW	Common Control 6 Bit[7]: Output of optical black line option 0: Disable HREF at optical black 1: Enable HREF at optical black Bit[6]: BLC input selection 0: Use electrical black line as BLC signal 1: Use optical black line as BLC signal Bit[5:4]: Reserved Bit[3]: Enable bias for ADBLC Bit[2]: ADBLC offset 0: Use 4-channel ADBLC 1: Use 2-channel ADBLC Bit[1]: Reset all timing when format changes Bit[0]: Enable ADBLC option
10	AECH	40	RW	Exposure Value Bit[7:0]: AEC[9:2] (see registers AECHH for AEC[15:10] and COM1 for AEC[1:0])
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7]: Digital PLL option 0: Disable double clock option, meaning the maximum PCLK can be as high as half input clock 1: Enable double clock option, meaning the maximum PCLK can be as high as input clock Bit[6]: Use external clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar F(internal clock) = F(input clock)/(Bit[5:0]+1) • Range: [0 0000] to [1 1111]
12	COM7	00	RW	Common Control 7 Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: Reserved Bit[5]: Output format - CIF selection Bit[4]: Output format - QVGA selection Bit[3]: Output format - QCIF selection Bit[2]: Output format - RGB selection Bit[1]: Reserved Bit[0]: Output format - Raw RGB (COM7[2] must be set high)

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	COM8	8F	RW	Common Control 8 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - Step size limit 0: 1/16 x AEC 1: Step size = AEC Bit[5]: Banding filter ON/OFF - In order to turn ON the banding filter, BD50ST (0x9D) or BD60ST (0x9E) must be set to a non-zero value. Bit[4:3]: Reserved Bit[2]: AGC Enable Bit[1]: AWB Enable Bit[0]: AEC Enable
14	COM9	4A	RW	Common Control 9 Bit[7]: Reserved Bit[6:4]: Automatic Gain Ceiling - maximum AGC value 000: 2x 001: 4x 010 8x 011: 16x 100: 32x 101 64x 110: 128x 111: 128x Bit[3]: Reserved Bit[2]: Data format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than VSYNC Bit[0]: Freeze AGC/AEC
15	COM10	00	RW	Common Control 10 Bit[7]: Reserved Bit[6]: HREF changes to HSYNC Bit[5]: PCLK output option 0: PCLK always output 1: No PCLK output when HREF is low Bit[4]: PCLK reverse Bit[3]: HREF reverse Bit[2]: Reserved Bit[1]: VSYNC negative Bit[0]: HSYNC negative
16	RSVD	XX	–	Reserved
17	HSTART	11	RW	Output Format - Horizontal Frame (HREF column) start high 8-bit (low 3 bits are at HREF[2:0])
18	HSTOP	61	RW	Output Format - Horizontal Frame (HREF column) end high 8-bit (low 3 bits are at HREF[5:3])

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
19	VSTRT	02	RW	Output Format - Vertical Frame (row) start high 8-bit (low 2 bits are at VREF[1:0])
1A	VSTOP	7A	RW	Output Format - Vertical Frame (row) end high 8-bit (low 2 bits are at VREF[3:2])
1B	PSHFT	00	RW	Data Format - Pixel Delay Select (delays timing of the D[7:0] data relative to HREF in pixel units) • Range: [00] (no delay) to [FF] (256 pixel delay which accounts for whole array)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	MVFP	00	RW	Mirror/VFlip Enable Bit[7]: 2x gain Bit[6]: Reserved Bit[5]: Mirror 0: Normal image 1: Mirror image Bit[4]: VFlip enable 1: VFlip enable Bit[3:0]: Reserved
1F	LAEC	00	RW	Reserved
20	BOS	80	RW	B Channel ADBLC Result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range (high 7 bits)
21	GBOS	80	RW	Gb channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
22	GROS	80	RW	Gr channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
23	ROS	80	RW	R channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
24	AEW	78	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	AEB	68	RW	AGC/AEC - Stable Operating Region (Lower Limit)

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
26	VPT	D4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: High nibble of upper limit Bit[3:0]: High nibble of lower limit
27	BBIAS	80	RW	B Channel Signal Output Bias (effective only when COM6[3] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
28	GbBIAS	80	RW	Gb Channel Signal Output Bias (effective only when COM6[3] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
29	RSVD	XX	–	Reserved
2A	EXHCH	00	RW	Dummy Pixel Insert MSB Bit[7]: Reserved Bit[6:4]: 3 MSB for dummy pixel insert in horizontal direction Bit[3:2]: HSYNC falling edge delay 2 MSB Bit[1:0]: HSYNC rising edge delay 2 MSB
2B	EXHCL	00	RW	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction
2C	RBIAS	80	RW	R Channel Signal Output Bias (effective only when COM6[3] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
2D	ADVFL	00	RW	LSB of insert dummy lines in vertical direction (1 bit equals 1 line)
2E	ADVFH	00	RW	MSB of insert dummy lines in vertical direction
2F	YAVE	00	RW	Y/G Channel Average Value
30	HSYST	08	RW	HSYNC Rising Edge Delay (low 8 bits)
31	HSYEN	30	RW	HSYNC Falling Edge Delay (low 8 bits)
32	HREF	A4	RW	HREF Control Bit[7:6]: HREF edge offset to data output Bit[5:3]: HREF end 3 LSB (high 8 MSB at register HSTOP) Bit[2:0]: HREF start 3 LSB (high 8 MSB at register HSTART)
33	CHLF	00	RW	Array Current Control Bit[7:0]: Reserved
34	ARBLM	03	RW	Array Reference Control Bit[7:0]: Reserved
35-36	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
37	ADC	04	RW	ADC Control Bit[7:4]: Reserved Bit[3]: ADC range adjustment 0: 1x range 1: 1.5x range Bit[2:0]: ADC range adjustment 000: 0.8x 100: 1x 111: 1.2x
38	ACOM	12	RW	ADC and Analog Common Mode Control Bit[7:4]: Reserved Bit[3:2]: ADC offset positive to make output greater than zero Bit[1:0]: Reserved
39	OFON	00	RW	ADC Offset Control Bit[7:4]: Reserved Bit[3]: Line buffer power down - must be set to "1" before chip power down Bit[2:0]: Reserved
3A	TSLB	0C	RW	Line Buffer Test Option Bit[7:5]: Reserved Bit[4]: UV output value 0: Use normal UV output 1: Use fixed UV value set in registers MANU and MANV as UV output instead of chip output Bit[3:2]: Output sequence 00: Y U Y V 01: Y V Y U 10: V Y U Y 11: U Y V Y Bit[1]: Reserved Bit[0]: Data output window reset enable

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3B	COM11	00	RW	Common Control 11 Bit[7]: Night mode 0: Night mode disable 1: Night mode enable - If the AGC gain goes over 2, then AGC gain drops to 0 and frame rate changes by half. COM11[6:5] limits the minimum frame rate. Also, ADVFH and ADVFL will be automatically updated. Bit[6:5]: Night mode insert frame option 00: Normal frame rate 01: 1/2 frame rate 10: 1/4 frame rate 11: 1/8 frame rate Bit[4]: Reserved Bit[3]: Banding filter value select 0: Select BD60ST[7:0] (0x9E) as Banding Filter Value 1: Select BD50ST[7:0] (0x9D) as Banding Filter Value Bit[2:0]: Reserved
3C	COM12	40	RW	Common Control 12 Bit[7]: HREF option 0: No HREF when VREF is low 1: Always has HREF Bit[6:3]: Reserved Bit[2]: Enable UV average Bit[1:0]: Reserved
3D	COM13	99	RW	Common Control 13 Bit[7:6]: Gamma selection for signal 00: No gamma function 01: Gamma used for Y channel only 10: Gamma used for Raw data before interpolation 11: Not allowed Bit[5]: Reserved Bit[4]: Enable color matrix for RGB or YUV Bit[3]: Enable Y channel delay option Bit[2:0]: Output Y/UV delay
3E	COM14	0E	RW	Common Control 14 Bit[7:0]: Reserved
3F	EDGE	88	RW	Edge Enhancement Adjustment Bit[7:2]: Edge enhancement threshold[7:2] Bit[1:0]: Edge enhancement factor[3:2] (see register DSPC2[7:6] for Edge enhancement factor[1:0])

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
40	COM15	C0	RW	Common Control 15 Bit[7:6]: Data format - output full range enable 0x: Output range: [10] to [F0] 10: Output range: [01] to [FE] 11: Output range: [00] to [FF] Bit[5:4]: RGB 555/565 option (must set COM7[2] = 1 and COM7[0] = 0) x0: Normal RGB output 01: RGB 565 11: RGB 555 Bit[3:0]: Reserved
41	COM16	10	RW	Common Control 16 Bit[7:6]: Reserved Bit[5]: Enable edge enhancement for YUV output (effective only for YUV/RGB, no use for Raw data) Bit[4]: Edge enhancement option 0: Edge enhancement factor = (EDGE[1:0], DSPC2[7:6]) 1: Edge enhancement factor = 2 x (EDGE[1:0], DSPC2[7:6]) Bit[3:2]: Reserved Bit[1]: Color matrix coefficient double option Bit[0]: RB average option for interpolation
42	COM17	08	RW	Common Control 17 Bit[7:3]: Reserved Bit[2]: Select single frame out Bit[1]: Tri-state output after single frame out Bit[0]: Reserved
43-4E	RSVD	XX	–	Reserved
4F	MTX1	58	RW	Matrix Coefficient 1
50	MTX2	48	RW	Matrix Coefficient 2
51	MTX3	10	RW	Matrix Coefficient 3
52	MTX4	28	RW	Matrix Coefficient 4
53	MTX5	48	RW	Matrix Coefficient 5
54	MTX6	70	RW	Matrix Coefficient 6
55	MTX7	40	RW	Matrix Coefficient 7
56	MTX8	40	RW	Matrix Coefficient 8
57	MTX9	40	RW	Matrix Coefficient 9
58	MTXS	0F	RW	Matrix Coefficient Sign for coefficient 9 to 2 0: Plus 1: Minus
59-61	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
62	LCC1	00	RW	Lens Correction Option 1
63	LCC2	00	RW	Lens Correction Option 2
64	LCC3	10	RW	Lens Correction Option 3
65	LCC4	80	RW	Lens Correction Option 4
66	LCC5	00	RW	Lens Correction Control Bit[7:3]: Reserved Bit[2]: Lens correction control select Bit[1]: Reserved Bit[0]: Lens correction enable
67	MANU	80	RW	Manual U Value (effective only when register TSLB[4] is high)
68	MANV	80	RW	Manual V Value (effective only when register TSLB[4] is high)
69	HV	00	RW	Manual Banding Filter MSB Bit[7:6]: B channel pre-gain Bit[5:4]: R channel pre-gain Bit[3:1]: Reserved Bit[0]: Matrix coefficient 1 sign
6A	GGAIN	00	RW	Reserved
6B	DBLV	3A	RW	Band Gap Reference Adjustment Bit[7:4]: Reserved Bit[3:0]: Band gap reference adjustment
6C-7B	GSP	XX	RW	Gamma curve
7C-8A	GST	XX	RW	Gamma curve
8B-91	RSVD	XX	–	Reserved
92	DM_LNL	00	RW	Dummy Line low 8 bits
93	DM_LNH	00	RW	Dummy Line high 8 bits
94-9C	RSVD	XX	–	Reserved
9D	BD50ST	99	RW	50 Hz Banding Filter Value (effective only when COM8[5] is low and COM11[3] is high)
9E	BD60ST	7F	RW	60 Hz Banding Filter Value (effective only when COM8[5] is low and COM11[3] is low)
9F	RSVD	XX	–	Reserved
A0	DSPC2	00	RW	DSP Control 2 Bit[7:6]: Edge enhancement factor[1:0] (see register EDGE[1:0] for Edge enhancement factor[3:2]) Bit[5:0]: Reserved
A1-A5	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7660/OV7161 uses a 22-ball Chip Scale Package (CSP). Refer to Figure 15 for package information, Table 6 for package dimensions and Figure 16 for the array center on the chip.

Note: For OVT devices that contain lead, all part marking letters are upper case. For OVT devices that are lead-free, all part marking letters are lower case

Figure 15 OV7660/OV7161 Package Specifications

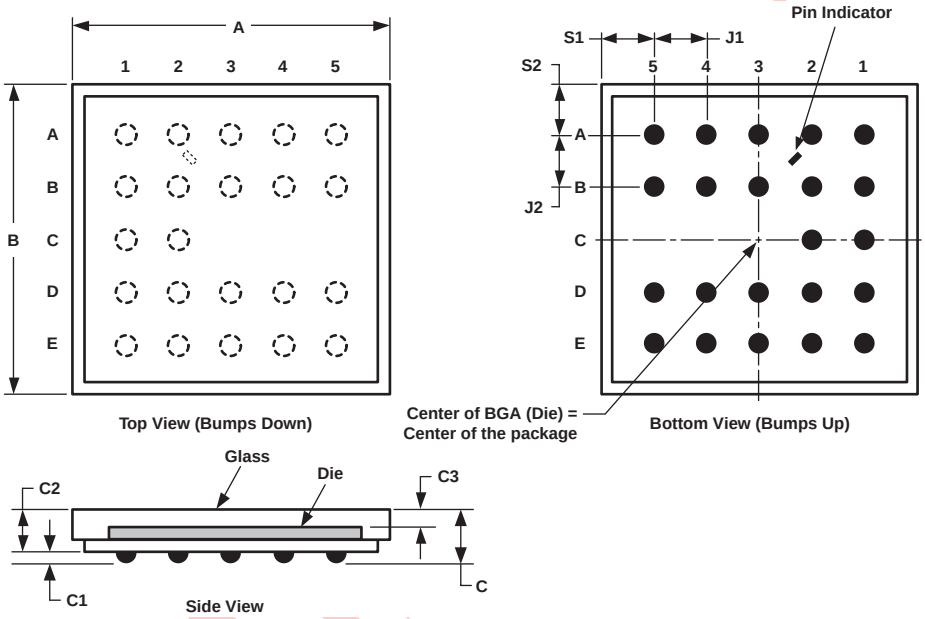
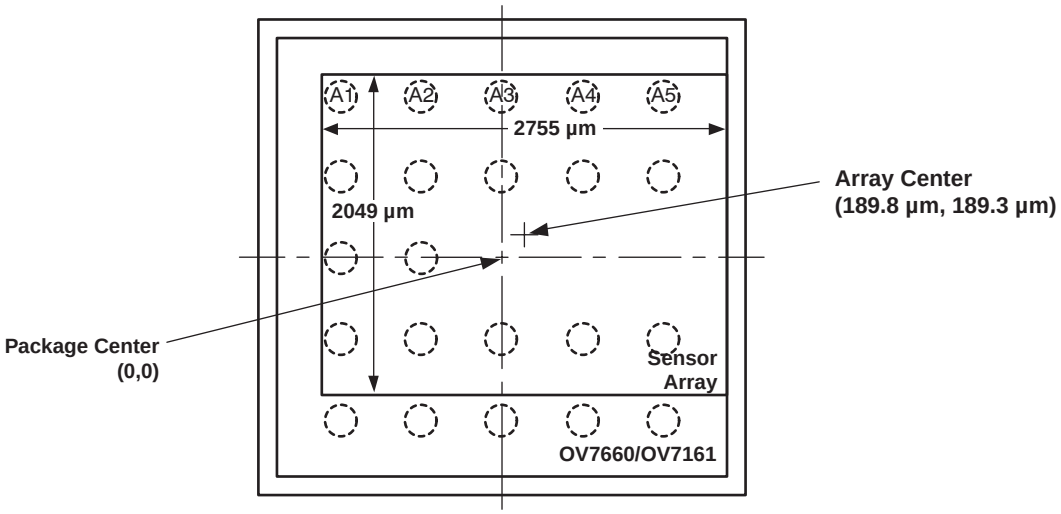


Table 6 OV7660/OV7161 Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package Body Dimension X	A	4130	4155	4180	µm
Package Body Dimension Y	B	3950	3975	4000	µm
Package Height	C	760	820	880	µm
Ball Height	C1	150	180	210	µm
Package Body Thickness	C2	605	640	675	µm
Thickness of Glass Surface to Wafer	C3	400	420	440	µm
Ball Diameter	D	320	350	380	µm
Total Pin Count	N		22		
Pin Count X-axis	N1		5		
Pin Count Y-axis	N2		5		
Pins Pitch X-axis	J1		700		µm
Pins Pitch Y-axis	J2		700		µm
Edge-to-Pin Center Distance Analog X	S1	647.5	677.5	707.5	µm
Edge-to-Pin Center Distance Analog Y	S2	557.5	587.5	617.5	µm

Sensor Array Center

Figure 16 OV7660/OV7161 Sensor Array Center



NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A5 oriented down on the PCB.

IR Reflow Ramp Rate Requirements

OV7660/OV7161 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 17 IR Reflow Ramp Rate Requirements

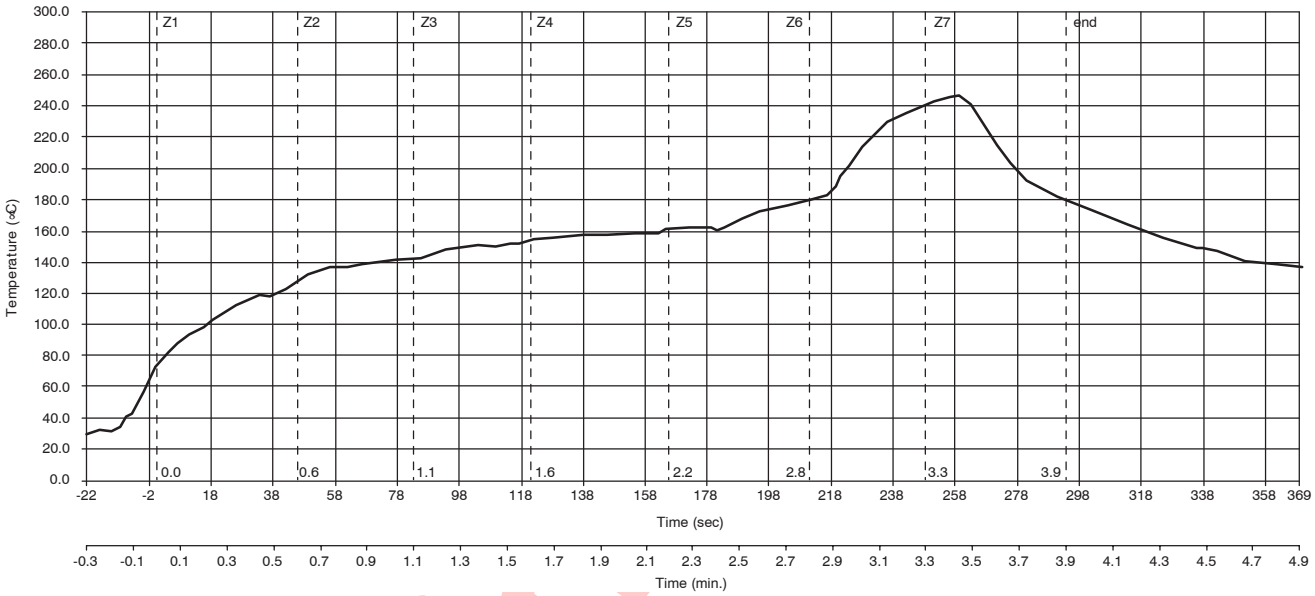


Table 7 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 255°C	No greater than 390 seconds

Environmental Specifications

Table 8 OV7660/OV7161 Reliability Test Results

Parameter	Test Condition
Temperature/Humidity	85°C/85% Relative Humidity, 1000 hrs.[a]
Temperature Cycling (Air-to-Air)	-25°C / +125°C, 72 cycles/day, 1000 cycles[a]
Highly Accelerated Stress Test (HAST)	110°C / 85% Relative Humidity, 168 hrs.[a]
High Temperature Storage (HTS)	150°C, 1000 hrs.[a]
High Temperature Static Bias (HTSB)	125°C, 1000 hrs.[a]

a. Pre-Condition (Moisture Level II): 125°C, 24h → 85°C/60% RH/168h → IR Reflow 235°C, 10 sec, 3 cycles

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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For further information, please feel free to contact OmniVision at info@ovt.com.

OmniVision Technologies, Inc.
1341 Orleans Drive
Sunnyvale, CA USA
(408) 542-3000