OV7950/OV7451 CMOS Analog NTSC CAMERACHIP™ with OmniPixel® Technology

General Description

The OV7950 (color) and OV7451 (black & white) single chip CMOS CAMERACHIPS™ are designed to provide a high level of functionality for all applications requiring a small footprint, low voltage, low power consumption and high performance color or B&W video camera.

Both devices support NTSC composite video output and can directly interface with a VCR TV monitor or other device with 75 ohm loading.

Note: The OV7950/OV7451 is available in a lead-free package.

Features

- Single chip 1/4" format video camera
- Composite video (NTSC) output
- High sensitivity
- Automatic exposure/gain with 16 zone control
- Horizontal and vertical windowing capability
- Auto white balance control
- Aperture/Gamma correction
- 50/60 Hz flicker cancellation
- External frame sync capability (Genlock)
- SPI/EEPROM used to control overlay and set other customer variables
- Two sets of dynamic overlay controls
- Master/slave compatible Serial Camera Control Bus (SCCB) control interface for register programming
- Low power consumption
- Extreme low dark current for high temperature applications
- Defective pixel correction

Ordering Information

Product	Package
OV07950-C10A (Color, NTSC)	CLCC-48
OV07451-C10A (B&W with microlens, NTSC)	CLCC-48

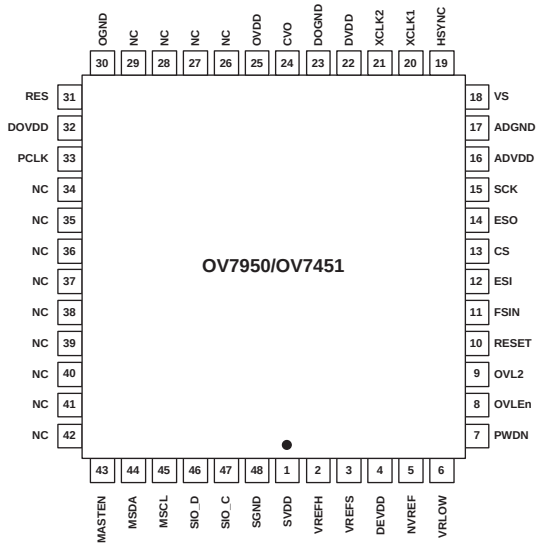
Applications

- Security/Surveillance cameras
- Video Conferencing
- Video phones
- Video e-mail
- Toys
- Finger print equipment
- Medical and dental equipment

Key Specifications

	Array Size	656 x 492
Power Supply	**Analog/ADC/IO**	3.3 VDC ± 5%
	Digital Core	1.8 VDC ± 5%
	Power Consumption	200 mW
	Image Area	4.080 mm x 3.102 mm
Exposure Time Range	**OV7950**	1/60s - 20 µs
	OV7451	1/30s - 20 µs
	Optical Format	1/4"
	S/N Ratio	48 dB
	Dynamic Range	49 dB
	Pixel Size	6.0 µm x 6.0 µm
	Dark Current	10 mW/s @ 60°C
	Fixed Pattern Noise	0.22% of $V_{PEAK-TO-PEAK}$
	Package Dimensions	14.22 mm x 14.22 mm

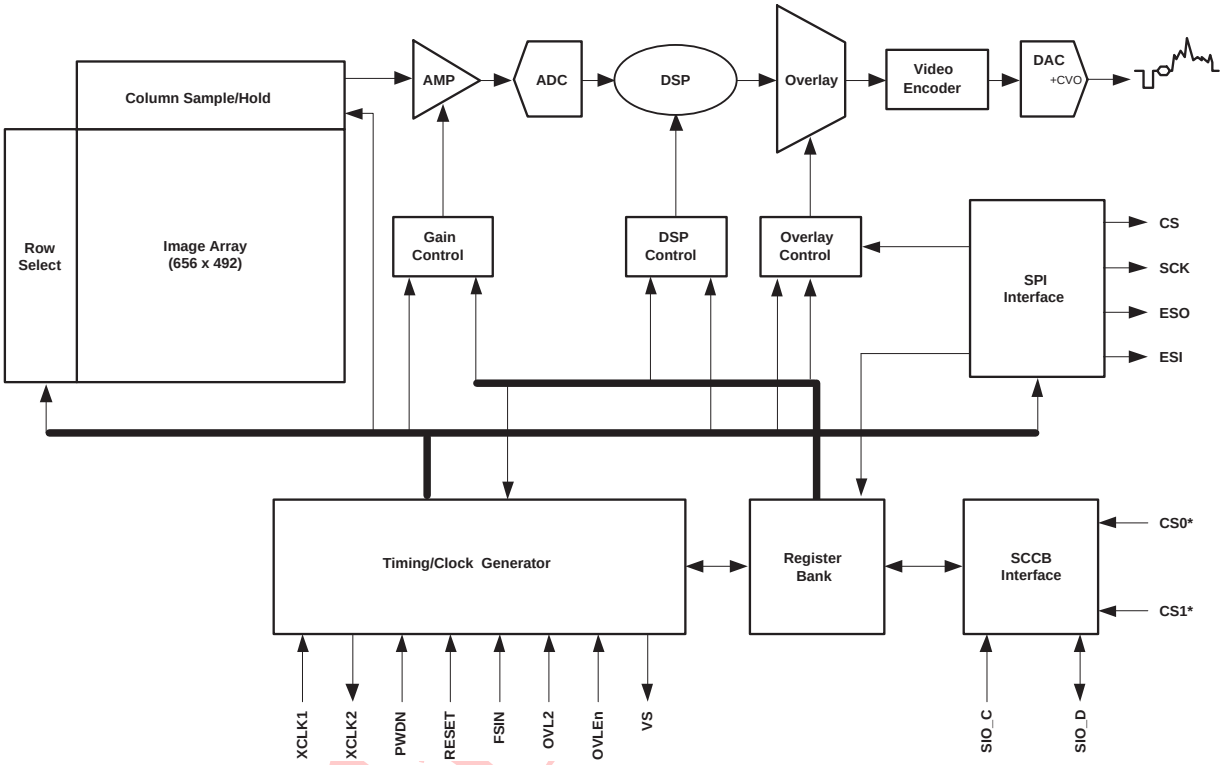
Figure 1 OV7950/OV7451 Pin Diagram (Top View)



Functional Description

This section describes the various functions of the OV7950/OV7451. Refer to Figure 2 for the functional block diagram of the OV7950/OV7451.

Figure 2 Functional Block Diagram



Video Standards

NTSC TV standards are implemented and available as output in the OV7950/OV7451 CAMERACHIPS. Note that the accuracy and stability of the crystal clock frequency is important to avoid unwanted color shift in the TV video system. OmniVision recommends using a 12.27 MHz crystal when utilizing the OV7950/OV7451 CAMERACHIP.

Video Format

The OV7950/OV7451 CAMERACHIP supports Composite (CVBS) video format only. Composite signals are generated from the built-in TV encoder. The OV7451 only outputs the luminance signal.

Image Sensor Functions

White Balance

The function of white balance in the OV7950/OV7451 CAMERACHIP is to adjust and calibrate the image device sensitivity on the primary (RGB) colors to match the color cast of the light source. The Auto White Balance (AWB) can be enabled or disabled by register control. If the AWB is enabled, the image sensors continuously perform white balancing.

Mirror and Vertical Flip

The OV7950/OV7451 provides horizontal mirror and vertical flip functions. These functions can be turned ON or OFF via register settings.

Multi-Chip Synchronize

The OV7950/OV7451 CAMERACHIP provides the multi-chip Synchronize function where one chip works as the master and all others as slave devices. The master chip provides the frame synchronize signal through pin VS (pin 18). All slave devices then accept the frame synchronize signal through pin FSIN. This mode allows all devices to synchronize together.

Chip Configuration

The OV7950/OV7451 CAMERACHIP has been designed for ease-of-use in many stand-alone applications. Some functions like serial interface slave address and NTSC selection can be set by connecting appropriate pins high (logic "1") or low (logic "0") through a 10 KΩ resistor. The OV7950/OV7451 CAMERACHIP also has a serial master and slave interface for programmable access to all register functions.

Additional Picture Controls

The OV7950/OV7451 CAMERACHIP provides additional picture control functions to enhance image quality and chip performance. These functions are listed as follows:

- AGC gain range control
- Gamma correction
- Brightness
- Contrast
- Full color bar test pattern

Serial Camera Control Bus (SCCB)

Many of the functions and configuration registers in the OV7950/OV7451 image sensors are available through the SCCB interface. The OV7950/OV7451 image sensor operates as a slave device that supports up to 400 kbps serial transfer rate using a 7-bit address/data transfer protocol.

SCCB Protocol Format

In SCCB operation (see Figure 5), the master must perform the following operations:

- Generate the Start/Stop condition
- Provide the serial clock on SIO_C
- Place the 7-bit slave address (RW bit) and the 8-bit sub-address on SIO_D

The receiver must pull down SIO_D during the acknowledgement bit time. During the write cycle, the OV7950/OV7451 device returns the acknowledgement and, during the read cycle, the master returns the acknowledgement, indicating to the slave that the read cycle can be terminated. Note that the restart feature is not supported here.

Within each byte, the MSB is transferred first. The read/write control bit is the LSB of the first byte. Standard SCCB communications require only two pins, SIO_C and SIO_D. SIO_D is configured as an open drain for bidirectional purposes. A HIGH to LOW transition on the SIO_D while SIO_C is HIGH indicates a START condition. A LOW to HIGH transition on the SIO_D while SIO_C is HIGH indicates a STOP condition. Only a master can generate START/STOP conditions.

Except for these two special conditions, the protocol that SIO_D remain stable during the HIGH period of the clock, SIO_C. Each bit is allowed to change state only when SIO_C is LOW (see Figure 3 and Figure 4).

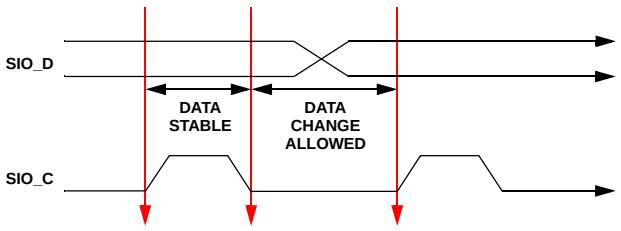
The OV7950/OV7451 SCCB interface supports multi-byte write and multi-byte read. The master must supply the sub-address in the write cycle, but not in the read cycle. Therefore, the OV7950/OV7451 takes the read sub-address from the previous write cycle. In multi-byte write or multi-byte read cycles, the sub-address automatically increments after the first data byte so that continuous locations can be accessed in one bus cycle. A multi-byte cycle overwrites its original sub-address; therefore, if a read cycle immediately follows a multi-byte cycle, a single byte write cycle that provides a new address must be inserted.

The OV7950/OV7451 supports a single slave ID. The ID is preset to 60 for write and 61 for read.

In the write cycle, the second byte in the SCCB is the sub-address for selecting the individual on-chip registers, and the third byte is the data associated with this register. Writing to the unimplemented sub-address is ignored.

In the read cycle, the second byte is the data associated with the previously stored sub-address. Reading of an unimplemented sub-address returns unknown.

Figure 3 Bit Transfer on the SCCB



SCCB Master

Connect external SCCB slave-compatible storage device through the OV7950/OV7451 SCCB master interface so the OV7950/OV7451 can self load the configuration data from it. Data stored in the external storage device should be arranged as follows:

Address	Value
0x00	Sub_add1 - first configuration register address
0x01	Add1_value - first configuration register value
0x02	Sub_add2 - second configuration register address
0x03	Add2_value - second configuration register value
.	.
.	.
.	.

When the sub_add = [FF] and add_value = [FF}, the SCCB master will stop operation.

Figure 4 Data Transfer on the SCCB

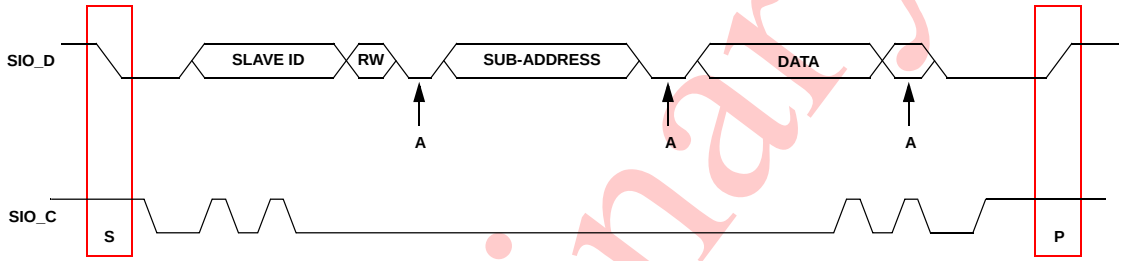
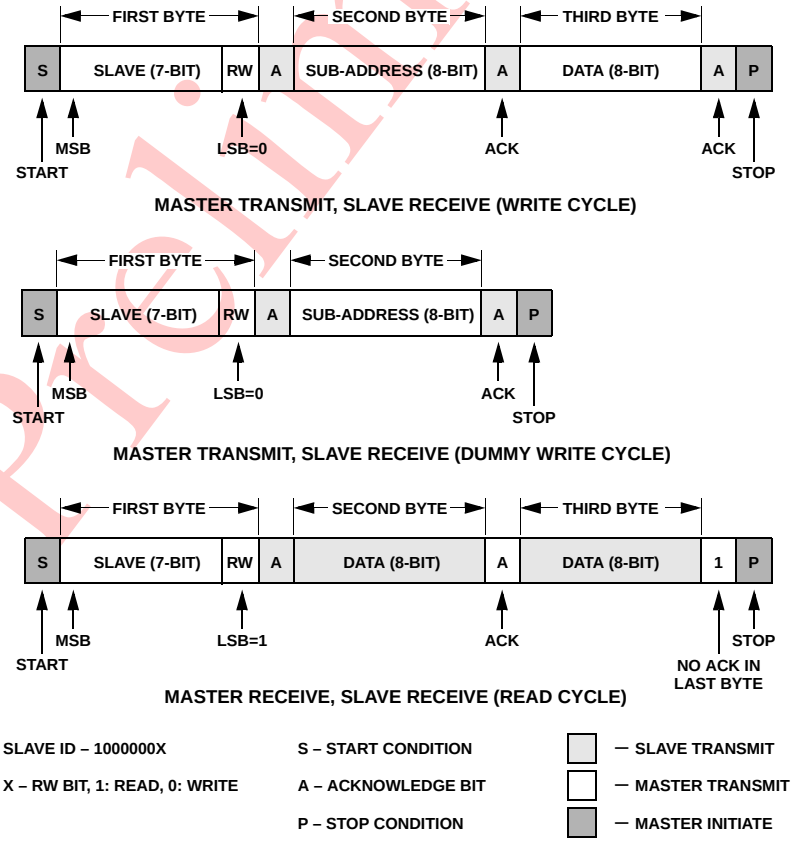


Figure 5 SCCB Protocol Format



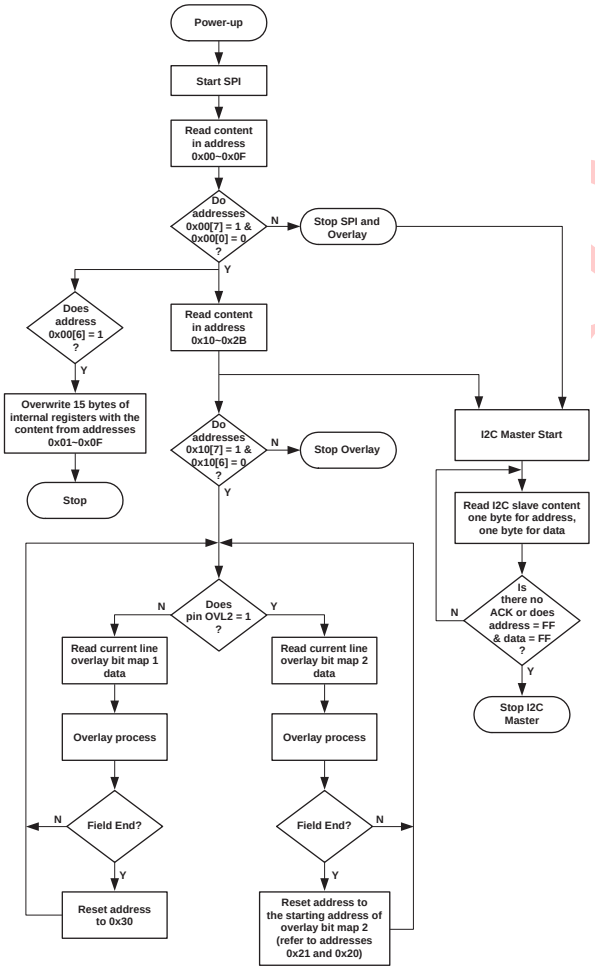
Overlay Control

The OV7950/OV7451 CAMERACHIP has an overlay capability where the user can store an overlay bit map image in an external storage device with an SPI interface.

At power up, OV7950/OV7451 will start the SPI interface when the OVLEn pin (pin 8) is set high. [Bit7, Bit0] ≠ "10" in the first address indicates that there is no SPI slave device attached, causing the SPI interface to stop. Otherwise, the OV7950/OV7451 will check bit 6 of first byte for overwrite control. The user can define up to 15 bytes in the control register to overwrite the internal default value (further details defining this register is not available at this time). These 15 bytes only read one time after power up.

If the first byte bit[7] is "1" and bit[0] is "0", OV7950/OV7451 will read the content in address 0x10 to 0x2B for the overlay setting.

Figure 6 SPI Overlay Process Sequence



Data formats are defined as follows:

Address		Description
0x10	Bit[7]: Bit[6]:	ON/OFF high bit ON/OFF low bit
0x11	Bit[7:6]: Bit[5:4]: Bit[3]:	Opacity1[1:0] Resolution1[1:0] YUV1 all replaced
0x12	Bit[7:0]:	Y1
0x13	Bit[7:0]:	U1
0x14	Bit[7:0]:	V1
0x15	Bit[7:0]:	V1 start[9:2]
0x16	Bit[7:0]:	V1 end[9:2]
0x17	Bit[7:0]:	H1 start[9:2]
0x18	Bit[7:0]:	H1 end[9:2]
0x19	Bit[7:0]:	V1 start[1:0], V1 end[1:0], H1 start[1:0], H1 end[1:0]
0x1A	Bit[7:0]:	MemLine1[7:0] (unit byte)
0x20	Bit[7:0]:	Overlay set 2 start address low 8-bit
0x21	Bit[7:0]:	Overlay set 2 start address high 8-bit
0x22	Bit[7:6]: Bit[5:4]: Bit[3]:	Opacity2[1:0] Resolution2[1:0] YUV2 all replaced
0x23	Bit[7:0]:	Y2
0x24	Bit[7:0]:	U2
0x25	Bit[7:0]:	V2
0x26	Bit[7:0]:	V2 start[9:2]
0x27	Bit[7:0]:	V2 end[9:2]
0x28	Bit[7:0]:	H2 start[9:2]
0x29	Bit[7:0]:	H2 end[9:2]
0x2A	Bit[7:0]:	V2 start[1:0], V2 end[1:0], H2 start[1:0], H2 end[1:0]
0x2B	Bit[7:0]:	MemLine2[7:0] (unit byte)
0x30 ~ 0xXX	Bit map 1	
Set2 start address ~ 0xXX	Bit map 2	

Byte[10]

Overlay function can only be enabled when bit[7] = 1 and bit[6] = 0.

There may be two sets of overlay bitmaps in one EPROM. Byte [11] ~ Byte [1A] are control bytes for first bitmap.

Byte [11]

Resolution =	00	01	10	11
	2x2	3x3	4x4	5x5

When choosing 3x3 or 5x5, be aware that because YUV sampling format is 4:2:2, there may be strong color aliasing around the overlay edges.

Opacity =	00	01	10	11
	25%	50%	75%	100%

YUV all replaced:

Enable:

Y overlay = Y target x q% + Y original x (1-q%)

U overlay = U target x q% + U original x (1-q%)

V overlay = V target x q% + V original x (1-q%)

Disable:

Y overlay = Y target x q% + Y original x (1-q%)

U overlay = U target

V overlay = V target

The q% is opacity.

Byte [12]~[14]

Y, U, V specifies overlay color. In BW mode, only Y needed to be set.

Byte [15]~[19]

The user is allowed to specify vertical and horizontal dimensions of their overlay bitmap. If the desired figure is very small compared to the dimensions of the whole screen, they may save a lot of memory.

Byte [1A]

Every time when a new line is started, it is necessary to go to a new address for memory reading. For example, if the user specifies 500 points per line, which is not an exact multiple of 8, they need at least 63 bytes (63 x 8 = 504) to save the information. So, they can only specify MemLine[7:0] to be a number equal or larger than [3F].

For example, If MemLine = [40]

Line 1 start address = [30],

reading sequence:

Byte[20]bit7, bit6,…bit0,
Byte[21]bit7, bit6…bit0,
Byte[22]bit8, bit7……
……..
Byte[5E]bit8, bit7, bit6, bit5, bit4.
END

Line 2 start address = [70],

Reading sequence:

Byte[60]bit7, bit6,…bit0,
Byte[61]bit7, bit6…bit0,
Byte[62]bit8, bit7……
……..
Byte[9E]bit8, bit7, bit6, bit5, bit4.
END

So, in each line, there are 500 bits was read.

Byte [20], Byte [21]

These two bytes indicate the 16-bit start address of the second bitmap.

Byte [22] ~ Byte [2B]

These are control bytes for second bitmap (refer to description for Byte [11] ~ Byte [1A]).

Pin Description

Table 1 Pin Description

Pin Location	Name	Pin Type	Default (V)	Function/Description
01	SVDD	Power	3.3	Sensor array power supply
02	VREFH	Analog	–	Internal reference
03	VREFS	Analog	–	Internal reference
04	DEVDD	Power	0	Sensor array decoder power supply
05	NVREF	Power	0	Internal reference
06	VRLOW	Analog	–	Internal reference
07	PWDN	Input	0	Power Down Mode ON/OFF Selection 0: OFF 1: ON
08	OVLEn	Input	0	Overlay ON/OFF selection 0: OFF 1: ON
09	OVL2	Input	0	Overlay bitmap file selection 0: Select first bitmap 1: Select second bitmap
10	RESET	Input	0	Hard reset ON/OFF selection 0: OFF 1: ON
11	FSIN	Input	0	Frame synchronizing signal input
12	ESI	Input	0	SPI interface data input
13	CS	Output	–	SPI interface chip select signal
14	ESO	I/O	0	SPI interface data output
15	SCK	I/O	0	SPI interface clock output
16	ADVDD	Power	3.3	ADC power supply
17	ADGND	Power	0	ADC ground
18	VS	Output	0	Frame synchronizing signal output
19	HSYNC	Output	0	Horizontal valid pixel reference signal output
20	XCLK1	Input	–	Crystal input
21	XCLK2	Output	–	Crystal output
22	DVDD	Power	1.8	Digital core power supply
23	DOGND	Power	0	Digital I/O interface ground
24	CVO	Analog	–	Composite video signal output
25	OVDD	Power	3.3	DAC power supply

Table 1 Pin Description

Pin Location	Name	Pin Type	Default (V)	Function/Description
26	NC	–	–	No connection
27	NC	–	–	No connection
28	NC	–	–	No connection
29	NC	–	–	No connection
30	OGND	Analog	–	DAC ground
31	RES	Analog	–	Internal reference adjustment pin (connect to ground using a 200Ω resistor)
32	DOVDD	Power	3.3	Digital I/O interface power supply
33	PCLK	Output	–	Pixel clock output
34	NC	–	–	No connection
35	NC	–	–	No connection
36	NC	–	–	No connection
37	NC	–	–	No connection
38	NC	–	–	No connection
39	NC	–	–	No connection
40	NC	–	–	No connection
41	NC	–	–	No connection
42	NC	–	–	No connection
43	MASTEN	Input	–	Master interface enable
44	MSDA	I/O	–	Serial master interface data I/O
45	MSCL	O	–	Serial master interface clock output
46	SIO_D	I/O	–	Serial slave interface data I/O
47	SIO_C	Input	–	Serial slave interface clock input
48	SGND	Power	0	Sensor array ground

Electrical Characteristics

Table 2 Operating Conditions

Parameter	Min	Max
Operating temperature	-40°C	+85°C
Storage temperature[a]	-40°C	+125°C

a. Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the sensor at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.

Table 3 DC Characteristics (-20°C < T_A < 85°C, Voltages Referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
VDD1	Supply voltage (SVDD, DOVDD, EVDD)	3.15	3.3	3.45	V
VDD2	Supply voltage (DVDD)	1.70	1.8	1.90	V
IDD	Supply current	–	60	–	mA
Digital Inputs					
V_{IL}	Input voltage LOW			0.2 x DOVDD	V
V_{IH}	Input voltage HIGH	0.8 x DOVDD			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3V					
V_{OH}	Output voltage HIGH	2			V
V_{OL}	Output voltage LOW			0.6	V
Serial Input					
V_{IL}	SIO_C and SIO_D	-0.5	0	1	V
V_{IH}	SIO_C and SIO_D	2.5	3.3	V_{DOVDD} + 0.5	V

Table 4 AC Characteristics (T_A = 25°C, VDD = 5V)

Symbol	Parameter	Min	Typ	Max	Unit
Clock Input / Crystal Oscillator					
f_{OSC}	Resonator frequency (NTSC)	–	12.27	–	MHz
	Load capacitor		33		pF
	Parallel resistance		1		MΩ
	Rise/fall time for external clock input	–	5	–	ns
	Duty cycle for external clock input	40	50	60	%
CVO Analog Video Output Parameters					
V_{TO_P}	Video peak signal level	0.969	1.020	1.071	V
V_{TO_B}	Video black signal level	0.339	0.357	0.375	V
V_{VSYNC}	Video sync pulse amplitude	0.291	0.306	0.321	V
$V_{SYNCLEVEL}$	Sync level	0.017	0.022	0.027	V
I_{VTO}	Video output drive current	–		30	mA
I/O Pin					
I_{SOURCE}	Output pin source current (Output = 1.5V)	8	10	12	mA
I_{SINK}	Output pin sink current (Output = 3V)	8	10	12	mA
Miscellaneous Timing					
t_{SYNC}	External FSIN cycle time	–	2	–	field
t_{PU}	Chip power-up time	–	–	100	µs

Timing Specifications

NTSC Timing

Figure 7 NTSC Standard Video Timing Diagram

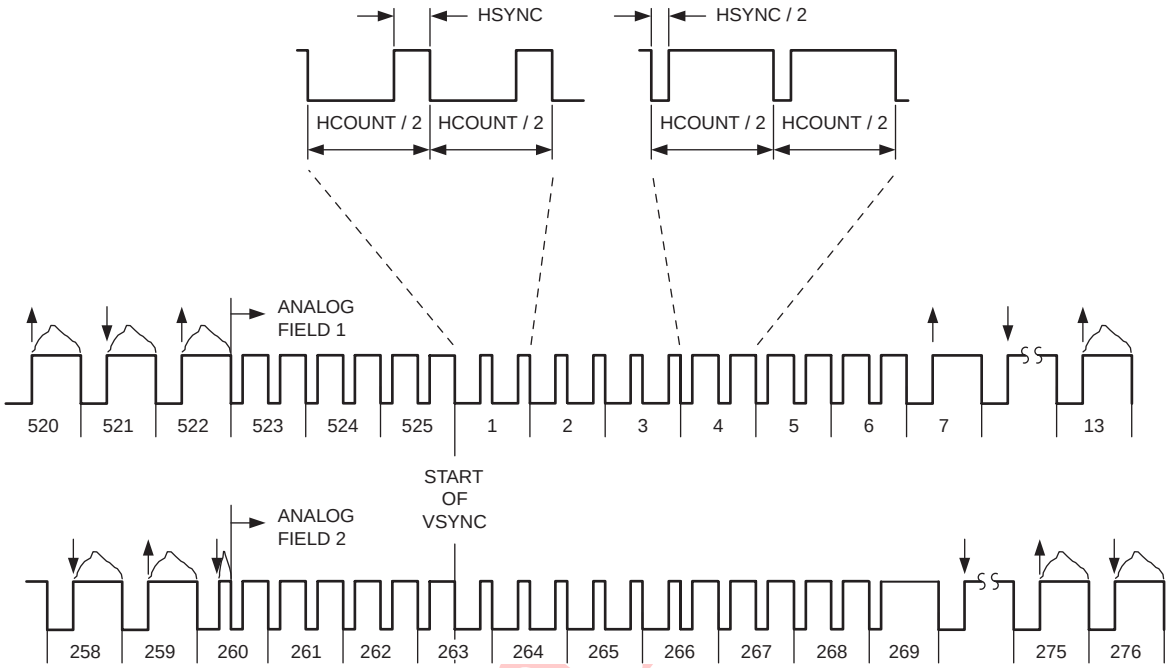
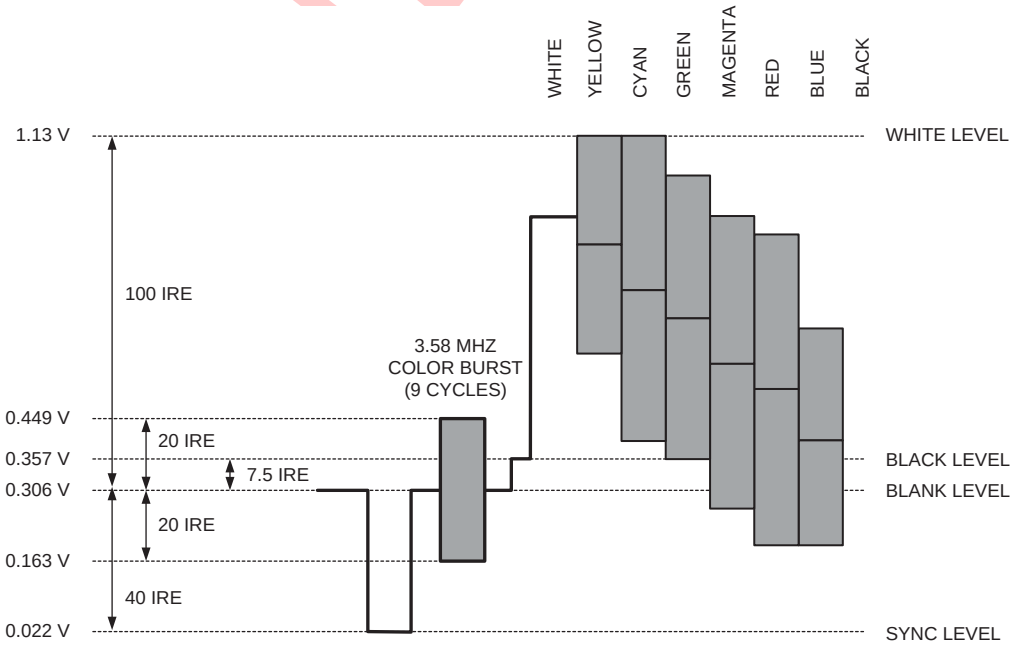
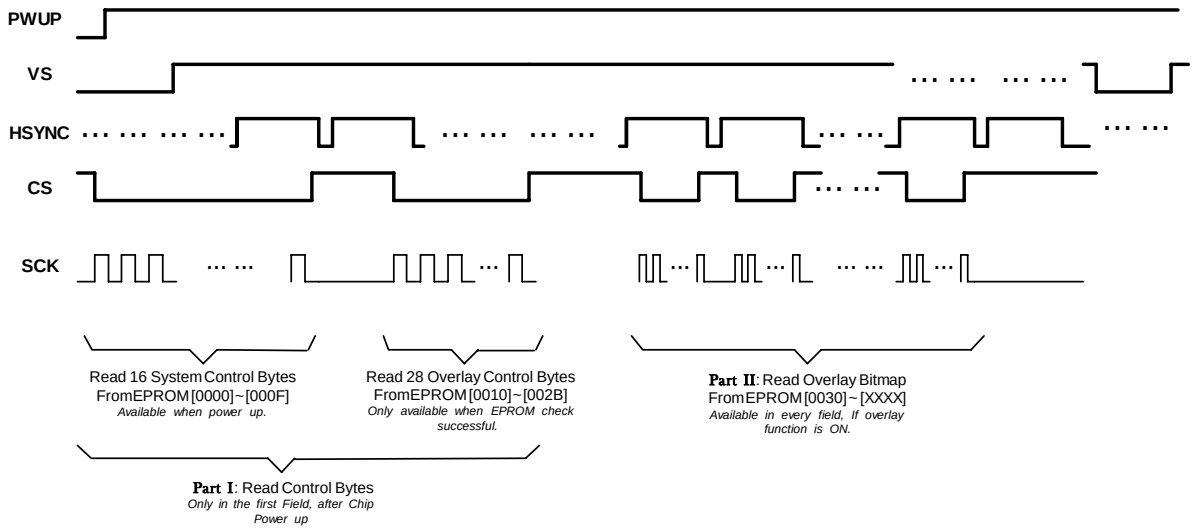


Figure 8 NTSC Composite Video Signal



Overlay Timing

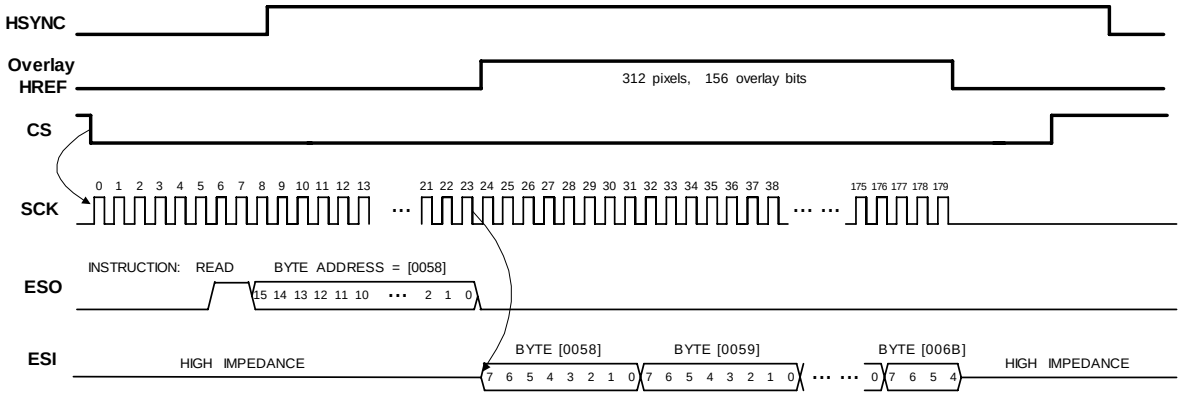
Figure 9 Vertical Timing Diagram



In **Part I**, SCK freq. is always 1/5 pixel clock freq;

In **Part II**, SCK freq. can be 1/2, 1/3, 1/4 or 1/5 pixel clock freq. according to overlay resolution (2x2, 3x3, 4x4 or 5x5).

Figure 10 Horizontal Timing Diagram



If overlay resolution is 2x2,
overlay horizontal start = [60]
overlay horizontal end = [198]
MEMLN = [14]
So, overlay HREF includes 312 pixels.
In each line, it need to read 156 bits from overlay bitmap in EPROM.
In overlay line1 or line2, read EPROM BYTE [0030] ~ [0043];
In overlay line3 or line4, read EPROM BYTE [0044] ~ [0057];
Figure 11 shows horizontal timing of overlay line5 or line6.

Interface Timing

Figure 11 SCCB Timing Diagram

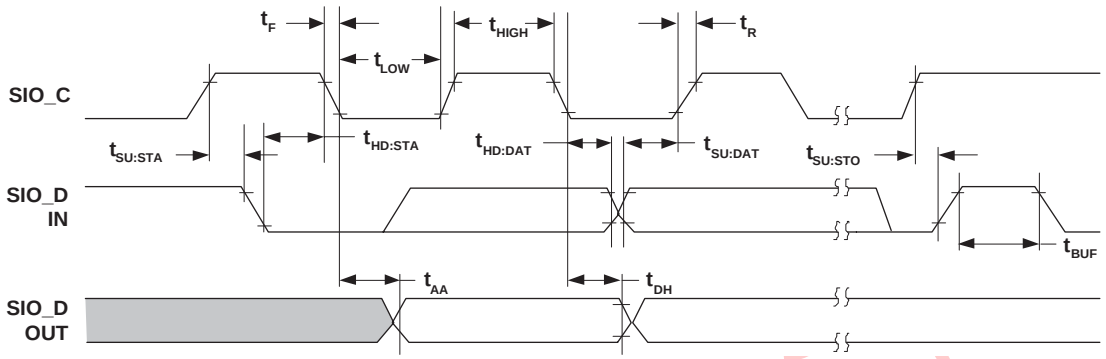


Table 5 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Figure 12 SPI Timing Diagram

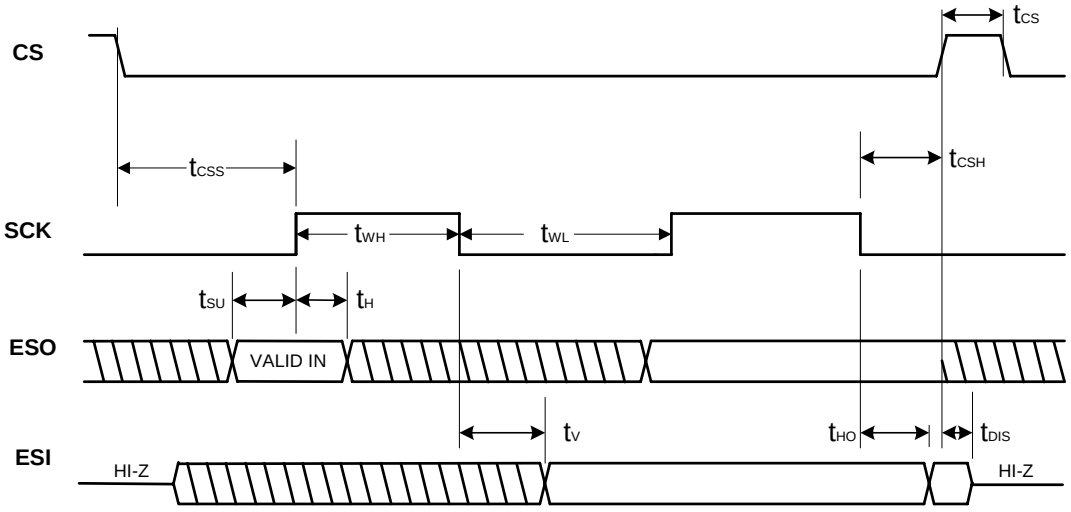
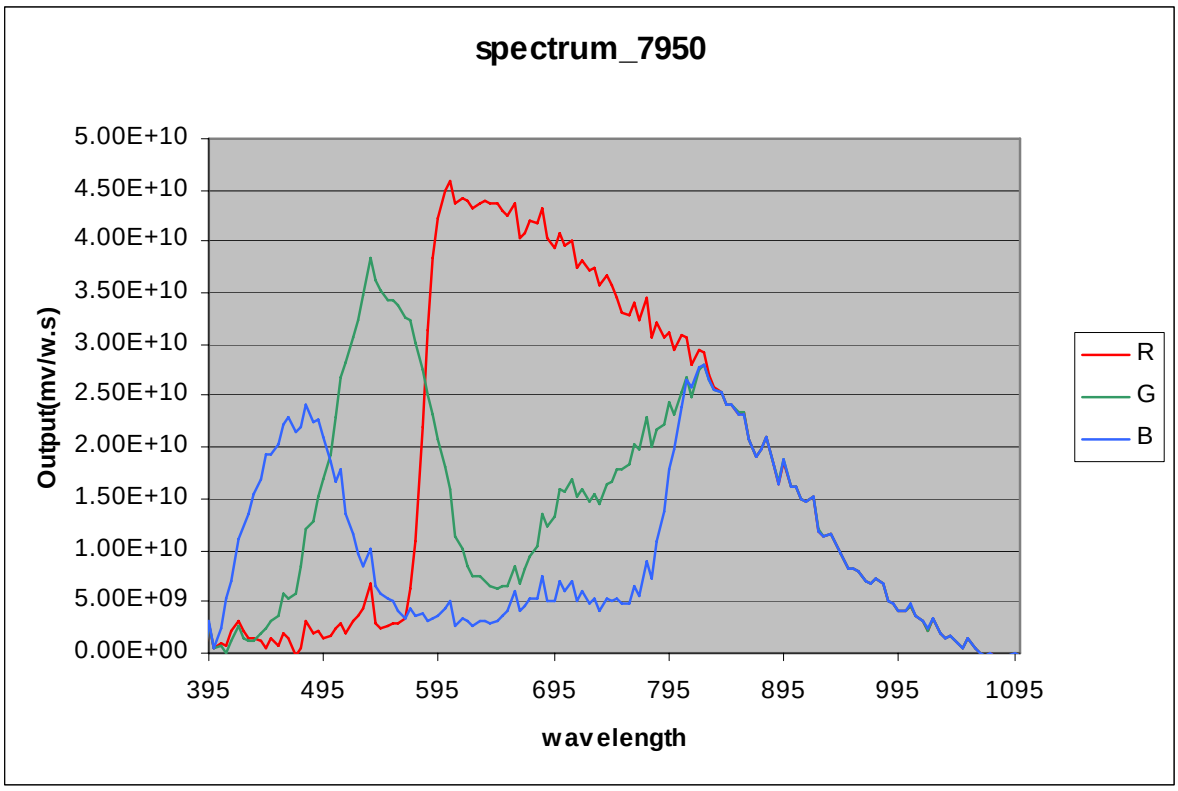


Table 6 SPI Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{WH}	SCK High Time	133			ns
t_{WL}	SCK Low Time	133			ns
t_{CS}	CS High Time	250			ns
t_{CSS}	CS Setup Time	250			ns
t_{CSH}	CS Hold Time	250			ns
t_{SU}	Data In Setup Time	50			ns
t_{H}	Data In Hold Time	50			ns
t_{V}	Output Valid			133	ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			250	ns

OV7950 Light Response

Figure 13 OV7950 Light Response



Register Set

Table 7 provides a list and description of the Device Control registers contained in the OV7950/OV7451. The device slave addresses are 60 for write and 61 for read.

Table 7 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control Bit[7:0]: Gain setting • Range: 1x - 32x Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16) ***Note:*** *This register is updated automatically when AGC is enabled. The user can adjust the value through the serial interface if AGC is disabled.*
01	BLUE	80	RW	Blue Gain Control
02	RED	80	RW	Red Gain Control
03	GREEN	80	RW	Green Gain Control
04	AECL	88	RW	AEC/AGC Control Bit[7:3]: Reserved Bit[2:1]: AGC Gain Control - high 2 bits Bit[0]: Exposure control LSB
05	BAVG	00	RW	B Channel Average
06	GAVG	00	RW	G Channel Average
07	RAVG	00	RW	R Channel Average
08	COM1	10	RW	Common Control 1 Bit[7]: Mirror function 0: Normal image 1: Mirror image Bit[6]: Vertical flip function 0: Normal image 1: Vertically flip image Bit[5]: Reserved Bit[4]: VS pin output selection 0: Output signal depends on COM7[1] (0x15) 1: Output Odd field indicator Bit[3]: Gamma function ON/OFF 0: Gamma OFF 1: Gamma ON Bit[2:0]: Reserved
09	RSVD	XX	–	Reserved
0A	PIDH	79	R	Product ID Number MSB (Read only)
0B	PIDL	50	R	Product ID Number LSB (Read only)
0C-0F	RSVD	XX	–	Reserved

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
10	AEC	82	RW	Automatic Exposure Control - AEC[8:1] (LSB in AECL[0] (0x04) and MSB in AECH[6:0] (0x39))
11	RSVD	XX	–	Reserved
12	COM4	50	RW	Common Control 4 Bit[7]: SRST 0: No change 1: Initiates system reset and resets all registers to factory default values after which the device resumes normal operation Bit[6:0]: Reserved
13	COM5	8F	RW	AEC, AGC, and AWB Auto/Manual Control Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: Reserved Bit[5]: Banding filter ON/OFF selection 0: OFF 1: ON Bit[4]: Reserved Bit[3]: Small exposure ON/OFF selection 0: OFF (minimum exposure is 1 Tv line period (65 µs)) 1: ON (minimum exposure is 20 µs) Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COM6	80	RW	Common Control 6 Bit[7:5]: AGC max gain ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101-111: Not allowed Bit[4]: Reserved Bit[3:2]: Digital gain ceiling 00: 1x 01: 2x 10: 4x 11: Not allowed Bit[1]: Reserved Bit[0]: Exposure freeze ON/OFF 0: OFF 1: ON
15	COM7	00	RW	Common Control 7 Bit[7:2]: Reserved Bit[1]: VSYNC output selection 0: Field VSYNC 1: Frame VSYNC Bit[0]: Reserved
16	COM8	40	RW	Common Control 8 Bit[7]: AEC/AGC algorithm selection 0: Average-based AEC/AGC control 1: Histogram-based AEC/AGC control Bit[6]: Auto/Manual digital gain select 0: Auto digital gain 1: Manual digital gain Bit[5:4]: Manual set digital gain [1:0] Bit[3:0]: Reserved
17-1A	RSVD	XX	–	Reserved
1B	PSHFT	6A	RW	Left Pixel Shift - 1 bit equals 2 pixel shift
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-20	RSVD	XX	–	Reserved

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
21	COM9	00	RW	Common Control 9 Bit[7]: Reserved Bit[6]: VSYNC output pattern control 0: VSYNC can start at line start or half line 1: VSYNC can only start at line start Bit[5]: VSYNC output only in field one Bit[4]: VSYNC output only in field two Bit[3:0]: Reserved
22-23	RSVD	XX	–	Reserved
24	AECW	78	RW	Luminance Signal High Range for AEC/AGC operation
25	AECB	68	RW	Luminance Signal Low Range for AEC/AGC operation
26	VWB	D4	RW	Fast Mode Large Step Luminance Range Threshold
27-2E	RSVD	XX	–	Reserved
2F	YAVG	00	RW	Luminance Average Value
30-32	RSVD	XX	–	Reserved
33	VSFT	00	RW	Vertical Window Shift
34-38	RSVD	XX	–	Reserved
39	AECH	82	RW	Automatic Exposure Control MSBs Bit[7]: Reserved Bit[6:0]: Automatic exposure control MSBs
3A-65	RSVD	XX	–	Reserved
66	MNTR	00	RW	Monitor Bit[7:4]: Register monitor control (refer to descriptions of registers COM22 (0xED), COM23 (0xEE), COM24 (0xEF) and COM25 (0xF0) Bit[3:0]: Reserved
67-7A	RSVD	XX	–	Reserved
7B	SLOP	24	RW	Gamma Curve Highest Segment Slop Should be calculated as follows: SLOP[7:0] = (FF - GAM15[7:0] + 1) x 40/30 ***Note:*** *Use hex numbers for calculation*
7C	GAM1	0F	RW	Gamma Curve - 1st segment input end point 0x010 output value
7D	GAM2	1F	RW	Gamma Curve - 2nd segment input end point 0x020 output value
7E	GAM3	36	RW	Gamma Curve - 3rd segment input end point 0x040 output value
7F	GAM4	54	RW	Gamma Curve - 4th segment input end point 0x080 output value
80	GAM5	5F	RW	Gamma Curve - 5th segment input end point 0x0A0 output value
81	GAM6	6A	RW	Gamma Curve - 6th segment input end point 0x0C0 output value

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
82	GAM7	74	RW	Gamma Curve - 7th segment input end point 0x0E0 output value
83	GAM8	7C	RW	Gamma Curve - 8th segment input end point 0x100 output value
84	GAM9	84	RW	Gamma Curve - 9th segment input end point 0x120 output value
85	GAM10	8C	RW	Gamma Curve - 10th segment input end point 0x140 output value
86	GAM11	9A	RW	Gamma Curve - 11th segment input end point 0x180 output value
87	GAM12	A7	RW	Gamma Curve - 12th segment input end point 0x1C0 output value
88	GAM13	BF	RW	Gamma Curve - 13th segment input end point 0x240 output value
89	GAM14	D3	RW	Gamma Curve - 14th segment input end point 0x2C0 output value
8A	GAM15	E5	RW	Gamma Curve - 15th segment input end point 0x340 output value
8B-9A	RSVD	XX	–	Reserved
9B	MTX1	40	RW	Color Matrix Parameter M1
9C	MTX2	34	RW	Color Matrix Parameter M2
9D	MTX3	0C	RW	Color Matrix Parameter M3
9E	MTX4	17	RW	Color Matrix Parameter M4
9F	MTX5	29	RW	Color Matrix Parameter M5
A0	MTX6	40	RW	Color Matrix Parameter M6
A1	MTX7	1E	RW	Color Matrix Control Bit[7]: Double matrix - double M1 to M6 Bit[6]: Reserved Bit[5]: Sign bit of M6 Bit[4]: Sign bit of M5 Bit[3]: Sign bit of M4 Bit[2]: Sign bit of M3 Bit[1]: Sign bit of M2 Bit[0]: Sign bit of M1
A2	BRT	00	RW	Brightness Control • Range [00] to [FF]
A3	CNTR	40	RW	Contrast Control
A4-BE	RSVD	XX	–	Reserved
BF	BPTH1	90	RW	Black Pixel Threshold Level 1
C0	BPTH2	40	RW	Black Pixel Threshold Level 2
C1	WPTH1	A0	RW	White Pixel Threshold Level 1
C2	WPTH2	D0	RW	White Pixel Threshold Level 2
C3	BPCNT1	CC	RW	Black Pixel Count Number 1
C4	BPCNT2	F0	RW	Black Pixel Count Number 2

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
C5	WPCNT1	64	RW	White Pixel Count Number 1
C6	WPCNT2	80	RW	White Pixel Count Number 2
C7-D0	RSVD	XX	–	Reserved
D1	ZONE1	FF	RW	Bit[7:6]: Zone 4 Bit[5:4]: Zone 3 Bit[3:2]: Zone 2 Bit[1:0]: Zone 1
D2	ZONE2	FF	RW	Bit[7:6]: Zone 8 Bit[5:4]: Zone 7 Bit[3:2]: Zone 6 Bit[1:0]: Zone 5
D3	ZONE3	FF	RW	Bit[7:6]: Zone 12 Bit[5:4]: Zone 11 Bit[3:2]: Zone 10 Bit[1:0]: Zone 8
D4	ZONE4	FF	RW	Bit[7:6]: Zone 16 Bit[5:4]: Zone 15 Bit[3:2]: Zone 14 Bit[1:0]: Zone 13
D5-EA	RSVD	XX	–	Reserved
EB	COM21	00	RW	Overlay Data Shift Select
EC	RSVD	XX	–	Reserved
ED	COM22	–	R	Register Monitor when MNTR[7:4] are: 0000: SPI input com1 0001: SPI input com2 0010: SPI input com3 0011: SPI input com4 0100: SPI input com5 0101: SPI input com6 0110: SPI input com7 0111: SPI input com8 1000: SPI input com9 1001: SPI input com10 1010: SPI input com11 1011: SPI input com12 1100: SPI input com13 1101: SPI input com14 1110: SPI input com15 1111: SPI input com16

16-Zone Y average select

In each zone, the two bits mean:

00: Not selected
01: Weight x1
10: Weight x2
11: Weight x4

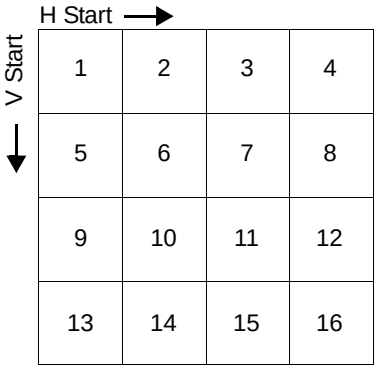


Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
EE	COM23	–	R	Register Monitor when MNTR[7:4] are: 0000: Overlay control register Bit[7:6]: Overlay function ON/OFF select 0x: Overlay function OFF 10: Overlay function ON 11: Overlay function OFF 0001: Overlay bitmap 1 control register Bit[7:6]: Overlay opacity 00: 25% overlay opacity 01: 50% overlay opacity 10: 75% overlay opacity 11: 100% overlay opacity Bit[7:6]: Overlay resolution 00: 2x2 01: 3x3 10: 4x4 11: 5x5 0010: Y overlay target 1 0011: U overlay target 1 0100: V overlay target 1 0101: Overlay vertical window 1 start point MSBs 0110: Overlay vertical window 1 stop point MSBs 0111: Overlay horizontal window 1 start point MSBs 1000: Overlay horizontal window 1 stop point MSBs 1001: Reserved Bit[7:6]: Overlay vertical window 1 start point LSBs Bit[5:4]: Overlay vertical window 1 stop point LSBs Bit[3:2]: Overlay horizontal window 1 start point LSBs Bit[1:0]: Overlay horizontal window 1 stop point LSBs 1010: Memory length for one line 1011: Overlay bit map 2 start address LSBs 1100: Overlay bit map 2 start address MSBs 1101: Overlay bitmap 2 control register 1110: Y overlay target 2 1111: U overlay target 2
EF	COM24	–	R	Register Monitor when MNTR[7:4] are: 0000: V overlay target 2 0001: Overlay vertical window 2 start point MSBs 0010: Overlay vertical window 2 stop point MSBs 0011: Overlay horizontal window 2 start point MSBs 0100: Overlay horizontal window 2 stop point MSBs 0101: Reserved Bit[7:6]: Overlay vertical window 2 start point LSBs Bit[5:4]: Overlay vertical window 2 stop point LSBs Bit[3:2]: Overlay horizontal window 2 start point LSBs Bit[1:0]: Overlay horizontal window 2 stop point LSBs 0110: Memory length 2 for one line

Table 7 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
F0	COM25	–	R	Register Monitor when MNTR[7:4] are: 0000: Y average zone 1 0001: Y average zone 2 0010: Y average zone 3 0011: Y average zone 4 0100: Y average zone 5 0101: Y average zone 6 0110: Y average zone 7 0111: Y average zone 8 1000: Y average zone 9 1001: Y average zone 10 1010: Y average zone 11 1011: Y average zone 12 1100: Y average zone 13 1101: Y average zone 14 1110: Y average zone 15 1111: Y average zone 16
F1-F2	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7950/OV7451 uses a 48-pin ceramic package (CLCC). Refer to Figure 14 and Table 8 for CLCC information and Figure 15 for the sensor array center.

Figure 14 OV7950/OV7451 Package Specifications

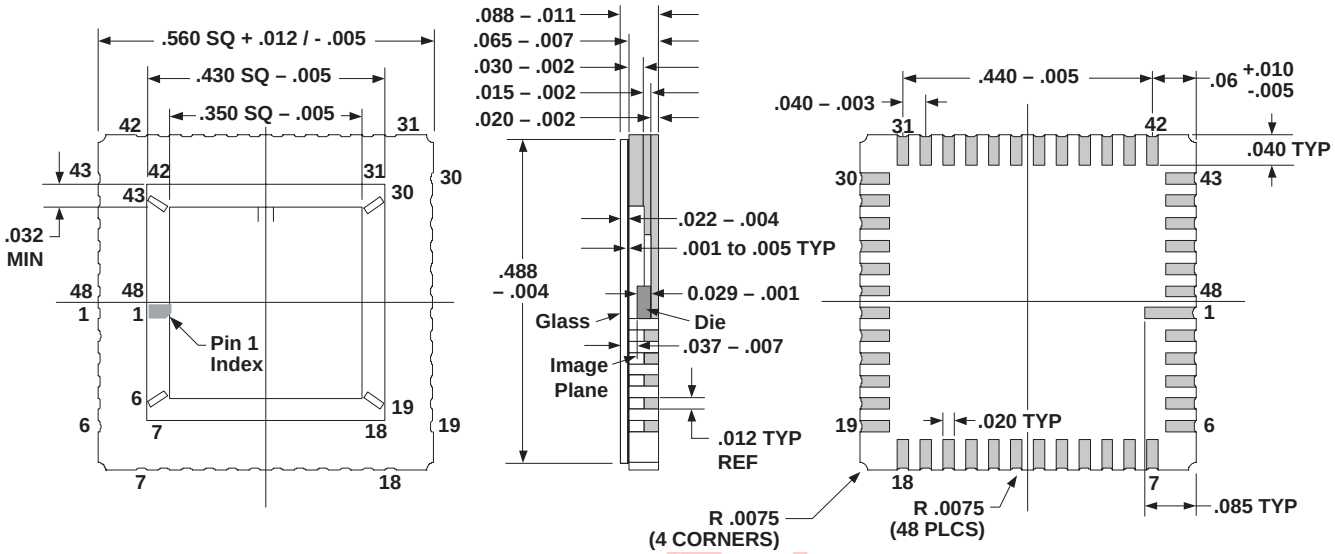
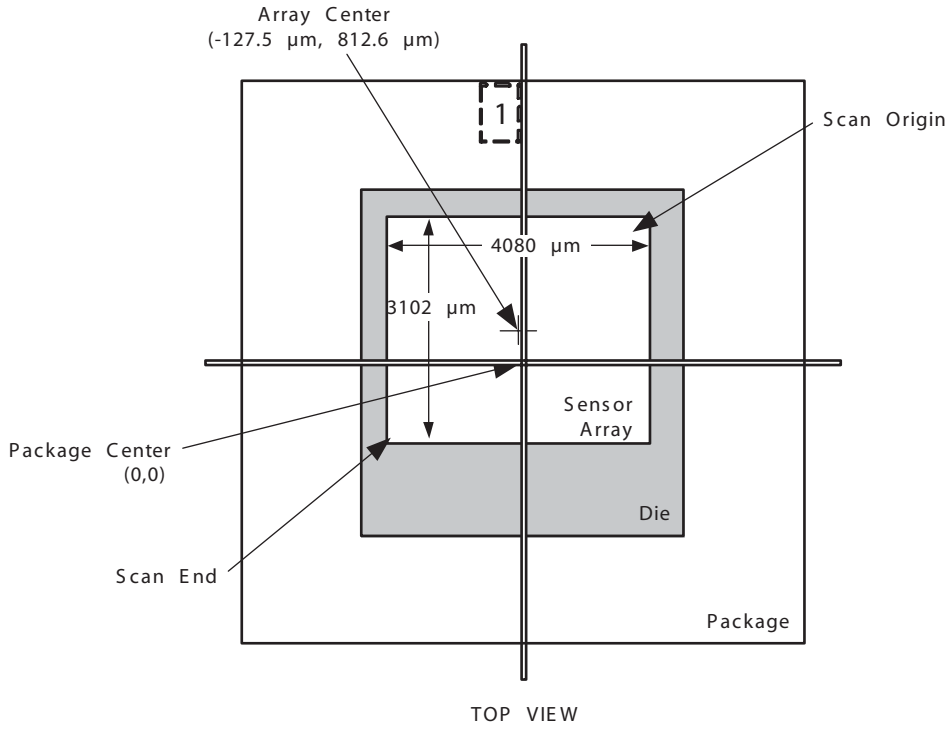


Table 8 OV7950/OV7451 Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 + 0.30 / -0.13 SQ	.560 + .012 / - .005 SQ
Package Height	2.23 ± 0.28	.088 ± .011
Substrate Base Height	0.51 ± 0.05	.020 ± .002
Cavity Size	8.89 ± 0.13 SQ	.350 ± .005 SQ
Castellation Height	1.14 ± 0.13	.045 ± .005
Pin #1 Pad Size	0.51 x 2.16	.020 x .085
Pad Size	0.51 x 1.02	.020 x .040
Pad Pitch	1.02 ± 0.08	.040 ± .003
Package Edge to First Lead Center	1.524 + 0.25 / -0.13	.06 + .010 / - .005
End-to-End Pad Center-Center	11.18 ± 0.13	.440 ± .005
Glass Size	12.40 ± 0.10 SQ / 13.00 ± 0.10 SQ	.488 ± .004 SQ / .512 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002
Die Thickness	0.733 ± 0.015	.029 ± .001
Top of Glass to Image Plane	0.95 ± 0.18	.037 ± .007
Substrate Height	1.65 ± 0.18	.065 ± .007

Sensor Array Center

Figure 15 OV7950/OV7451 Sensor Array Center



NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pin one oriented down on the PCB.

IR Reflow Ramp Rate Requirements

OV7950/OV7451 Lead-Free Packaged Devices

Figure 16 IR Reflow Ramp Rate Requirements

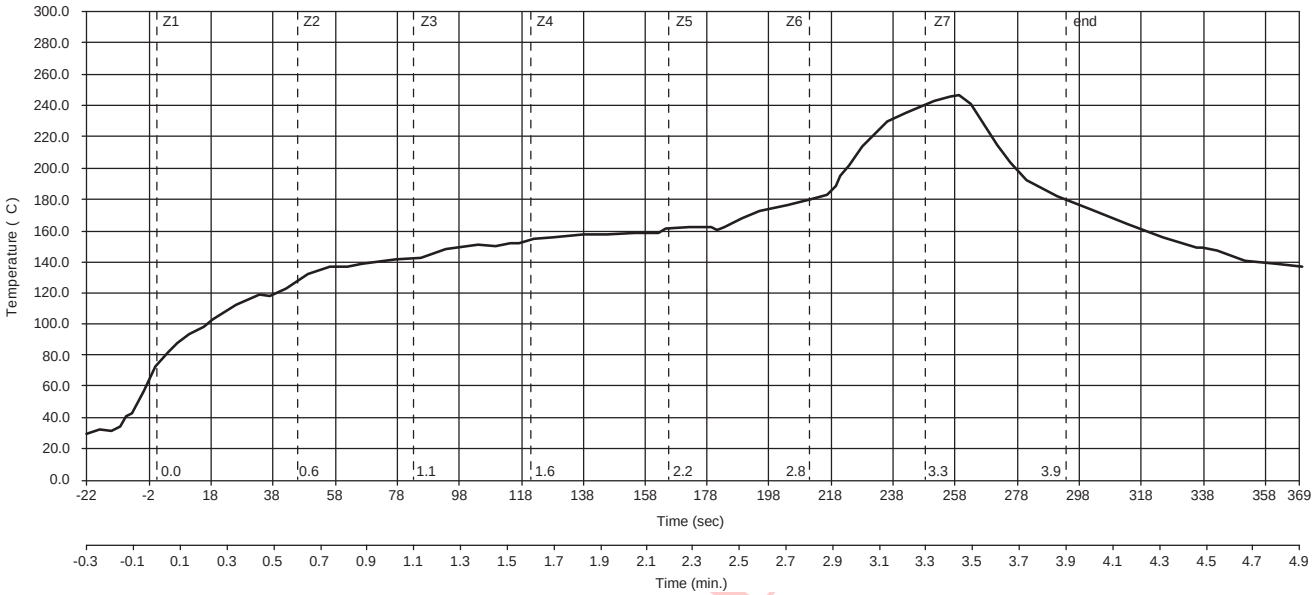


Table 9 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV7950/OV7451 Datasheet (non-auto apps) **Version:** 2.3

DESCRIPTION OF CHANGES

Initial Release (created using OV7950/OV7451 ver 1.3 (for auto apps) with the following changes):

- Deleted “for Automotive Applications” from the title.
- Under Ordering Information, changed the part number from OV07950-Q10V and OV07451-Q10V to OV07950-C10A and OV07451-C10A.
- Changed bullet list under Applications on page 1.
- Changed Figure 1 to show pinout diagram for CLCC package.
- Under Package Specifications on page 24, changed Figure 14 and Table 8 to show CLCC package drawing and CLCC package dimensions table.

REVISION CHANGE LIST

Document Title: OV7950/OV7451 Datasheet (non-auto apps) **Version:** 2.4

DESCRIPTION OF CHANGES

The following changes were made to version 2.3:

- Added Figure 13 (OV7950 Light Response graph) on page 15
- Under Features on page 1, changed second bullet from “Composite video (NTSC) differential output drive” to “Composite video (NTSC) output”

REVISION CHANGE LIST

Document Title: OV7950/OV7451 Datasheet (non-auto apps) **Version:** 2.5

DESCRIPTION OF CHANGES

The following changes were made to version 2.4:

- Under Key Specifications on page 1, changed Power Consumption from “TBD” to “200 mW”
- Under Key Specifications on page 1, changed S/N Ratio from “TBD” to “48 dB”
- Under Key Specifications on page 1, changed Dynamic Range from “TBD” to “49 dB”
- Under Key Specifications on page 1, changed Dark Current from “TBD” to “10 mW/s @ 60°C”
- Under Key Specifications on page 1, changed Fixed Pattern Noise from “TBD” to “0.22% of $V_{PEAK-TO-PEAK}$”
- In Table 1 on page 7, changed Default value for pin 02 from “TBD” to “–”
- In Table 1 on page 7, changed Default value for pin 03 from “TBD” to “–”
- In Table 1 on page 7, changed Default value for pin 06 from “TBD” to “–”
- In Table 2 on page 9, changed Min and Max for Operating temperature from “TBD” and “TBD” to “-40°C” and “+85°C”, respectively.
- In Table 2 on page 9, deleted table row for Storage Humidity.
- In Table 3 on page 9, added the table footnote: “Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the sensor at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.”
- In Table 3 on page 9, changed Typ for Supply current (IDD) from “TBD” to “60”
- In Figure 8 on page 11, changed callout from “1.020 V” to “1.13V”