



PRELIMINARY

## NT7651

### *LCD controller/driver* *16Cx2 characters + 160 icons*

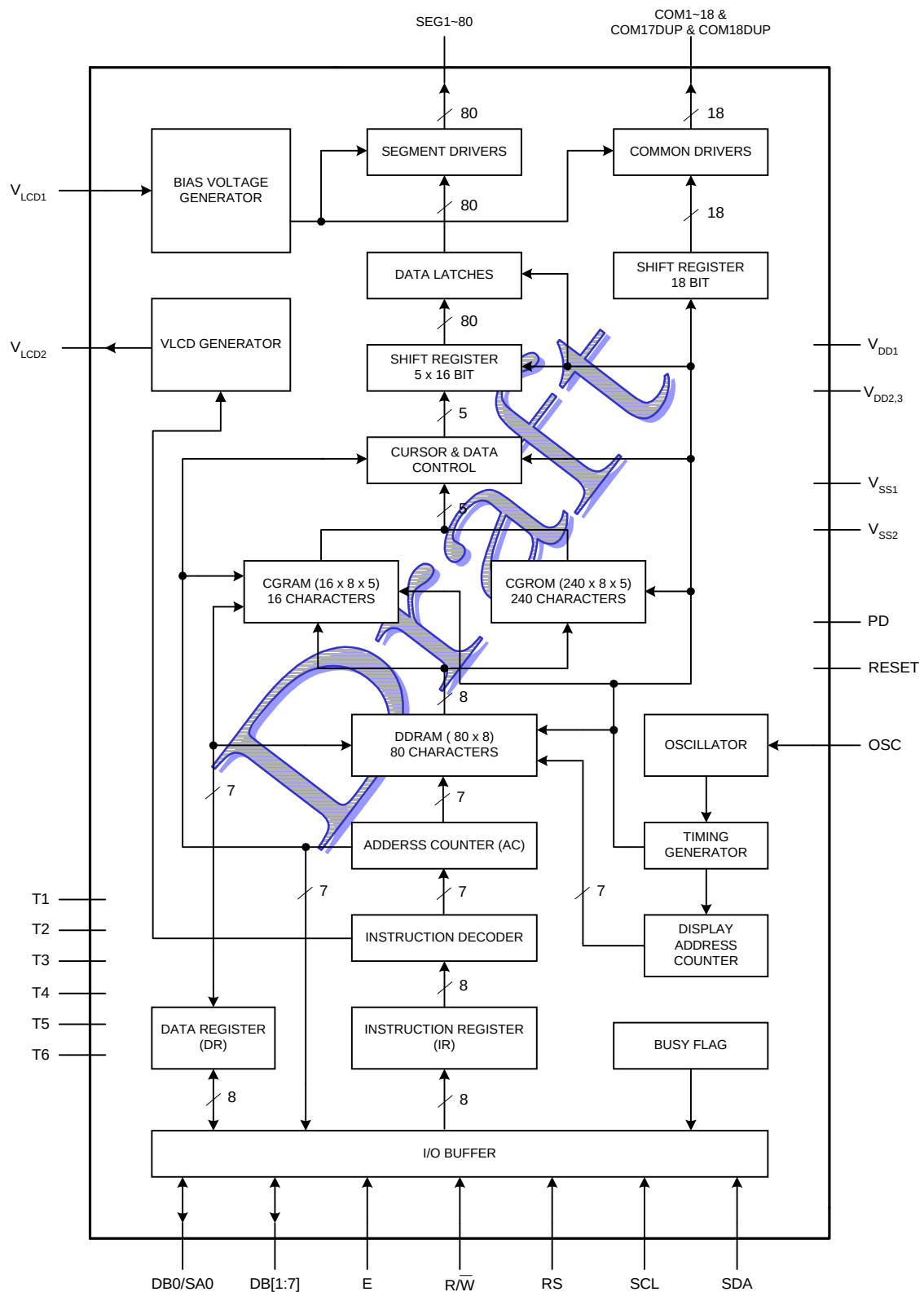
#### Features

- Single-chip LCD controller/driver
- 2-line display of up to 16 characters + 160 icons, 1-line display of up to 32 characters + 160 icons, or 1-line display of up to 16 characters + 80 icons
- 5 × 7 character format plus cursor; 5 × 8 for user defined symbols
- Icon mode:
  - Reduced current consumption while displaying icons only
- On-chip:
  - DC-DC converter generation of LCD supply voltage, independent of V<sub>DD</sub>
  - Temperature compensation of on-chip generated V<sub>LCD</sub>: -8 to -12 mV/K at 5.0 V (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- Versatile display functions provided on chip:
  - Clear display, Return home, Entry mode set, Display control, Cursor /display shift, Character blink, Icon blink, Screen configuration, Icon display control.
- Character Generator ROM:
  - 240 characters (240 × 5 × 8 bits).
- Character Generator RAM:
  - 16 characters (16 × 5 × 8 bits); 4 characters used to drive 160 icons, 8 characters used if icon blink feature is used in application.
- Display Data RAM:
  - 80 characters (80 × 8 bits)
- 18 common and 80 segment outputs
- Three duty factors selected by program:
  - 1/2 duty for icon only mode
  - 1/9 duty for single line operation
  - 1/18 duty for normal operation
- Logic supply voltage range:
  - Chip may be driven with two battery cells.
  - V<sub>DD1</sub> = 1.5 to 3.5 V
- High voltage generator supply voltage range:
  - V<sub>DD2</sub> = 2.2 to 3.5V
- Display supply voltage range:
  - V<sub>LCD</sub> = 4.5 to 6.5 V
- Very low current consumption (V<sub>DD</sub>=3.0V):
  - Icon mode: < 160 μA (DC-DC on)
  - Power-down mode: < 2 μA.
  - Normal mode: < 180 μA (DC-DC on)
- 4 or 8-bit parallel bus and 2-wire I<sup>2</sup>C-bus interface
- CMOS compatible
- Available in COG FORM

#### General Description

The NT7651 is a low power CMOS LCD controller and driver designed to drive a dot matrix LCD display of 2-line by 16 or 1-line by 32 characters with 5 × 8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The NT7651 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I<sup>2</sup>C-bus. The chip contains a character generator and displays alphanumeric character.

## Block Diagram





|         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |        |    |    |        |    |    |        |    |    |        |    |    |        |    |    |        |    |    |        |    |    |        |    |    |        |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |    |    |         |   |   |         |   |   |         |   |   |         |   |   |         |   |   |         |     |     |         |     |     |         |     |     |         |     |     |         |     |     |         |     |     |         |     |     |         |     |     |   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| SEG[70] | 83 | 82 | SEG[71] | 81 | 80 | SEG[72] | 79 | 78 | SEG[73] | 77 | 76 | SEG[74] | 75 | 74 | SEG[75] | 73 | 72 | SEG[76] | 71 | 70 | SEG[77] | 69 | 68 | SEG[78] | 67 | 66 | SEG[79] | 65 | 64 | SEG[80] | 63 | 62 | SEG[1] | 61 | 60 | SEG[2] | 59 | 58 | SEG[3] | 57 | 56 | SEG[4] | 55 | 54 | SEG[5] | 53 | 52 | SEG[6] | 51 | 50 | SEG[7] | 49 | 48 | SEG[8] | 47 | 46 | SEG[9] | 45 | 44 | SEG[10] | 43 | 42 | SEG[11] | 41 | 40 | SEG[12] | 39 | 38 | SEG[13] | 37 | 36 | SEG[14] | 35 | 34 | SEG[15] | 33 | 32 | SEG[16] | 31 | 30 | SEG[17] | 29 | 28 | SEG[18] | 27 | 26 | SEG[19] | 25 | 24 | SEG[20] | 23 | 22 | SEG[21] | 21 | 20 | SEG[22] | 19 | 18 | SEG[23] | 17 | 16 | SEG[24] | 15 | 14 | SEG[25] | 13 | 12 | SEG[26] | 11 | 10 | SEG[27] | 9 | 8 | SEG[28] | 7 | 6 | SEG[29] | 5 | 4 | SEG[30] | 3 | 2 | SEG[31] | 1 | 0 | SEG[32] | 143 | 142 | SEG[33] | 141 | 140 | SEG[34] | 139 | 138 | SEG[35] | 137 | 136 | SEG[36] | 135 | 134 | SEG[37] | 133 | 132 | SEG[38] | 131 | 130 | SEG[39] | 129 | 128 | SEG[40] | 127 | 126 | SEG[41] | 125 | 124 | SEG[42] | 123 | 122 | SEG[43] | 121 | 120 | SEG[44] | 119 | 118 | SEG[45] | 117 | 116 | SEG[46] | 115 | 114 | SEG[47] | 113 | 112 | SEG[48] | 111 | 110 | SEG[49] | 109 | 108 | SEG[50] | 107 | 106 | SEG[51] | 105 | 104 | SEG[52] | 103 | 102 | SEG[53] | 101 | 100 | SEG[54] | 99 | 98 | SEG[55] | 97 | 96 | SEG[56] | 95 | 94 | SEG[57] | 93 | 92 | SEG[58] | 91 | 90 | SEG[59] | 89 | 88 | SEG[60] | 87 | 86 | SEG[61] | 85 | 84 | SEG[62] | 83 | 82 | SEG[63] | 81 | 80 | SEG[64] | 79 | 78 | SEG[65] | 77 | 76 | SEG[66] | 75 | 74 | SEG[67] | 73 | 72 | SEG[68] | 71 | 70 | SEG[69] | 69 | 68 | SEG[70] | 67 | 66 | SEG[71] | 65 | 64 | SEG[72] | 63 | 62 | SEG[73] | 61 | 60 | SEG[74] | 59 | 58 | SEG[75] | 57 | 56 | SEG[76] | 55 | 54 | SEG[77] | 53 | 52 | SEG[78] | 51 | 50 | SEG[79] | 49 | 48 | SEG[80] | 47 | 46 | SEG[81] | 45 | 44 | SEG[82] | 43 | 42 | SEG[83] | 41 | 40 | SEG[84] | 39 | 38 | SEG[85] | 37 | 36 | SEG[86] | 35 | 34 | SEG[87] | 33 | 32 | SEG[88] | 31 | 30 | SEG[89] | 29 | 28 | SEG[90] | 27 | 26 | SEG[91] | 25 | 24 | SEG[92] | 23 | 22 | SEG[93] | 21 | 20 | SEG[94] | 19 | 18 | SEG[95] | 17 | 16 | SEG[96] | 15 | 14 | SEG[97] | 13 | 12 | SEG[98] | 11 | 10 | SEG[99] | 9 | 8 | SEG[100] | 7 | 6 | SEG[101] | 5 | 4 | SEG[102] | 3 | 2 | SEG[103] | 1 | 0 | SEG[104] | 143 | 142 | SEG[105] | 141 | 140 | SEG[106] | 139 | 138 | SEG[107] | 137 | 136 | SEG[108] | 135 | 134 | SEG[109] | 133 | 132 | SEG[110] | 131 | 130 | SEG[111] | 129 | 128 | SEG[112] | 127 | 126 | SEG[113] | 125 | 124 | SEG[114] | 123 | 122 | SEG[115] | 121 | 120 | SEG[116] | 119 | 118 | SEG[117] | 117 | 116 | SEG[118] | 115 | 114 | SEG[119] | 113 | 112 | SEG[120] | 111 | 110 | SEG[121] | 109 | 108 | SEG[122] | 107 | 106 | SEG[123] | 105 | 104 | SEG[124] | 103 | 102 | SEG[125] | 101 | 100 | SEG[126] | 99 | 98 | SEG[127] | 97 | 96 | SEG[128] | 95 | 94 | SEG[129] | 93 | 92 | SEG[130] | 91 | 90 | SEG[131] | 89 | 88 | SEG[132] | 87 | 86 | SEG[133] | 85 | 84 | SEG[134] | 83 | 82 | SEG[135] | 81 | 80 | SEG[136] | 79 | 78 | SEG[137] | 77 | 76 | SEG[138] | 75 | 74 | SEG[139] | 73 | 72 | SEG[140] | 71 | 70 | SEG[141] | 69 | 68 | SEG[142] | 67 | 66 | SEG[143] | 65 | 64 | SEG[144] | 63 | 62 | SEG[145] | 61 | 60 | SEG[146] | 59 | 58 | SEG[147] | 57 | 56 | SEG[148] | 55 | 54 | SEG[149] | 53 | 52 | SEG[150] | 51 | 50 | SEG[151] | 49 | 48 | SEG[152] | 47 | 46 | SEG[153] | 45 | 44 | SEG[154] | 43 | 42 | SEG[155] | 41 | 40 | SEG[156] | 39 | 38 | SEG[157] | 37 | 36 | SEG[158] | 35 | 34 | SEG[159] | 33 | 32 | SEG[160] | 31 | 30 | SEG[161] | 29 | 28 | SEG[162] | 27 | 26 | SEG[163] | 25 | 24 | SEG[164] | 23 | 22 | SEG[165] | 21 | 20 | SEG[166] | 19 | 18 | SEG[167] | 17 | 16 | SEG[168] | 15 | 14 | SEG[169] | 13 | 12 | SEG[170] | 11 | 10 | SEG[171] | 9 | 8 | SEG[172] | 7 | 6 | SEG[173] | 5 | 4 | SEG[174] | 3 | 2 | SEG[175] | 1 | 0 | SEG[176] | 143 | 142 | SEG[177] | 141 | 140 | SEG[178] | 139 | 138 | SEG[179] | 137 | 136 | SEG[180] | 135 | 134 | SEG[181] | 133 | 132 | SEG[182] | 131 | 130 | SEG[183] | 129 | 128 | SEG[184] | 127 | 126 | SEG[185] | 125 | 124 | SEG[186] | 123 | 122 | SEG[187] | 121 | 120 | SEG[188] | 119 | 118 | SEG[189] | 117 | 116 | SEG[190] | 115 | 114 | SEG[191] | 113 | 112 | SEG[192] | 111 | 110 | SEG[193] | 109 | 108 | SEG[194] | 107 | 106 | SEG[195] | 105 | 104 | SEG[196] | 103 | 102 | SEG[197] | 101 | 100 | SEG[198] | 99 | 98 | SEG[199] | 97 | 96 | SEG[200] | 95 | 94 | SEG[201] | 93 | 92 | SEG[202] | 91 | 90 | SEG[203] | 89 | 88 | SEG[204] | 87 | 86 | SEG[205] | 85 | 84 | SEG[206] | 83 | 82 | SEG[207] | 81 | 80 | SEG[208] | 79 | 78 | SEG[209] | 77 | 76 | SEG[210] | 75 | 74 | SEG[211] | 73 | 72 | SEG[212] | 71 | 70 | SEG[213] | 69 | 68 | SEG[214] | 67 | 66 | SEG[215] | 65 | 64 | SEG[216] | 63 | 62 | SEG[217] | 61 | 60 | SEG[218] | 59 | 58 | SEG[219] | 57 | 56 | SEG[220] | 55 | 54 | SEG[221] | 53 | 52 | SEG[222] | 51 | 50 | SEG[223] | 49 | 48 | SEG[224] | 47 | 46 | SEG[225] | 45 | 44 | SEG[226] | 43 | 42 | SEG[227] | 41 | 40 | SEG[228] | 39 | 38 | SEG[229] | 37 | 36 | SEG[230] | 35 | 34 | SEG[231] | 33 | 32 | SEG[232] | 31 | 30 | SEG[233] | 29 | 28 | SEG[234] | 27 | 26 | SEG[235] | 25 | 24 | SEG[236] | 23 | 22 | SEG[237] | 21 | 20 | SEG[238] | 19 | 18 | SEG[239] | 17 | 16 | SEG[240] | 15 | 14 | SEG[241] | 13 | 12 | SEG[242] | 11 | 10 | SEG[243] | 9 | 8 | SEG[244] | 7 | 6 | SEG[245] | 5 | 4 | SEG[246] | 3 | 2 | SEG[247] | 1 | 0 | SEG[248] | 143 | 142 | SEG[249] | 141 | 140 | SEG[250] | 139 | 138 | SEG[251] | 137 | 136 | SEG[252] | 135 | 134 | SEG[253] | 133 | 132 | SEG[254] | 131 | 130 | SEG[255] | 129 | 128 | SEG[256] | 127 | 126 | SEG[257] | 125 | 124 | SEG[258] | 123 | 122 | SEG[259] | 121 | 120 | SEG[260] | 119 | 118 | SEG[261] | 117 | 116 | SEG[262] | 115 | 114 | SEG[263] | 113 | 112 | SEG[264] | 111 | 110 | SEG[265] | 109 | 108 | SEG[266] | 107 | 106 | SEG[267] | 105 | 104 | SEG[268] | 103 | 102 | SEG[269] | 101 | 100 | SEG[270] | 99 | 98 | SEG[271] | 97 | 96 | SEG[272] | 95 | 94 | SEG[273] | 93 | 92 | SEG[274] | 91 | 90 | SEG[275] | 89 | 88 | SEG[276] | 87 | 86 | SEG[277] | 85 | 84 | SEG[278] | 83 | 82 | SEG[279] | 81 | 80 | SEG[280] | 79 | 78 | SEG[281] | 77 | 76 | SEG[282] | 75 | 74 | SEG[283] | 73 | 72 | SEG[284] | 71 | 70 | SEG[285] | 69 | 68 | SEG[286] | 67 | 66 | SEG[287] | 65 | 64 | SEG[288] | 63 | 62 | SEG[289] | 61 | 60 | SEG[290] | 59 | 58 | SEG[291] | 57 | 56 | SEG[292] | 55 | 54 | SEG[293] | 53 | 52 | SEG[294] | 51 | 50 | SEG[295] | 49 | 48 | SEG[296] | 47 | 46 | SEG[297] | 45 | 44 | SEG[298] | 43 | 42 | SEG[299] | 41 | 40 | SEG[300] | 39 | 38 | SEG[301] | 37 | 36 | SEG[302] | 35 | 34 | SEG[303] | 33 | 32 | SEG[304] | 31 | 30 | SEG[305] | 29 | 28 | SEG[306] | 27 | 26 | SEG[307] | 25 | 24 | SEG[308] | 23 | 22 | SEG[309] | 21 | 20 | SEG[310] | 19 | 18 | SEG[311] | 17 | 16 | SEG[312] | 15 | 14 | SEG[313] | 13 | 12 | SEG[314] | 11 | 10 | SEG[315] | 9 | 8 | SEG[316] | 7 | 6 | SEG[317] | 5 | 4 | SEG[318] | 3 | 2 | SEG[319] | 1 | 0 | SEG[320] | 143 | 142 | SEG[321] | 141 | 140 | SEG[322] | 139 | 138 | SEG[323] | 137 | 136 | SEG[324] | 135 | 134 | SEG[325] | 133 | 132 | SEG[326] | 131 | 130 | SEG[327] | 129 | 128 | SEG[328] | 127 | 126 | SEG[329] | 125 | 124 | SEG[330] | 123 | 122 | SEG[331] | 121 | 120 | SEG[332] | 119 | 118 | SEG[333] | 117 | 116 | SEG[334] | 115 | 114 | SEG[335] | 113 | 112 | SEG[336] | 111 | 110 | SEG[337] | 109 | 108 | SEG[338] | 107 | 106 | SEG[339] | 105 | 104 | SEG[340] | 103 | 102 | SEG[341] | 101 | 100 | SEG[342] | 99 | 98 | SEG[343] | 97 | 96 | SEG[344] | 95 | 94 | SEG[345] | 93 | 92 | SEG[346] | 91 | 90 | SEG[347] | 89 | 88 | SEG[348] | 87 | 86 | SEG[349] | 85 | 84 | SEG[350] | 83 | 82 | SEG[351] | 81 | 80 | SEG[352] | 79 | 78 | SEG[353] | 77 | 76 | SEG[354] | 75 | 74 | SEG[355] | 73 | 72 | SEG[356] | 71 | 70 | SEG[357] | 69 | 68 | SEG[358] | 67 | 66 | SEG[359] | 65 | 64 | SEG[360] | 63 | 62 | SEG[361] | 61 | 60 | SEG[362] | 59 | 58 | SEG[363] | 57 | 56 | SEG[364] | 55 | 54 | SEG[365] | 53 | 52 | SEG[366] | 51 | 50 | SEG[367] | 49 | 48 | SEG[368] | 47 | 46 | SEG[369] | 45 | 44 | SEG[370] | 43 | 42 | SEG[371] | 41 | 40 | SEG[372] | 39 | 38 | SEG[373] | 37 | 36 | SEG[374] | 35 | 34 | SEG[375] | 33 | 32 | SEG[376] | 31 | 30 | SEG[377] | 29 | 28 | SEG[378] | 27 | 26 | SEG[379] | 25 | 24 | SEG[380] | 23 | 22 | SEG[381] | 21 | 20 | SEG[382] | 19 | 18 | SEG[383] | 17 | 16 | SEG[384] | 15 | 14 | SEG[385] | 13 | 12 | SEG[386] | 11 | 10 | SEG[387] | 9 | 8 | SEG[388] | 7 | 6 | SEG[389] | 5 | 4 | SEG[390] | 3 | 2 | SEG[391] | 1 | 0 | SEG[392] | 143 | 142 | SEG[393] | 141 | 140 | SEG[394] | 139 | 138 | SEG[395] | 137 | 136 | SEG[396] | 135 | 134 | SEG[397] | 133 | 132 | SEG[398] | 131 | 130 | SEG[399] | 129 | 128 | SEG[400] | 127 | 126 | SEG[401] | 125 | 124 | SEG[402] | 123 | 122 | SEG[403] | 121 | 120 | SEG[404] | 119 | 118 | SEG[405] | 117 | 116 | SEG[406] | 115 | 114 | SEG[407] | 113 | 112 | SEG[408] | 111 | 110 | SEG[409] | 109 | 108 | SEG[410] | 107 | 106 | SEG[411] | 105 | 104 | SEG[412] | 103 | 102 | SEG[413] | 101 | 100 | SEG[414] | 99 | 98 | SEG[415] | 97 | 96 | SEG[416] | 95 | 94 | SEG[417] | 93 | 92 | SEG[418] | 91 | 90 | SEG[419] | 89 | 88 | SEG[420] | 87 | 86 | SEG[421] | 85 | 84 | SEG[422] | 83 | 82 | SEG[423] | 81 | 80 | SEG[424] | 79 | 78 | SEG[425] | 77 | 76 | SEG[426] | 75 | 74 | SEG[427] | 73 | 72 | SEG[428] | 71 | 70 | SEG[429] | 69 | 68 | SEG[430] | 67 | 66 | SEG[431] | 65 | 64 | SEG[432] | 63 | 62 | SEG[433] | 61 | 60 | SEG[434] | 59 | 58 | SEG[435] | 57 | 56 | SEG[436] | 55 | 54 | SEG[437] | 53 | 52 | SEG[438] | 51 | 50 | SEG[439] | 49 | 48 | SEG[440] | 47 | 46 | SEG[441] | 45 | 44 | SEG[442] | 43 | 42 | SEG[443] | 41 | 40 | SEG[444] | 39 | 38 | SEG[445] | 37 | 36 | SEG[446] | 35 | 34 | SEG[447] | 33 | 32 | SEG[448] | 31 | 30 | SEG[449] | 29 | 28 | SEG[450] | 27 | 26 | SEG[451] | 25 | 24 | SEG[452] | 23 | 22 | SEG[453] | 21 | 20 | SEG[454] | 19 | 18 | SEG[455] | 17 | 16 | SEG[456] | 15 | 14 | SEG[457] | 13 | 12 | SEG[458] | 11 | 10 | SEG[459] | 9 | 8 | SEG[460] | 7 | 6 | SEG[461] | 5 | 4 | SEG[462] | 3 | 2 | SEG[463] | 1 | 0 | SEG[464] | 143 | 142 | SEG[465] | 141 | 140 | SEG[466] | 139 | 138 | SEG[467] | 137 | 136 | SEG[468] | 135 | 134 | SEG[469] | 133 | 132 | SEG[470] | 131 | 130 | SEG[471] | 129 | 128 | SEG[472] | 127 | 126 | SEG[473] | 125 | 124 | SEG[474] | 123 | 122 | SEG[475] | 121 | 120 | SEG[476] | 119 | 118 | SEG[477] | 117 | 116 | SEG[478] | 115 | 114 | SEG[479] | 113 | 112 | SEG[480] | 111 | 110 | SEG[481] | 109 | 108 | SEG[482] | 107 | 106 | SEG[483] | 105 | 104 | SEG[484] | 103 | 102 | SEG[485] | 101 | 100 | SEG[486] | 99 | 98 | SEG[487] | 97 | 96 | SEG[488] | 95 | 94 | SEG[489] | 93 | 92 | SEG[490] | 91 | 90 | SEG[491] | 89 | 88 | SEG[492] | 87 | 86 | SEG[493] | 85 | 84 | SEG[494] | 83 | 82 |
|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|--------|----|----|--------|----|----|--------|----|----|--------|----|----|--------|----|----|--------|----|----|--------|----|----|--------|----|----|--------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|---|---|---------|---|---|---------|---|---|---------|---|---|---------|---|---|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|-----|-----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|----|----|---------|---|---|----------|---|---|----------|---|---|----------|---|---|----------|---|---|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|---|---|----------|---|---|----------|---|---|----------|---|---|----------|---|---|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|-----|-----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|----|----------|----|--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**Pad Description**

| Pad No.               |                       | Designation                      | I/O      | Description                                                                                                                                                                                                                                                                             |
|-----------------------|-----------------------|----------------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NT7651                | NT7651R               |                                  |          |                                                                                                                                                                                                                                                                                         |
| 23~26                 | 23~26                 | V <sub>DD1</sub>                 | P        | Logic supply voltage.                                                                                                                                                                                                                                                                   |
| 27~34                 | 27~34                 | V <sub>DD2,3</sub>               | P        | Supply voltage for the high voltage generator. (Always put V <sub>DD2</sub> = V <sub>DD3</sub> ).                                                                                                                                                                                       |
| 39~44                 | 39~44                 | V <sub>SS1</sub>                 | P        | Ground pad for all except the high voltage generator.                                                                                                                                                                                                                                   |
| 45~50                 | 45~50                 | V <sub>SS2</sub>                 | P        | Ground pad for the high voltage generator.                                                                                                                                                                                                                                              |
| 51~56                 | 51~56                 | V <sub>LCD1</sub>                | P        | This input used for the generation of the LCD bias levels.                                                                                                                                                                                                                              |
| 57~62                 | 57~62                 | V <sub>LCD2</sub>                | P        | V <sub>LCD</sub> output pad. If V <sub>LCD</sub> is generated internally, this pad must be connected to V <sub>LCD1</sub> . If in the application an external V <sub>LCD</sub> is used, then the V <sub>LCD2</sub> pin must be left open-circuit.                                       |
| 35                    | 35                    | E                                | I        | The parallel interface data bus clock input. It is set HIGH to signal the start of a read or write operation and data in or out of the chip on falling edge of the clock.<br>When I <sup>2</sup> C-bus is used, the parallel interface pad E must be at logic 0.                        |
| 36                    | 36                    | T1                               | I        | Test pads.<br>T1 and T2 must be connected to V <sub>SS1</sub> ,<br>Others are left open-circuit and are not user accessible. No connect for user.                                                                                                                                       |
| 37                    | 37                    | T2                               | I        |                                                                                                                                                                                                                                                                                         |
| 38                    | 38                    | T3(4)                            | I        |                                                                                                                                                                                                                                                                                         |
| 20                    | 20                    | T4(RC)                           | I        |                                                                                                                                                                                                                                                                                         |
| 19                    | 19                    | T5(M)                            | I        |                                                                                                                                                                                                                                                                                         |
| 10                    | 10                    | T6(D)                            | I        |                                                                                                                                                                                                                                                                                         |
| 63<br>64~71<br>72     | 63<br>71~64<br>72     | COM[17]<br>COM[1:8]<br>COM17DUP  | O        | LCD common driver outputs. COM17 has two pads COM17 and COM17DUP.                                                                                                                                                                                                                       |
| 73~152                | 73~152                | SEG[80:1]                        | O        | LCD segment driver outputs.                                                                                                                                                                                                                                                             |
| 153<br>154~161<br>162 | 153<br>161~154<br>162 | COM18DUP<br>COM[16:9]<br>COM[18] | O        | LCD common driver outputs. COM18 has two pads COM18 and COM18DUP.                                                                                                                                                                                                                       |
| 1,2                   | 1,2                   | SCL                              | I        | I <sup>2</sup> C-bus serial clock input.<br>When the parallel bus is used, It must be connected to V <sub>SS1</sub> or V <sub>DD1</sub> .                                                                                                                                               |
| 4                     | 4                     | RESET                            | I        | External power-on reset input. (High active)                                                                                                                                                                                                                                            |
| 5                     | 5                     | PD                               | I        | Chip power-down mode selects input. Normal operation PD = 0.                                                                                                                                                                                                                            |
| 6,7                   | 6,7                   | SDA                              | I/O      | I <sup>2</sup> C-bus serial data input/output.<br>When the parallel bus is used, It must be connected to V <sub>SS1</sub> or V <sub>DD1</sub> .                                                                                                                                         |
| 8                     | 8                     | R/W                              | I        | Data read/write selects input. Read (R/W = 1) or write (R/W = 0). Internal pull-up.                                                                                                                                                                                                     |
| 9                     | 9                     | RS                               | I        | Register selects signal input. Internal pull-up. RS = 0, selects the instruction register for write and the busy flag and address counter for read. RS = 1, selects the data register for both read and write.                                                                          |
| 11                    | 11                    | DB[0]<br>SA0                     | I/O<br>I | Bidirectional data bus (3-state). In 4-bit operations, It must be left open-circuit. It has its own internal pull-up. In the I <sup>2</sup> C-bus operation, shared with alternative function input (SA0), It can allow connecting two NT7651 drivers to the same I <sup>2</sup> C-bus. |

| Pad No. |         | Designation | I/O | Description                                                                                                                                                                                                              |
|---------|---------|-------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NT7651  | NT7651R |             |     |                                                                                                                                                                                                                          |
| 12~18   | 12~18   | DB[1:7]     | I/O | Bidirectional data bus (3-state). DB7 may be used as the busy flag. In 4-bit operations the 4 higher order lines DB7 to DB4 are used, DB3 to DB0 must be left open-circuit. Each data line has its own internal pull-up. |
| 21,22   | 21,22   | OSC         | I   | Oscillator or external clock input.<br>When the on-chip oscillator is used this pad must be connected to V <sub>DD1</sub> .                                                                                              |
| 3       | 3       | DUMMY       | -   | Left open-circuit or connected to V <sub>SS1</sub> .                                                                                                                                                                     |

Total 162 pads

Draft

## Functional Description

### 1. LCD supply voltage generator

The LCD supply voltage may be generated on-chip. Two internal 6-bit registers control the voltage generator: VA and VB. The nominal LCD operating voltage at room temperature ( $T_{REF} = 27^{\circ}\text{C}$ ) is given by the relationship:

$$V_{LCD} = (\text{integer value of register} \times 0.082) + 1.82$$

Integer value of register programming ranges: 1 to 63.  
Operating voltage ranges: 1.902 to 6.986 V.

#### Notice:

Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage the  $V_{LCD}$  temperature coefficient must be taken into account.

Values below 4.5 V are below the LCD display bias levels threshold voltage and are therefore not allowed.

Value 0 for VA and VB switches the generator off.

Usually register VA is programmed with the voltage for character mode and register VB with the voltage for icon mode.

Table 1 Bias levels for the different duty

| Duty | Bias Levels | V1        | V2                   | V3                   | V4                   | V5                   | V6       |
|------|-------------|-----------|----------------------|----------------------|----------------------|----------------------|----------|
| 1:18 | 5           | $V_{LCD}$ | $V_{LCD} \times 3/4$ | $V_{LCD} \times 1/2$ | $V_{LCD} \times 1/2$ | $V_{LCD} \times 1/4$ | $V_{SS}$ |
| 1:9  | 5           | $V_{LCD}$ | $V_{LCD} \times 3/4$ | $V_{LCD} \times 1/2$ | $V_{LCD} \times 1/2$ | $V_{LCD} \times 1/4$ | $V_{SS}$ |
| 1:2  | 4           | $V_{LCD}$ | $V_{LCD} \times 2/3$ | $V_{LCD} \times 2/3$ | $V_{LCD} \times 1/3$ | $V_{LCD} \times 1/3$ | $V_{SS}$ |

$V_{SS} = 0V$ .

### 3. Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC pad must be connected to  $V_{DD}$ .

Only in the power-down state is the clock allowed to be stopped (OSC connected to  $V_{SS}$ ), otherwise the LCD is frozen in a DC state.

### 4. Power-on reset

It must be reset externally. This is an internal synchronous reset that requires 3 OSC cycles to be executed after release of the external reset signal. If no external reset is performed, the chip might start-up in an unwanted state. The external reset is active HIGH.

### 5. Power-down mode

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to  $V_{SS}$ ) when PD = 1.

When  $V_{LCD}$  is generated on-chip the  $V_{LCD}$  pads should be decoupled to  $V_{SS}$  with a suitable capacitor. The generated  $V_{LCD}$  is independent of  $V_{DD}$  and is temperature compensated.

When the generator is switched off an external voltage may be supplied at connected pads  $V_{LCD1}$ .  $V_{LCD1}$  may be higher than  $V_{DD}$ .

The LCD supply voltage generator ensures that, as long as  $V_{DD}$  is in the valid range (2.2 to 3.5V), the required peak voltage  $V_{LCD} = 6.5V$  can be generated at any time.

### 2. LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. The optimum value of  $V_{LCD}$  depends on the LCD duty, the LCD threshold voltage ( $V_{TH}$ ) and the number of bias levels. Using a 5-level bias scheme for 1:18 maximum duty allows  $V_{LCD} < 5V$  for most LCD liquids. The intermediate bias levels for the different duty are shown in Table 1. These bias levels are automatically set to the given values when switching to the corresponding LCD duty.

To ensure  $I_{DD} < 1 \mu A$ , the parallel bus pads DB7 to DB0 should be connected to  $V_{DD}$ ; RS and  $\overline{R/W}$  to  $V_{DD}$  or left open-circuit.

During power-down, information in the RAMs and the Chip State are preserved. Instruction execution during power-down is possible when pad OSC is externally clocked.

Recovery from power-down mode: PD back to logic 0, if necessary OSC back to  $V_{DD}$  and send a 'display control' instruction.

### 6. Busy flag

The busy flag indicates the internal status of the chip. Logic 1 indicates that the chip is busy and further instructions will not be accepted.

The busy flag is output to pad DB7 when RS = 0 and  $\overline{R/W} = 1$ . Instructions should only be written after checking that the busy flag is at logic 0 or waiting for the required number of cycles.

## 7. Registers

The NT7651 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM).

The instruction register can be written to but not read from by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the 'read data' instruction.

## 8. Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands 'set CGRAM address' and 'set DDRAM address'. After a read/write operation the address counter is automatically incremented or decremented by 1.

Table 2 Address space and wrap-around operation

| MODE                                          | 1 × 32   | 2 × 16             | 1 × 16   |
|-----------------------------------------------|----------|--------------------|----------|
| Address space                                 | 00 to 4F | 00 to 27; 40 to 67 | 00 to 27 |
| Read/write wrap-around (moves to next line)   | 4F to 00 | 27 to 40; 67 to 00 | 27 to 00 |
| Display shift wrap-around (stays within line) | 4F to 00 | 27 to 00; 67 to 40 | 27 to 00 |

## 10. Character Generator ROM (CGROM)

The Character Generator ROM generates 240 character patterns in a 5 × 8 dot format from 8-bit character codes.

Figure 5, Figure 6 shows the character set that is currently implemented.

The address counter contents are output to the bus (DB6 to DB0) when RS = 0 and  $\overline{R/\overline{W}} = 1$ .

## 9. Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations that are not used for storing display data can be used as general purpose RAM. The basic RAM to display addressing scheme is shown in Figure 2. With no display shift the characters represented by the codes in the first 32 RAM locations starting at address 00H in line 1 are displayed. Figure 3 and Figure 4 show the display mapping for right and left shift respectively. When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.

The address ranges and wrap-around operations for the various modes are shown in Table 2.

## 11. Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Figure 1) at the DDRAM address contained in the address counter. When the address counter contains the CGRAM address the cursor will be inhibited.

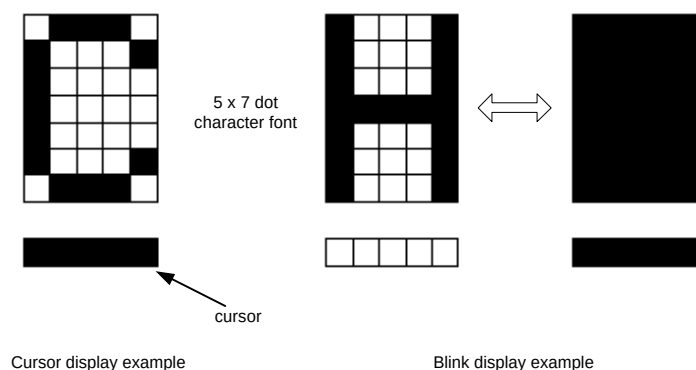


Figure 1 Cursor and blink display examples.



## 12. Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the Character Generator RAM. Some CGRAM characters (see Figure 10) are also used to drive icons (8 if icons blink and both icon commons are used in the application; 4 if no blink but both icon commons are used in the application; 0 if no icons are driven by the icon commons).

The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM.

Table 3 shows the addressing principle for the CGRAM.

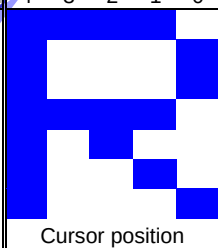
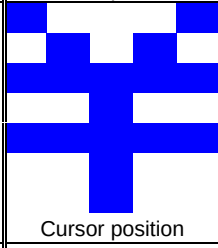
Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the 'set CGRAM address' command. Bit 6 can be set using the 'set DDRAM address' command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the 'read busy flag and address counter' command.

Table 3 Relationship between CGRAM addresses data and display patterns

| Character codes (DDRAM data) |   |   |   |            |   |   |   | CGRAM address |        |   |   |   |            |   |                                                                                      | CGRAM data (example) |       |                    |   |   |   |   |                |   |  |  |  |
|------------------------------|---|---|---|------------|---|---|---|---------------|--------|---|---|---|------------|---|--------------------------------------------------------------------------------------|----------------------|-------|--------------------|---|---|---|---|----------------|---|--|--|--|
| Higher                       |   |   |   | Order bits |   |   |   | Lower         | Higher |   |   |   | Order bits |   |                                                                                      |                      | Lower | Character patterns |   |   |   |   | Character code |   |  |  |  |
| 7                            | 6 | 5 | 4 | 3          | 2 | 1 | 0 | 6             | 5      | 4 | 3 | 2 | 1          | 0 | 4                                                                                    | 3                    | 2     | 1                  | 0 | 4 | 3 | 2 | 1              | 0 |  |  |  |
| 0                            | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0             | 0      | 0 | 0 | 0 | 0          | 0 |   |                      |       |                    |   | 1 | 1 | 1 | 1              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 0 | 0 | 0              | 1 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 0 | 0 | 0              | 1 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 1 | 1 | 1              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 0 | 1 | 0              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 0 | 0 | 1              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 0 | 0 | 0              | 1 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 0 | 0 | 0              | 1 |  |  |  |
| 0                            | 0 | 0 | 0 | 0          | 0 | 0 | 1 | 0             | 0      | 0 | 1 | 0 | 0          | 0 |  |                      |       |                    |   | 1 | 0 | 0 | 0              | 1 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 0 | 1 | 0 | 1              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 1 | 1 | 1              | 1 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 0 | 0 | 1 | 0              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 1 | 1 | 1 | 1              | 1 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 0 | 0 | 1 | 0              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 0 | 0 | 1 | 0              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   | 0 | 0 | 1 | 0              | 0 |  |  |  |
| 0                            | 0 | 0 | 0 | 0          | 0 | 0 | 1 | 0             | 0      | 1 | 0 | 0 | 0          | 0 |                                                                                      |                      |       |                    |   | 0 | 0 | 0 | 0              | 0 |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   |   |   |   |                |   |  |  |  |
|                              |   |   |   |            |   |   |   |               |        |   |   |   |            |   |                                                                                      |                      |       |                    |   |   |   |   |                |   |  |  |  |
| 0                            | 0 | 0 | 0 | 1          | 1 | 1 | 1 | 1             | 1      | 1 | 1 | 1 | 1          | 0 |                                                                                      |                      |       |                    |   |   |   |   |                |   |  |  |  |
| 0                            | 0 | 0 | 0 | 1          | 1 | 1 | 1 | 1             | 1      | 1 | 1 | 1 | 1          | 1 |                                                                                      |                      |       |                    |   |   |   |   |                |   |  |  |  |

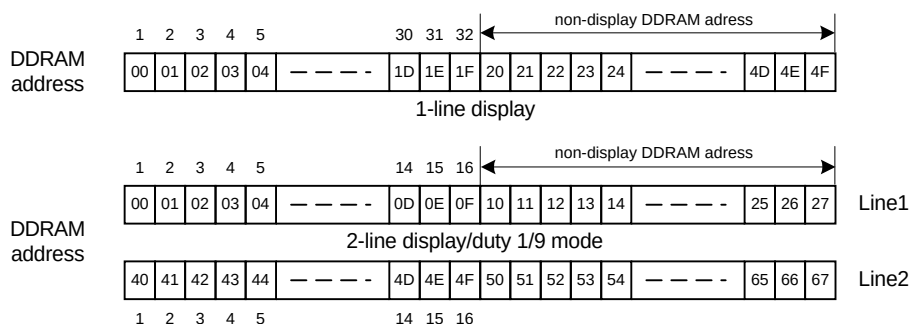


Figure 2 DDRAM to display mapping: no shift.

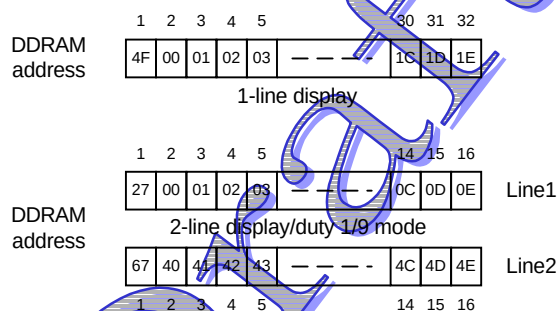


Figure 3 DDRAM to display mapping: right shift.

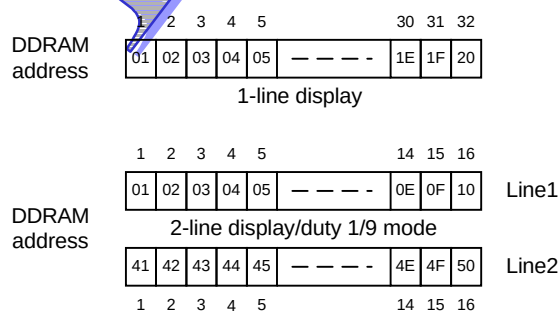


Figure 4 DDRAM to display mapping: left shift.

| upper<br>lower<br>4bits<br>4bits |    | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|----------------------------------|----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| xxx 0000                         | 1  | 1    | 2    | 3    | 4    | 5    | 6    | 7    | 8    | 9    | A    | B    | C    | D    | E    | F    | G    |
| xxx 0001                         | 2  | H    | I    | J    | K    | L    | M    | N    | O    | P    | Q    | R    | S    | T    | U    | V    | W    |
| xxx 0010                         | 3  | X    | Y    | Z    | [    | \    | ]    | ^    | _    | `    | a    | b    | c    | d    | e    | f    | g    |
| xxx 0011                         | 4  | h    | i    | j    | k    | l    | m    | n    | o    | p    | q    | r    | s    | t    | u    | v    | w    |
| xxx 0100                         | 5  | x    | y    | z    | {    |      | }    | ~    |      | ¡    | ¢    | £    | ¥    | ¦    | §    | ¨    | ©    |
| xxx 0101                         | 6  | ª    | «    | ¬    | ®    | ¯    | °    | ±    | ²    | ³    | ´    | µ    | ¶    | ·    | ¸    | ¹    | º    |
| xxx 0110                         | 7  | »    | ¼    | ½    | ¾    | ¿    | À    | Á    | Â    | Ã    | Ä    | Å    | Æ    | Ç    | Ð    | Ñ    | Ò    |
| xxx 0111                         | 8  | Ó    | Ô    | Õ    | Ö    | ×    | Ø    | Ù    | Ú    | Û    | Ü    | Ý    | Þ    | ß    | à    | á    | â    |
| xxx 1000                         | 9  | ã    | ä    | å    | æ    | ç    | ð    | ñ    | ò    | ó    | ô    | õ    | ö    | ÷    | ø    | ù    | ú    |
| xxx 1001                         | 10 | û    | ü    | ý    | þ    | ß    | À    | Á    | Â    | Ã    | Ä    | Å    | Æ    | Ç    | Ð    | Ñ    | Ò    |
| xxx 1010                         | 11 | Ó    | Ô    | Õ    | Ö    | ×    | Ø    | Ù    | Ú    | Û    | Ü    | Ý    | Þ    | ß    | à    | á    | â    |
| xxx 1011                         | 12 | ã    | ä    | å    | æ    | ç    | ð    | ñ    | ò    | ó    | ô    | õ    | ö    | ÷    | ø    | ù    | ú    |
| xxx 1100                         | 13 | û    | ü    | ý    | þ    | ß    | À    | Á    | Â    | Ã    | Ä    | Å    | Æ    | Ç    | Ð    | Ñ    | Ò    |
| xxx 1101                         | 14 | Ó    | Ô    | Õ    | Ö    | ×    | Ø    | Ù    | Ú    | Û    | Ü    | Ý    | Þ    | ß    | à    | á    | â    |
| xxx 1110                         | 15 | ã    | ä    | å    | æ    | ç    | ð    | ñ    | ò    | ó    | ô    | õ    | ö    | ÷    | ø    | ù    | ú    |
| xxx 1111                         | 16 | û    | ü    | ý    | þ    | ß    | À    | Á    | Â    | Ã    | Ä    | Å    | Æ    | Ç    | Ð    | Ñ    | Ò    |

Figure 5 Character set 'stand code R' in CGROM.

| upper<br>4bits<br>lower<br>4bits |    | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|----------------------------------|----|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| xxx 0000                         | 1  | ▲    |      | □    | ▣    | ▤    | ▥    | ▦    | ▧    | ▨    | ▩    |      | ▪    | ▫    | ▬    | ▭    | ▮    |
| xxx 0001                         | 2  | ⬤    | ⬥    | ⬦    | ⬧    | ⬨    | ⬩    | ⬪    | ⬫    | ⬬    | ⬭    | ⬮    | ⬯    | ⬰    | ⬱    | ⬲    | ⬳    |
| xxx 0010                         | 3  | ⬴    | ⬵    | ⬶    | ⬷    | ⬸    | ⬹    | ⬺    | ⬻    | ⬼    | ⬽    | ⬾    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 0011                         | 4  | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 0100                         | 5  | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 0101                         | 6  | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 0110                         | 7  | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 0111                         | 8  | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 1000                         | 9  | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 1001                         | 10 | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 1010                         | 11 | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 1011                         | 12 | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 1100                         | 13 | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 1101                         | 14 | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 1110                         | 15 | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |
| xxx 1111                         | 16 | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    | ⬿    |

Figure 6 Character set 'stand code S' in CGROM .

### 13. LCD common and segment drivers

The NT7651 contains 18 common and 80 segment drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. COM17 and COM18 drive the icon common. The bias voltages and the timing are selected automatically when the number of lines in the display is selected.

$f_{\text{FRAME}} = f_{\text{OSC}}/2880$ , Figure 7 to Figure 9 show typical waveforms.

Unused outputs should be left unconnected.

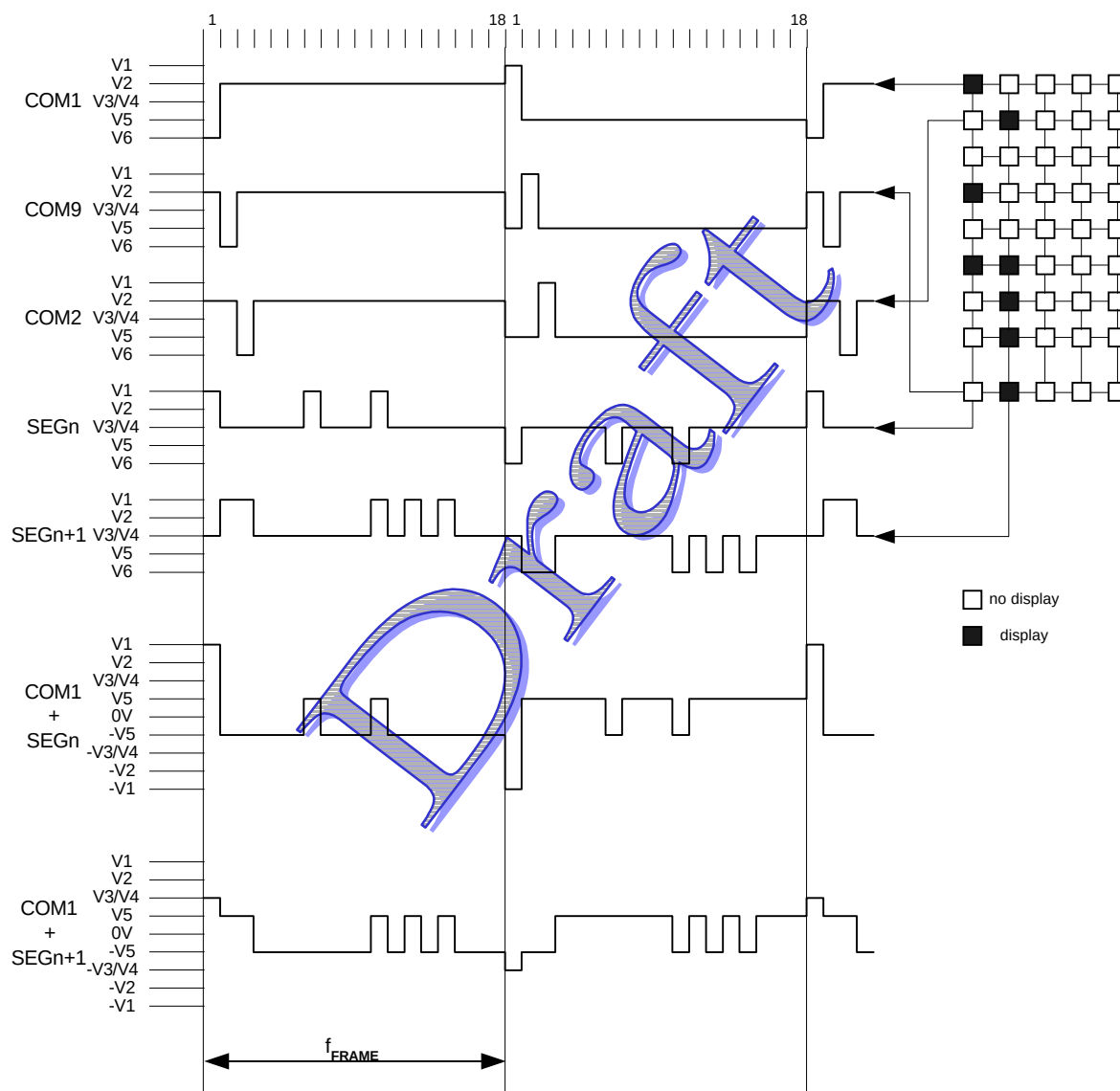


Figure 7 1/18 duty LCD waveforms (Characters + 160 icons mode).

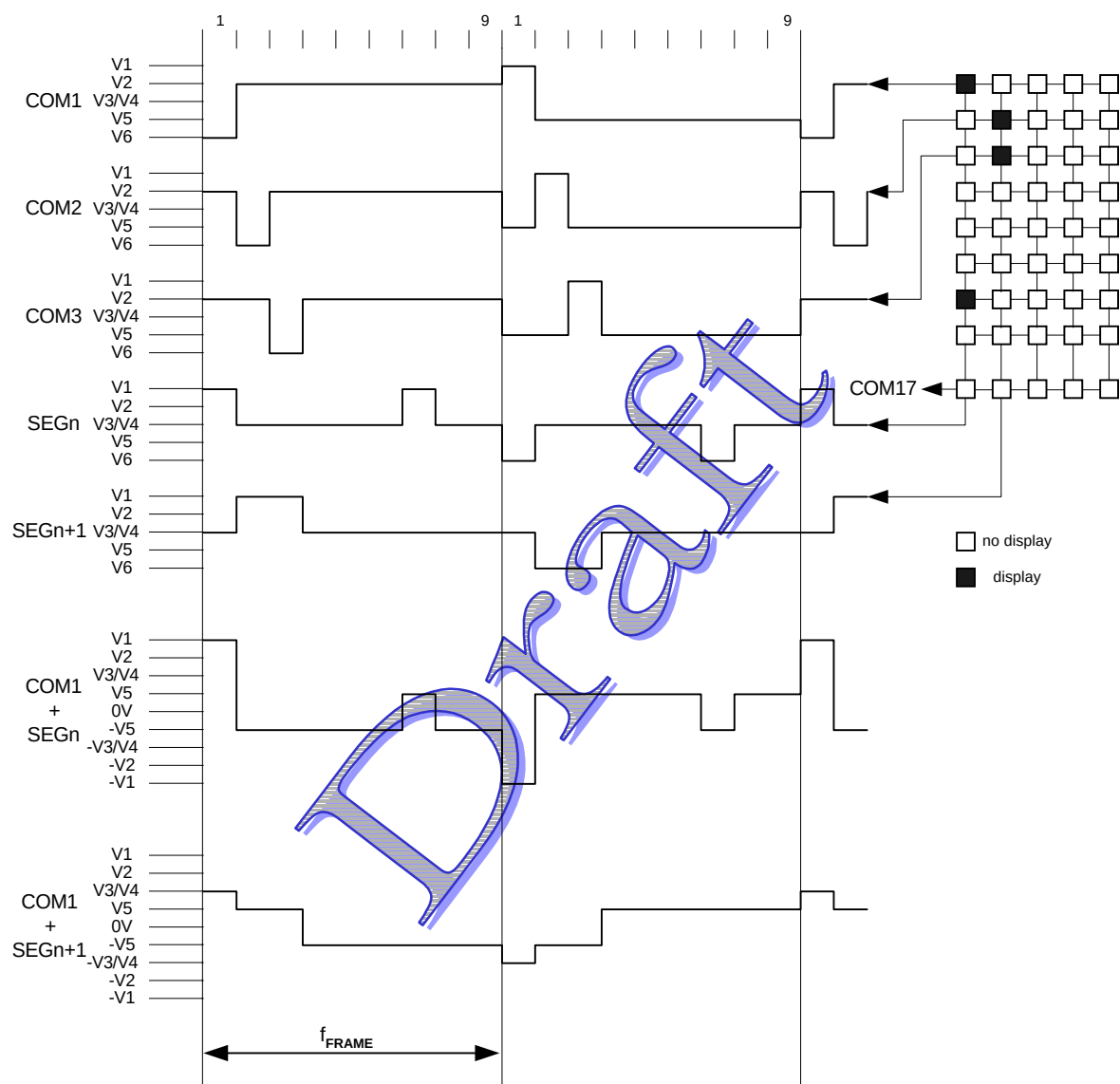


Figure 8 1/9 duty LCD waveforms (Characters + 80 icons mode).

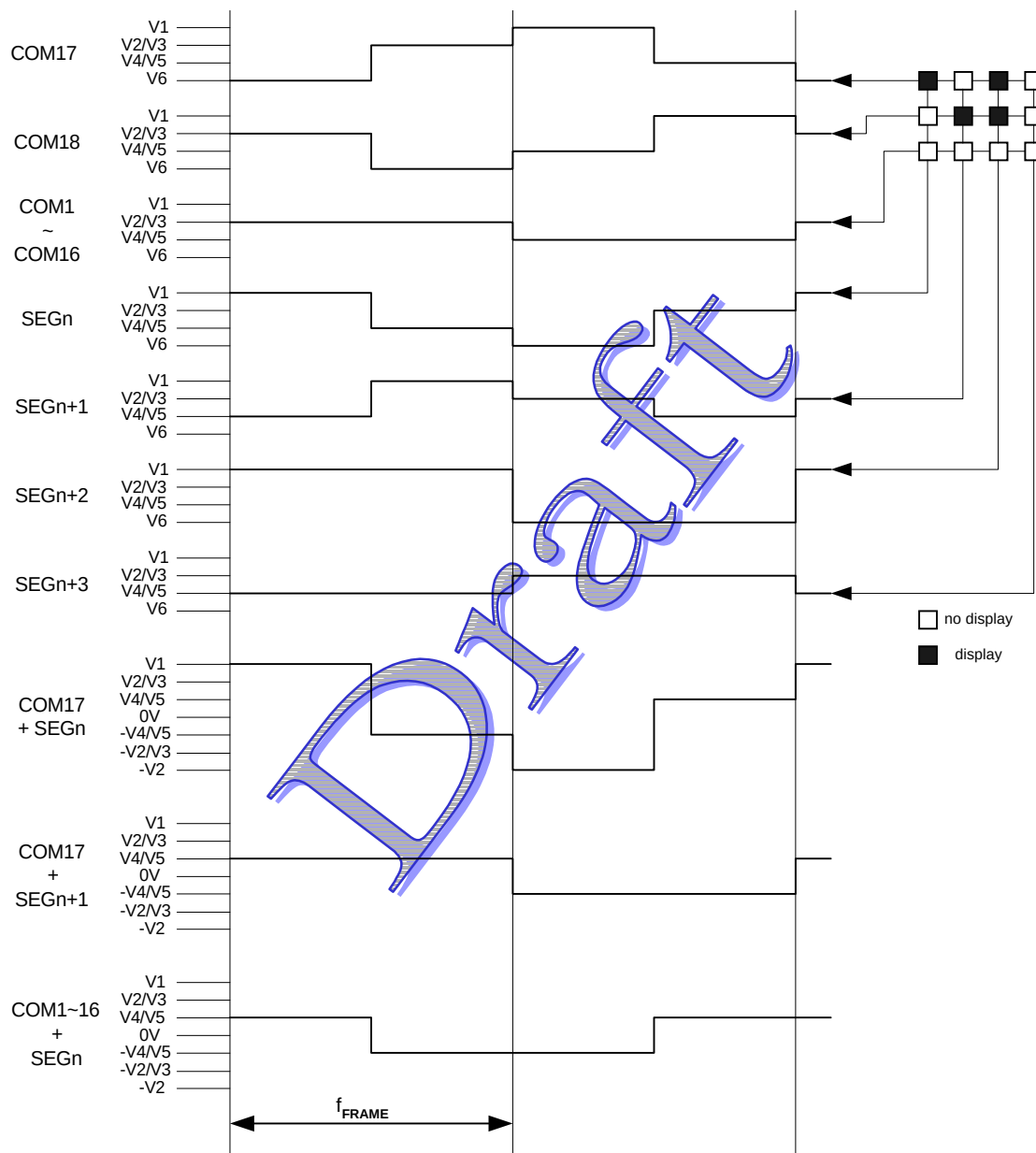


Figure 9 1/2 duty LCD waveforms (Icon mode).

## Initial State

The NT7651 must be reset externally when power is turned on. The reset executes a 'clear display', requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 4.

Table 4 State after reset

| Step | Function                                 | Control bit state | Remarks                                                                                                                     |
|------|------------------------------------------|-------------------|-----------------------------------------------------------------------------------------------------------------------------|
| 1    | Clear display                            |                   |                                                                                                                             |
| 2    | Entry mode set                           | I/D= 1            | +1 (increment)                                                                                                              |
|      |                                          | S=0               | No shift                                                                                                                    |
| 3    | Display control                          | D=0               | Display off                                                                                                                 |
|      |                                          | C=0               | Cursor off                                                                                                                  |
|      |                                          | B=0               | Cursor character blink off                                                                                                  |
| 4    | Function set                             | DL= 1             | 8-bit interface                                                                                                             |
|      |                                          | M=0               | 1-line display                                                                                                              |
|      |                                          | H=0               | Normal instruction set                                                                                                      |
|      |                                          | SL=0              | Duty 1/18 mode                                                                                                              |
| 5    | Default address pointer to DDRAM         |                   |                                                                                                                             |
| 6    | Busy Flag (BF) indicates                 | BF = 1            | The busy state lasts 2 ms, until initialization ends. The chip may also be initialized by software. see Table 5 and Table 6 |
| 7    | Icon control                             | IM; IB=00         | icons/icon blink disabled                                                                                                   |
| 8    | Display/screen configuration             | L=0; P = 0; Q=0   | default configurations                                                                                                      |
| 9    | V <sub>LCD</sub> temperature coefficient | TC1= 0; TC2=0     | default temperature coefficient                                                                                             |
| 10   | Set V <sub>LCD</sub>                     | VA =0; VB =0      | V <sub>LCD</sub> generator off                                                                                              |
| 11   | I <sup>2</sup> C-bus interface reset     |                   |                                                                                                                             |
|      |                                          |                   |                                                                                                                             |



Table 5 Initialization by instruction, 8- bit interface

| Step                                           |            |            |            |            |            |            |            |            |            | Description                                                                                                      |
|------------------------------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------------------------------------------------------------------------------------------------------------|
| Power-on or unknown state                      |            |            |            |            |            |            |            |            |            |                                                                                                                  |
| Wait 2ms after external reset has been applied |            |            |            |            |            |            |            |            |            |                                                                                                                  |
| <b>RS</b>                                      | <b>R/W</b> | <b>DB7</b> | <b>DB6</b> | <b>DB5</b> | <b>DB4</b> | <b>DB3</b> | <b>DB2</b> | <b>DB1</b> | <b>DB0</b> | Function set (interface is 8bits long).<br>BF cannot be checked before this instruction.<br>X = don't care.      |
| 0                                              | 0          | 0          | 0          | 1          | 1          | X          | X          | X          | X          |                                                                                                                  |
| Wait 2ms                                       |            |            |            |            |            |            |            |            |            |                                                                                                                  |
| 0                                              | 0          | 0          | 0          | 1          | 1          | X          | X          | X          | X          |                                                                                                                  |
| Wait more than 40μs                            |            |            |            |            |            |            |            |            |            | The waiting time between instructions is the specified instruction time. (See Table 9)                           |
| 0                                              | 0          | 0          | 0          | 1          | 1          | X          | X          | X          | X          | Function set (interface is 8bits long)<br>BF can be checked after the following instructions.<br>X = don't care. |
| 0                                              | 0          | 0          | 0          | 1          | 1          | 0          | M          | SL         | H          | Function set (interface is 8bits long),<br>specify the number of display lines                                   |
| 0                                              | 0          | 0          | 0          | 0          | 0          | 1          | 0          | 0          | 0          | display off                                                                                                      |
| 0                                              | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 1          | clear display                                                                                                    |
| 0                                              | 0          | 0          | 0          | 0          | 0          | 0          | 1          | I/D        | S          | entry mode set                                                                                                   |
| Instruction initialization ends                |            |            |            |            |            |            |            |            |            |                                                                                                                  |

Table 6 Initialization by instruction, 4- bit interface

| Step                                           |            |            |            |            |            | Description                                                                                   |
|------------------------------------------------|------------|------------|------------|------------|------------|-----------------------------------------------------------------------------------------------|
| Power-on or unknown state                      |            |            |            |            |            |                                                                                               |
| Wait 2ms after external reset has been applied |            |            |            |            |            |                                                                                               |
| <b>RS</b>                                      | <b>R/W</b> | <b>DB7</b> | <b>DB6</b> | <b>DB5</b> | <b>DB4</b> | Function set (interface is 8bits long).<br>BF cannot be checked before this instruction.      |
| 0                                              | 0          | 0          | 0          | 1          | 1          |                                                                                               |
| Wait 2ms                                       |            |            |            |            |            |                                                                                               |
| 0                                              | 0          | 0          | 0          | 1          | 1          |                                                                                               |
| Wait more than 40μs                            |            |            |            |            |            | The waiting time between instructions is the specified instruction time. (See Table 9)        |
| 0                                              | 0          | 0          | 0          | 1          | 1          | Function set (interface is 8bits long)<br>BF can be checked after the following instructions. |
| 0                                              | 0          | 0          | 0          | 1          | 0          | Function set (interface to 4bits long)                                                        |
| 0                                              | 0          | 0          | 0          | 1          | 0          | Function set (interface is 4bits long),<br>specify the number of display lines                |
| 0                                              | 0          | 0          | M          | SL         | H          |                                                                                               |
| 0                                              | 0          | 0          | 0          | 0          | 0          | display off                                                                                   |
| 0                                              | 0          | 1          | 0          | 0          | 0          |                                                                                               |
| 0                                              | 0          | 0          | 0          | 0          | 0          | clear display                                                                                 |
| 0                                              | 0          | 0          | 0          | 0          | 1          |                                                                                               |
| 0                                              | 0          | 0          | 0          | 0          | 0          | entry mode set                                                                                |
| 0                                              | 0          | 0          | 1          | I/D        | S          |                                                                                               |
| Instruction initialization ends                |            |            |            |            |            |                                                                                               |

## Instructions

Only the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers, to allow interfacing to various types of MPUs that operate at different speeds or to allow interface to peripheral control ICs.

The NT7651 operation is controlled by the instructions shown in Table 9 together with their execution time.

During internal operation, no instructions other than the 'read busy flag' and 'read address' instructions will be executed. Because the busy flag is set to a logic 1 while an instruction is being executed, check to ensure it is a logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 9.

### Standard instruction details explain

H = 0, sets the chip into standard instruction set mode.

#### 1. Clear display

'Clear display' writes character code A0H into all DDRAM addresses (the character pattern for character code A0H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the first display line. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed.

#### 2. Return home

'Return home' sets the DDRAM address counter to logic 0 and returns the display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

#### 3. Entry mode set

##### (a) I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

##### (b) S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM.

When S = 0, the display does not shift.

#### 4. Display control (and partial power-down mode)

##### (a) D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting D to logic 1.

When the display is off (D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V<sub>ss</sub>
- The LCD voltage generator and bias generator are turned off.
- Three oscillator cycles are required after sending the 'display off' instruction ensure all outputs are at V<sub>ss</sub>, afterwards OSC can be stopped, if the oscillator is running, the chip can still execute instructions.

##### (b) C

The cursor is displayed when C = 1 and inhibited when C = 0. The cursor is displayed using 5 dots in the 8th line (see Figure 1).

##### (c) B

B = 0, cursor character blink off.

B = 1, the character indicated by the cursor blinks.

The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 second. The cursor underline and the cursor character blink can be set to display simultaneously.

#### 5. Function set

##### (a) DL (Parallel mode only)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus.

In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on, M, SL and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set M, SL and H to their required values.

I<sup>2</sup>C-bus interface set the DL bit to logic 1.

##### (b) M

Selects either 1-line by 32 display (M = 0) or 2-line by 16 display (M = 1).

(c) SL

Selects duty 1/9, 1-line by 16 display (independent of M and L). Only COMs 1 to 8 and 17 are to be used. All other COMs must be left open-circuit. The DDRAM map is the same as in the 2-line by 16 display mode, however, the second line is not displayable.

(d) H

When H = 0 the chip can be programmed via the standard 11 instruction codes.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

## 6. Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

## 7. Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address into the address counter (binary A5 to A0). Data can then be written to or read from the CGRAM.

**Attention:** The CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A6 to A0). With the 'set CGRAM address' command, only bits 5 to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write. All bits 6 to 0 can be read using the 'read busy flag' and 'read address' command.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

## 8. Set DDRAM address

'Set DDRAM address' sets the DDRAM address into the address counter (binary A6 to A0). Data can then be written to or read from the DDRAM.

## 9. Read busy flag and read address

'Read busy flag' and 'read address' read the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0. It is recommended that the BF status is checked before the next write operation is executed.

At the same time, the value of the address counter expressed in binary A6 to A0 is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

## 10. Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D7 to D0 to the CGRAM or the DDRAM. Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command.

Only bits D4 to D0 of CGRAM data are valid, bits D7 to D5 are 'don't care'.

After writing, the address automatically increments or decrements by 1, in accordance with the entry mode.

## 11. Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D7 to D0 from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while E is HIGH. After E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

There are only three instructions that update the data register:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions do not modify the data register content.

## Extended instruction details explain

H = 1, sets the chip into extended instruction set mode.

### 1. Icon control

The NT7651 can drive up to 160 icons. See Figure 10 for CGRAM to icon mapping.

#### (a) IM (Display mode)

When IM = 0, the chip is in character mode. In the character mode characters and icons are driven (duty 1/18). The V<sub>LCD</sub> generator, if used, produces the V<sub>LCD</sub> voltage programmed in register VA.

When IM = 1, the chip is in icon mode. In the icon mode only the icons are driven (duty 1/2) and the V<sub>LCD</sub> voltage generator, if used, produces the V<sub>LCD</sub> voltage as programmed in register VB.

#### (b) IB (Icon blink control)

Icon blink control is independent of the cursor and character blink function.

When IB = 0, icon blink is disabled. Icon data is stored in CGRAM character 0 to 3 ( $4 \times 5 \times 8 = 160$  bits for 160 icons).

When IB = 1, icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor character blink all on and normal display phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 3 ( $4 \times 5 \times 8 = 160$  bits for 160 icons). These bits also define icon state when icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 7 (another 160 bits for the 160 icons).

When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

### 2. Screen configuration L

Only in 1-line 32 characters display mode.

Default is L = 0.

L = 0: the two halves of a split screen are connected in a standard way. 1st 16characters of 32: segments are from 1to80, 2nd 16characters of 32: segments are from 1 to 80.

L = 1: the two halves of a split screen are connected in a mirrored way. 1st 16characters of 32: segments are from 1to80, 2nd 16characters of 32: segments are from 80 to 1.

This allows single layer PCB or glass layout.

### 3. Display configuration

P, Q: default is P, Q = 0.

P = 1: mirrors the segment data.

Q = 1: mirrors the common data.

### 4. Temperature control

Default is TC1 and TC2 = 0.

This selects the default temperature coefficient for the internally generated V<sub>LCD</sub>. See Table 11.

### 5. Set V<sub>LCD</sub>

The V<sub>LCD</sub> value is programmed by instruction. Two on-chip registers hold V<sub>LCD</sub> values for the character mode and the icon mode respectively (VA and VB). The generated V<sub>LCD</sub> value is independent of V<sub>DD</sub>, allowing battery operation of the chip.

V<sub>LCD</sub> programming:

1. Send 'function set' instruction with H = 1

2. Send 'set VLCD' instruction to write to voltage register.

a) DB7, DB6 = 10:

DB5 to DB0 are V<sub>LCD</sub> of character mode (VA)

b) DB7, DB6 = 11:

DB5 to DB0 are V<sub>LCD</sub> of icon mode (VB)

c) DB5 to DB0 = 000000

Switches V<sub>LCD</sub> generator off (when selected)

3. Send 'function set' instruction with H = 0 to resume normal programming.

During 'display off' and power-down the V<sub>LCD</sub> generator is also disabled.

### 6. Reducing current consumption

Reducing current consumption can be achieved by one of the options given in Table 7.

When V<sub>LCD</sub> lie outside the V<sub>DD</sub> range and must be generated, it is usually more efficient to use the on-chip generator than an external regulator.

Table 7 Reducing current consumption

| Original Mode  | Alternative Mode            |
|----------------|-----------------------------|
| Character mode | icon mode (control bit IM)  |
| Display on     | display off (control bit D) |
| Any mode       | power-down (PD pad)         |

Table 8 Instruction set for I<sup>2</sup>C-bus commands

| CONTROL BYTE |    |   |   |   |   |   |   | COMMAND BYTE |     |     |     |     |     |     |     | I <sup>2</sup> C-BUS COMMANDS               |  |
|--------------|----|---|---|---|---|---|---|--------------|-----|-----|-----|-----|-----|-----|-----|---------------------------------------------|--|
| Co           | RS | 0 | 0 | 0 | 0 | 0 | 0 | DB7          | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | R/W is set together with the slave address. |  |

Table 9 Instruction set with parallel bus commands

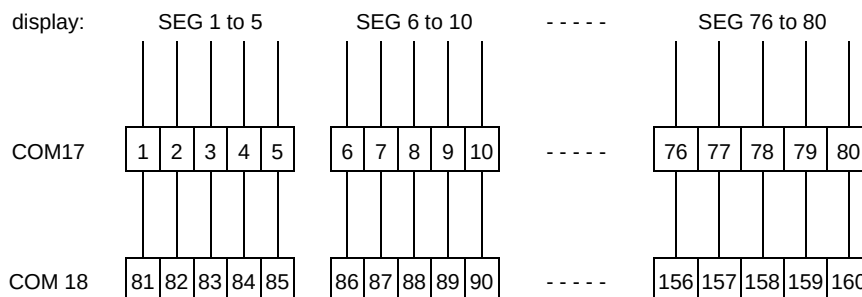
| Instruction                        | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Description                                                                                                                                         | Required clock cycles |
|------------------------------------|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| <b>H=0 or 1</b>                    |    |     |     |     |     |     |     |     |     |     |                                                                                                                                                     |                       |
| NOP                                | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | no operation                                                                                                                                        | 3                     |
| Function set                       | 0  | 0   | 0   | 0   | 1   | DL  | 0   | M   | SL  | H   | sets interface Data Length (DL) and number of display lines (M); single line/duty 1/9 (SL), extended instruction set control (H)                    | 3                     |
| Read busy flag and address counter | 0  | 1   | BF  | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | reads the Busy Flag (BF) indicating internal operating is being performed and reads address counter contents                                        | 0                     |
| Read data                          | 1  | 1   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | reads CGRAM or DDRAM data                                                                                                                           | 3                     |
| Write data                         | 1  | 0   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | writes CGRAM or DDRAM data                                                                                                                          | 3                     |
| <b>H=0</b>                         |    |     |     |     |     |     |     |     |     |     |                                                                                                                                                     |                       |
| Clear display                      | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | clears entire display and sets DDRAM address counter =0                                                                                             | 165                   |
| Return home                        | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 0   | sets DDRAM address counter =0, also returns shifted display to original position, DDRAM contents remain unchanged                                   | 165                   |
| Entry mode set                     | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | I/D | S   | sets cursor move direction and specifies shift of display, these operations are performed during data write and read                                | 3                     |
| Display control                    | 0  | 0   | 0   | 0   | 0   | 0   | 1   | D   | C   | B   | sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D =0 (display off) puts chip into the power-down mode | 3                     |
| Cursor /display shift              | 0  | 0   | 0   | 0   | 0   | 1   | S/C | R/L | 0   | 0   | moves cursor and shifts display without changing DDRAM contents                                                                                     | 3                     |
| Set CGRAM address                  | 0  | 0   | 0   | 1   | A5  | A4  | A3  | A2  | A1  | A0  | sets CGRAM address, bit 6 is to be set by the command 'set DDRAM address'                                                                           | 3                     |
| Set DDRAM address                  | 0  | 0   | 1   | A6  | A5  | A4  | A3  | A2  | A1  | A0  | sets DDRAM address                                                                                                                                  | 3                     |
| <b>H = 1</b>                       |    |     |     |     |     |     |     |     |     |     |                                                                                                                                                     |                       |
| Reserved                           | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | do not use                                                                                                                                          | -                     |
| Screen configuration               | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | L   | set screen configuration                                                                                                                            | 3                     |
| Display configuration              | 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | P   | Q   | set display configuration                                                                                                                           | 3                     |
| Icon control                       | 0  | 0   | 0   | 0   | 0   | 0   | 1   | IM  | IB  | 0   | set icon mode (IM), icon blink (IB)                                                                                                                 | 3                     |
| Temperature control                | 0  | 0   | 0   | 0   | 0   | 1   | 0   | 0   | TC1 | TC2 | set temperature coefficient (TCx)                                                                                                                   | 3                     |
| Set VLCD                           | 0  | 0   | 1   | V   | D5  | D4  | D3  | D2  | D1  | D0  | store V <sub>LCD</sub> in register VA or VB (V)                                                                                                     | 3                     |

Table 10 Explanations of symbols used in Table 9

| Bit                          | State                                                                                                                                       |                                                                                                                                            |
|------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
|                              | Logic0                                                                                                                                      | Logic1                                                                                                                                     |
| I/D                          | decrement                                                                                                                                   | increment                                                                                                                                  |
| S                            | display freeze                                                                                                                              | display shift                                                                                                                              |
| D                            | display off                                                                                                                                 | display on                                                                                                                                 |
| C                            | cursor off                                                                                                                                  | cursor on                                                                                                                                  |
| B                            | cursor character blink off: character at cursor position does not blink                                                                     | cursor character blink on: character at cursor position blinks                                                                             |
| S/C                          | cursor move                                                                                                                                 | display shift                                                                                                                              |
| R/L                          | left shift                                                                                                                                  | right shift                                                                                                                                |
| DL                           | 4bits                                                                                                                                       | 8bits                                                                                                                                      |
| H                            | use basic instruction set                                                                                                                   | use extended instruction set                                                                                                               |
| L (no impact, if M=1or SL=1) | left/right screen: standard connection.<br>1st 16characters of 32: columns are from 1to80<br>2nd 16characters of 32: columns are from 1to80 | left/right screen: mirrored connection<br>1st 16characters of 32: columns are from 1to80<br>2nd 16characters of 32: columns are from 80to1 |
| P                            | segment data is displayed from 1 to 80.<br>(column data: left to right)                                                                     | segment data is displayed from 80 to 1<br>(column data: right to left)                                                                     |
| Q                            | common data is displayed from COM1 to COM16 and icon common data is in COM17 and COM18. (row data: top to bottom/2 lines)                   | common data is displayed from COM16 to COM1 and icon common data is in COM18 and COM17. (row data: bottom to top/2 lines)                  |
| IM                           | character mode; full display                                                                                                                | icon mode; only icons displayed                                                                                                            |
| IB                           | icon blink disabled                                                                                                                         | icon blink enabled                                                                                                                         |
| V                            | set VA                                                                                                                                      | set VB                                                                                                                                     |
| M (no impact, if SL=1)       | 1-line by 32display                                                                                                                         | 2-line by 16display                                                                                                                        |
| SL                           | duty 1/18 (1 x 32 or 2 x 16 character display)                                                                                              | duty 1/9 (1 x 16 character display)                                                                                                        |
| Co                           | last control byte; see Table 8                                                                                                              | another control byte follows after data or command.                                                                                        |

Table 11 Explanations of TC1 and TC2 used in Table 9

| TC1 | TC2 | Description                                                                                   |
|-----|-----|-----------------------------------------------------------------------------------------------|
| 0   | 0   | V <sub>LCD</sub> temperature coefficient0, It is – 8.0 mV/K ±2 mV/K (V <sub>LCD</sub> =5.0V)  |
| 1   | 0   | V <sub>LCD</sub> temperature coefficient1, It is – 9.0 mV/K ±2 mV/K (V <sub>LCD</sub> =5.0V)  |
| 0   | 1   | V <sub>LCD</sub> temperature coefficient2, It is – 10.5 mV/K ±2 mV/K (V <sub>LCD</sub> =5.0V) |
| 1   | 1   | V <sub>LCD</sub> temperature coefficient3, It is – 11.8 mV/K ±2 mV/K (V <sub>LCD</sub> =5.0V) |



| icon no. | phase       | COM/SEG  | character codes |   |   |   |   |   |   |   | CGRAM address |   |   |   |   |   |   |   | CGRAM data |   |   |                                                                                       |  |  |  |  | icon view |     |  |  |  |
|----------|-------------|----------|-----------------|---|---|---|---|---|---|---|---------------|---|---|---|---|---|---|---|------------|---|---|---------------------------------------------------------------------------------------|--|--|--|--|-----------|-----|--|--|--|
|          |             |          | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 6             | 5 | 4 | 3 | 2 | 1 | 0 | 4 | 3          | 2 | 1 | 0                                                                                     |  |  |  |  |           |     |  |  |  |
|          |             |          | MSB             |   |   |   |   |   |   |   | LSBMSB        |   |   |   |   |   |   |   | LSBMSB     |   |   |                                                                                       |  |  |  |  |           | LSB |  |  |  |
| 1-5      | even        | 17/1-5   | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1          | 0 | 1 |    |  |  |  |  |           |     |  |  |  |
| 6-10     | even        | 17/6-10  | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1          | 0 | 1 |    |  |  |  |  |           |     |  |  |  |
| 11-15    | even        | 17/11-15 | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1          | 1 | 0 |    |  |  |  |  |           |     |  |  |  |
| ...      | ...         | ...      | ...             |   |   |   |   |   |   |   | ...           |   |   |   |   |   |   |   | ...        |   |   |                                                                                       |  |  |  |  | ...       |     |  |  |  |
| 76-80    | even        | 17/76-80 | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0             | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1          | 1 | 1 |  |  |  |  |  |           |     |  |  |  |
| 81-85    | even        | 18/1-5   | 0               | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0             | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1          | 0 | 0 |  |  |  |  |  |           |     |  |  |  |
| ...      | ...         | ...      | ...             |   |   |   |   |   |   |   | ...           |   |   |   |   |   |   |   | ...        |   |   |                                                                                       |  |  |  |  | ...       |     |  |  |  |
| 156-160  | even        | 18/76-80 | 0               | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0             | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0          | 1 | 1 |  |  |  |  |  |           |     |  |  |  |
| 1-5      | odd (blink) | 17/1-5   | 0               | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0             | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 |  |  |  |  |  |           |     |  |  |  |
| ...      | ...         | ...      | ...             |   |   |   |   |   |   |   | ...           |   |   |   |   |   |   |   | ...        |   |   |                                                                                       |  |  |  |  | ...       |     |  |  |  |
| 156-160  | odd (blink) | 18/76-80 | 0               | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0             | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0          | 1 | 1 |  |  |  |  |  |           |     |  |  |  |

Figure 10 CGRAM to icon mapping



## Interfaces to MPU

### 1. Parallel interface

The NT7651 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and  $\overline{R/W}$  are required.

In 4-bit mode data is transferred in two cycles of 4 bits each using pads DB7 to DB4 for the transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction, see Figure 12 to Figure 13 for examples of bus protocol.

In 4-bit mode, pads DB3 to DB0 must be left open-circuit. They are pulled up to  $V_{DD}$  internally. If the 4-bit interface is used without reading out from the chip (i.e.

$\overline{R/W}$  is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to  $V_{SS1}$  or  $V_{DD1}$  instead of leaving them open-circuit.

### 2. I<sup>2</sup>C-bus interface

The I<sup>2</sup>C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial Data line (SDA) and the Serial Clock Line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

In the I<sup>2</sup>C-bus read mode, DB7 to DB1 should be connected to  $V_{DD1}$  or left open-circuit.

#### (a) I<sup>2</sup>C-BUS Protocol

Before any data is transmitted on the I<sup>2</sup>C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure. The I<sup>2</sup>C-bus configuration for the different NT7651 read and write cycles is shown in Figure 14 to Figure 18. The slow down feature of the I<sup>2</sup>C-bus protocol (receiver holds SCL LOW during internal operations) is not used in the NT7651.

#### (b) Definitions

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.
- NT7651 slave address: 011101SA0.

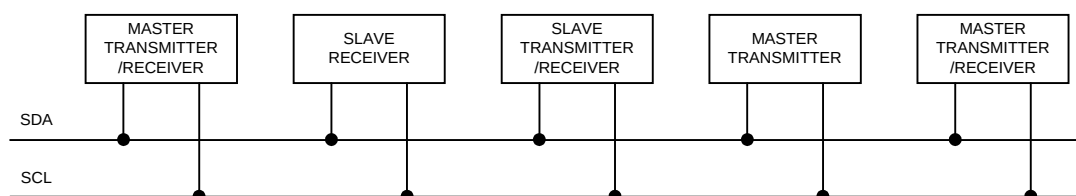


Figure 11 System configuration.



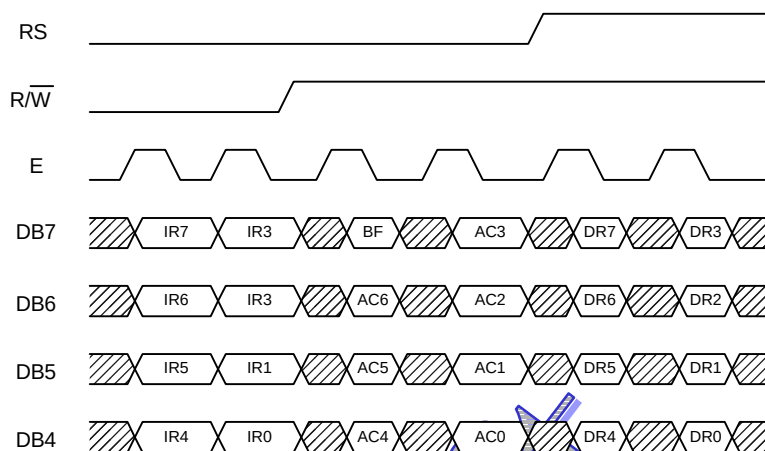


Figure 12 4-bit transfer

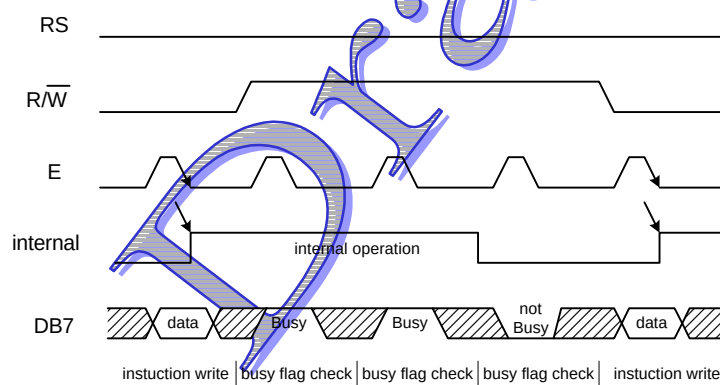


Figure 13 Busy flag checking timing sequence

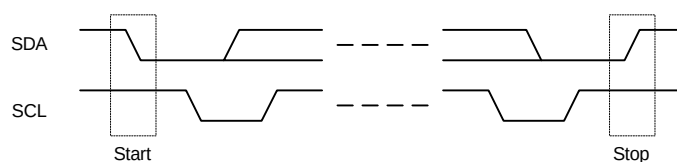


Figure 14 Definition of START and STOP conditions

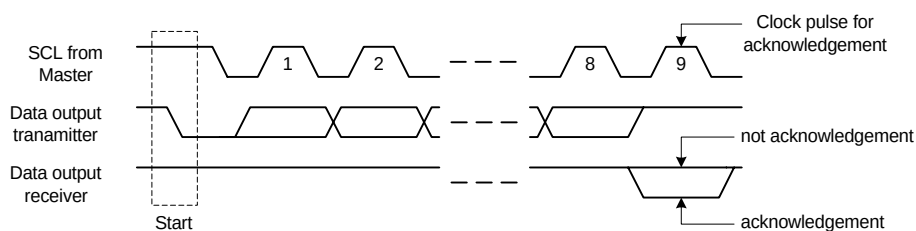


Figure 15 Acknowledgement on the I<sup>2</sup>C-bus

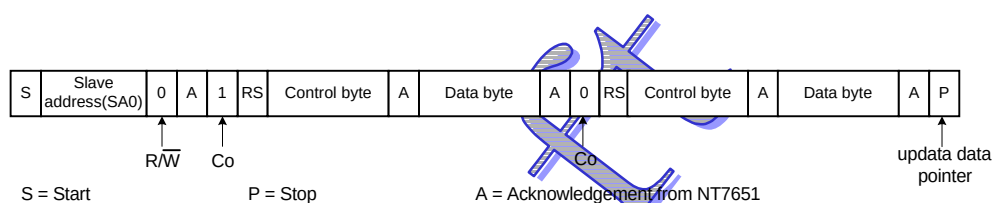


Figure 16 Master transmits to slave receiver; write mode

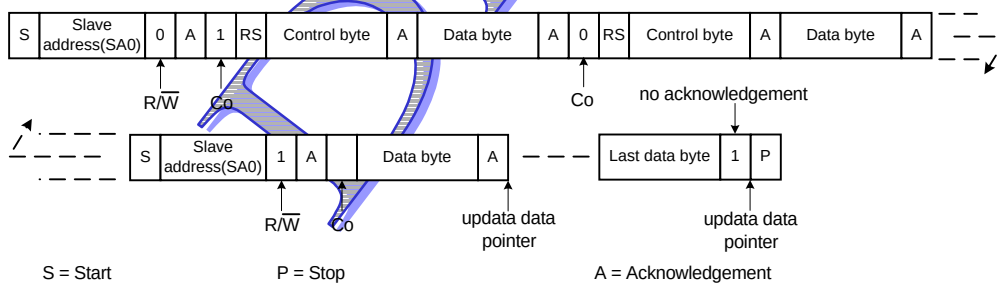


Figure 17 Master reads after setting word address; writes word address, set RS; 'read data'

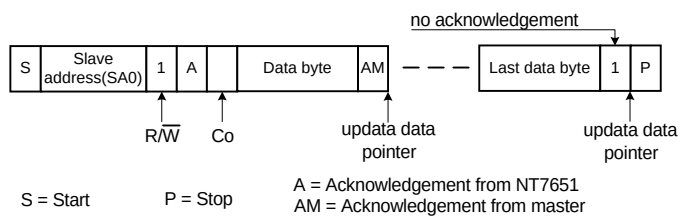


Figure 18 Master reads slave immediately after first byte; read mode (RS previously defined)

**Absolute Maximum Rating\***

DC Supply Voltage . . . . . -0.3V to +5.0V  
 LCD Supply Voltage . . . . . -0.3V to +7.0V  
 Input Voltage . . . . . -0.3V to  $V_{DD}+0.3V$   
 Input Voltage . . . . . -0.3V to  $V_{LCD}+0.3V$   
 Operating Temperature . . . . . -40°C to +85°C  
 Storage Temperature . . . . . -55°C to +125°C

**\*Comments**

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Characteristics**

$V_{DD1} = V_{DD2} = 3.0V$ ,  $V_{LCD} = 5.0V$ ,  $V_{SS1} = V_{SS2} = 0V$ ,  $T_A = 25^\circ C$ ,  $f_{OSC} = 200KHz$ , unless otherwise specified

| Symbol          | Parameter                             | Min.                 | Typ.  | Max.                 | Unit      | Conditions                                                                                   |
|-----------------|---------------------------------------|----------------------|-------|----------------------|-----------|----------------------------------------------------------------------------------------------|
| $V_{DD1}$       | Operating voltage                     | 1.5                  | –     | 3.5                  | V         |                                                                                              |
| $V_{DD2}$       | High voltage generator supply voltage | 2.2                  | –     | 3.5                  | V         | When internal $V_{LCD}$ generation                                                           |
| $V_{LCD}$       | LCD supply voltage                    | 4.5                  | –     | 6.5                  | V         |                                                                                              |
| $I_{DD}$        | Operating current                     | –                    | 150   | 180                  | $\mu A$   | Normal mode, DC-DC converter on, LCD outputs are open-circuit inputs at $V_{DD}$ or $V_{SS}$ |
| $I_{SB1}$       | Standby current 1                     | –                    | –     | 160                  | $\mu A$   | Icon mode, DC-DC converter on, LCD outputs are open-circuit inputs at $V_{DD}$ or $V_{SS}$   |
| $I_{SB2}$       | Standby current 2                     | –                    | –     | 2                    | $\mu A$   | Power-down mode, DB7 to DB0, RS and $R/\overline{W} = 1$ , OSC = 0, E = 0, PD = 1            |
| $V_{IL1}$       | Low-level input voltage               | 0                    | –     | $0.3 \times V_{DD1}$ | V         | E, RS, $R/\overline{W}$ , DB7 to DB0, SA0, SDA, SCL                                          |
| $V_{IH1}$       | High-level input voltage              | $0.7 \times V_{DD1}$ | –     | $V_{DD1}$            | V         | E, RS, $R/\overline{W}$ , DB7 to DB0, SA0, SDA, SCL                                          |
| $V_{IL2}$       | Low-level input voltage               | 0                    | –     | $0.2 \times V_{DD1}$ | V         | PD, RESET                                                                                    |
| $V_{IH2}$       | High-level input voltage              | $0.8 \times V_{DD1}$ | –     | $V_{DD1}$            | V         | PD, RESET                                                                                    |
| $V_{IL3}$       | Low-level input voltage               | 0                    | –     | $V_{DD1} - 1.5$      | V         | OSC                                                                                          |
| $V_{IH3}$       | High-level voltage                    | $V_{DD1} - 0.1$      | –     | $V_{DD1}$            | V         | OSC                                                                                          |
| $I_{OL}$        | Low-level output current              | 1.6                  | 4     | –                    | mA        | $V_{OL} = 0.4V$ , DB7 to DB0, SDA                                                            |
| $I_{OH}$        | High-level output current             | –1                   | –8    | –                    | mA        | $V_{OH} = 2.4V$ , DB7 to DB0                                                                 |
| $I_{PU}$        | Pull-up current                       | 0.04                 | 0.15  | 1                    | $\mu A$   | $V_I = V_{SS}$ , DB7 to DB0, RS, $R/\overline{W}$                                            |
| $I_L$           | Leakage current                       | –1                   | –     | +1                   | $\mu A$   | $V_I = V_{DD}$ or $V_{SS}$ , all input pads                                                  |
| $R_{LCOM}$      | Common output resistance              | –                    | 10    | 30                   | $K\Omega$ | External $V_{LCD} = 5.0V$ , $I_O = 20\mu A$                                                  |
| $R_{LSEG}$      | Segment output resistance             | –                    | 15    | 40                   | $K\Omega$ | External $V_{LCD} = 5.0V$ , $I_O = 20\mu A$                                                  |
| $V_{BIAS\ TOL}$ | Bias voltage tolerance                | –                    | 20    | 130                  | mV        | External $V_{LCD}$ , LCD outputs unload                                                      |
| $V_{LCD\ TOL}$  | $V_{LCD}$ tolerance                   | –                    | –     | 340                  | mV        | $V_{LCD2} = 5.0V$ , load current $I_{VLCD} = 5\mu A$ , LCD outputs open-circuit              |
| TC0             | $V_{LCD}$ temperature coefficient     | –10.0                | –8.0  | –6.0                 | mV/K      | $V_{LCD} = 5.0V$                                                                             |
| TC1             | $V_{LCD}$ temperature coefficient     | –11.0                | –9.0  | –7.0                 | mV/K      | $V_{LCD} = 5.0V$                                                                             |
| TC2             | $V_{LCD}$ temperature coefficient     | –12.5                | –10.5 | –8.5                 | mV/K      | $V_{LCD} = 5.0V$                                                                             |
| TC3             | $V_{LCD}$ temperature coefficient     | –13.8                | –11.8 | –9.8                 | mV/K      | $V_{LCD} = 5.0V$                                                                             |

## AC Characteristics

$V_{DD} = 3.0V$ ,  $V_{LCD} = 5.0V$ ,  $V_{SS} = 0V$ ,  $T_A = 25^\circ C$ ,  $f_{OSC} = 200KHz$ , unless otherwise specified

| Symbol                                                                                        | Parameter                                  | Min. | Typ. | Max. | Unit    | Conditions               |
|-----------------------------------------------------------------------------------------------|--------------------------------------------|------|------|------|---------|--------------------------|
| $f_{FRAME}$                                                                                   | LCD frame frequency                        | 65   | –    | 160  | Hz      | internal clock           |
| $f_{OSC}$                                                                                     | Oscillator frequency                       | 190  | –    | 450  | KHz     | not available at any pad |
| $f_{OSC(EXT)}$                                                                                | External clock frequency                   | 140  | –    | 450  | KHz     |                          |
| $t_{OSCST}$                                                                                   | Oscillator start-up time                   | –    | 1    | 1.2  | ms      | after power-down         |
| <b>Bus timing characteristics: parallel interface</b>                                         |                                            |      |      |      |         |                          |
| Write Operation (Writing DATA from MPU to NT7651)                                             |                                            |      |      |      |         |                          |
| $T_{cy(EN)}$                                                                                  | enable cycle time                          | 500  | –    | –    | ns      |                          |
| $t_{w(EN)}$                                                                                   | enable pulse width                         | 220  | –    | –    | ns      |                          |
| $t_{SU(A)}$                                                                                   | address set-up time                        | 50   | –    | –    | ns      |                          |
| $t_{H(A)}$                                                                                    | address hold time                          | 25   | –    | –    | ns      |                          |
| $t_{SU(D)}$                                                                                   | data set-up time                           | 60   | –    | –    | ns      |                          |
| $t_{H(D)}$                                                                                    | data hold time                             | 25   | –    | –    | ns      |                          |
| Read Operation (Reading DATA from NT7651 to MPU)                                              |                                            |      |      |      |         |                          |
| $T_{cy(EN)}$                                                                                  | enable cycle time                          | 500  | –    | –    | ns      |                          |
| $t_{w(EN)}$                                                                                   | enable pulse width                         | 220  | –    | –    | ns      |                          |
| $t_{SU(A)}$                                                                                   | address set-up time                        | 50   | –    | –    | ns      |                          |
| $t_{H(A)}$                                                                                    | address hold time                          | 25   | –    | –    | ns      |                          |
| $t_{d(D)}$                                                                                    | data delay time                            | –    | –    | 150  | ns      |                          |
| $t_{H(D)}$                                                                                    | data hold time                             | 20   | –    | 100  | ns      |                          |
| <b>Timing characteristics: I<sup>2</sup>C-bus interface</b> (input capacitance $C_i = 10pF$ ) |                                            |      |      |      |         |                          |
| $f_{SCL}$                                                                                     | SCL clock frequency                        | –    | –    | 400  | KHz     |                          |
| $t_{LOW}$                                                                                     | SCL clock low period                       | 1.3  | –    | –    | $\mu s$ |                          |
| $t_{HIGH}$                                                                                    | SCL clock high period                      | 0.6  | –    | –    | $\mu s$ |                          |
| $t_{SU;DAT}$                                                                                  | data set-up time                           | 100  | –    | –    | ns      |                          |
| $t_{HD;DAT}$                                                                                  | data hold time                             | 0    | –    | –    | ns      |                          |
| $t_r$                                                                                         | SCL, SDA rise time                         | –    | –    | 300  | ns      |                          |
| $t_f$                                                                                         | SCL, SDA fall time                         | –    | –    | 300  | ns      |                          |
| $C_B$                                                                                         | capacitive bus line load                   | –    | –    | 400  | pF      |                          |
| $t_{SU;STA}$                                                                                  | set-up time for a repeated START condition | 0.6  | –    | –    | $\mu s$ |                          |
| $t_{HD;STA}$                                                                                  | START condition hold time                  | 0.6  | –    | –    | $\mu s$ |                          |
| $t_{SU;STO}$                                                                                  | set-up time for STOP condition             | 0.6  | –    | –    | $\mu s$ |                          |
| $t_{SW}$                                                                                      | tolerable spike width on bus               | –    | –    | 50   | ns      |                          |

## Timing Characteristics

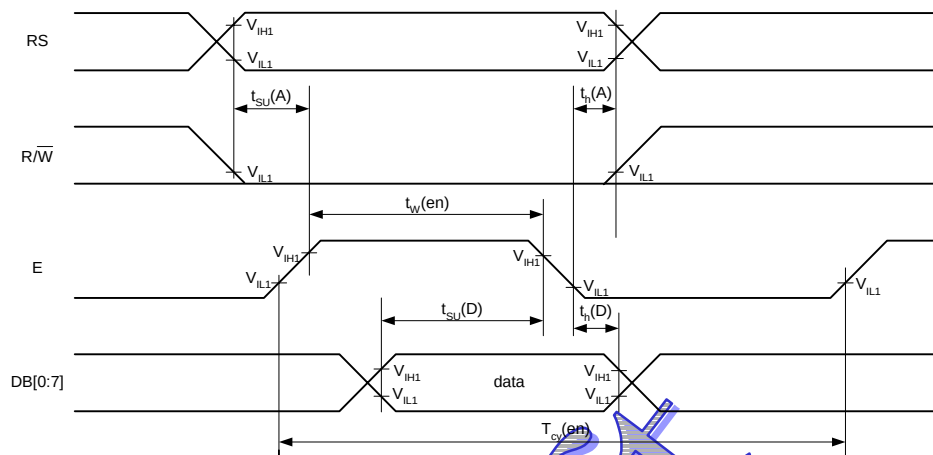


Figure 19 Parallel bus writing data from MPU to NT7651

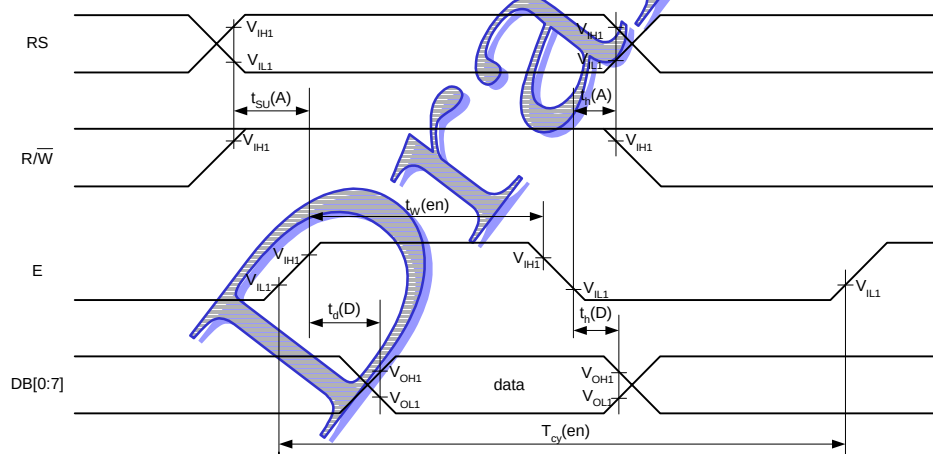


Figure 20 Parallel bus reading data from NT7651 to MPU

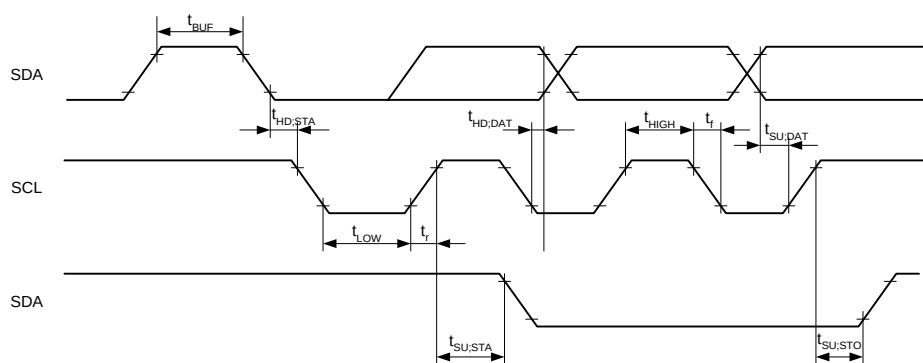
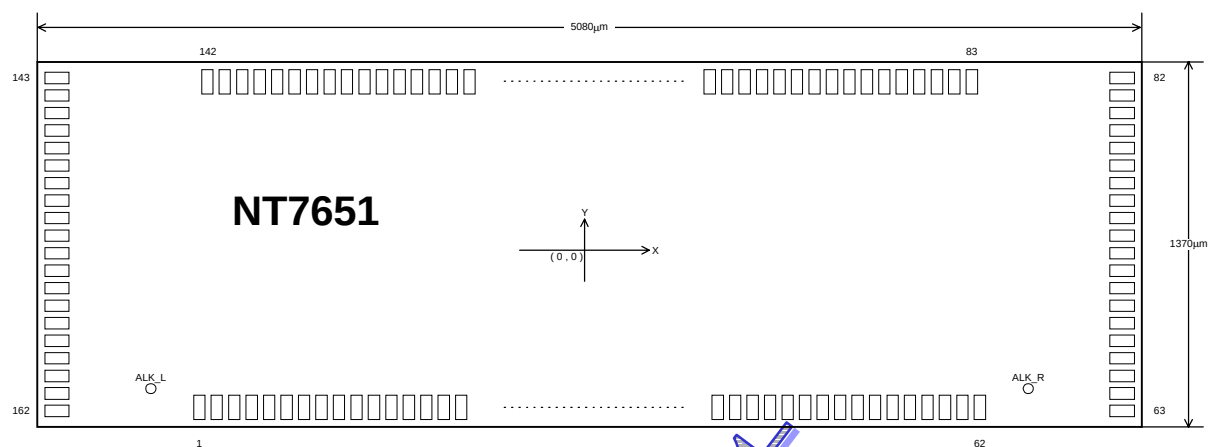


Figure 21 I2C-bus timing diagram.

**Application Information**

Draft

**Bonding Diagram**


| Pad No. | Designation               | X       | Y    | Pad No. | Designation       | X      | Y    |
|---------|---------------------------|---------|------|---------|-------------------|--------|------|
| 1       | SCL                       | -1982.5 | -620 | 31      | V <sub>DD3</sub>  | -32.5  | -620 |
| 2       | SCL                       | -1917.5 | -620 | 32      | V <sub>DD3</sub>  | 32.5   | -620 |
| 3       | DUMMY (V <sub>SS1</sub> ) | -1852.5 | -620 | 33      | V <sub>DD3</sub>  | 97.5   | -620 |
| 4       | RESET                     | -1787.5 | -620 | 34      | V <sub>DD3</sub>  | 162.5  | -620 |
| 5       | PD                        | -1722.5 | -620 | 35      | E                 | 227.5  | -620 |
| 6       | SDA                       | -1657.5 | -620 | 36      | T1                | 292.5  | -620 |
| 7       | SDA                       | -1592.5 | -620 | 37      | T2                | 357.5  | -620 |
| 8       | R/W                       | -1527.5 | -620 | 38      | T3                | 422.5  | -620 |
| 9       | RS                        | -1462.5 | -620 | 39      | V <sub>SS1</sub>  | 487.5  | -620 |
| 10      | T6                        | -1397.5 | -620 | 40      | V <sub>SS1</sub>  | 552.5  | -620 |
| 11      | DB[0]/SA0                 | -1332.5 | -620 | 41      | V <sub>SS1</sub>  | 617.5  | -620 |
| 12      | DB[1]                     | -1267.5 | -620 | 42      | V <sub>SS1</sub>  | 682.5  | -620 |
| 13      | DB[2]                     | -1202.5 | -620 | 43      | V <sub>SS1</sub>  | 747.5  | -620 |
| 14      | DB[3]                     | -1137.5 | -620 | 44      | V <sub>SS1</sub>  | 812.5  | -620 |
| 15      | DB[4]                     | -1072.5 | -620 | 45      | V <sub>SS2</sub>  | 877.5  | -620 |
| 16      | DB[5]                     | -1007.5 | -620 | 46      | V <sub>SS2</sub>  | 942.5  | -620 |
| 17      | DB[6]                     | -942.5  | -620 | 47      | V <sub>SS2</sub>  | 1007.5 | -620 |
| 18      | DB[7]                     | -877.5  | -620 | 48      | V <sub>SS2</sub>  | 1072.5 | -620 |
| 19      | T5                        | -812.5  | -620 | 49      | V <sub>SS2</sub>  | 1137.5 | -620 |
| 20      | T4                        | -747.5  | -620 | 50      | V <sub>SS2</sub>  | 1202.5 | -620 |
| 21      | OSC                       | -682.5  | -620 | 51      | V <sub>LCD1</sub> | 1267.5 | -620 |
| 22      | OSC                       | -617.5  | -620 | 52      | V <sub>LCD1</sub> | 1332.5 | -620 |
| 23      | V <sub>DD1</sub>          | -552.5  | -620 | 53      | V <sub>LCD1</sub> | 1397.5 | -620 |
| 24      | V <sub>DD1</sub>          | -487.5  | -620 | 54      | V <sub>LCD1</sub> | 1462.5 | -620 |
| 25      | V <sub>DD1</sub>          | -422.5  | -620 | 55      | V <sub>LCD1</sub> | 1527.5 | -620 |
| 26      | V <sub>DD1</sub>          | -357.5  | -620 | 56      | V <sub>LCD1</sub> | 1592.5 | -620 |
| 27      | V <sub>DD2</sub>          | -292.5  | -620 | 57      | V <sub>LCD2</sub> | 1657.5 | -620 |
| 28      | V <sub>DD2</sub>          | -227.5  | -620 | 58      | V <sub>LCD2</sub> | 1722.5 | -620 |
| 29      | V <sub>DD3</sub>          | -162.5  | -620 | 59      | V <sub>LCD2</sub> | 1787.5 | -620 |
| 30      | V <sub>DD3</sub>          | -97.5   | -620 | 60      | V <sub>LCD2</sub> | 1852.5 | -620 |

**Bonding Diagram (continued)**

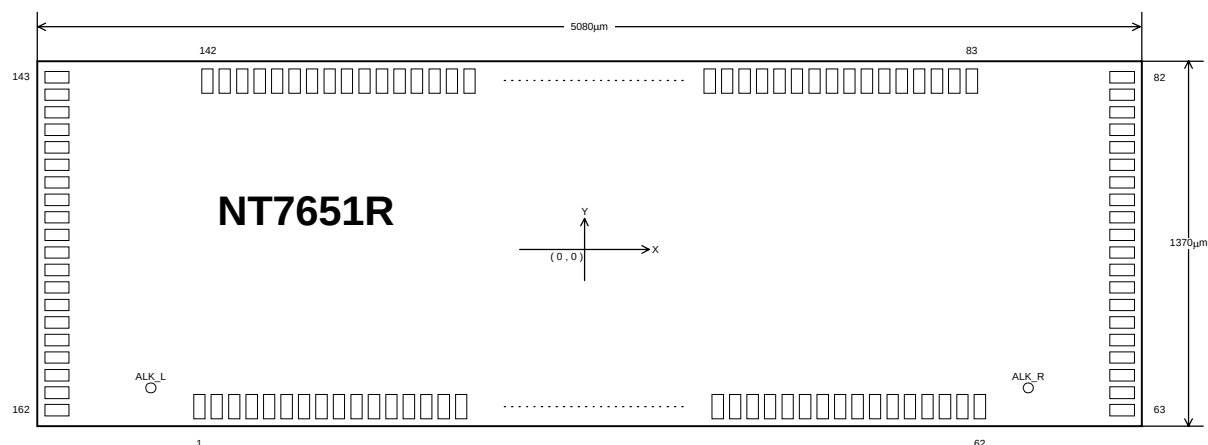
| Pad No. | Designation       | X      | Y      | Pad No. | Designation | X       | Y   |
|---------|-------------------|--------|--------|---------|-------------|---------|-----|
| 61      | V <sub>LCD2</sub> | 1917.5 | -620   | 101     | SEG[52]     | 747.5   | 620 |
| 62      | V <sub>LCD2</sub> | 1982.5 | -620   | 102     | SEG[51]     | 682.5   | 620 |
| 63      | COM[17]           | 2475   | -617.5 | 103     | SEG[50]     | 617.5   | 620 |
| 64      | COM[1]            | 2475   | -552.5 | 104     | SEG[49]     | 552.5   | 620 |
| 65      | COM[2]            | 2475   | -487.5 | 105     | SEG[48]     | 487.5   | 620 |
| 66      | COM[3]            | 2475   | -422.5 | 106     | SEG[47]     | 422.5   | 620 |
| 67      | COM[4]            | 2475   | -357.5 | 107     | SEG[46]     | 357.5   | 620 |
| 68      | COM[5]            | 2475   | -292.5 | 108     | SEG[45]     | 292.5   | 620 |
| 69      | COM[6]            | 2475   | -227.5 | 109     | SEG[44]     | 227.5   | 620 |
| 70      | COM[7]            | 2475   | -162.5 | 110     | SEG[43]     | 162.5   | 620 |
| 71      | COM[8]            | 2475   | -97.5  | 111     | SEG[42]     | 97.5    | 620 |
| 72      | COM17DUP          | 2475   | -32.5  | 112     | SEG[41]     | 32.5    | 620 |
| 73      | SEG[80]           | 2475   | 32.5   | 113     | SEG[40]     | -32.5   | 620 |
| 74      | SEG[79]           | 2475   | 97.5   | 114     | SEG[39]     | -97.5   | 620 |
| 75      | SEG[78]           | 2475   | 162.5  | 115     | SEG[38]     | -162.5  | 620 |
| 76      | SEG[77]           | 2475   | 227.5  | 116     | SEG[37]     | -227.5  | 620 |
| 77      | SEG[76]           | 2475   | 292.5  | 117     | SEG[36]     | -292.5  | 620 |
| 78      | SEG[75]           | 2475   | 357.5  | 118     | SEG[35]     | -357.5  | 620 |
| 79      | SEG[74]           | 2475   | 422.5  | 119     | SEG[34]     | -422.5  | 620 |
| 80      | SEG[73]           | 2475   | 487.5  | 120     | SEG[33]     | -487.5  | 620 |
| 81      | SEG[72]           | 2475   | 552.5  | 121     | SEG[32]     | -552.5  | 620 |
| 82      | SEG[71]           | 2475   | 617.5  | 122     | SEG[31]     | -617.5  | 620 |
| 83      | SEG[70]           | 1917.5 | 620    | 123     | SEG[30]     | -682.5  | 620 |
| 84      | SEG[69]           | 1852.5 | 620    | 124     | SEG[29]     | -747.5  | 620 |
| 85      | SEG[68]           | 1787.5 | 620    | 125     | SEG[28]     | -812.5  | 620 |
| 86      | SEG[67]           | 1722.5 | 620    | 126     | SEG[27]     | -877.5  | 620 |
| 87      | SEG[66]           | 1657.5 | 620    | 127     | SEG[26]     | -942.5  | 620 |
| 88      | SEG[65]           | 1592.5 | 620    | 128     | SEG[25]     | -1007.5 | 620 |
| 89      | SEG[64]           | 1527.5 | 620    | 129     | SEG[24]     | -1072.5 | 620 |
| 90      | SEG[63]           | 1462.5 | 620    | 130     | SEG[23]     | -1137.5 | 620 |
| 91      | SEG[62]           | 1397.5 | 620    | 131     | SEG[22]     | -1202.5 | 620 |
| 92      | SEG[61]           | 1332.5 | 620    | 132     | SEG[21]     | -1267.5 | 620 |
| 93      | SEG[60]           | 1267.5 | 620    | 133     | SEG[20]     | -1332.5 | 620 |
| 94      | SEG[59]           | 1202.5 | 620    | 134     | SEG[19]     | -1397.5 | 620 |
| 95      | SEG[58]           | 1137.5 | 620    | 135     | SEG[18]     | -1462.5 | 620 |
| 96      | SEG[57]           | 1072.5 | 620    | 136     | SEG[17]     | -1527.5 | 620 |
| 97      | SEG[56]           | 1007.5 | 620    | 137     | SEG[16]     | -1592.5 | 620 |
| 98      | SEG[55]           | 942.5  | 620    | 139     | SEG[15]     | -1657.5 | 620 |
| 99      | SEG[54]           | 877.5  | 620    | 139     | SEG[14]     | -1722.5 | 620 |
| 100     | SEG[53]           | 812.5  | 620    | 140     | SEG[13]     | -1787.5 | 620 |



**Bonding Diagram (continued)**

| Pad No. | Designation | X       | Y     | Pad No. | Designation | X     | Y      |
|---------|-------------|---------|-------|---------|-------------|-------|--------|
| 141     | SEG[12]     | -1852.5 | 620   | 153     | COM18DUP    | -2475 | -32.5  |
| 142     | SEG[11]     | -1917.5 | 620   | 154     | COM[16]     | -2475 | -97.5  |
| 143     | SEG[10]     | -2475   | 617.5 | 155     | COM[15]     | -2475 | -162.5 |
| 144     | SEG[9]      | -2475   | 552.5 | 156     | COM[14]     | -2475 | -227.5 |
| 145     | SEG[8]      | -2475   | 487.5 | 157     | COM[13]     | -2475 | -292.5 |
| 146     | SEG[7]      | -2475   | 422.5 | 158     | COM[12]     | -2475 | -357.5 |
| 147     | SEG[6]      | -2475   | 357.5 | 159     | COM[11]     | -2475 | -422.5 |
| 148     | SEG[5]      | -2475   | 292.5 | 160     | COM[10]     | -2475 | -487.5 |
| 149     | SEG[4]      | -2475   | 227.5 | 161     | COM[9]      | -2475 | -552.5 |
| 150     | SEG[3]      | -2475   | 162.5 | 162     | COM[18]     | -2475 | -617.5 |
| 151     | SEG[2]      | -2475   | 97.5  |         | ALK_L       | -2149 | -535   |
| 152     | SEG[1]      | -2475   | 32.5  |         | ALK_R       | 2149  | -535   |

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| Pad No. | Designation               | X       | Y    | Pad No. | Designation       | X      | Y    |
|---------|---------------------------|---------|------|---------|-------------------|--------|------|
| 1       | SCL                       | -1982.5 | -620 | 31      | V <sub>DD3</sub>  | -32.5  | -620 |
| 2       | SCL                       | -1917.5 | -620 | 32      | V <sub>DD3</sub>  | 32.5   | -620 |
| 3       | DUMMY (V <sub>SS1</sub> ) | -1852.5 | -620 | 33      | V <sub>DD3</sub>  | 97.5   | -620 |
| 4       | RESET                     | -1787.5 | -620 | 34      | V <sub>DD3</sub>  | 162.5  | -620 |
| 5       | PD                        | -1722.5 | -620 | 35      | E                 | 227.5  | -620 |
| 6       | SDA                       | -1657.5 | -620 | 36      | T1                | 292.5  | -620 |
| 7       | SDA                       | -1592.5 | -620 | 37      | T2                | 357.5  | -620 |
| 8       | R/W                       | -1527.5 | -620 | 38      | T3                | 422.5  | -620 |
| 9       | RS                        | -1462.5 | -620 | 39      | V <sub>SS1</sub>  | 487.5  | -620 |
| 10      | T6                        | -1397.5 | -620 | 40      | V <sub>SS1</sub>  | 552.5  | -620 |
| 11      | DB[0]/SA0                 | -1332.5 | -620 | 41      | V <sub>SS1</sub>  | 617.5  | -620 |
| 12      | DB[1]                     | -1267.5 | -620 | 42      | V <sub>SS1</sub>  | 682.5  | -620 |
| 13      | DB[2]                     | -1202.5 | -620 | 43      | V <sub>SS1</sub>  | 747.5  | -620 |
| 14      | DB[3]                     | -1137.5 | -620 | 44      | V <sub>SS1</sub>  | 812.5  | -620 |
| 15      | DB[4]                     | -1072.5 | -620 | 45      | V <sub>SS2</sub>  | 877.5  | -620 |
| 16      | DB[5]                     | -1007.5 | -620 | 46      | V <sub>SS2</sub>  | 942.5  | -620 |
| 17      | DB[6]                     | -942.5  | -620 | 47      | V <sub>SS2</sub>  | 1007.5 | -620 |
| 18      | DB[7]                     | -877.5  | -620 | 48      | V <sub>SS2</sub>  | 1072.5 | -620 |
| 19      | T5                        | -812.5  | -620 | 49      | V <sub>SS2</sub>  | 1137.5 | -620 |
| 20      | T4                        | -747.5  | -620 | 50      | V <sub>SS2</sub>  | 1202.5 | -620 |
| 21      | OSC                       | -682.5  | -620 | 51      | V <sub>LCD1</sub> | 1267.5 | -620 |
| 22      | OSC                       | -617.5  | -620 | 52      | V <sub>LCD1</sub> | 1332.5 | -620 |
| 23      | V <sub>DD1</sub>          | -552.5  | -620 | 53      | V <sub>LCD1</sub> | 1397.5 | -620 |
| 24      | V <sub>DD1</sub>          | -487.5  | -620 | 54      | V <sub>LCD1</sub> | 1462.5 | -620 |
| 25      | V <sub>DD1</sub>          | -422.5  | -620 | 55      | V <sub>LCD1</sub> | 1527.5 | -620 |
| 26      | V <sub>DD1</sub>          | -357.5  | -620 | 56      | V <sub>LCD1</sub> | 1592.5 | -620 |
| 27      | V <sub>DD2</sub>          | -292.5  | -620 | 57      | V <sub>LCD2</sub> | 1657.5 | -620 |
| 28      | V <sub>DD2</sub>          | -227.5  | -620 | 58      | V <sub>LCD2</sub> | 1722.5 | -620 |
| 29      | V <sub>DD3</sub>          | -162.5  | -620 | 59      | V <sub>LCD2</sub> | 1787.5 | -620 |
| 30      | V <sub>DD3</sub>          | -97.5   | -620 | 60      | V <sub>LCD2</sub> | 1852.5 | -620 |

**Bonding Diagram (continued)**

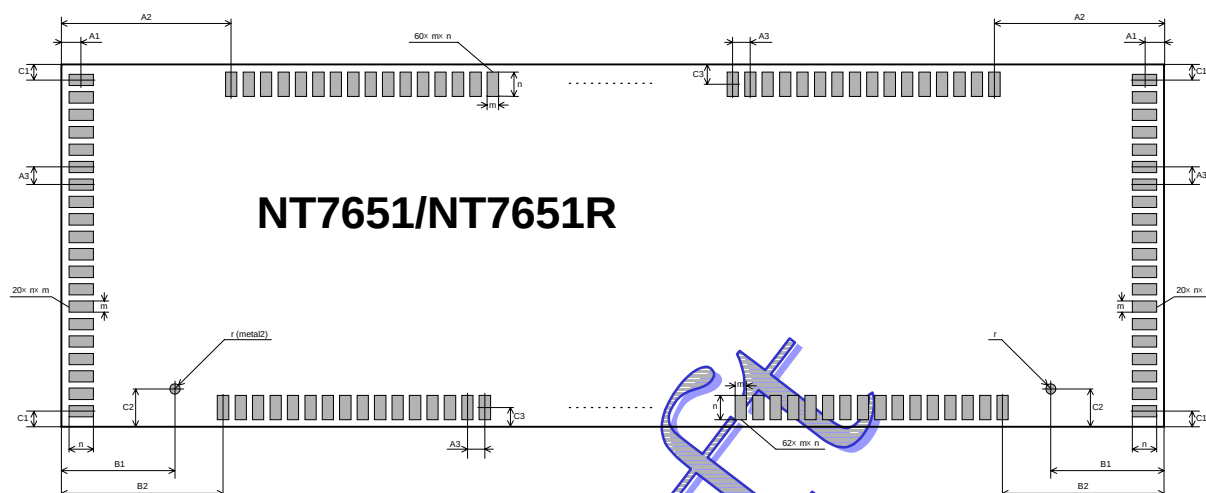
| Pad No. | Designation       | X      | Y      | Pad No. | Designation | X       | Y   |
|---------|-------------------|--------|--------|---------|-------------|---------|-----|
| 61      | V <sub>LCD2</sub> | 1917.5 | -620   | 101     | SEG[52]     | 747.5   | 620 |
| 62      | V <sub>LCD2</sub> | 1982.5 | -620   | 102     | SEG[51]     | 682.5   | 620 |
| 63      | COM[17]           | 2475   | -617.5 | 103     | SEG[50]     | 617.5   | 620 |
| 64      | COM[8]            | 2475   | -552.5 | 104     | SEG[49]     | 552.5   | 620 |
| 65      | COM[7]            | 2475   | -487.5 | 105     | SEG[48]     | 487.5   | 620 |
| 66      | COM[6]            | 2475   | -422.5 | 106     | SEG[47]     | 422.5   | 620 |
| 67      | COM[5]            | 2475   | -357.5 | 107     | SEG[46]     | 357.5   | 620 |
| 68      | COM[4]            | 2475   | -292.5 | 108     | SEG[45]     | 292.5   | 620 |
| 69      | COM[3]            | 2475   | -227.5 | 109     | SEG[44]     | 227.5   | 620 |
| 70      | COM[2]            | 2475   | -162.5 | 110     | SEG[43]     | 162.5   | 620 |
| 71      | COM[1]            | 2475   | -97.5  | 111     | SEG[42]     | 97.5    | 620 |
| 72      | COM17DUP          | 2475   | -32.5  | 112     | SEG[41]     | 32.5    | 620 |
| 73      | SEG[80]           | 2475   | 32.5   | 113     | SEG[40]     | -32.5   | 620 |
| 74      | SEG[79]           | 2475   | 97.5   | 114     | SEG[39]     | -97.5   | 620 |
| 75      | SEG[78]           | 2475   | 162.5  | 115     | SEG[38]     | -162.5  | 620 |
| 76      | SEG[77]           | 2475   | 227.5  | 116     | SEG[37]     | -227.5  | 620 |
| 77      | SEG[76]           | 2475   | 292.5  | 117     | SEG[36]     | -292.5  | 620 |
| 78      | SEG[75]           | 2475   | 357.5  | 118     | SEG[35]     | -357.5  | 620 |
| 79      | SEG[74]           | 2475   | 422.5  | 119     | SEG[34]     | -422.5  | 620 |
| 80      | SEG[73]           | 2475   | 487.5  | 120     | SEG[33]     | -487.5  | 620 |
| 81      | SEG[72]           | 2475   | 552.5  | 121     | SEG[32]     | -552.5  | 620 |
| 82      | SEG[71]           | 2475   | 617.5  | 122     | SEG[31]     | -617.5  | 620 |
| 83      | SEG[70]           | 1917.5 | 620    | 123     | SEG[30]     | -682.5  | 620 |
| 84      | SEG[69]           | 1852.5 | 620    | 124     | SEG[29]     | -747.5  | 620 |
| 85      | SEG[68]           | 1787.5 | 620    | 125     | SEG[28]     | -812.5  | 620 |
| 86      | SEG[67]           | 1722.5 | 620    | 126     | SEG[27]     | -877.5  | 620 |
| 87      | SEG[66]           | 1657.5 | 620    | 127     | SEG[26]     | -942.5  | 620 |
| 88      | SEG[65]           | 1592.5 | 620    | 128     | SEG[25]     | -1007.5 | 620 |
| 89      | SEG[64]           | 1527.5 | 620    | 129     | SEG[24]     | -1072.5 | 620 |
| 90      | SEG[63]           | 1462.5 | 620    | 130     | SEG[23]     | -1137.5 | 620 |
| 91      | SEG[62]           | 1397.5 | 620    | 131     | SEG[22]     | -1202.5 | 620 |
| 92      | SEG[61]           | 1332.5 | 620    | 132     | SEG[21]     | -1267.5 | 620 |
| 93      | SEG[60]           | 1267.5 | 620    | 133     | SEG[20]     | -1332.5 | 620 |
| 94      | SEG[59]           | 1202.5 | 620    | 134     | SEG[19]     | -1397.5 | 620 |
| 95      | SEG[58]           | 1137.5 | 620    | 135     | SEG[18]     | -1462.5 | 620 |
| 96      | SEG[57]           | 1072.5 | 620    | 136     | SEG[17]     | -1527.5 | 620 |
| 97      | SEG[56]           | 1007.5 | 620    | 137     | SEG[16]     | -1592.5 | 620 |
| 98      | SEG[55]           | 942.5  | 620    | 139     | SEG[15]     | -1657.5 | 620 |
| 99      | SEG[54]           | 877.5  | 620    | 139     | SEG[14]     | -1722.5 | 620 |
| 100     | SEG[53]           | 812.5  | 620    | 140     | SEG[13]     | -1787.5 | 620 |

**Bonding Diagram (continued)**

| Pad No. | Designation | X       | Y     | Pad No. | Designation | X     | Y      |
|---------|-------------|---------|-------|---------|-------------|-------|--------|
| 141     | SEG[12]     | -1852.5 | 620   | 153     | COM18DUP    | -2475 | -32.5  |
| 142     | SEG[11]     | -1917.5 | 620   | 154     | COM[9]      | -2475 | -97.5  |
| 143     | SEG[10]     | -2475   | 617.5 | 155     | COM[10]     | -2475 | -162.5 |
| 144     | SEG[9]      | -2475   | 552.5 | 156     | COM[11]     | -2475 | -227.5 |
| 145     | SEG[8]      | -2475   | 487.5 | 157     | COM[12]     | -2475 | -292.5 |
| 146     | SEG[7]      | -2475   | 422.5 | 158     | COM[13]     | -2475 | -357.5 |
| 147     | SEG[6]      | -2475   | 357.5 | 159     | COM[14]     | -2475 | -422.5 |
| 148     | SEG[5]      | -2475   | 292.5 | 160     | COM[15]     | -2475 | -487.5 |
| 149     | SEG[4]      | -2475   | 227.5 | 161     | COM[16]     | -2475 | -552.5 |
| 150     | SEG[3]      | -2475   | 162.5 | 162     | COM[18]     | -2475 | -617.5 |
| 151     | SEG[2]      | -2475   | 97.5  |         | ALK_L       | -2149 | -535   |
| 152     | SEG[1]      | -2475   | 32.5  |         | ALK_R       | 2149  | -535   |

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**Package Information**
**Chip Outline Dimensions**

 unit:  $\mu\text{m}$ 


| Symbol | Dimensions in $\mu\text{m}$ | Symbol | Dimensions in $\mu\text{m}$ |
|--------|-----------------------------|--------|-----------------------------|
| A1     | 65                          | C2     | 150                         |
| A2     | 622.5                       | C3     | 65                          |
| A3     | 65                          | r      | 35                          |
| B1     | 391                         | m      | 42                          |
| B2     | 557.5                       | n      | 90                          |
| C1     | 67.5                        |        |                             |

**Ordering Information**

| Part No.       | CGROM Code   | Package  |
|----------------|--------------|----------|
|                | Stand code R | COG FORM |
| NT7651H-BDT02  | Stand code S | COG FORM |
|                | Stand code R | COG FORM |
| NT7651RH-BDT02 | Stand code S | COG FORM |

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